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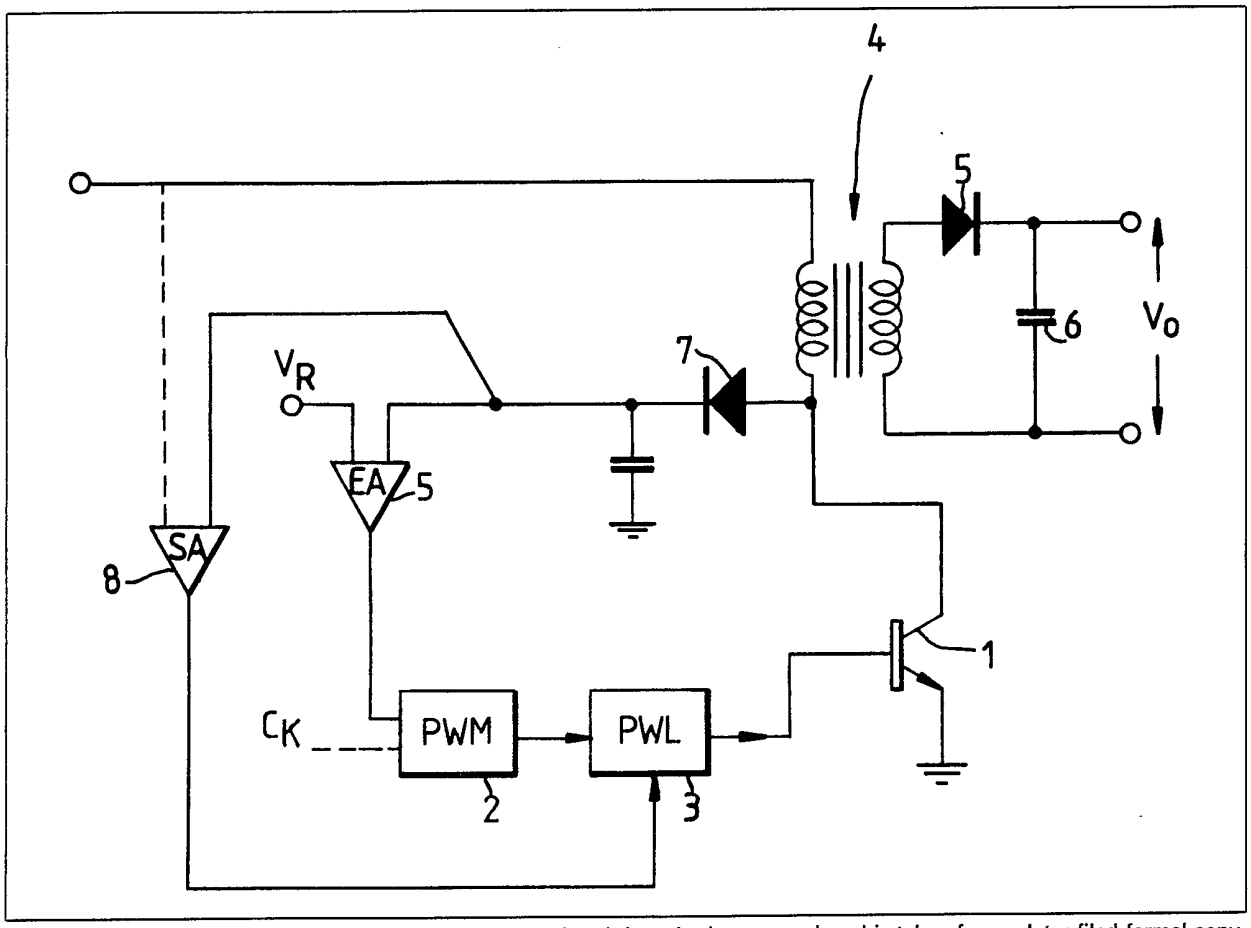
(54) DC–DC converter

(57) A DC-to-DC converter of the so-called flyback type has a switching transistor (1) which applies a pulsed waveform to the primary of a transformer (4). Thus during the pulses energy is stored in the core of the transformer (4), which energy is ''dumped'' via a rectifier (5) into the load when the pulse ends.

The output voltage depends on the widths of the pulses applied to the transformer (4): to control this an error signal is derived from the primary of the transformer and applied via a rectifier (7) to an amplifier (5), where it is compared with a reference voltage (V_R). Any discrepancy between V_R and the signal produces a control signal which is applied to a pulse width modulator (2), which suitably adjusts the widths of the pulses applied to the transistor (1). To avoid undesirable effects of overload a summing amplifier (8) and a pulse width limiter (3) ensure that when the load exceeds a preset level, pulse width is reduced. The summing amplifier (8) can have another input, shown by a broken line connection, so that changes in the input voltage can be taken into account.



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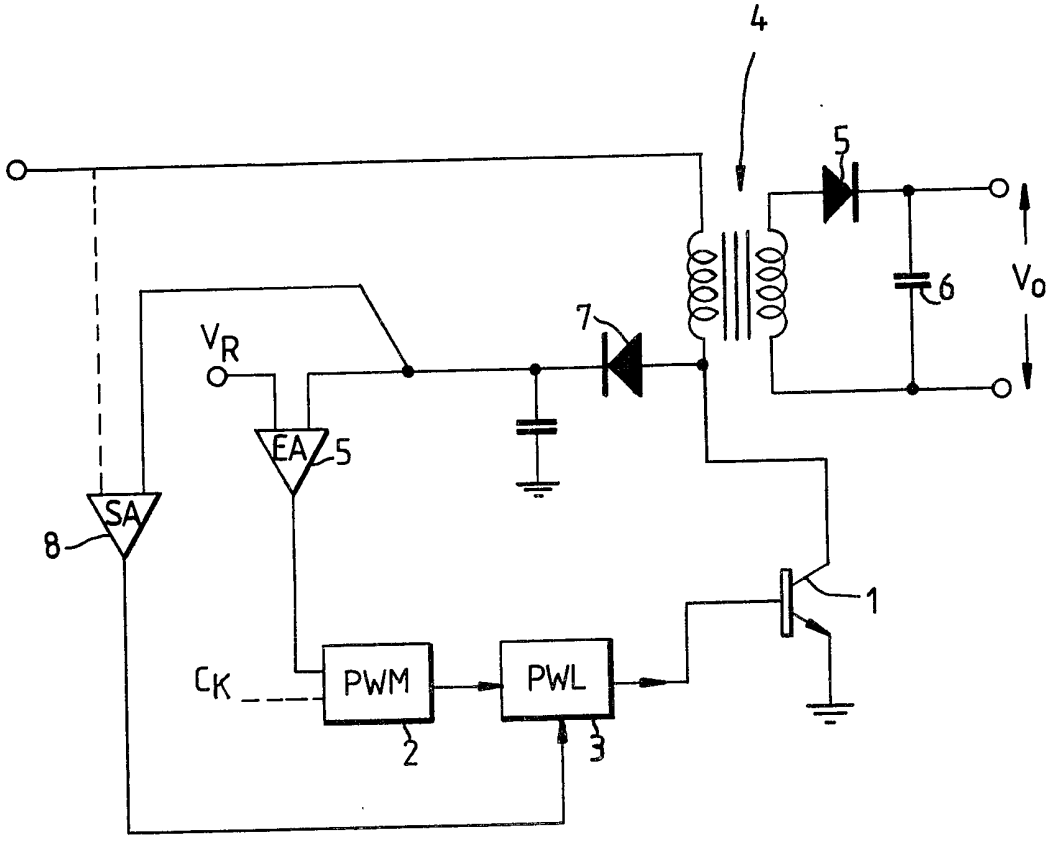
The drawing originally filed was informal and the print here reproduced is taken from a later filed formal copy.


4
5
6
V_o
7
V_R
EA
5
SA
8
1
CK
PWM
PWL
2
3

SPECIFICATION

DC–DC converter

This invention relates to DC-to-DC converters of the so-called "fly-back" type.

In a typical fly-back converter a single switching transistor is used which is operated in a pulsed mode and which feeds a transformer or choke. During the pulses from the transistor, current flows in a winding on the transformer or choke, and when the pulse ends the transistor cuts off. When this occurs the energy stored in the transformer or choke is released via an output winding thereof, so that a pulsed output is obtained which is applied to the load via a rectifier.

To regulate the output direct current in such a converter, the output current or voltage is sensed, often by a connection to the output of the converter, and the result of such sensing is compared with a reference voltage or current. Dependent on the relation between the sensed voltage or current and the reference, an adjustment is made to the pulsed waveform applied to the transformer or choke via the transistor.

An object of the invention is to provide a DC-to-DC converter which is improved and simplified as compared with known circuits of the type referred to above.

According to the present invention, there is provided a DC-to-DC converter which includes a switching transistor which is pulse-driven so as to cause a pulsed current to flow in a transformer, energy being stored in the transformer while the transistor conducts and being discharged into the load during the inter pulse gaps, a rectifier to which the output current from the transformer is applied to the load, pulse width control means connected to the transistor to control the on-off ratio thereof, a first feed back control loop via which an error signal derived from the transistor output is applied to a comparator for comparison with a reference signal, a connection from the output of the comparator to the pulse width control means via which the pulse width is varied in accordance with the load's demand on the converter, and a second feed back control loop via which the error signal is used to limit the output of the converter when the load's demand reaches a preset maximum.

An embodiment of the invention will now be described with reference to the accompanying drawing, which is a simplified representation of a DC-to-DC converter embodying the invention.

In the circuit shown, the switching transistor 1 is controlled by a pulse width modulator 2, which exerts its control on the base of the transistor 1 via a pulse width limiter 3. This arrangement periodically switches the transistor 1 on for the duration of the pulse supplied to its base via the modulator limiter combination 2–3. During the period of conduction of the transistor 1, energy is stored in the transformer 4, and when the transistor cuts off at the end of the pulse, this energy is discharged via a rectifier 5 into the load so that an output voltage V_0 is produced at the circuit's output. The capacitor 6 is a smoothing capacitor.

The pulse width modulator 2 can be controlled by a clock pulse input C_K, to define the frequency of the pulses applied to the transistor 1 if this is considered useful, e.g. when used in a digital system. In addition the modulator 2 is controlled from an error amplifier 5 and the limiter 3 is controlled from a summing amplifier 6.

The error amplifier 5 is in essence a comparator, such as a differential amplifier, which compares a reference voltage V_R, whose value depends on the desired output voltage, with a voltage derived from the converter output. In the present case this is taken from the primary winding of the transformer 4 via a further rectifier 7, so that the voltage at the collector of the transistor 1 is rectified for comparison with the reference voltage V_R. If the result of the comparison indicates that the voltage produced is other than what it should be a control voltage is applied to the modulator 2 to adjust the pulse width, and possibly also the amplitude accordingly.

Thus the starting up condition is with rather narrow pulses applied to the transistor 1, in which case as the load builds up, the discrepancy detected by the error amplifier 5 produces a control signal which, via the modulator 2 causes the pulse width to be increased. Similarly if the load falls, the pulse width is reduced.

To avoid any disastrous consequences, there is a defined maximum pulse width which is permissible, and to provide this facility another control loop is used. This includes a summing amplifier 8, also fed from the rectifier 7. At this point we assume that the broken line connections from the input voltage terminal is not present. Thus a control signal on the output voltage (as reflected via the transformer) is applied to the pulse width limiter 3. If the output taken from the converter reaches a dangerous level, e.g. when a short circuit or partial short circuit is present, the pulse width is reduced by the action of the limiter 3.

The dashed line connection enables a summation to be effected between the input voltage and the output voltage (or current). Hence variations in input voltage can be, at least to some extent catered for.

In the circuit shown the control voltage for the two control loops is taken from the primary side of the transformer 4. However, it could equally be taken from the output side, although this would need the addition of extra components to derive the error signal. This could be effected by connecting a high-resis-

tance circuit across the output terminals, and deriving the error signal from a tapping thereon. This would, of course, introduce a current drain additional to that produced by the load to be supplied. Another possible way to derive an error signal is to connect a small resistor in screen with the load and to monitor the voltage between its ends to derive the error signal.

CLAIMS

1. A DC-to-DC converter which includes a switching transistor which is pulse-driven so as to cause a pulsed current to flow in a transformer, energy being stored in the transformer while the transistor conducts and being discharged into the load during the inter pulse gaps, a rectifier to which the output current from the transformer is applied to the load, pulse width control means connected to the transistor to control the on-off ratio thereof, a first feed back control loop via which an error signal derived from the transistor output is applied to a comparator for comparison with a reference signal, a connection from the output of the comparator to the pulse-width control means via which the pulse width is varied in accordance with the load's demand on the converter, and a second feed back control loop via which the error signal is used to limit the output of the converter when the load's demand reaches a preset maximum.

2. A converter as claimed in claim 1, and in which said second feed back control means includes a summing amplifier to which the error signal is applied and to which the input voltage is also applied so that variations in the input voltage do not cause the output of the converter to exceed said preset maximum.

3. A converter as claimed in claim 1 or 2, and in which said error signal is derived via a further rectifier circuit fed from the primary side of the transformer.

4. A converter as claimed in claim 1 or 2, and in which said error signal is derived via a further rectifier circuit fed from the output side of the transformer.

5. A DC-to-DC converter, substantially as described herein with reference to the accompanying drawing.

CLAIMS (21 Oct 1980)

6. A DC-to-DC converter, which includes a switching transistor which is pulse-driven so as to cause a pulsed current to flow in a transformer, energy being stored in the transformer while the transistor conducts and being discharged into the load during the inter-pulse gaps, a rectifier via which the output current from the transistor is applied to the load, pulse width control means connected to the base of the transistor to control the on-off ratio thereof, a first feed back control loop via which an error signal derived from the transistor output is applied to a comparator for comparison with a reference signal, said error signal being derived via a further rectifier circuit from the primary winding of the transformer, a connection from the output of the comparator to the pulse-width control means via which the pulse width is varied in accordance with the load's demand on the converter, as represented by the output of the comparator current, and a second feed back control loop via which the error signal derived via the further rectifier circuit is applied to a pulse width limiter which limits the width of the pulses applied to the transistor's base such that the output can be limited when the load's demand reaches or exceeds a preset maximum.

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