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(54) Address translation control system.

(57) The system comprises an address translation buffer (1) has entries each including a valid flag (V), a logical address field (LOG ADD), and a physical address field (PHY ADD), a memory array (10) having copies of the valid flag and the physical address field, and a purge register (7) for storing information showing a portion of the contents of the address translation buffer to partially purge the latter. In case of no coincidence between the physical address of the address translation buffer (1) and the contents of the purge register (7), the ordinary access processing can be carried out, and when the entry of the memory array (10) is accessed in turn and the coincidence between the physical address in the memory array and the contents of the purge register occurs, the partial purge is performed by clearing the valid flags of the corresponding entries of the address translation buffer (1) and the memory array. Thus, the partial purge processing can be carried out separately from the ordinary access processing, and the performance efficiency, particularly for the application of this invention to a pipeline system or a virtual machine, can be increased.

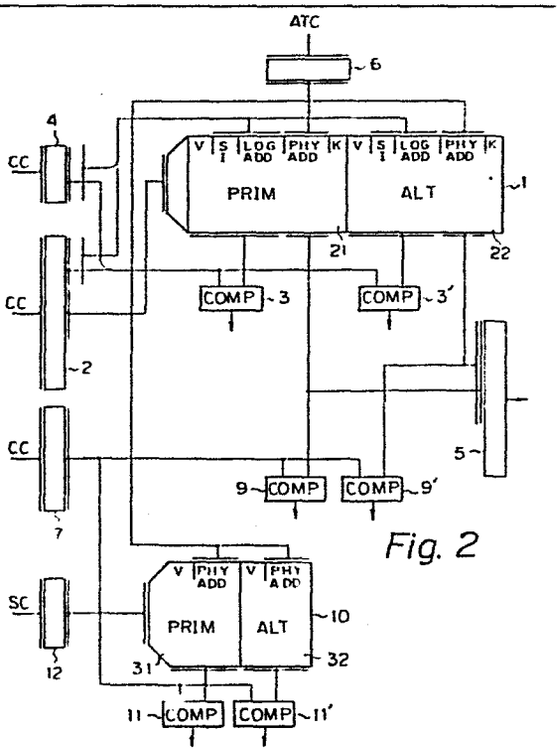

Fig. 2

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ADDRESS TRANSLATION CONTROL SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an address translation control system, more particularly to an address translation control system which, in addition to an address translation buffer performing a high speed translation from a logical address to a physical address, comprises a memory array copied from a portion of the contents of the address translation buffer, and in which a partial purge in the address translation buffer is performed by searching the memory array.

2. Description of the Related Art

In a data processing system using a virtual storage method, the translation from a logical address to a physical address at a high speed is performed by an address translation control system wherein address translated pairs of logical addresses and physical addresses are registered in a TLB (Translation Lookaside Buffer), i.e., an address translation buffer, and a high speed address translation is performed by accessing the address translation buffer.

The address translation buffer comprises a primary block and an alternate block, wherein each block has a plurality of entries. Each entry comprises a valid flag showing the validity of the entry, a multiple virtual storage identification field identifying a multiple virtual storage space, a logical address field, a physical address field, and a storage protection key field.

In a conventional address translation control system having such an address translation buffer, for an ordinary command fetch or operand access, the above-mentioned address translation buffer is accessed by applying a portion of the logical address to be translated, i.e., access address from an effective address register. By

this accessing, the entire contents of the accessed entry memorized in the primary block and the alternate block in the address translation buffer are read. A multiple virtual storage identification and the partial logical address which are read from the address translation buffer are compared with a multiple virtual storage identification from a multiple virtual storage identification register and another portion of the logical address from the effective address register, respectively. If the identifications of the comparing contents are obtained, the physical address in the entry is sent to a real address register as a physical address corresponding to a logical address in the effective address register.

In a virtual storage system, since the logical address covers a wider range than the utilizable physical address, a physical address, in turn, is allocated to another logical address when the physical address becomes non-utilizable. At that time, if a translation table in a main storage unit is renewed, since pairs of logical addresses and physical addresses translated before the renewal may remain in the address translation buffer, the pairs must be searched for and then purged. For this reason, in a conventional address translation control system, a partial purge method wherein each entry in the address translation buffer is searched for a physical address, is frequently used. According to this method, when a physical address to be purged is applied to a purge register, the access address in the effective address register is sequentially increased, an entry in the address translation buffer is sequentially read, the physical address in the purge register is compared with the physical address in the address translation buffer, and if the addresses are identical, a valid flag of the entry is made invalid.

In such a conventional address translation control system, when the partial purge is carried out,

since all the contents of the address translation buffer must be read out, there is a defect in that the address translation buffer cannot be used at an ordinary command fetch or operand access.

The above defect in the conventional address translation control system causes a decrease in the operating efficiency of the address translation buffer, and in particular a considerable reduction in the performance when using the pipeline method.

SUMMARY OF THE INVENTION

An object of the present invention is to provide an address translation control system wherein a partial purge of an address translation buffer can be processed separately from an ordinary command fetch or operand access, thus allowing no decrease in the operating efficiency of the address translation buffer, and achieving a high performance when using the pipeline method.

According to an aspect of the present invention there is provided an address translation control system comprising an address translation buffer having a plurality of entries each including at least a valid flag, a logical address field, and a physical address field; a memory array having copies of at least the valid flag and the physical address field in the contents of the address translation buffer; a purge register for storing information showing a portion of the contents of the address translation buffer, to partially purge the address translation buffer; a first comparator means for comparing the portion of the contents of the address translation buffer with the contents of the purge register; and a second comparator means for comparing the portion of the contents of the memory array with the contents of the purge register; wherein when the two applied contents do not coincide at the first comparator means, an ordinary access for the address translation buffer is processed; and when the entry of the memory

array is accessed in turn and the two applied contents coincide in the second comparator means, the partial purge is performed by clearing the valid flags of the corresponding entries of the address translation buffer and the memory array.

According to another aspect of the present invention there is provided an address translation control system comprising an address translation buffer having a plurality of entries each including at least a valid flag, a logical address field, a physical address field, and a virtual machine identification field; a memory array having copies of at least the valid flag, the physical address field, and the virtual machine identification field in the contents of the address translation buffer; a purge register for storing information showing a portion of the contents of the address translation buffer, to partially purge the address translation buffer; a first comparator means for comparing the partial contents in the address translation buffer with the contents of the purge register; a second comparator means for comparing the partial contents in the memory array with the purge register; a purge virtual machine identification register for storing a virtual machine identification to be purged; a third comparator means for comparing the contents of the virtual machine identification field in the address translation buffer with the contents of the purge virtual machine identification register; and a fourth comparator means for comparing the contents of the virtual machine identification field in the memory array with the contents of the purge virtual machine identification register; wherein when the coincidence in the first comparator means and the coincidence in the third comparator means does not occur, ordinary access for the address translation buffer is processed; and when the entry of the memory array is accessed in turn and the coincidence in the second comparator means and the coincidence in the

fourth comparator means occurs, the partial purge is performed by clearing the valid flags of the corresponding entry of the address translation buffer and the memory array.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block circuit diagram showing a conventional address translation control system;

Fig. 2 is a block circuit diagram showing an address translation control system according to a first embodiment of the present invention; and

Fig. 3 is a block circuit diagram showing an address translation control system according to a second embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Prior to the explanation of the embodiments of the present invention, a conventional address translation control system is explained with reference to Fig. 1, to supplement the above-mentioned prior art description and as a comparison with the embodiments of the present invention.

In the system in Fig. 1, for an ordinary command fetch or operand access, the address translation buffer 1 is accessed by applying a portion of the logical address to be translated, i.e., an access address from an effective address register 2. By this accessing, the entire contents of the accessed entry memorized in the primary block (PRIM) 21 and the alternate block (ALT) 22 in the address translation buffer 1 are read. A multiple virtual storage identification and a partial logical address in each entry, read from the address translation buffer 1 are compared with a multiple virtual storage identification from a multiple virtual storage identification register 4 and a corresponding partial logical address from the effective address register 2, respectively, at the comparator 3 for the primary block 21 and at the comparator 3' for the alternate block 22. If the identifications of the comparing contents are obtained,

the physical address in the entry is sent to a real address register 5 as a physical address corresponding to a logical address in the effective address register 2.

When the logical address from the effective address register 2 is not stored in the address translation buffer 1, the physical address is obtained by the address translation means using a translation table in a main storage unit. The obtained physical address is sent to a registration register 6 and registered in the address translation buffer 1 with a portion of the logical address and the like.

In a virtual storage system, since the logical address covers a wider range than the utilizable physical address, a physical address, in turn, is allocated to another logical address when the physical address becomes non-utilizable. At that time, if a translation table in a main storage unit is renewed, since pairs of logical addresses and physical addresses translated before the renewal may remain in the address translation buffer 1, the pairs must be searched for and then purged. For this reason, in a conventional address translation control system, as shown in Fig. 1. a partial purge method wherein each entry in the address translation buffer 1 is searched for a physical address, is frequently used. According to this method, when a physical address to be purged is applied to a purge register 7, the access address in the effective address register 2 is sequentially increased, an entry in the address translation buffer 1 is sequentially read, and the physical address in the purge register 7 is compared with the physical address in the address translation buffer 1 at a comparator 8 for the primary block 21 and at a comparator 8' for the alternate block 22. If coincidence is obtained at the comparators, the valid flag of the corresponding entry is made invalid.

When performing partial purging, in such a conventional address translation control system, since the

entire contents of the address translation buffer 1 must be read, there is a defect in that the ordinary command fetch operand access cannot be performed using the address translation buffer 1 during the term of the partial purging.

While, even when the coincidence is obtained at the comparator 3 or 3', the stored physical address sometimes cannot be referred. Namely, when the physical address is identical with the physical address set in the purge register 7, the result is as mentioned above; because, in this case, the remaining physical addresses not yet purged in the address translation buffer 1 still exist.

Now, a first embodiment of the present invention is explained with reference to Fig. 2. In Fig. 2, an address translation buffer 1, an effective address register 2, comparators 3 and 3', a multiple virtual storage identification register 4, a real address register 5, a registration register 6, and a purge register 7 are respectively the same as that of the conventional system in Fig. 1. Therefore the same elements are referred by the same reference numbers hereinafter.

The address translation control system of the first embodiment comprises, in addition to the above-mentioned elements, a first comparator means which consists of a comparator 9 for the primary block 21 and a comparator 9' for the alternate block 22 in the address translation buffer 1, for comparing the physical address stored in the address translation buffer 1 with the physical address set in the purge register 7, a memory array 10 for storing the copies of the valid flags (V) and the physical addresses (PHY ADD) in the address translation buffer 1, a second comparator means which consists of a comparator 11 for the primary block 31 and a comparator 11' for the alternate block 32, for comparing the physical addresses stored in the memory array 10 with the physical addresses set in the purge register 7, and

an access address register 12 for accessing the memory array 10. The memory array 10 is connected to the registration register 6.

The operation of the system of the first embodiment is explained as follows. For the ordinary command fetch or operand access, the address translation buffer 1 is carried out by supplying a portion of a logical address to be translated, i.e., an access address from the effective address register 2. By this access, the entire contents of the entry included in the primary block 21 and the alternate block 22 are read out. Multiple virtual storage identifications and portions of the logical addresses from the read out entry are compared with a multiple virtual storage identification from the multiple virtual storage identification register 4 and a portion of the logical address from the effective address register 2, respectively, using the comparators 3 and 3'. Further, the physical addresses of the read out entry are compared with the physical address set in the purge register 7 using the comparators 9 and 9'.

When in either comparator 3 for the primary block 21 or comparator 3' for the alternate block 22, the coincidence is not obtained, the address translation is performed by an address translation means (not shown) using an address translation table stored in a main storage unit. The physical address thus obtained is set in the registration register 6, and a valid flag (V), a multiple virtual storage identification (SI), a logical address (LOG ADD), a physical address (PHY ADD), and a storage protection key (k) are then registered in the address translation buffer 1. The address in the address translation buffer 1, wherein the above-mentioned valid flag and the like are stored, is also set in the access address register 12. Copies of the valid flag (V) and the physical address (PHY ADD) registered in the address translation buffer 1 are stored in the address of the memory array accessed from the access

address register 12. Then, the address for the next command fetch or operand access is again set in the effective address register 2 and the address translation buffer 1 is accessed.

When the coincidence of the comparing inputs is obtained at either comparator 3 or 3', if at least one of the physical addresses from the read out entry coincide with the physical address set in the purge register 7 using the comparators 9 and 9', the partial purge operation is not completed and the physical address to be purged remains in the address translation buffer 1. Therefore, the physical address cannot be used. In this case, the command fetch or operand access is controlled to inhibit the translation thereof. Thus, if the coincidence at the comparator 9 or 9' does not occur, the ordinary access is allowed to use the address translation buffer 1 without waiting for the completion of the partial purge.

If the coincidence at either comparator 3 or 3' does occur, when the physical address of the read out entry is not identical with the physical address set in the purge register 7 using the comparators 9 and 9', the physical address of the read out entry is sent to the real address register 5. Then, the physical address is used, for example, as an access address for a buffer storage unit or a main storage unit.

The operation where the partial purge is performed is explained below. When the physical address to be purged is set in the purge register 7, the access address in the access address register 12 increases sequentially and the entry of the memory array 10 is accessed in turn. In the access of each entry, the physical address is compared with the physical address in the purge register 7 using the comparators 11 and 11'. If the coincidence in the comparators is obtained, the accessed address is applied again to the access address register 12 as an input. Simultaneously, the accessed

address is also set in the effective address register 2. Then, the corresponding entries in the address translation buffer 1 and the memory array 10 are accessed and the valid flags of the entries are made invalid. After all the entries of the memory array 10 are searched for by the indication of the access address register 12, the partial purge operation ends and the purge register 7 becomes empty.

As explained above, the partial purge is carried out by using the memory array 10, therefore, for the ordinary command fetch or operand access, the address translation buffer 1 can operate separately from the partial purge. Thus, the confinement for the ordinary access using the address translation buffer 1 by the partial purge operation does not occur. As far as the coincidence in the comparator 9 or 9' is not detected, the physical address from address translation buffer 1 can be applied effectively.

Figure 3 is a block circuit diagram of an address translation control system applied in a virtual machine according to a second embodiment of the present invention. The virtual machine comprises a plurality of operating systems and a control program by which these operating systems operate simultaneously using one real computer. The control program is allocated in the main storage unit by adding a virtual machine identification (VI) to the plurality of operating systems.

The virtual machine identification is registered in the entry of the address translation buffer 1, therefore, the once-registered virtual machine identification must be partially purged if operation of the corresponding virtual machine is no longer needed or if the virtual machine identification is allocated to another virtual machine due to the capacity of the main storage unit. In this case, as for the first embodiment, the system comprises a memory array and performs a partial purge using the memory array.

In Fig. 3, the elements having the same function as those in Fig. 2 are referred to by the same reference numerals. Further, the virtual machine identification (VI) is registered in the address translation buffer 1, which includes a primary block (PRIM) 23 and an alternate block (ALT) 24. Stored in the memory array 10, which includes a primary block (PRIM) 33 and an alternate block (ALT) 34, are the copies of valid flags (V), virtual machine identifications (VI), and physical addresses (PHY ADD) in the contents of the address translation buffer 1. In this embodiment, the system further comprises a virtual machine identification register 13, a purge virtual machine identification register 14 to set a virtual machine identification to be partially purged, a first comparator means including comparators 15 and 15', a second comparator means including comparators 16 and 16', a third comparator means including comparators 17 and 17', and a fourth comparator means including comparators 18 and 18'. The virtual machine identification register 13 is connected to the memory array 10.

In the comparators 3 and 3', the multiple virtual storage identification (SI), the virtual machine identification (VI), and the logical address (LOG ADD) in each entry of the address translation buffer 1 are compared with the multiple virtual storage identification from the multiple virtual storage identification register 4, the virtual machine identification from the virtual machine identification register 13, and the logical address from the effective address register 2, respectively.

In the comparator 15 and 15', the physical addresses of the entry in the address translation buffer 1 are compared with the physical address from the purge register 7. In the comparator 17 and 17', the virtual machine identifications from the address translation buffer 1 are compared with the contents of the purge

virtual machine identification register 14. In the comparators 16 and 16', the physical addresses from the memory array 10 are compared with the physical address from the purge register 7. In the comparators 18 and 18', the virtual machine identifications from the memory array 10 are compared with the contents of the purge virtual machine identification register 14.

The operation of this embodiment is basically the same as that of the embodiment of Fig. 2. The partial purge can be carried out with reference to the virtual machine identification.

In addition, the reference letters indicating input units are as follows: ATC (address translation circuit), CC (command control unit), and SC (storage control unit). The output of the real address register 5 is applied to the main storage unit as an access address. The output of the comparators is used as a control signal to control the system as mentioned above.

CLAIMS

1. An address translation control system comprising an address translation buffer having a plurality of entries each including at least a valid flag, a logical address field, and a physical address field; a memory array having copies of at least said valid flag and said physical address field in the contents of said address translation buffer; a purge register for storing information showing a portion of the contents of said address translation buffer to partially purge said address translation buffer; a first comparator means for comparing the portion of the contents of said address translation buffer with the contents of said purge register; and a second comparator means for comparing the portion of the contents of said memory array with the contents of said purge register;

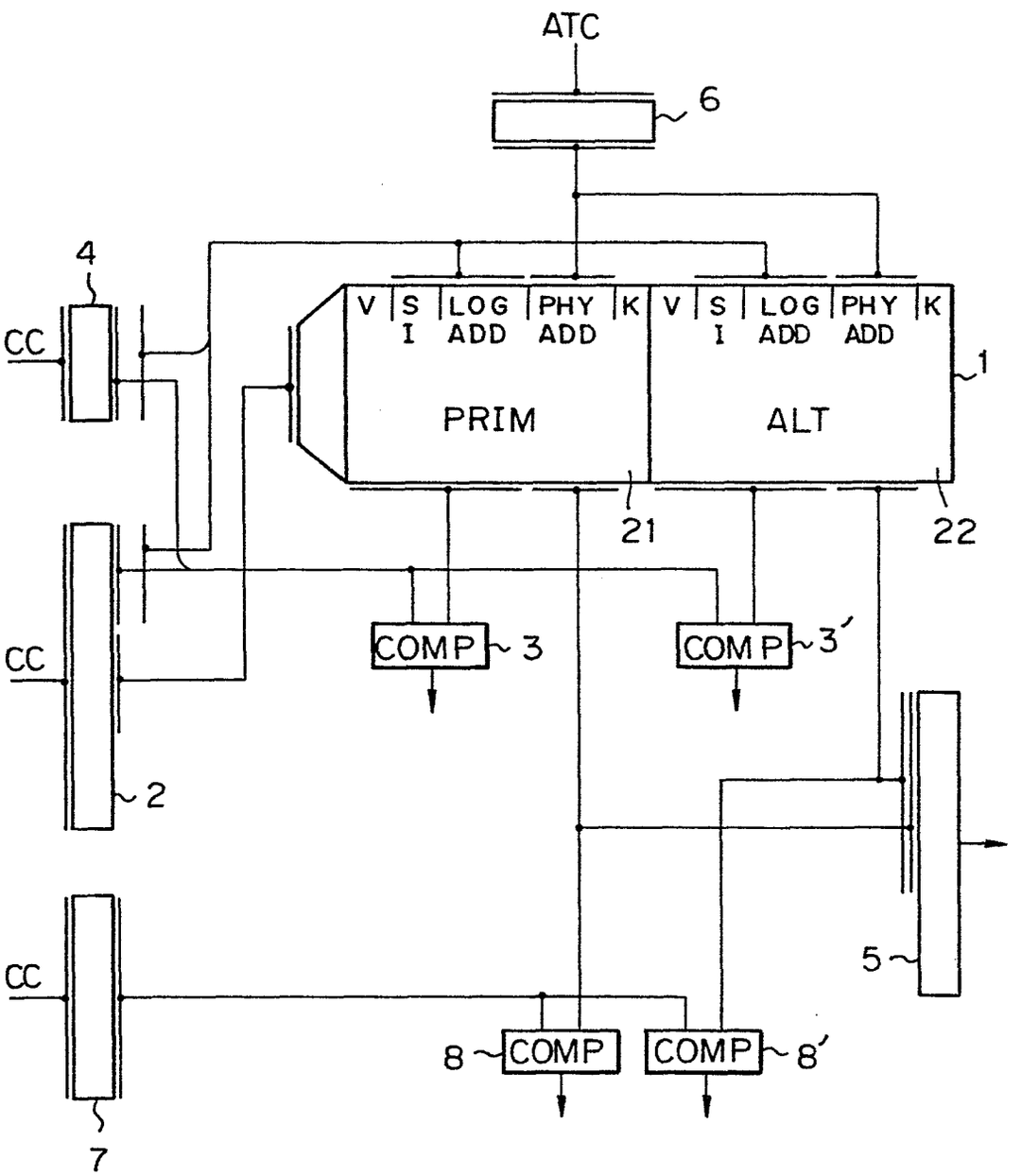
when the two applied contents do not coincide at said first comparator means, the corresponding physical address read out from said address translation buffer being utilized; and when the entry of said memory array is accessed in turn and the two applied contents coincide in said second comparator means, the partial purge being performed by invalidating said valid flags of the corresponding entries of said address translation buffer and said memory array.

2. An address translation control system comprising an address translation buffer having a plurality of entries each including at least a valid flag, a logical address field, a physical address field, and a virtual machine identification field; a memory array having copies of at least said valid flag, said physical address field, and said virtual machine identification field in the contents of said address translation buffer; a purge register for storing information showing a portion of the contents of said address translation buffer to partially purge said address translation buffer; a first comparator means for comparing the

partial contents in said address translation buffer with the contents of said purge register; a second comparator means for comparing the partial contents in said memory array with said purge register; a purge virtual machine identification register for storing a virtual machine identification to be purged; a third comparator means for comparing the contents of said virtual machine identification field in said address translation buffer with the contents of said purge virtual machine identification register; and a fourth comparator means for comparing the contents of said virtual machine identification field in said memory array with the contents of said purge virtual machine identification register;

when the coincidence in said first comparator means or the coincidence in said third comparator does not occur, the corresponding physical address read out from said address translation buffer being utilized; and when the entry of said memory array is accessed in turn and the coincidence in said second comparator means or the coincidence in said fourth comparator means occurs, the partial purge being performed by invalidating said valid flags of the corresponding entry of said address translation buffer and said memory array.

Fig. 1


ATC
6
4
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V
S I
LOG ADD
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V
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Fig. 2

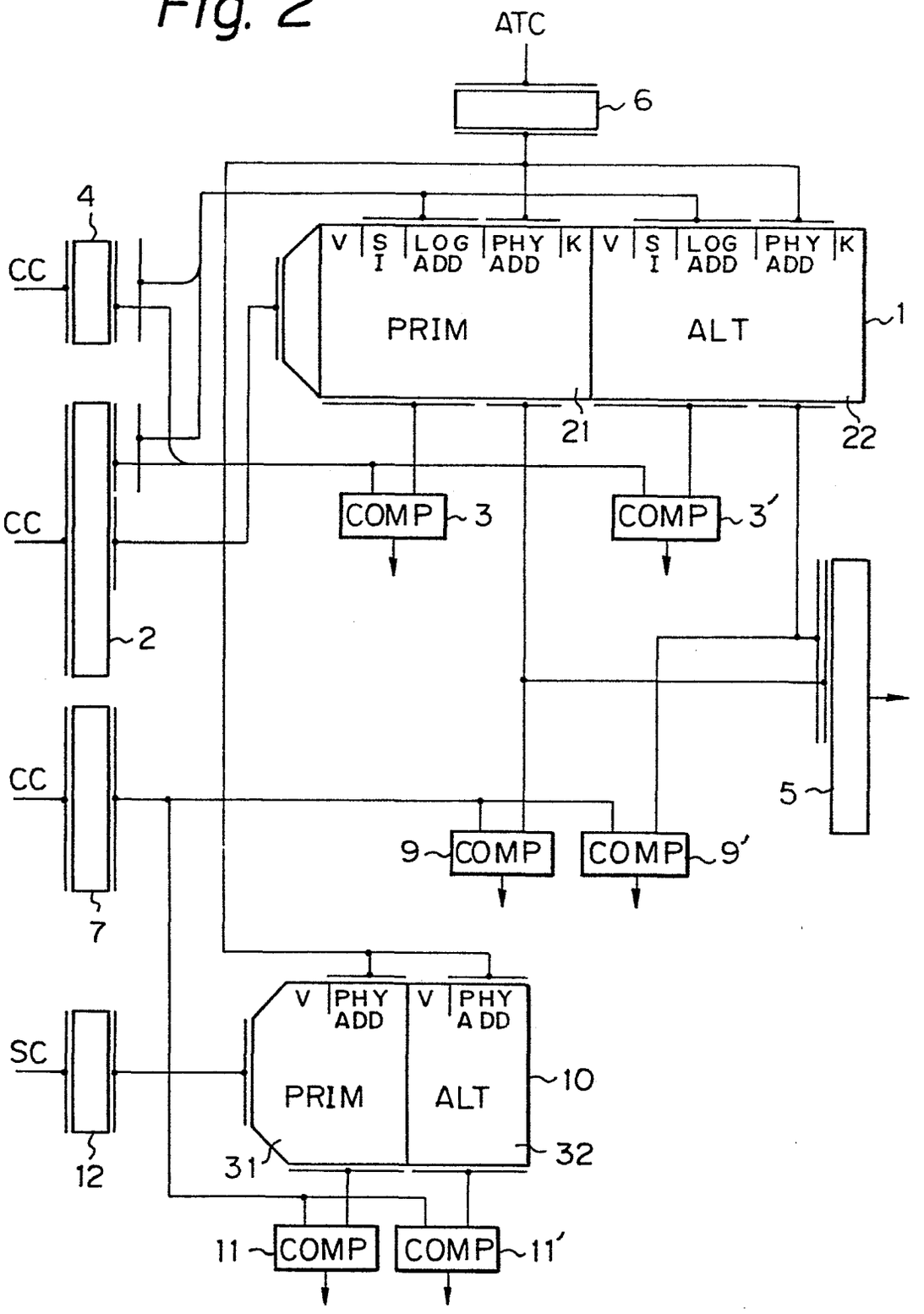
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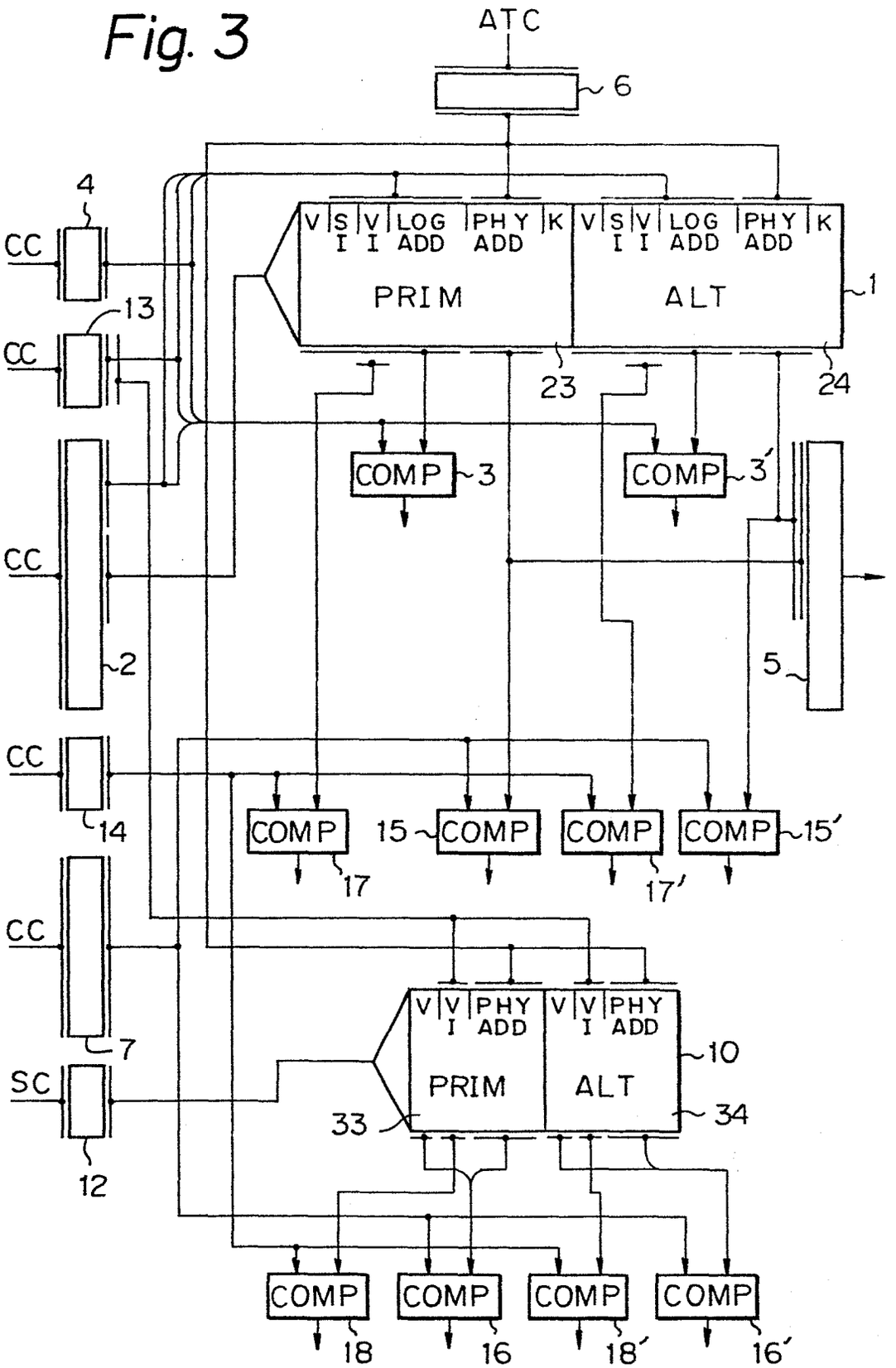
Fig. 3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