(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(10) International Publication Number
WO 2021/148980 A1

(43) International Publication Date
29 July 2021 (29.07.2021)

(51) International Patent Classification:
G03F 7/20 (2006.01) *H01L 29/66* (2006.01)
H01L 27/02 (2006.01) *H01L 29/94* (2006.01)
H01L 23/00 (2006.01) *G03F 1/00* (2012.01)
G03F 1/38 (2012.01)

(21) International Application Number: PCT/IB2021/050459

(22) International Filing Date: 21 January 2021 (21.01.2021)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
20305045.5 21 January 2020 (21.01.2020) EP

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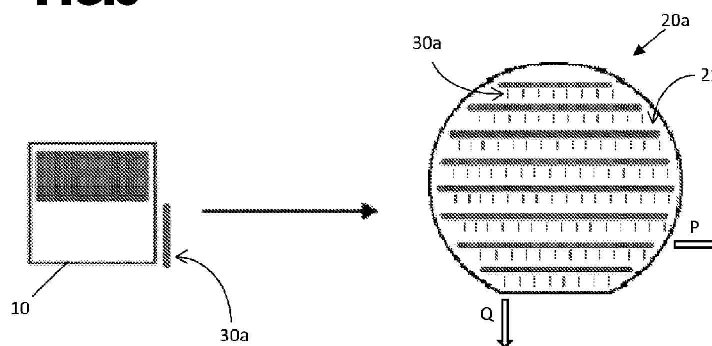
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

(54) Title: METHODS OF MANUFACTURING IC DEVICES ON WAFERS, ASSOCIATED WAFERS AND RETICLES

FIG.5



(57) Abstract: In the case of reproducing across a wafer (20) surface a first set of repetitions of an integrated circuit (10), the integrated circuit comprising structures extending in the thickness-direction of the wafer and comprising a first region (A) where the concentration of thickness-direction structures is high and a second region (B,C) where there are no thickness-direction structures or their concentration is low, and first regions (A) of the integrated circuits are aligned in rows extending in a first direction (P) across the wafer, wafer warpage can be reduced by providing compensation elements (30a) in the same wafer surface. The compensation elements (30a) each comprise a set of one or more slots, the slot depth extending in the thickness direction of the wafer, and the slot length extending in a second direction (Q) transverse to the first direction(P).

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Published:

— *with international search report (Art. 21(3))*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*
— *in black and white; the international application as filed contained color or greyscale and is available for download from PATENTSCOPE*

METHODS OF MANUFACTURING IC DEVICES ON WAFERS, ASSOCIATED WAFERS AND RETICLES

Field of the Invention

5 The present invention relates to the field of semiconductor manufacture and, in particular, to methods of manufacturing integrated circuit (IC) devices on wafers, to wafers, and to reticles, for reduction of warping or stress in wafers.

Technical Background

10 In semiconductor manufacture it is commonplace to reproduce an integrated circuit (die) multiple times over the surface of a wafer and then to separate the individual ICs by cutting the wafer along dicing lanes. During the process of reproducing the IC multiple times over the wafer surface, light is shone through a reticle to define patterning for a layer in or on the wafer. The reticle usually defines 15 patterning for one circuit, or for a small number of instances of the circuit, so a stepper translates the position of the reticle relative to the wafer by small steps in the x and/or y directions in-between successive illumination steps, until the full useful surface of the wafer has been exposed. Spaces are left in-between the various instances of the circuit on the wafer, so that singulation of the dies (scribing or dicing 20 of the wafer to separate the individual ICs) does not damage active parts of the circuitry.

During semiconductor manufacture, stresses can arise in the semiconductor wafer due to a number of causes, and the stresses can lead to warping of the wafer. For example, the different materials present in the wafer may have different 25 coefficients of thermal expansion and this can lead to creation of stress as the temperature changes. Whatever the origin of the stress/warping, if it becomes sufficiently extreme it may become difficult or impossible to complete the manufacturing process, for example, because the wafer becomes too fragile to be handled, without breaking, using conventional handling apparatus. Various 30 proposals have been made to tackle the problem of stress/warping of semiconductor wafers due, for example, to thermal effects, such as US 8080870 and US 2014/374914.

US 6337498 and US 2014/0175541 describe techniques for overcoming stress in a wafer that results from an elongate shape of certain repeated structures that are etched in the wafer surface, e.g. a set of parallel elongated trenches (i.e. trenches having an elongate cross-sectional shape). When the temperature of the wafer changes, the stresses in the direction parallel to the long axis of the trenches are different from the stresses in the direction parallel to the short axis of the trenches. Both documents suggest that stresses arising for this reason can be reduced by adding rotated sets of trenches in the wafer, arranged at 90° to the original orientation.

The present inventors have realized that there is a specific cause of stress/warping in semiconductor wafers that has not been recognized previously. In particular, significant stresses may arise in a case where the basic circuit being reproduced across the wafer is asymmetrical in terms of the distribution therein of structures that extend in the thickness direction of the wafer, notably 3D structures that extend 1-60μm (or more) in the depth-direction of the wafer.

It should be emphasized that the stress problem considered here is not stress derived from an elongated shape of 3D structures formed in the depth direction of the wafer but rather stress deriving from a different phenomenon, namely due to the fact that the basic circuit comprises a first region having a large number of depth-direction structures and a second region having no, or few, depth-direction structures and the fact that when the basic circuit is repeated across a wafer according to conventional manufacturing practices the first regions tend to align.

For example, in a case where the circuit to be reproduced contains a large number of three-dimensional structures – for example 3D capacitors, through vias, etc. - the circuit may require a large number of deep holes, or pillars, to be formed in the wafer. The situation may arise that the distribution of the capacitors within the circuit is uneven, e.g. a region on one side of the circuit may have a large number of deep holes, trenches or pillars, whereas the remainder of the circuit may have no or few holes/trenches/pillars. When a circuit of such a type is reproduced across the wafer, the regions containing holes/trenches/pillars tend to align with one another and the regions lacking holes/trenches/pillars (or having few holes/trenches/pillars) also tend to align with one another, resulting in macroscopic features extending

across the wafer and causing stresses in a preferential direction. This phenomenon is illustrated in Figs.1 and 2.

Fig.1 is a plan view of an integrated passive device 1 which has a first region, A, in which there is a high density of holes in the thickness direction of the wafer. In this example, the holes contain dielectric and electrode layers forming 3D capacitors. The regions A are represented as dark rectangles in Fig.1 and in Figs.2-5 discussed below. The remainder of the circuit (regions B and C) has no holes but in region C there is surface metallization, e.g. a metal electrode-pad having width of 2mm and length of 1mm is provided on the surface of the circuit. It can be understood that in this device 10 there is a highly uneven distribution of structures that extend in the thickness direction (into the page), with many thickness-direction structures present in the region A and none in the regions B and C.

Fig.2 is a diagram illustrating the result of reproducing the circuit 1 of Fig.1 using a reticle and stepper in a conventional manner. It can be seen from Fig.2 that when the integrated device of Fig.1 is reproduced across a wafer 2 in a conventional manner, the regions A having a high density of thickness-direction structures line up with one another, and the regions B, C having a low density of thickness-directions structures also line up with one another. This produces elongated linear regions L having a high density of thickness-direction structures, these linear regions L extend across the wafer in a preferential direction (the side-to-side direction in Fig.2) and this produces macroscopic stress effects leading to warping of the wafer.

Indeed, when the circuit of Fig.1 is reproduced across a silicon wafer of diameter 15 cm (6-inch wafer), it has been found not only that the wafer warps but also that the curvature across the width of the wafer (i.e. in the side-to-side direction of Fig.2) is significantly different from the curvature across the length of the wafer (i.e. in the top-to-bottom direction of Fig.2) both in magnitude and in direction. When the curvature is expressed as a diameter of a circle containing the curved surface, the diameter is 11m and -112m in the two directions, respectively. This high degree of warping, and the difference between the curvatures in the two directions, can make processing of the wafer using conventional manufacturing apparatus difficult, or even impossible.

Once again, it should be noted that the stress problem discussed with reference to Figs.1 and 2 is independent of whether or not the individual 3D structures whose concentration is non-uniform within the basic circuit have an elongated shape. Indeed, this particular problem arises even in the case of 3D structures that are holes or pillars having cross-section that is circular or shaped as a regular polyhedron, pillars having a cross-section shaped like a triskelion, etc.

Fig.3 illustrates one approach that could be taken in an attempt to reduce the macroscopic stresses caused when the circuit reproduced across a wafer 2a has a high degree of non-uniformity in the distribution of thickness-direction structures, notably a high concentration of 3D structures at one side of the circuit. According to the illustrated approach, a certain number of repetitions of the circuit are omitted at locations, O, which interrupt the linear structures that would otherwise form across the wafer. However, this approach has the disadvantage of reducing the manufacturing yield because, typically, the number of circuits that could be produced on a given wafer would be approximately halved.

KR 20010037889 describes techniques for manufacturing plural repetitions of a merged memory and logic (MML) device on a wafer, in the case where the basic MML device has a memory array portion (containing arrayed patterns) and a logic circuit portion (containing randomly-arranged patterns). KR 20010037889 teaches that accurate representations of the desired circuit patterns fail to be produced on the wafer because photolithographic processes have difficulties due to the heterogeneous layout of patterns in the memory array portion and in the logic circuit portion of the MML devices. Accordingly, this document proposes inverting the circuit orientation between the top half of the wafer and the bottom half of the wafer, or between adjacent devices on a row spanning the width of the wafer. KR 20010037889 does not discuss stress in the wafer.

The present invention has been made in the light of the above problems.

Summary of the Invention

The present invention provides a method of manufacturing integrated circuit devices on a wafer, comprising:

forming in a first surface of the wafer a first set of repetitions of an integrated circuit, said integrated circuit comprising structures extending in the thickness-

direction of the wafer and said integrated circuit comprising a first region where the concentration of thickness-direction structures is high and a second region where there are no thickness-direction structures or the concentration of thickness-direction structures is low, wherein the positions of the integrated circuits of the first set on
5 the wafer cause alignment of the first regions of said integrated circuits in rows extending in a first direction across the wafer, and

forming, in said first surface of the wafer, compensation elements each comprising a set of one or more slots, the slot depth extending in the thickness direction of the wafer, and the slot length extending in a second direction, the second
10 direction being transverse to the first direction.

The manufacturing method according to the invention improves the uniformity of the distribution, across the wafer, of three-dimensional structures (i.e. structures that extend in the thickness direction of the wafer) in the case where the wafer is being used to manufacture multiple instances of an integrated circuit device
15 that has 3D structures unevenly distributed within it. The improved uniformity in the distribution of the 3D structures tends to even out stresses in different directions across the wafer, leading to reduced difference in the curvature of the wafer in different directions, and may reduce warping overall.

The compensation elements may be formed in different ways.

20 According to one approach that has been developed by the present inventors, the compensation elements would be formed by creating in the first surface of the substrate a second set of repetitions of the basic integrated circuit, having a rotated orientation on the wafer relative to the orientation of the integrated circuits of the first set. This amounts to forming the ICs on the wafer in more than one orientation.
25 This approach is simple to implement because the different orientations of the IC can be produced on the wafer using a reticle that has patterns corresponding to the different orientations of the IC, or the relative orientation of the wafer and a standard reticle (i.e. a reticle including one or more repetitions of a layer of the IC in a single orientation) can be changed, in rotation, between different exposures of the wafer.

30 According to a second approach that has been developed by the present inventors, and which is recited in the appended claims, in a case where the integrated circuits of the first set are formed on the wafer at positions causing alignment of

thickness-direction structures in rows extending in a first direction across the wafer, the compensation elements are formed, in the first surface of the substrate, to extend in a direction transverse to the first direction.

Compensation elements of the latter type, extending in a direction transverse to the first direction, may be formed in dicing lanes of the wafer. In such a case the compensation elements do not take up useful real estate on the wafer surface, and thus they leave space for formation of a large number of ICs on the wafer.

The compensation elements may be disposed between adjacent rows of aligned first regions of the integrated circuits. The compensation elements may be aligned, in the first direction, with the second regions of the integrated circuits

The second direction may be perpendicular to the first direction or in a range ±30° from the perpendicular to the first direction.

In the case where the first regions of the integrated circuits align in rows having line length L, each compensation element adjacent to a row having line length L may have a width in the range 5%-30% of the line length L. The set of slots in a compensation element may consist of a single slot having a width in the range 5%-30% of the line length L. The set of slots in a compensation element may consist of a group of a plurality of slots disposed side by side and the aggregate width of the group of slots may be in the range 5%-30% of the line length L.

In the above-described manufacturing method, there may be approximately one compensation element, or a plurality of compensation elements, per integrated circuit formed on the wafer.

The formation of compensation elements according to the invention can be achieved in an efficient manner, avoiding increase in the overall number of process steps, by using common process steps to form both the 3D structures in the integrated circuits of the first set and the compensation elements extending in the thickness-direction of the wafer. Thus, for example, both sets of structures can be patterned and etched in common patterning and etching processes. Accordingly, wafer warping can be reduced without significant increase in complexity of the manufacturing process.

In a similar manner, in some embodiments of the invention common process steps can be used to deposit material in the thickness-direction structures in the first

set of integrated circuits and to deposit the same material in the compensation elements that extend in the thickness direction of the wafer. So, for example, if the 3D structures in the IC are 3D trench capacitors having dielectric and electrode layers extending conformally over wells in the wafer, the compensation elements can likewise be wells and the same dielectric and electrode layers can be deposited in the compensation elements in the same process step which deposits those layers in the 3D capacitors. Once again, this enables wafer warping to be reduced without significant increase in complexity of the manufacturing process. Moreover, by putting the same materials into the compensation elements as are put into the 3D structures of the IC, stress effects related to the nature of the filling materials will tend to be compensated more accurately.

The present invention further provides a wafer comprising:

in a first surface of the wafer, a first set of repetitions of an integrated circuit, said integrated circuit comprising structures extending in the thickness-direction of the wafer and said integrated circuit comprising a first region where the concentration of thickness-direction structures is high and a second region where there are no thickness-direction structures or the concentration of thickness-direction structures is low, wherein the positions of the integrated circuits of the first set on the wafer cause alignment of the first regions of said integrated circuits in rows extending in a first direction across the wafer, and

compensation elements each comprising a set of one or more slots, the slot depth extending in the thickness direction of the wafer, and the slot length extending in a second direction, the second direction being transverse to the first direction.

Wafers according to the present invention may tend to have less warping overall, and more even curvature in different directions, than comparable wafers which bear repetitions of an IC having a non-uniform distribution of 3D structures but lack the compensation elements.

In certain wafers embodying the invention, the compensation elements comprise a second set of repetitions of the integrated circuit, each disposed on the wafer in an orientation rotated relative to the orientation of the integrated circuits of the first set.

In certain wafers embodying the invention, the compensation elements may comprise compensation elements disposed in dicing lanes of the wafer.

In certain wafers embodying the invention, one or more materials are present in the thickness-direction structures of the integrated circuits of the first set and the same one or more materials are present in the compensation elements extending in the thickness-direction of the wafer.

The present invention further provides a reticle to pattern a layer of a wafer in manufacture of an integrated circuit, the integrated circuit comprising structures extending in the thickness-direction of the wafer and said integrated circuit comprising a first region where the concentration of thickness-direction structures is high and a second region where there are no thickness-direction structures or the concentration of thickness-direction structures is low, the reticle comprising:

a set of one or more first patterns corresponding to a layer of the integrated circuit and defining positions of a first set of the integrated circuits on the wafer causing alignment of the first regions of said integrated circuits in rows extending in a first direction across the wafer, and

a set of one or more second patterns corresponding to said layer of the integrated circuit, said second pattern defining compensation elements each comprising a set of one or more slots, the slot depth extending in the thickness direction of the wafer, and the slot length extending in a second direction, the second direction being transverse to the first direction.

The above-defined reticle makes it simple to fabricate a wafer comprising compensations structures as well as the repetitions of the integrated circuit.

Brief Description of the Drawings

Further features and advantages of the present invention will become apparent from the following description of certain embodiments thereof, given by way of illustration only, not limitation, with reference to the accompanying drawings in which:

FIG. 1 is a plan view illustrating an example of an integrated circuit (IC) that has a markedly different concentration of 3D structures in different regions thereof;

FIG. 2 is a diagram illustrating how reproduction of the circuit of Fig.1 leads to macroscopic features on a wafer;

FIG. 3 is a diagram illustrating a possible approach for breaking up the macroscopic features illustrated in Fig.2;

FIG. 4 is a diagram illustrating an example implementation of a first approach developed by the present inventors, using a first type of compensation element;

5 FIG. 5 is a diagram illustrating an example implementation of a second approach developed by the present inventors, using a second type of compensation element, according to an embodiment of the claimed invention;

FIGs. 6A and 6B are diagrams comparing wafer warpage when a first circuit is reproduced on a wafer, in which:

10 FIG.6A illustrates the warping of the wafer according to a first comparative example, and

FIG.6B illustrates the warping of the wafer according to an example implementation of the first approach developed by the present inventors;

FIGs. 7A-7C are diagrams comparing wafer warpage when a second circuit is 15 reproduced on a wafer, in which:

FIG.7A illustrates the warping of the wafer according to a second comparative example,

FIG.7B illustrates the warping of the wafer according to an example implementation embodying the invention (cross-sectional view), and

20 FIG.7C is a perspective view corresponding to the example implementation of FIG.7B.

Detailed Description of Example Embodiments

Principles of the present invention will become clear from the following description of certain example embodiments.

25 The example embodiments described below relate to fabrication of ICs containing so-called 3D capacitors, that is, capacitors formed using layers deposited over relief features in the wafer (e.g. dielectric and electrode layers formed over wells in the wafer, or dielectric and electrode layers formed over columns/pillars formed in the wafer). However, the skilled person will readily understand that the 30 same principles may be applied in cases where the IC being reproduced across the wafer has structures, other than capacitors, extending in the thickness direction of the wafer.

The present inventors have realized that, in the case where an IC being reproduced across a wafer has non-uniformity in the distribution therein of 3D structures (structures extending in the thickness direction of the wafer), warping of the wafer can be mitigated by forming compensation elements that tend to improve
5 the uniformity in the distribution of 3D structures over the wafer layout as a whole.

Factors which affect the degree of warpage of the wafer include the depth of the thickness-direction structures in the IC to be reproduced across the wafer, the shape of these structures, the number and distribution of such structures within the IC and across the wafer, and the nature of the materials used on the device. The
10 principles of the present invention can be applied to reduce wafer warpage by compensation that can be adapted to these different factors. Thus, in certain embodiments o the invention, the distribution and number of 3D compensation structures formed in the wafer can be set in a manner adapted to the depth, shape, distribution etc. of 3D structures in the IC.

15 A first approach that has been developed by the present inventors is illustrated by a diagram reproduced in Fig.4.

As illustrated in Fig.4, according to this first approach a first set 11 of repetitions of an IC 10 are provided on a wafer 20, distributed across a first surface, 21, of the wafer. The IC 10 has 3D capacitors formed therein primarily in a region
20 A of the circuit. The regions A are represented as solid, dark rectangles in Fig.4. In the example illustrated in Fig.4, when the first set 11 of repetitions of the IC 10 are reproduced on the wafer 20 they are aligned in a plurality of rows on the wafer surface and the regions A of the different ICs tend to line up, such that there is considerable lack of uniformity in the distribution across the wafer 20 of 3D structures
25 in the first set 11 of repetitions of the IC.

According to the first approach, compensation elements 30 are formed across the surface of the wafer 20, in the same surface as the 3D structures of the IC 10, and these compensation elements 30 correspond to rotated copies of the IC. The regions A in the compensation elements 30 are represented as hashed rectangles in
30 Fig.4. The compensation elements 30 are interposed between adjacent instances of the IC 10 along a row on the wafer surface. The interposing of the compensation elements 30 and their rotated orientation relative to the orientation of the first set

11 of repetitions of the IC 10 on the wafer surface 21, tends to render the distribution of 3D structures more uniform across the wafer surface as a whole.

In the example illustrated in Fig.4, the region A where the 3D structures are concentrated occupies approximately one half of the IC (when viewed in plan view). 5 Accordingly, an 180° rotation of the orientation of the circuit reverses the positions of the regions of the IC that have a high concentration and a low concentration of 3D structures. Thus, in this example, the compensation elements 30 correspond to the IC 10 rotated through 180°. However, the invention is not limited to this example. Depending on the distribution of 3D structures in the IC 10 the 10 compensation elements 30 may correspond to a rotation of the basic circuit through angles other than 180°. Furthermore, depending on the distribution of 3D structures in the IC 10 there may be different sets of compensation elements 30 oriented at different angles from each other and from the basic circuit 10.

In the implementation illustrated in Fig.4, because the compensation 15 elements 30 contain the same circuit components as the circuit 10, the materials and dimensions used therein are the same, with the consequence that the 3D structures in the compensation elements 30 have corresponding behavior (e.g. in term of thermal expansion) as the 3D structures in the first set of repetitions of the circuit 10. Accordingly, the stress-compensation achieved using the compensation 20 elements 30 is well-matched to the properties of the IC circuit 10.

An example implementation of a second approach that has been developed by the present inventors, which second approach is the object of the appended claims, will now be described with reference to Fig.5.

According to the second approach, compensation elements 30a are formed 25 across the surface of the wafer 20, in the same surface as the 3D structures of the IC 10, and these compensation elements 30a are configured to extend in a direction which is transverse to the direction in which regions A of the IC 10 tend to line up on the wafer. In the example illustrated in Fig.5, where the regions A of the IC 10 tend to line up in the widthwise direction of the wafer (as illustrated in the figure), 30 the compensation structures 30a are configured to extend in the up-and-down direction in the figure.

It is convenient to associate one compensation structure to each IC reproduced on the wafer surface, but this is not essential. The number and dimensions of the compensation elements 30a can be adjusted as convenient for the manufacturing process. By providing on the wafer surface 21 compensation elements 30a extending in a direction transverse to the alignment direction of regions A of the ICs, the distribution of 3D structures across the wafer surface as a whole becomes more uniform.

In the example illustrated in Fig.5, each compensation element 30a is a single elongated slot whose long direction extends in the direction Q transverse to the alignment direction P of the regions A on the wafer. In this specific example, the length direction of each compensation element 30a is approximately perpendicular to the alignment direction of the regions A. By extending in a direction that is perpendicular to the alignment direction P of the regions A of the IC that have a high-density of 3D structures, the compensation elements 30a have a large effect in helping to render the distribution of 3D structures over the wafer more uniform. However, the invention is not limited to compensation elements 30a that extend in the perpendicular direction. A certain degree of compensation is still obtained even when the compensation element 30a extends in a direction which is not strictly the perpendicular to the alignment direction of the regions A and, in particular, useful amounts of compensation are likely to be obtained in a range of ±30° from the perpendicular direction.

Fig.5 illustrates a single slot 30a, but the present embodiment is not limited to that case. Two, or more than two slots 30a may be used as each compensation element.

Fig.5 illustrates a case where there is one compensation element 30a per IC in the first set 11 of repetitions of the IC, but the present embodiment is not limited to that case. Two, or more than two compensation elements 30a may be used per IC on the wafer, provided that space allows.

In order to avoid wasting space on the surface of the wafer, it can be advantageous to form the compensation elements 30a at locations that are within, or overlap with, the dicing lanes allocated for dicing or scribing the wafer.

The width and length of the compensation structures 30a are primarily chosen to compensate for the unbalanced distribution of 3D structures in the ICs 10. These dimensions of the compensation elements 30a will tend to be set larger for increasing length of the line L of aligned 3D structures in the ICs 10 (see Fig.2). In certain preferred embodiments of the invention, the width of each compensation element is set in the range of 5% to 30% of the width of the 3D pattern line L, i.e. typically the width is set in the range of 30μm – 180μm. However, the invention is not limited to use of a width within this range.

In the case where the compensation element 30a consists of a single slot, and this slot has a width in the range of approximately 30μm to approximately 180μm, it is likely that empty space will remain within the slot even if material is deposited therein during process steps that deposit material in the 3D structures of the ICs. One or more other filling steps may be provided to fill up the empty space (thus avoiding ingress of particles, residues and the like during subsequent manufacturing processes).

In the case where each compensation element 30a consists in a set of slots disposed side by side, it is the total width of the group of slots that is controlled, for example, to be in the range 30μm – 180μm mentioned above. For instance, each compensation element 30a may be a set of 15 slots, each 1μm wide with a spacing of 1μm between adjacent slots in the group, resulting in a total width of 29μm (approximately 30μm).

As noted above, it is also advantageous when the compensation structures 30a fit in the sawing line. Given that a sawing line typically is 100μm wide, compensation elements having width in the range 30μm – 180μm can either be positioned wholly within the sawing lines or they can be positioned so that a large fraction of their width is co-located with the sawing lines.

In preferred embodiments of the invention, the length of pattern 30a is dependent on the length of the regions of the IC that have low density of 3D structures (i.e. the length of region B+C in the IC illustrated in Fig.1). For the IC illustrated in Fig.1, an appropriate length for the compensation element 30a is in the range from approximately from 1mm to approximately 1.5 mm.

In preferred embodiments of the invention, the slot(s) forming the compensation element 30a is (are) formed in one or more process steps which also form 3D structures in the IC 10. Accordingly, in such embodiments the depth of the slot 30a is the same as or close to the depth of the 3D structures in the IC 10. For 5 example, the slots of the compensation elements 30a may be etched in a step that also etches wells or pillars for use in forming 3D capacitors in the IC 10, or in a step that etches via-holes in the IC 10.

As noted above, it is preferable for the slots forming the compensation elements 30a not to be left empty, because this could cause issues during 10 lithographic processes performed afterwards during the manufacturing process. Accordingly, in certain embodiments of the invention material is deposited in the compensation elements 30a. In preferred embodiments of the invention, material is deposited into the slot(s) forming the compensation element 30a in one or more process steps which also deposit material to form components of the 3D structures 15 in the IC 10 (e.g. deposited material that forms dielectric and electrode layers in 3D capacitors, deposited material that forms conductive filling in a via, etc.). Accordingly, in such embodiments the materials in the slot 30a are the same as those present in the 3D structures in the ICs 10.

In some cases, it may be advantageous to use compensation elements 30a 20 as of the type illustrated in Fg.5 in preference to compensation elements 30 which correspond to a rotated copy of the basic IC. For example, if the IC has a significant aspect ratio (i.e. is significantly rectangular, rather than relatively square) it may be difficult to accommodate the compensation structures 30 among the ICs of the first set 11 without wasting space on the wafer surface. Also, it may be complicated for 25 pick-and-place equipment to adjust to the different orientations of the singulated devices after the wafer has been cut.

A method of manufacturing wafers such as the wafer 20 illustrated in Fig.4 and the wafer 20a illustrated in Fig.5 will be described below.

The manufacturing method comprises forming in a first surface of the wafer 30 a first set 11 of repetitions of the integrated circuit 10 which has structures extending in the thickness-direction of the wafer and these thickness-direction structures are laid out unevenly across the integrated circuit. The positions of the integrated

circuits 10 of the first set 11 on the wafer cause a non-uniform distribution of thickness-direction structures over the surface of the wafer. Accordingly, to improve the uniformity of distribution of 3D structures across the overall face of the wafer, the method also comprises forming, in the same surface of the wafer, compensation
5 elements that extend in the thickness direction of the wafer.

Different variants of the manufacturing method may be used to fabricate a wafer 20 as illustrated in Fig.4 or a wafer 20a as illustrated in Fig.5.

In the case of fabricating a wafer 20 as illustrated in Fig.4, one manufacturing method makes use of a special reticle (not shown) which has first and second
10 patterns corresponding to the different IC orientations to be formed on the wafer. More particularly, a set of one or more first patterns on the reticle are designed to form a layer of the integrated circuit 10 in its "normal" orientation (corresponding to the set of repetitions 11 on the wafer) whereas the reticle also has a set of one or more second patterns to form the corresponding IC layer in the rotated orientation
15 required for the compensation pattern 30. This new kind of reticle can be used to expose the wafer, and its position can be shifted using a stepper, according to known techniques.

A new reticle of this type is configured to pattern a layer of a wafer in manufacture of an integrated circuit, the integrated circuit comprising structures
20 extending in the thickness-direction of the wafer and the thickness-direction structures being laid out unevenly across the integrated circuit. The reticle comprises a set of one or more first patterns corresponding to a layer of the integrated circuit, and a set of one or more second patterns corresponding to said layer of the integrated circuit, said second pattern being a rotated version of said first pattern to
25 compensate for lack of uniformity in the distribution of thickness-direction structures in said integrated circuit. Such a reticle makes it simple to fabricate a wafer comprising compensations structures that are a rotated version of the basic IC, because the usual exposure and stepper devices can be used with the reticle to create the basic ICs and the compensation structures at the same time.

30 Another manufacturing method for fabricating a wafer 20 as illustrated in Fig.4, makes use of a standard type of reticle which has a set of one or more patterns on the reticle designed to form a layer of the integrated circuit 10. The surface of

the wafer can be exposed using this standard type of reticle in a first operation to define patterning on the wafer for forming ICs of the first set 11. The surface of the wafer can be exposed using this standard type of reticle in a second operation to define patterning on the wafer for forming the compensation elements 30. During
5 the second operation the relative orientation of the wafer and reticle is rotated relative to the orientation that exists during performance of the first operation.

Despite their names, the first and second operations can be performed in any order. Moreover, the translation of the position of the reticle relative to the wafer (e.g. using a stepper) may be performed at different stages in the process. Thus,
10 for example, the first and second operation may be performed in a given region of the wafer before the stepper translates the position of the reticle relative to the wafer. Alternatively, the stepping could be performed to implement one of the first and second operations over a large region of the wafer before changing the relative orientation of the wafer and reticle in rotation and performing the other of the first
15 and second operations over the large region of the wafer.

A manufacturing method for fabricating a wafer 20a as illustrated in Fig.5 may make use of a new reticle (not shown) that includes a pattern to form the compensation element 30a as well as a pattern to form the IC 10. The reticle can then be used to expose the wafer surface using standard exposure and stepper
20 devices.

Figs.6A-6B and 7A-7C illustrate how use of the techniques developed by the present inventors can reduce warping of a wafer.

FIGs. 6A and 6B are cross-sectional diagrams comparing warping of a wafer 2b in which repetitions of a first example circuit have been manufactured using
25 conventional techniques (first comparative example) and reduced warping that occurs for a wafer 20b manufactured using compensation elements 30 as in Fig.4.

FIGs. 7A and 7B are cross-sectional diagrams comparing warping of a wafer 2c in which repetitions of a second example circuit have been manufactured using conventional techniques (second comparative example) and reduced warping that
30 occurs for a wafer 20c manufactured using compensation elements 30ac which are of the general type illustrated in Fig.5.

Fig.7C is a perspective view of the wafer illustrated in Fig.7B and shows that, in this example, each IC has a region S where there is a high density of 3D structures and a region T where there are few 3D structures (even though other circuit elements, terminals, etc. may be present). In this example, each compensation element 30ac consists of a pair of elongated trenches extending in a direction Q which is substantially perpendicularly to the direction P in which the regions of the IC that have a high density of 3D structures align across the wafer. In this example, the compensation elements 30ac are aligned with the regions T of the ICs in the direction P. It can be seen that the addition of the compensation elements 30ac tends to improve the uniformity of the distribution of 3D structures across the surface 21 of the wafer 20c.

It can be seen from Figs.6A-7C that the techniques developed by the present inventors allow wafer warping to be reduced to a significant degree.

Additional Variants

Although the present invention has been described above with reference to certain specific embodiments, it will be understood that the invention is not limited by the particularities of the specific embodiments. Numerous variations, modifications and developments may be made in the above-described embodiments within the scope of the appended claims.

CLAIMS

1. A method of manufacturing integrated circuit devices on a wafer, comprising:

5 forming in a first surface of the wafer a first set of repetitions of an integrated circuit, said integrated circuit comprising structures extending in the thickness-direction of the wafer and said integrated circuit comprising a first region (A/S) where the concentration of thickness-direction structures is high and a second region (B,C/T) where there are no thickness-direction structures or the concentration of
10 thickness-direction structures is low, wherein the positions of the integrated circuits of the first set on the wafer cause alignment of the first regions (A/S) of said integrated circuits in rows extending in a first direction (P) across the wafer, and

forming, in said first surface of the wafer, compensation elements (30a) each comprising a set of one or more slots, the slot depth extending in the thickness
15 direction of the wafer, and the slot length extending in a second direction (Q), the second direction (Q) being transverse to the first direction (P).

2. The manufacturing method according to claim 1, wherein the compensation elements (30ac) are disposed between adjacent rows of aligned first
20 regions (A/S) of said integrated circuits.

3. The manufacturing method according to claim 1, wherein in said first direction (P) the compensation elements (30ac) are aligned with said second regions (B,C/T) of the integrated circuits.

25

4. The manufacturing method according to any one of claims 1 to 3, wherein said second direction (Q) is perpendicular to said first direction (P) or in a range ±30° from the perpendicular to the first direction.

30 5. The manufacturing method according to any one of claims 1 to 4, wherein said first regions (A/S) of said integrated circuits align in rows having line length L, and the forming of the compensation elements (30a) on the wafer

comprises setting the width, of each compensation element (30a) adjacent to a row having line length L, in the range 5%-30% of the line length L.

6. The manufacturing method according to claim 5, wherein the set of
5 slots in a compensation element (30a) consists of a single slot having a width in the range 5%-30% of said line length L.

7. The manufacturing method according to claim 5, wherein the set of slots in a compensation element (30a) consists of a group of a plurality of slots
10 disposed side by side and the aggregate width of the group of slots is in the range 5%-30% of said line length L.

8. The manufacturing method according to claim 1, wherein the forming of the compensation elements extending in said second direction transverse to the
15 first direction comprises forming compensation elements (30a) that are co-located with dicing lanes of the wafer.

9 The manufacturing method according to any previous claim, comprising common process steps to form the thickness-direction structures in the
20 first set of integrated circuits and to form the compensation elements (30a) extending in the thickness direction of the wafer.

10 The manufacturing method according to any previous claim, comprising common process steps to deposit material in the thickness-direction
25 structures in the first set of integrated circuits and to deposit said material in the compensation elements extending in the thickness direction of the wafer.

11. A wafer comprising:

in a first surface of the wafer, a first set of repetitions of an integrated circuit,
30 said integrated circuit comprising structures extending in the thickness-direction of the wafer and said integrated circuit comprising a first region (A/S) where the concentration of thickness-direction structures is high and a second region (B,C/T)

where there are no thickness-direction structures or the concentration of thickness-direction structures is low, wherein the positions of the integrated circuits of the first set on the wafer cause alignment of the first regions (A/S) of said integrated circuits in rows extending in a first direction (P)across the wafer, and

5 compensation elements (30a) each comprising a set of one or more slots, the slot depth extending in the thickness direction of the wafer, and the slot length extending in a second direction (Q), the second direction (Q) being transverse to the first direction (P).

10 12. A wafer according to claim 11, wherein said second direction (Q) is perpendicular to said first direction (P) or in a range ±30° from the perpendicular to the first direction.

13. A wafer according to claim 11 or 12, wherein said first regions (A/S) 15 of said integrated circuits align in rows having line length L, and the width, of each compensation element (30a) adjacent to a row having line length L, is in the range 5%-30% of the line length L.

14. A wafer according to any one of claims 11 to 13, wherein the 20 compensation elements comprise compensation elements (30a) co-located with dicing lanes of the wafer.

15. A reticle to pattern a layer of a wafer in manufacture of an integrated circuit, the integrated circuit comprising structures extending in the thickness-25 direction of the wafer and said integrated circuit comprising a first region (A/S) where the concentration of thickness-direction structures is high and a second region (B,C/T) where there are no thickness-direction structures or the concentration of thickness-direction structures is low, the reticle comprising:

a set of one or more first patterns corresponding to a layer of the integrated 30 circuit and defining positions of a first set of the integrated circuits on the wafer causing alignment of the first regions (S) of said integrated circuits in rows extending in a first direction (P) across the wafer, and

a set of one or more second patterns corresponding to said layer of the integrated circuit, said second pattern defining compensation elements (30a) each comprising a set of one or more slots, the slot depth extending in the thickness direction of the wafer, and the slot length extending in a second direction (Q), the
5 second direction (Q) being transverse to the first direction (P).

FIG.1

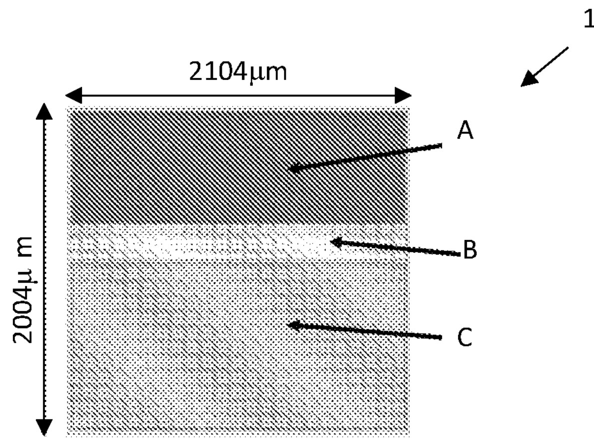


FIG.2

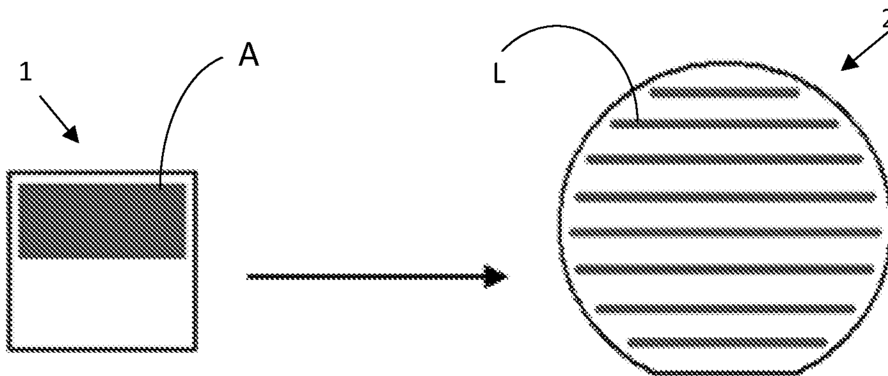
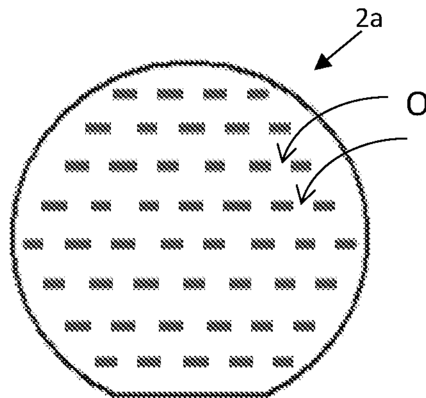


FIG.3



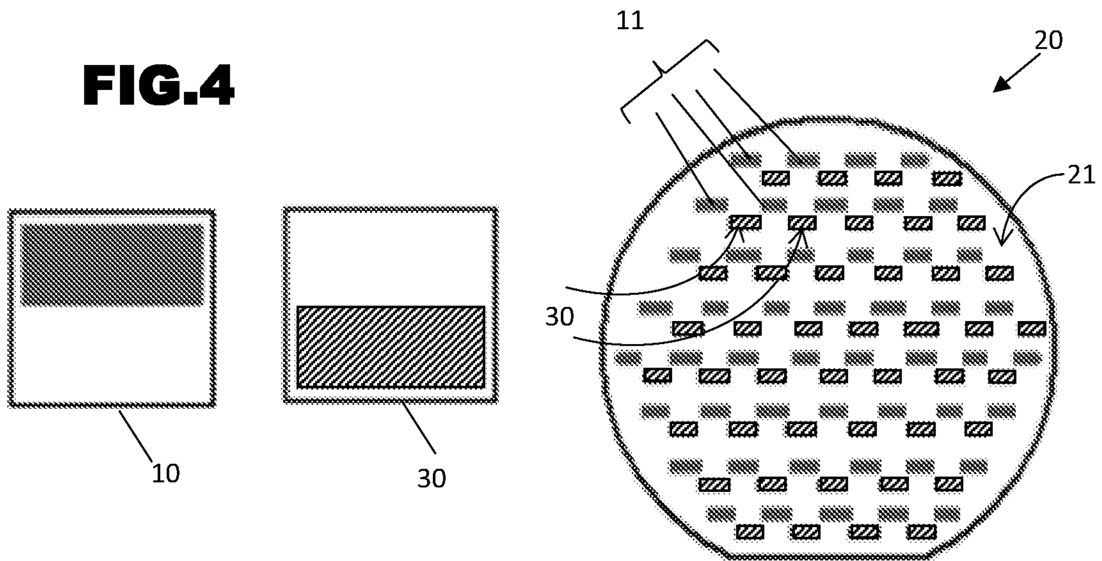


FIG.4
11
20
21
30
10
30

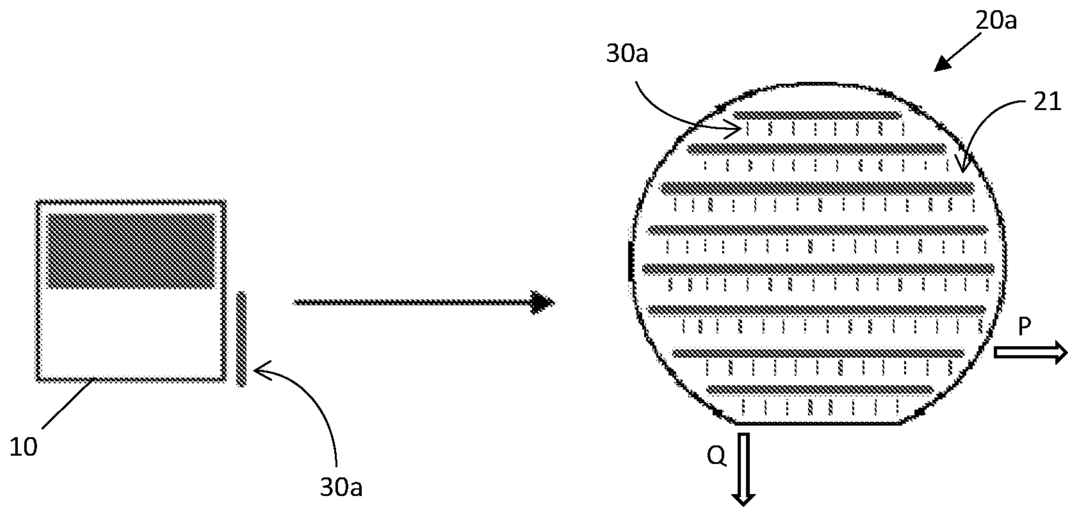


FIG.5
20a
30a
21
P
Q
10
30a

FIG.6A

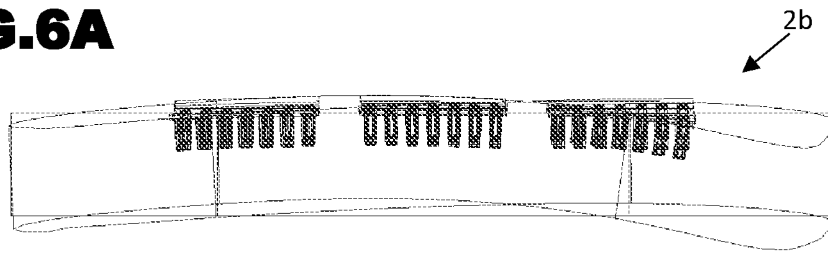


FIG.6B

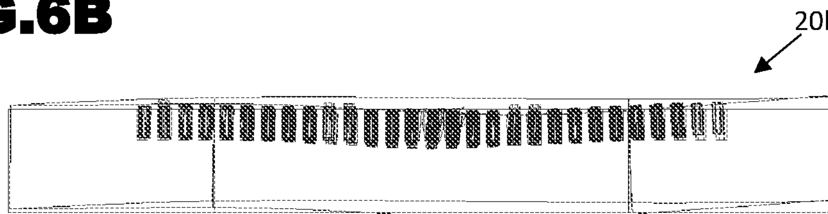


FIG.7A

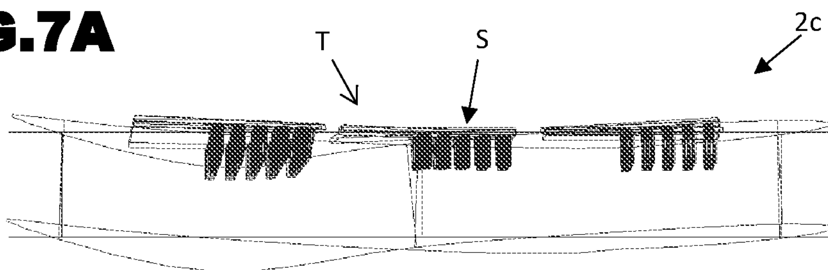


FIG.7B

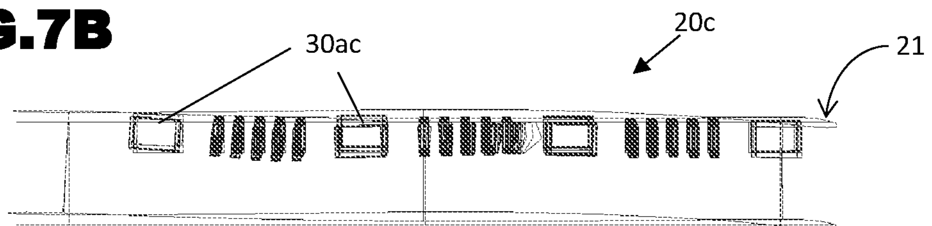
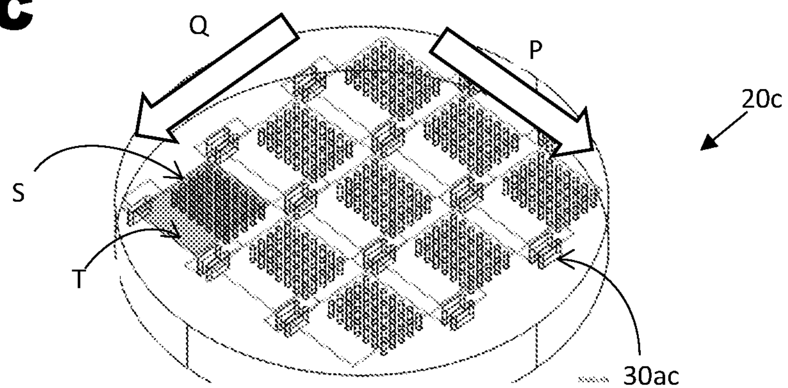


FIG.7C



INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2021/050459

A. CLASSIFICATION OF SUBJECT MATTER
INV. G03F7/20 H01L27/02 H01L23/00 G03F1/38 H01L29/66
H01L29/94
ADD. G03F1/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L G03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2018/005959 A1 (WANG XIAOBIN [US] ET AL) 4 January 2018 (2018-01-04) paragraph [0019] - paragraph [0020]; figures 1A, 5 paragraph [0027] paragraph [0035] paragraph [0047] -----	1,2,4, 9-12,15
X	US 2014/175541 A1 (MATRI ANGELO [IT] ET AL) 26 June 2014 (2014-06-26) paragraph [0030] - paragraph [0049]; figure 2B -----	1,3,5-8, 11,13,14
Y	KR 2001 0037889 A (HYNIX SEMICONDUCTOR INC [KR]) 15 May 2001 (2001-05-15) abstract; figures 3/5-4/5 ----- -/--	1,3,8, 11,14

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 June 2021	28/06/2021

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Hirsch, Alexander

6

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	KR 100 849 359 B1 (DONGBU ELECTRONICS CO LTD [KR]) 29 July 2008 (2008-07-29) paragraph [0043]; figures 4, 8d paragraph [0084] - paragraph [0085] paragraph [0050] paragraph [0021] - paragraph [0022] -----	1,3,8, 11,14

International application No.
PCT/IB2021/050459

INTERNATIONAL SEARCH REPORT

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. [ ] Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. [ ] Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. [ ] Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. [X] As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. [ ] As all searchable claims could be searched without effort justifying an additional fees, this Authority did not invite payment of additional fees.

3. [ ] As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. [ ] No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

[ ] The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

[ ] The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

[X] No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. claims: 1-4, 8-12, 14, 15

Manufacturing method, wafer and reticle, wherein a repetition region has an inhomogeneous distribution of a first set of structures, wherein high concentration sub-regions of multiple repetitions of said repetition regions line up in rows on a wafer and wherein respective low concentration sub-regions comprise an additional second set of structures, being called compensation elements, and extending as slots in traverse direction to said wafer rows.

1.1. claims: 1-3, 8, 11, 14, 15(completely); 4, 12(partially)

Compensation elements being arranged in various locations with respect to said wafer rows, namely
- between wafer rows,
- aligned with low concentration sub-regions in said row-direction or
- co-located with dicing lanes.

1.2. claims: 1, 9-11, 15(completely); 4, 12(partially)

First set of structures and compensation structures are formed and filled in common method steps.

1.3. claims: 1, 11(completely); 4, 12(partially)

Method of claim 1 and wafer of claim 11 for the case where "traverse direction" is limited to "perpendicular direction".

1.4. claims: 1, 11(completely); 4, 12(partially)

Method of claim 1 and wafer of claim 11 for the case where "traverse directions" lie in a range of +/- 30° from perpendicular but excluding perpendicular.

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2. claims: 5-7, 13

Compensation structures being slots, which have a width of 5-30% of a high density sub-region length in row direction, the width being constituted by one single slot or a group of slots.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2021/050459

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2018005959 A1	04-01-2018	CN 107564962 A	09-01-2018
		TW 201801186 A	01-01-2018
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KR 100849359 B1	29-07-2008	CN 101299129 A	05-11-2008
		KR 100849359 B1	29-07-2008