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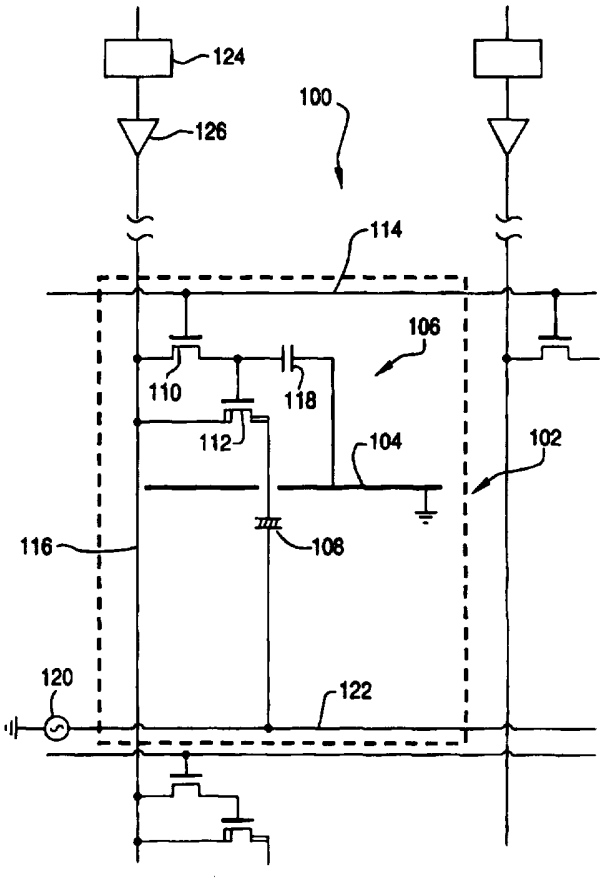
(57) Abstract

In an active matrix electroluminescent display, a pixel (102) containing a grounded conductive electric field shield (104) formed between an EL cell (108) and the switching electronics (106), thus any electric fields produced in the EL cell do not interfere with the operation of the switching electronics. In a method of fabricating the pixel, first, an EL cell switching circuit is formed, then an insulating layer (244) and the field shield (104) are sequentially formed thereon. Furthermore, the switching circuitry contains a low voltage MOS transistor (110) and a high voltage MOS transistor (112). When activated, the low voltage transistor activates the high voltage transistor by charging the gate of the high voltage transistor. Additionally, to improve the breakdown voltage of the high voltage transistor, a capacitive divider network (400) is fabricated proximate the drift region of that transistor.



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ACTIVE MATRIX ELECTROLUMINESCENT DISPLAY PIXEL AND METHOD OF FABRICATING SAME

The United States Government has rights in the invention pursuant to Contract No. MDA972-92-C-0037.

The invention relates to active matrix electroluminescent displays and, more particularly, to an electroluminescent display pixel having an electric field shield between pixel switching electronics and the electroluminescent cell of the pixel.

Thin film active matrix electroluminescent (EL) displays (AMELD) are well known in the art and are used as flat panel displays in a variety of applications. A typical display includes a plurality of picture elements (pixels) arranged in rows and columns. Each pixel contains an EL cell having an EL phosphor active layer between a pair of insulators and a pair of electrodes. Additionally, each pixel contains switching circuitry that controls illumination of the cell.

A prior art AMELD, as disclosed in U.S. patent 5,302,966, includes a switching circuit associated with each pixel for controlling application of a high voltage to the EL cell. The switching circuit comprises a first transistor having its gate connected to a select line, its source connected to a data line and its drain connected to a gate of a second transistor and through a first capacitor to ground. The drain of the second transistor is connected to ground potential, its source is connected through a second capacitor to ground and to one electrode of an EL cell. The second electrode of the EL cell is connected to a high voltage alternating current source for exciting the phosphor within the EL cell. A number of other arrangements of transistors that can comprise the cell switching circuitry are also disclosed. In operation, the data and select lines are appropriately energized to cause a particular switching circuit, e.g., transistor pair, to apply high voltage to a particular EL cell. Once the voltage is applied to the cell, current passing through the EL cell causes the phosphor layer therein to become luminescent.

In an AMELD having a high density of EL cells, electric fields generated by the high voltage applied to the EL cells interferes with the operation of the cell switching circuitry. Specifically, the electric fields couple to the transistors as well as the data and select lines that are located proximate to an active EL cell. Consequently, in response to errant coupling of the electric fields, the EL cells may be activated or deactivated in error.

The invention overcomes the disadvantages associated with the prior art AMELD pixels by incorporating a conductive electric field shield between

each EL cell and the switching electronics for each EL cell. Specifically, in a method of fabricating a pixel with such a shield, EL cell switching circuitry is formed upon a substrate, an insulating layer is then formed over the circuitry, and then a conductive layer (the electric field shield) is formed over the insulating layer. A dielectric layer is formed over the shield. A through hole is provided through the shield and the dielectric layer such that an electrical connection can be made between the switching circuitry and an EL cell. The EL cell is conventionally formed on top of the dielectric layer. One electrode of the EL cell is connected to the switching circuitry via the through hole and another electrode of the EL cell is connected to a high voltage alternating current source. The electric field shield is connected to ground. Consequently, the shield isolates the switching circuitry, especially the storage node, from the EL cell and ensures that any electric fields produced in the EL cell do not interfere with the operation of the switching electronics.

Furthermore, the switching circuitry for each cell contains two transistors; a low voltage MOS transistor and a high voltage MOS transistor. The low voltage transistor is controlled by signals on a data and a select line. When activated, the low voltage transistor activates the high voltage transistor by charging the gate of the high voltage transistor. The gate charge is stored between the gate electrode of the transistor and the electric field shield. Additionally, to improve the breakdown voltage of the high voltage transistor, a capacitive divider network is fabricated proximate the drift region of that transistor. As such, the network uniformly distributes an electric field over the drift region of the high voltage transistor.

The invention can be readily understood by considering the following description together with the accompanying figures, in which:

FIG. 1 is a schematic diagram of an AMELD pixel including an electric field shield;

FIG. 2A-2L are schematic cross-sectional illustrations of the steps in a process for fabricating an AMELD pixel;

FIG. 3 is a cross-sectional illustration of an alternative embodiment of the AMELD pixel; and

FIG. 4 is a cross sectional view of a capacitive divider network within a high voltage transistor.

To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

FIG. 1 depicts a schematic diagram of an active matrix electroluminescent display (AMELD) 100. The AMELD contains an

arrangement of rows and columns of AMELD pixels. For simplicity, FIG. 1 depicts one of these AMELD pixels 102. In accordance with a preferred embodiment, the pixel 102 contains an electric field shield 104 between a switching circuit 106 and an EL cell 108.

As for the specific structure of the pixel 102, the switching circuit 106 contains a pair of transistors 110 and 112 that are switchable using a select line 114 and a data line 116. To form circuit 106, transistor 110, typically a low voltage metal oxide semiconductor (MOS) transistor, has its gate connected to the select line 114, its source connected to the data line 116, and its drain connected to the gate of the second transistor 112 and through a first capacitor 118 to the shield 104. The electric field shield is connected to ground. Importantly, as shall be discussed in detail below, the first capacitor is actually manifested as the capacitance between the shield 104 and the gate electrode of transistor 112. To complete the switching circuit, transistor 112, typically a high voltage MOS transistor, has its source connected to the data line 116 and its drain connected to one electrode of the EL cell 108. A high voltage bus 122 connects the second electrode of the EL cell to a high voltage (e.g., 250 volts) alternating current (AC) source 120.

The transistors used to form the switching circuit 106 may be of any one of a number of designs. Typically, the first transistor is a low breakdown voltage (less than 10 volts) MOS transistor. The second transistor is typically a double diffused MOS (DMOS) device having a high breakdown voltage (greater than 150 volts). The transistors can be either n- or p-channel devices or a combination thereof, e.g., two NMOS transistors, two PMOS transistors or a combination of NMOS and PMOS transistors. For a further discussion of the fabrication of switching circuitry for an AMELD, the reader should consult U.S. patent 5,302,966, incorporated by reference.

In an alternative arrangement of the switching circuit, the drain of the second transistor is connected to one electrode of the EL cell via a resistor. The resistor is typically 50 to 100 kΩ and is typically fabricated in the drift region of the second transistor. This resistor limits the drain current through the second transistor and, as such, provides circuit protection from excessive drain current.

In operation, images are displayed on the AMELD as a sequence of frames, in either an interlace or progressive scan mode. During an individual scan, the frame time is sub-divided into a separate LOAD period and an ILLUMINATE period. During the LOAD period, an analog-to-digital converter 124 and a low impedance buffer 126 produce data for storage in the switching circuitry. The data is loaded from the data line 116 through

transistor 110 and stored in capacitor 118. Specifically, the data lines are sequentially activated one at a time for the entire display. During activation of a particular data line, a select number of select lines are activated (strobed). Any transistor 110, located at the junction of activated data and select lines, is turned ON and, as such, the voltage on the data line charges the gate of transistor 112. This charge is primarily stored in a capacitance between the gate and the electric field shield (represented as capacitor 118). This charge storage is discussed in detail with regard to FIG. 2L. As the charge accumulates on the gate of transistor 112, the transistor begins conduction, i.e., is turned ON. At the completion of the LOAD period, the high voltage transistor in each pixel that is intended to be illuminated is turned ON. As such, during the ILLUMINATE period, the high voltage AC source that is connected to all the pixels in the display through bus 122 is activated and simultaneously applies the AC voltage to all the pixels. However, current flows from the AC source through the EL cell and the transistor 112 to the data line 116 in only those pixels having an activated transistor 112. Consequently, during the ILLUMINATE period of each frame, the active pixels produce electroluminescent light from their associated EL cells.

FIGS. 2A-2L schematically depict a process for fabricating the AMELD pixel depicted in FIG. 1. Ultimately, the illustrative pixel contains two NMOS devices as the switching circuitry. From the following discussion, those skilled in the art will be able to fabricate other combinations of transistors to form the switching circuitry such as two PMOS devices or a combination of PMOS and NMOS devices.

As shown in FIG. 2A, the fabrication process begins with etching an N- layer 200 to form discrete islands 202 and 204. The N layer is approximately .35 to 1 μm thick and is supported by a 1 μm thick SiO_2 substrate 206. The N layer is a layer of phosphorus doped silicon. The discrete islands 202 and 204 designate areas where transistors 112 and 110 are respectively formed.

In FIG. 2B, an N drift region for transistor 112 is produced by implanting ions such as phosphorus using 110 keV into island 202. In FIG. 2C, a P- well for transistor 110 is produced by implanting ions such as boron using 80 keV into island 204. These two implantation steps define the active transistor areas.

In FIG. 2D, a LOCOS oxidation process is used to form both thick and thin oxide layers over the silicon islands by first growing an oxide layer 208 over the islands. Thereafter, a silicon nitride layer 210 is formed over the oxide layer 208 as a mask that permits a second oxide layer 212 to be grown above

the left side of the N drift region. As such, the oxide layer is thin on the right side 214 of the N drift region and thick on the left side 216 of the N drift region. In FIG. 2E, the silicon nitride layer 210 is removed by etching and leaves a step shaped oxide layer over the N drift region.

In FIG. 2F, a first polysilicon layer (poly1) is deposited and patterned to form gates 218 and 220 and a select line (not shown) connected to the gate of transistor 110. Additionally, the left side of the poly1 layer forms elements 224 of a capacitive divider network 222. The remaining elements of the network 222 are deposited, as described below, when subsequent layers of polysilicon are deposited. As shown in FIG. 2G, a P type region 226 is formed by implanting boron ions using a 40 keV beam. The implanted ions are then driven through the silicon by heating the structure to approximately 1150 degrees C for about 4 hours. Thereafter, another oxide layer is grown over the entire structure. The resulting structure is shown in FIG. 2H.

As shown in FIG. 2I, four N^+ regions are implanted using an ion beam of arsenic atoms at 110 keV. These regions form the source and drain regions of the transistors. Specifically, regions 228 and 230 respectively form the source and drain of transistor 110, while regions 234 and 232 respectively are the drain and source of transistor 112. Thereafter, an oxide layer is formed over the entire pixel area.

FIG. 2J depicts the resulting structure after etching an opening to access the drain and source regions of transistors 110 and 112, depositing a second polysilicon layer (poly2) and patterning the poly2 layer to form the data line 116 as well as conductive pads 236 and 240 for connecting the data line 116 to the source regions 228 and 232. Additionally, openings are etched such that the patterned poly2 layer forms conductive contact pads 238 and 242 for drain regions 234 and 230. The poly2 layer is also used to connect the gate of transistor 112 to the drain of transistor 110; however, for simplicity, this connection is not shown.

FIG. 2K depicts the resulting structure after an oxide layer 244 is grown to a thickness of approximately 200 NM over the entire pixel area, a third polysilicon layer (poly3) is deposited and patterned to form the shield 104. Also, as this layer is formed, elements 246 of the capacitive divider network 222 are formed. These elements are spaced apart from the underlying elements 224 of the network. However, the edges of elements 246 overlap the edges of elements 224 by approximately 2 μm. Operation of the network is described in detail below with respect to FIG. 4.

As an alternative to using polysilicon as the electric field shield and the elements of the capacitive network, a refractory metal such as tungsten can

be used. Generally, the only requirement for the material used to form the electric field shield is that it be a conductor and have a melting point greater than 800 degrees C. To facilitate isolation of the electric field generated by the EL cell, the shield is connected to ground (for simplicity, this connection is not shown).

Once the field shield 104 is created, a conventional EL cell 108 is formed over the pixel area. Specifically, as shown in FIG. 2L, a 1μm thick layer 248 of borophosphosilicate glass (BPSG) is deposited over the entire structure. Thereafter, the BPSG layer and underlying oxide layers are etched to produce an opening to the drain contact pad 240 of transistor 112 and a conductor such as polysilicon (a poly4 layer) or aluminum is deposited and patterned to form one of the EL cell electrodes 250. A layer 252 of ZnS phosphor, or some other appropriate electroluminescent material, in combination with two layers of dielectric material is deposited over the entire structure. This ZnS phosphor and dielectric combination is known in the art as a dielectric-semiconductor-dielectric (DSD) deposition (indicated by reference numeral 252). Lastly, to complete the EL cell 108, a layer 254 of indium tin oxide (ITO) is deposited over the entire structure. The foregoing process utilizes eighteen mask steps to fabricate both transistors and the EL cell in the pixel.

The foregoing description discussed fabricating the inventive pixel in a manner that is conventional in the semiconductor arts, i.e., fabricating the entire device upon one side of a substrate. In an alternative embodiment of the inventive pixel structure shown in FIG. 3, the pixel structure is fabricated on both sides of the substrate 206. In the alternative embodiment of FIG. 3, the N^+ regions 228, 230, 232 and 234 are driven completely through the transistor structures by heating the pixel structure to 1150 degrees C for 4 hours. Thereafter, openings are etched through the silicon substrate 206 and metallic contacts 300 (e.g., aluminum metallization) are deposited on what would normally be the "backside" of the structure. As such, the interconnections of the transistors and the connections to the data and select lines are accomplished on the backside of the structure.

Importantly, in the embodiments shown in FIGS. 2L and 3, the shield 104 lies between the switching circuit 106 and the EL cell 108. The shield is connected to ground such that it isolates the switching circuit, especially the storage node, from the electric field generated during activation of the EL cell. As such, the electric field does not interfere with the operation of the switching circuit. In addition, positioning the shield proximate to the gate of the high voltage transistor forms a well defined storage capacitor (i.e.,

the gate electrode and the shield form a capacitor) for storing data transferred from the data line through the low voltage transistor.

Another aspect of the invention is the use of a capacitive divider coupling network 222 to uniformly distribute an electric field in the drift region 202 of the high voltage transistor 112. FIG. 4 depicts a cross sectional view of the capacitive network 222 of the high voltage transistor 112. The capacitive network 222 is formed from portions of the poly1 layer (elements 224), the poly3 layer (elements 246) and the poly4 layer (EL cell electrode 250). These portions of the network lie directly above the drift region 202 in transistor 112. The edges of elements 246 overlap the edges of elements 224 by approximately 2 μm. As such, capacitive coupling exists between the overlapping elements. This coupling is represented by dashed capacitors 400. Additionally, capacitive coupling exists between each of elements 246 and the electrode 250 (indicated by dashed capacitors 402) and capacitive coupling exists between each of elements 224 and the drift region 202 (as indicated by dashed capacitors 404). This capacitive network uniformly distributes an electric field in the drift region. Such uniformity achieves a high breakdown voltage for the transistor. Without such a network, the electric field tends to concentrate at particular points within the drift region due to the direct influence of either the high voltage field or ground and cause breakdown of the transistor at a low voltage. By including this capacitive network, the electric field is more uniformly distributed over the drift region and the breakdown voltage is increased. Such a network is useful in all forms of high-voltage MOS transistors and should not be construed as limited only to high-voltage MOS transistors used in AMELD.

Although various embodiments which incorporate the teachings of the invention have been shown and described in detail herein, those skilled in the art can readily devise many other varied embodiments that still incorporate these teachings.

WE CLAIM:

1. A high-voltage transistor (112) comprising:

a drain region (234) and a source region (232) being separated by a drift region (202);

a gate electrode (218) being parallel to and separated from said drift region by an insulating layer (212), said gate electrode partially covering said drift region; and

a capacitive divider network (222), located proximate to and spaced apart from said drift region, for producing a substantially uniform electric field within said drift region.

2. The transistor of claim 1 wherein said capacitive divider network further comprises:

a high voltage electrode (250);

a plurality of first conductive elements (246), spaced apart from said high voltage electrode by an insulating layer (248), for accumulating charge from said high voltage electrode;

a plurality of second conductive elements (224), spaced apart from said plurality of first conductive elements by an insulating layer (212), for accumulating charge coupled from said plurality of first conductive elements; and

said drift region of said second transistor, parallel to and spaced apart from said plurality of second conductive elements by an insulating layer, where the charge accumulated upon said plurality of second conductive elements produces a substantially uniform electric field within said drift region.

3. The transistor of claim 2 wherein each of said first conductive elements partially overlap at least one of said plurality of second conductive elements in said plurality of second conductive elements.

4. A method of fabricating a pixel (102) within an electroluminescent display comprising the steps of:

forming, upon a substrate (206), a switching circuit (106) for controlling current through an electroluminescent cell (108) connected to said switching circuit;

depositing, upon said switching circuit, an insulating layer (212); and

depositing, between said insulating layer and said electroluminescent cell, an electric field shield (104) that isolates an electric field within said electroluminescent cell from said switching circuit.

5. A method of claim 3 wherein said forming step further comprises the steps of:

forming, between a drain region (234) and a source region (232), a drift region (202) for a high voltage transistor;

forming an insulating layer (212) over said drift region;

depositing a gate electrode (218) on said insulating layer, said gate electrode partially overlapping said drift region and parallel to said electric field shield such that said electric field shield and said gate electrode form a storage capacitor (118).

6. The method of claim 5 further comprising the step of forming a resistor in said drain region for connecting said drain region to said electroluminescent cell.

7. The method of claim 4 wherein said forming step further comprising the steps of:

forming, between a drain region (234) and a source region (232), a drift region (202) for a transistor (112);

forming an insulating layer (212) over said drift region;

depositing a gate electrode (218) on said insulating layer, said gate electrode partially overlapping said drift region;

depositing a first plurality of capacitive elements (224) on said insulating layer, said elements overlapping a portion of said drift region not overlapped by said gate electrode;

forming a second insulating layer (212) over said capacitive elements and said gate electrode;

depositing a second plurality of capacitive elements (246) on said second oxide layer, said second plurality of elements partially overlaps said first plurality of capacitive elements;

forming a third insulating layer (248) over said second plurality of capacitive elements; and

depositing a high voltage electrode (250) of said electroluminescent cell on said third insulating layer such that, when a high voltage is applied to said high voltage electrode, a charge accumulates on said first and second plurality of electrodes and an electric field is uniformly distributed in said drift region.

8. A method of fabricating a high-voltage transistor (112) comprising the steps of:

forming, between a drain region (234) and a source region (232), a drift region (202) for a transistor (112);

forming an insulating layer (212) over said drift region;

depositing a gate electrode (218) on said insulating layer, said gate electrode partially overlapping said drift region;

forming a capacitive divider network (222) located proximate to and spaced apart from said drift region, for producing a substantially uniform electric field within said drift region.

9. The method of claim 8 wherein said step of forming said capacitive dividing network further comprises the steps of:

depositing a first plurality of capacitive elements (224) on said insulating layer, said elements overlapping a portion of said drift region not overlapped by said gate electrode;

forming a second insulating layer (212) over said capacitive elements and said gate electrode;

depositing a second plurality of capacitive elements (246) on said second oxide layer, said second plurality of elements partially overlaps said first plurality of capacitive elements;..

forming a third insulating layer (248) over said second plurality of capacitive elements; and

depositing a high voltage electrode (250) on said third insulating layer such that, when a high voltage is applied to said high voltage electrode, a charge accumulates on said first and second plurality of electrodes and an electric field is uniformly distributed in said drift region.

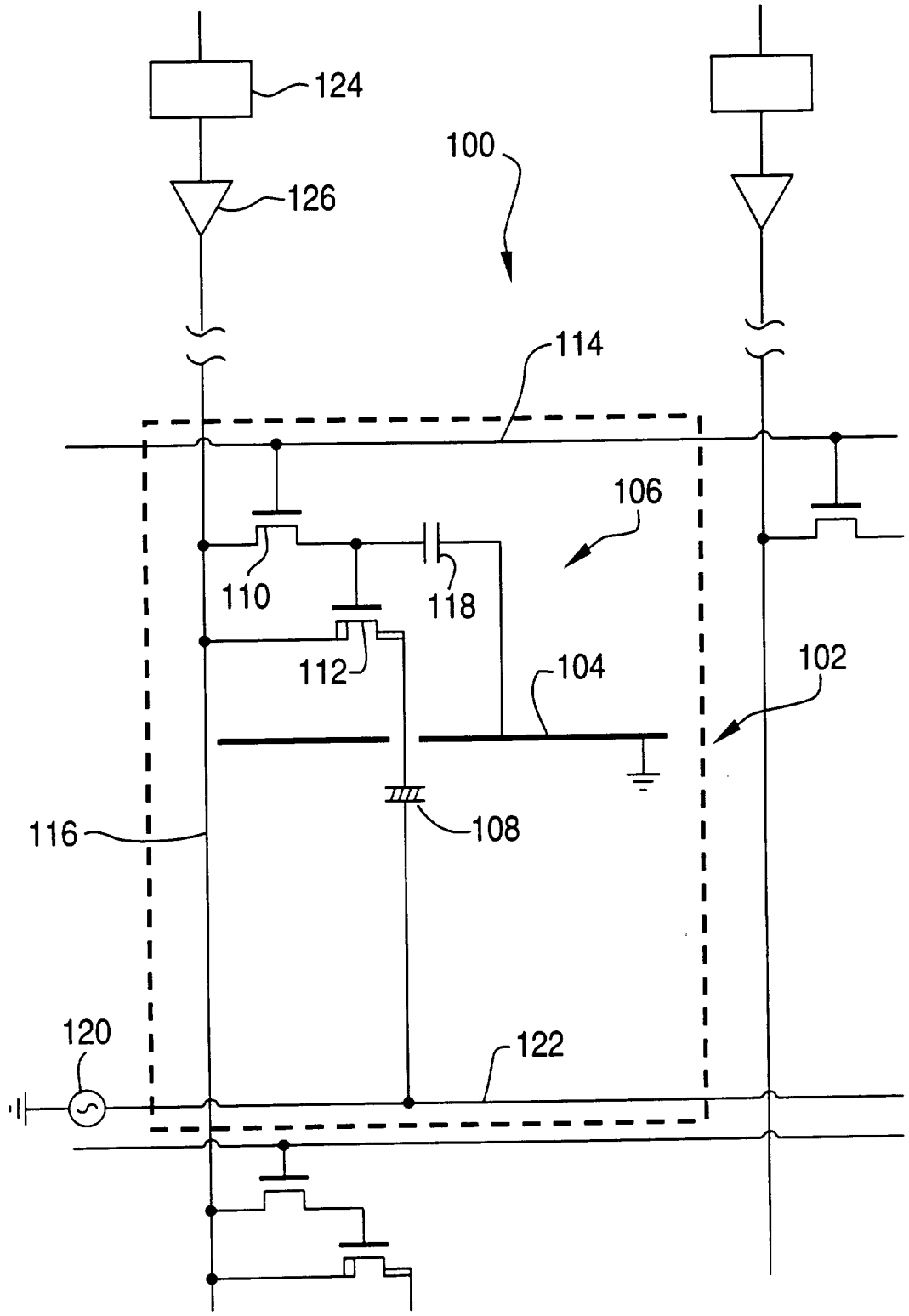


FIG. 1

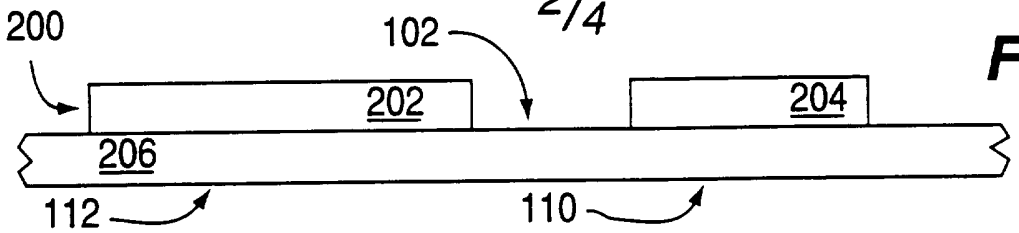


FIG. 2A

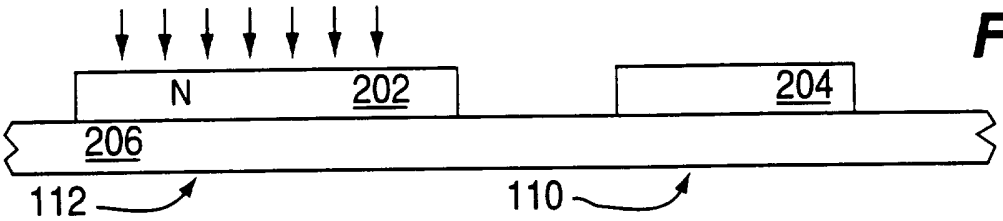


FIG. 2B

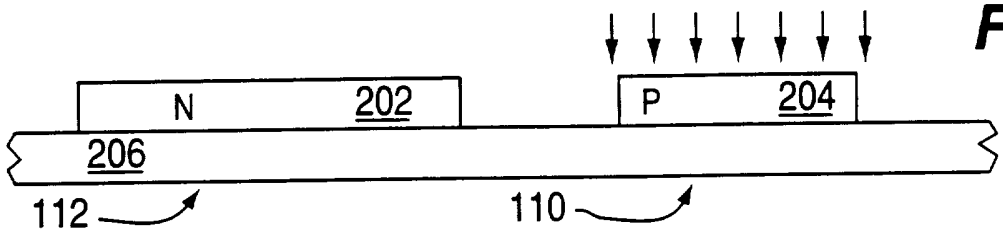


FIG. 2C

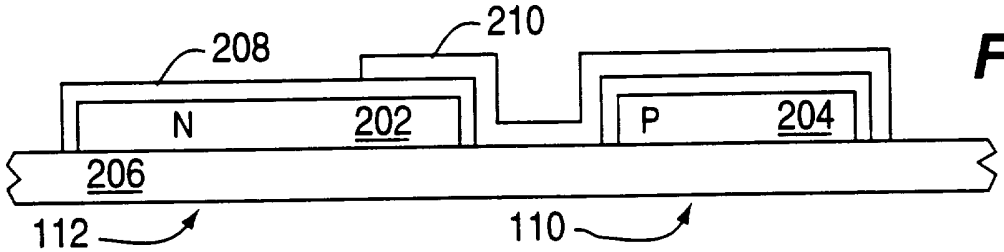


FIG. 2D

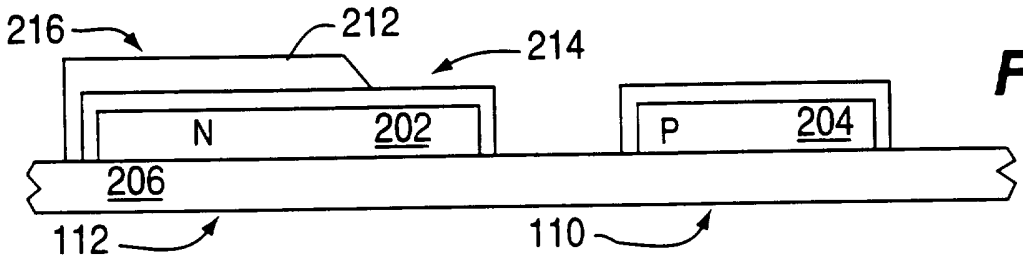


FIG. 2E

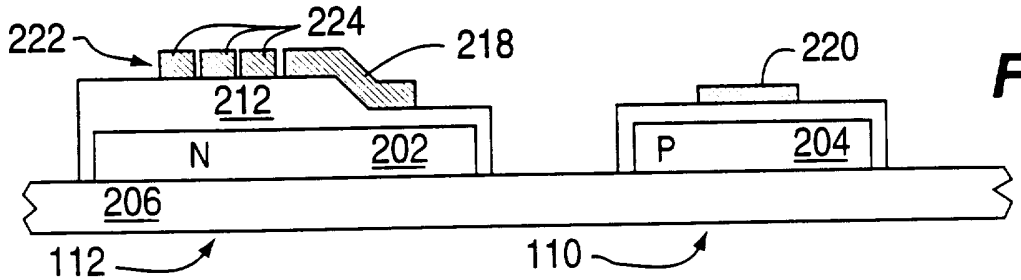


FIG. 2F

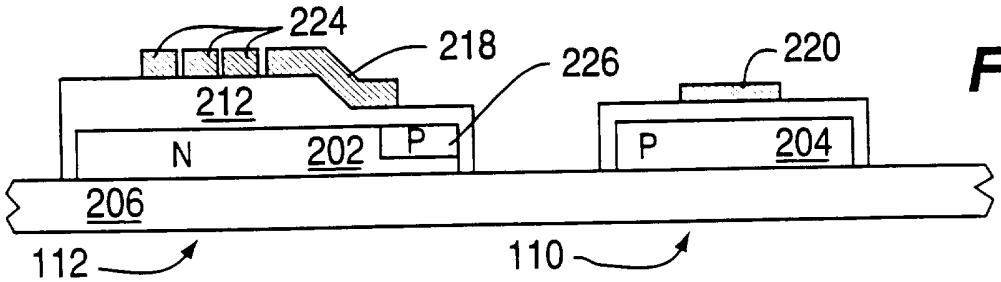


FIG. 2G

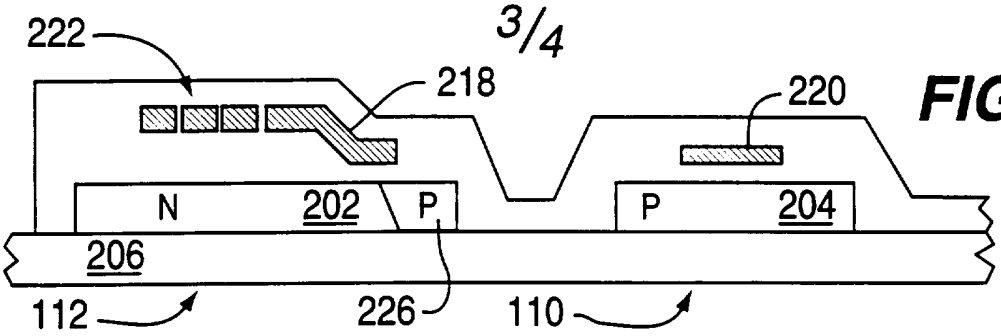


FIG. 2H

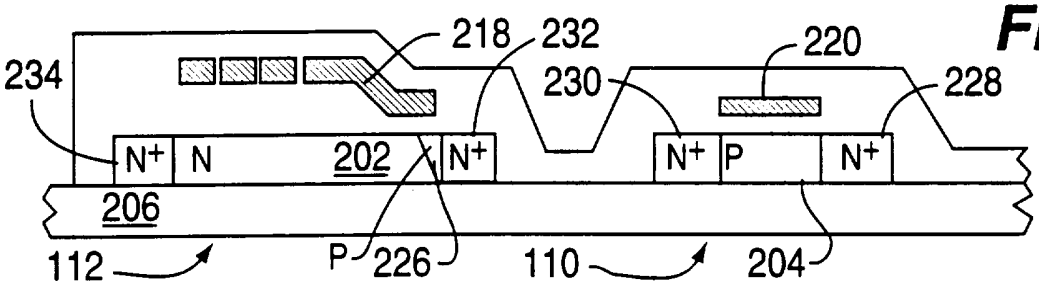


FIG. 2I

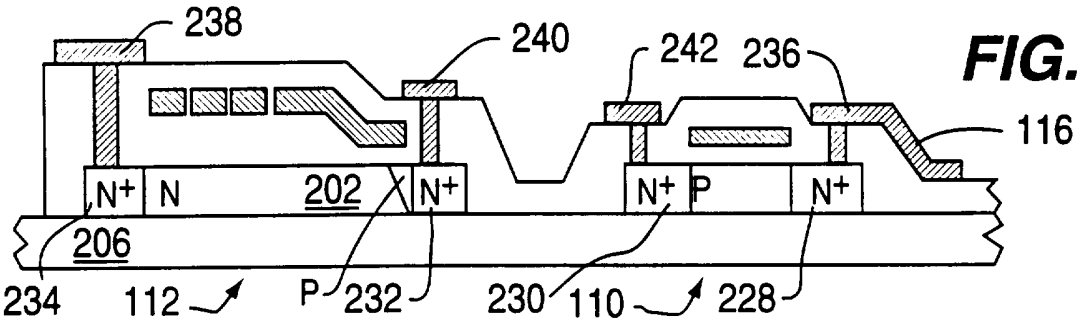


FIG. 2J

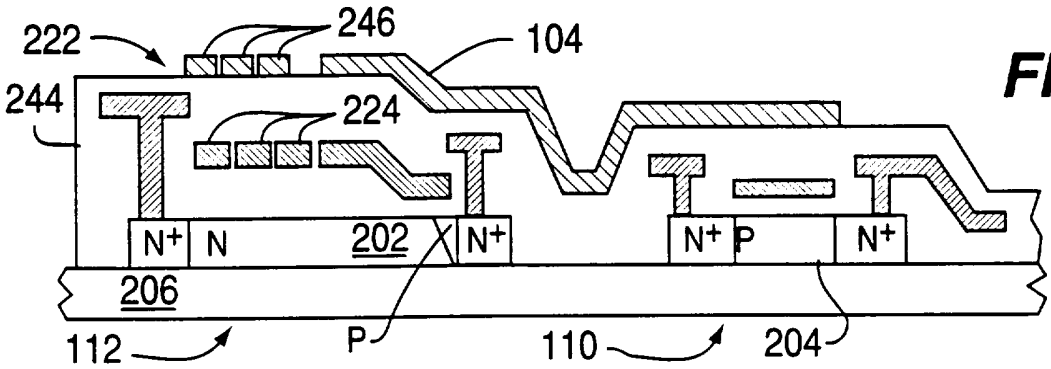


FIG. 2K

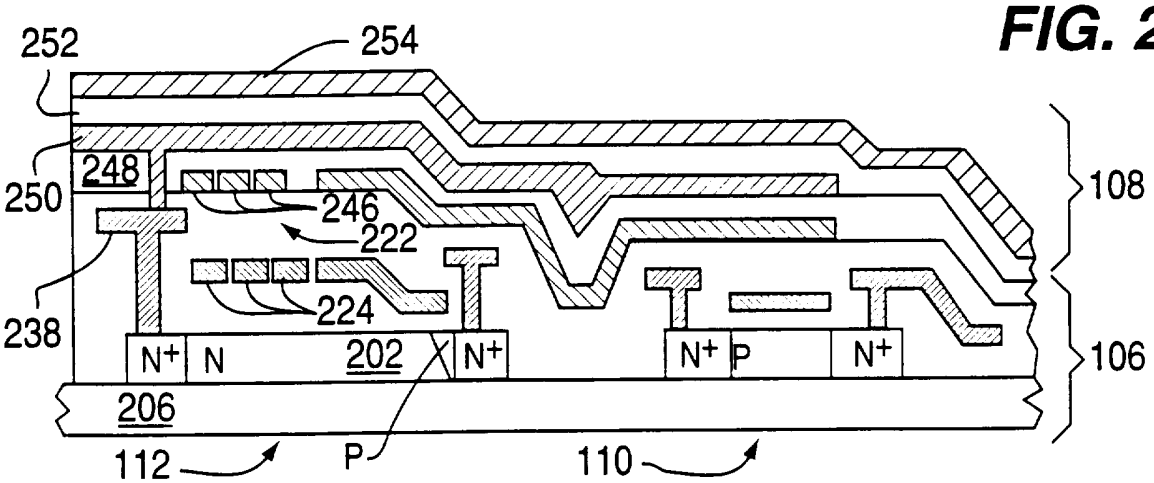
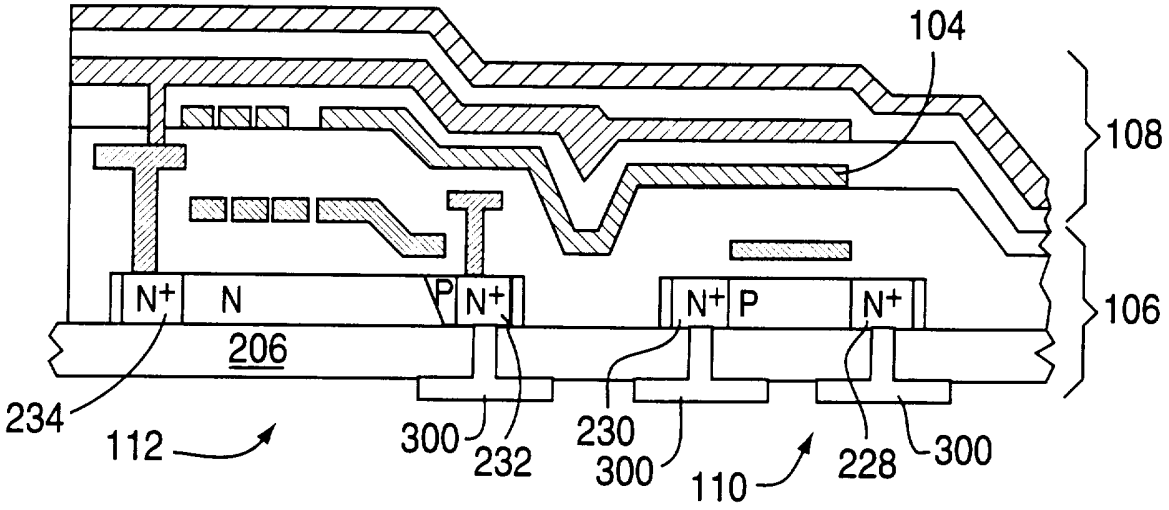


FIG. 2L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206
234
112
300
232
230
300
110
228
300

FIG. 3

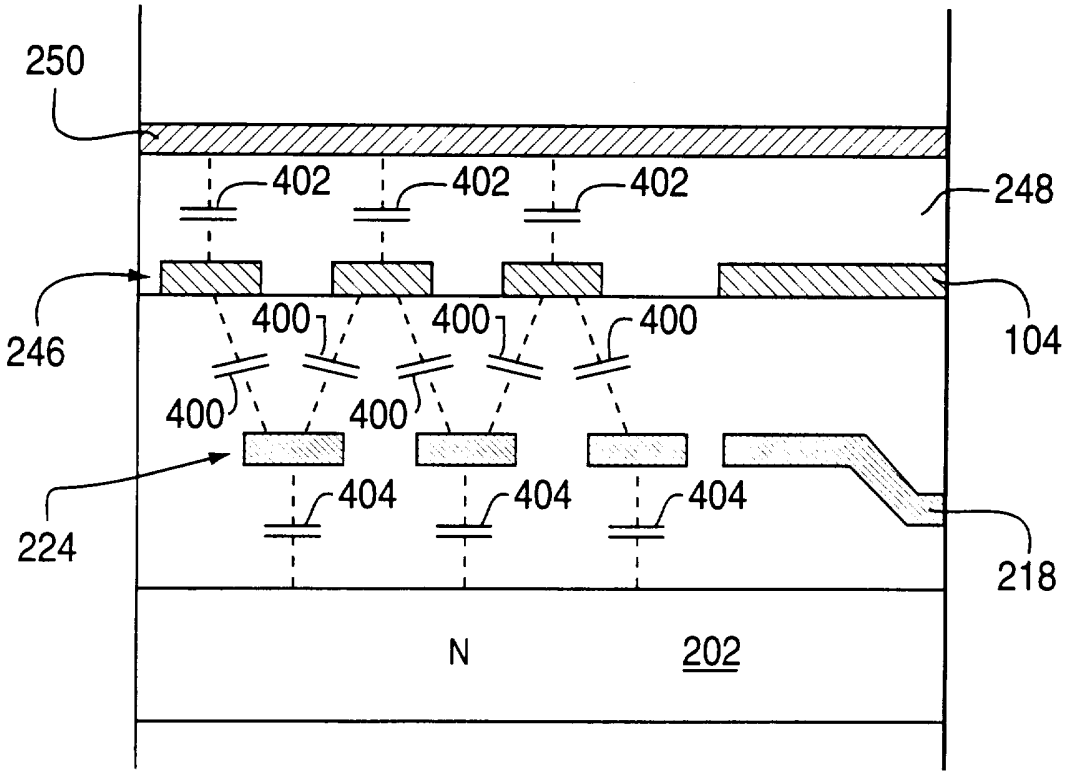
250
402
402
402
248
246
400
400
400
104
400
400
404
404
404
224
218
N
202

FIG. 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/10621

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :H01L 21/8234, 21/786; G09G 3/30
US CL : 437/40TFT, 41TFT, 913; 148/DIG 150; 257/351,352
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 437/40TFT, 41TFT, 913; 148/DIG 150; 257/351,352

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 4,006,383 [Luo et al.] 01 February 1977, Fig2, columns 2, line 48 through column 4.	1,4,8
A	US, A, 4,087,792, [Asars] 02 May 1978, Fig 1, column 1.	
X	US, A, 4,528,480, [Unagami et al.], 09 July 1985, Figs 1-2, columns 3 through column 6.	1,8
A	US, A, 4,532,506, [Kitazima et al.], 30 July 1985, Fig 4a, column 3.	
X ---- Y	US, A, 4,602,192, [Nomura et al.], 22 July 1986, Fig 9b, columns 5-6.	1 ---- 1,4,8

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 22 DECEMBER 1995	Date of mailing of the international search report 26 JAN 1996
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer TOM THOMAS Telephone No. (703) 308-0661

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/10621

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, A, 4,954,747, [Tuenge et al.], 04 September 1990, all Figs, columns 2-4.	
A	US, A, 5,020,881, [Matsuda et al.], 04 June 1991, Figs 3,4,6, columns 6-7.	
X	US, A, 5,056,895, [Kahn], 15 October 1991, columns 5-7, Figures 1A,2,3.	1,4,8
Y	US, A, 5,302,966, [Stewart] 12 April 1994, all texts and Figures.	1,4,8
X ---- Y	SID 92 DIGEST issued 1992, T. Suzuki et al, "The Fabrication of TFEL Displays Driven by a-Si TFTs", pages 344-347, Figures 3-4.	1 ------ 1,4,8

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US95/10621

B. FIELDS SEARCHED
Electronic data bases consulted (Name of data base and where practicable terms used):

APS, JPO
Search terms: El or electroluminea?; tft# or (MOS or MOSFET or NMOS) or (thin film)(w)(transistor# or device#); capacit?; shield?.