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(54) A DISPLAY PANEL WITH SIMPLIFIED THIN FILM INTERCONNECTION ARRANGEMENT

(71) We, WESTINGHOUSE ELECTRIC CORPORATION of Westinghouse Building, Gateway Center, Pittsburgh, Pennsylvania, United States of America, a company organised and existing under the laws of the Commonwealth of Pennsylvania, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

This invention relates generally to display panels and more particularly to thin film interconnection arrangements in thin film display panels.

It has been suggested in display technology comprising a flat display panel that an array of electro-optic elements be disposed as rows and columns upon a substrate with individual thin film electronic control circuitry associated with each of the display elements upon the substrate. In the suggested display, the number of display medium elements in each row is equal and the number of elements in each row is equal, and addressing circuitry bus bar interconnections are provided for rows and columns of display elements on such panels. The panels utilize line-at-a-time video information addressing techniques with the video information applied via the column bus bars. The row bus bars are used to apply synchronizing switching signals. There is another set of common bus bars in addition to these addressing sets associated with the rows and columns of the display. This additional set of common bus bars which are really thin film deposits of aluminum or other such conductive metal at a peripheral edge of the panel and typically connected to ground to provide a common reference potential level which is connected to the thin film electronic circuitry associated at each display medium point on the panel. The provision of such common reference signal bus bars increases by one-half the number of bus bars which must be deposited on the panel and doubles the number of

crossovers between bus bars which must be insulated relative to one another on the panel. It also requires additional deposition steps through the masking system. These crossover or overlap points between bus bars constitute a major reliability problem area in fabricating such display panels. This is because it is difficult to effectively completely insulate these crossover points. The need for such common reference signal bus bars also contributes to limiting the resolution factor for such display panels. This is because of the need to adequately space all deposited components upon the substrate from one another to maintain isolation between the conductor components of the panel. The less the total number of components, including thin film transistors as well as bus bar elements required for the circuitry, the smaller the total element size can be because of the reduced spacing requirements, which size reduction can contribute to increasing the resolution of the individual display medium.

It is the principal object of the present invention to eliminate the set of common reference signal bus bars.

The invention resides in a display panel arrangement comprising a flat display panel having electro-optic display medium cells disposed as rows and columns, and thin film electronic control circuitry disposed on the substrate, one signal bus for each column of display cells being connected to the control circuitry associated with each display cell in the column, and a switching bus for each row and one additional switching bus, each individual control circuit of the circuitry being connected between adjacent row switching buses such that the adjacent switching buses complete a switching circuit path for each of the control circuits.

A preferred embodiment of the invention will now be described by way of example only, with reference to the accompanying drawings, in which:

Figure 1 is an overall schematic representation of the display panel and a peripheral drive signal means for addressing

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and controlling the display panel operation to provide a visual display;

Figure 2 is a portion of the circuit layout of the suggested display panel;

5 Figure 3 is a partial circuit schematic of the display panel of the present invention; and

10 Figure 4 is a schematic diagram in greater detail of the vertical scan register 18 seen in Figure 1.

The display panel system of the present invention is seen in schematic form in Figure 1. The display panel 10 is connected to peripheral drive circuitry at two sides of the panel. Video information signals are fed in one side of the panel from the line-at-a-time address scheme means 12 and the analog video register 14 which is connected at the panel periphery to information signal buses 16 which run in parallel columns on the display panel. Vertical scan means 18 is provided on an orthogonal side of the display panel and is connected individually to rows of switching signal bus bars 20 which extend across the display panel orthogonal to the information signal buses 16, with the switching signal buses 20 being insulated from the information signal buses at crossover points by a suitable insulation layer. As will be explained later in greater detail, a uniform light transmissive conductive electrode 22 is disposed over the entire display panel and is connected at a peripheral side to the power supply means 24.

25 The display panel 10 actually comprises rows and columns of display medium elements which comprise individual picture points to make up the overall display. This can be best seen in the schematic electrical diagrams of Figure 2, which is a previously suggested display panel, and Figure 3 which is a partial circuit schematic of the display panel of the present invention. In both the suggested panel of Figure 2 and the present invention panel in Figure 3, the individual display element is defined between the intersections of adjacent information signal buses and switching signal buses, and generally defined by the area shown in the dotted line in Figures 2 and 3. The basic electronic control circuitry for both panels is essentially the same and is explained in greater detail in US Patent Specifications Nos 4006381 and 4100656. The circuitry consists of a switching transistor T_1 which is a thin film transistor, the gate of which is connected to the switching signal bus to permit information signals applied via bus 16 and the source of switching signal transistor T_1 to be transferred and loaded in the storage capacitor C_s . The power drive transistor T_2 has its gate connected to the drain of T_1 , and to the storage signal side of capacitor C_s . One side of the power

70 transistor T_2 is connected to individual electrodes 23 which are part of each display element. The preferred display medium is electroluminescent phosphor which is disposed upon the electrode 23 at each display element, and the uniform top electrode 22 discussed above is disposed over the electroluminescent layer. This top electrode 22 is connected to the power supply means 24 for driving the electroluminescent phosphor to produce light output. In the previously suggested display panel embodiment, it was necessary to utilize a common reference signal bus which was connected to the power transistor T_2 and to the other side of the storage capacitor C_s and was typically grounded to permit referencing the information signal level to a fixed potential level for the entire display panel. Such a grounded or reference signal bus bar permitted a power return path to the power supply means to provide a complete circuit across the electroluminescent layer electrodes. The inclusion of this common reference signal bus bar significantly increases the number of bus bar crossovers and reduces the available spacing for separating components on the panel within an area covered by a single display element. This has the effect of placing a limit on the resolution of display panel since it makes it difficult to reduce the size of the individual display elements.

100 In the display panel system of the present invention as seen in Figure 3, the basic display element format is essentially the same, with switching transistor T_1 connected in the same manner as in the prior art device. The gate of T_1 is connected to switching signal bus 20, and the source of T_1 is connected to the information signal bus 16. The drain of T_1 is again connected to the power transistor T_2 , with T_2 connected to the individual electrode 23 upon which the electroluminescent layer is disposed. The top electrode 22 again is the uniform electrode covering the entire display panel and is connected to the power supply means 24. The storage capacitor C_s and the opposed contact of power transistor T_2 are not connected to a separate common reference signal bus as in the prior art display panel but are instead directly connected to the adjacent switching signal bus, so that for the dotted unit cell of Figure 3 transistor T_2 is connected to adjacent bus Y_2 . This pattern is continued for each display element with the storage capacitor and the power transistor in each case being connected to the adjacent switch signal bus. The peripheral circuitry at the side of the panel connected to the switching signal buses 20 includes a means for connecting a given switching signal bus to the vertical

scan switching signal input means, while connecting all other switching signal buses which are connected to the storage capacitors and the power transistors to a reference signal means which would commonly be grounded. This will permit simultaneous application of the uniform reference signal and the information signal applied via information signal buses to the individual display elements, and also to permit a return path for the current flowing through the electroluminescent layer from the front electrode in the power supply. The common reference signal means would be connected to the power supply to complete this circuit.

The switching signal buses thus perform two functions in the display panel system of the present invention. This is possible because the line-at-a-time address format for such a display panel means that the duty cycle for an individual switching signal bus is relatively low, so that when the adjacent switching signal bus is not being utilized for switching purposes, it can serve the function as a common reference signal bus.

It should be pointed out that the thin film transistor devices utilized in the electronic control circuitry disposed at each picture display element are to be enhancement type devices. Such an enhancement type thin film transistor can be provided by actively controlling the characteristics of the semiconductive layer which is typically cadmium selenide, and by controlling the source and drain contact layers as well as the indium doping layer to provide the desired enhancement mode of operation. By an enhancement type transistor device is meant here that at zero voltage applied between the gate and the source of the transistor there is essentially zero leakage current across the device. This would not be the case with a depletion mode transistor device. The switching transistor T_1 must have essentially zero current leakage between its gate and source when the gate which is connected to the switching signal bus has a zero applied voltage, otherwise it will not be possible to store the information signal on the storage capacitor C_s . If the power transistor T_2 exhibits some leakage current at zero gate voltage, the practical effect will be to permit some excitation of the electroluminescent signal on a continuing basis which would provide a background light level for the individual display element. While this would be undesirable, it is not a critical factor in producing a usable display.

The vertical scan register 18 is seen in greater detail in Figure 4. The function of vertical scan register 18 is to synchronize the proper information signal with the proper display element of the array, and for

line-at-a-time addressing to synchronize transfer of a line of display information stored in the analog video register to the desired line of display elements. Since the y_m bus bars are time shared to serve as the reference potential return when not being used for switching a line of display elements on, the register 18 must serve to sequentially drive a particular line Y_m with a switching signal while connecting all other Y buses with the reference potential means. A system for achieving this function is shown diagrammatically in Figure 4, wherein the vertical scan register includes a binary clock 30, counter 32, decoder 34, and buffer 36. The synchronizing signal from the analog video register 14 is fed to the clock 30, with clock pulses fed to the serially connected counter 32 and decoder 34, which effects the sequential selection of Y lines for switching. The clock pulses V_c here shown as positive step pulses are applied to the buffer 36, as is the switching signal V_y which is here shown as a negative pulse timed to coincide with the positive clock pulse. The buffer has a plurality of output lines equal in number to the Y_m buses and are connected to each Y_m bus bar of the display panel by a suitable panel peripheral connector. The negative pulse V_y which is the output of the decoder is converted in the buffer to a positive switching pulse applied to the selected Y_m bus of the panel, while all other Y buses are connected to a reference signal means which is not shown, which is in turn connected to the power supply 24.

WHAT WE CLAIM IS:—

1. A display panel arrangement comprising: a flat display panel having electro-optic display medium cells disposed as rows and columns and thin film electronic control circuitry disposed on the substrate, with one signal bus for each column of display cells being connected to the control circuitry associated with each display cell in the column, and a switching bus for each row and one additional switching bus, each individual control circuit of the circuitry being connected between adjacent row switching buses such that the adjacent switching buses complete a switching circuit path for each of the control circuits.

2. A display panel according to claim 1 wherein the electro-optic display medium cells comprise elements disposed between two spaced apart electrodes, one electrode of which is light transmissive and common to all the display cells of the panel, with the other electrode being connected to the control circuitry consisting of an information signal addressing transistor the gate of which is connected to a switching signal bus which is connected to a row of

display cells, and the source of the information signal transistor is connected to an information signal bus which is connected to the column of display cells, with the drain of the information signal transistor connected to one side of an information signal storage capacitor, and also to the gate of a power transistor, with the power transistor source and drain contacts connected between said other electrode for the display medium and the switching signal bus for the adjacent row of display cells.

5 3. A display panel according to claim 2, wherein the transistors are enhancement mode devices. 15

10 4. A display panel substantially as hereinbefore described with reference to and as shown in Figs. 1, 3 and 4 of the accompanying drawings. 20

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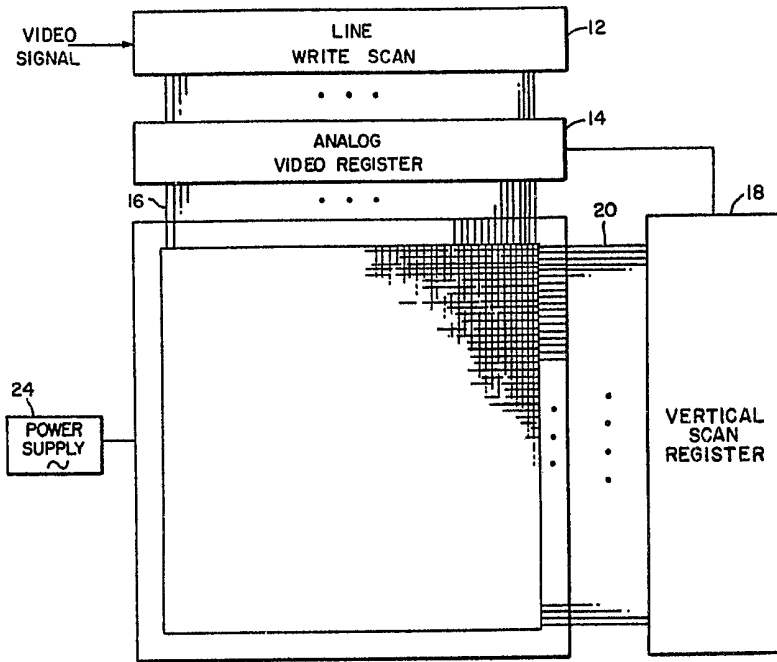


FIG. 1

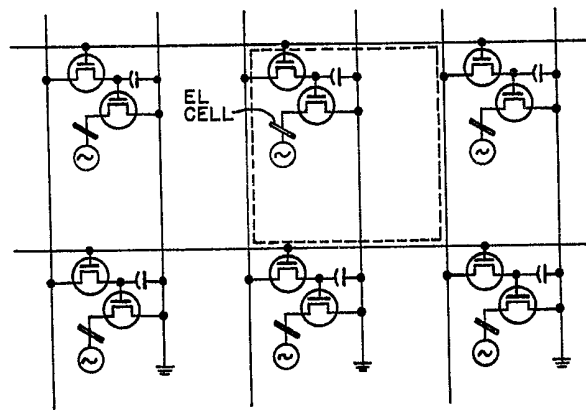


FIG. 2
 PRIOR ART

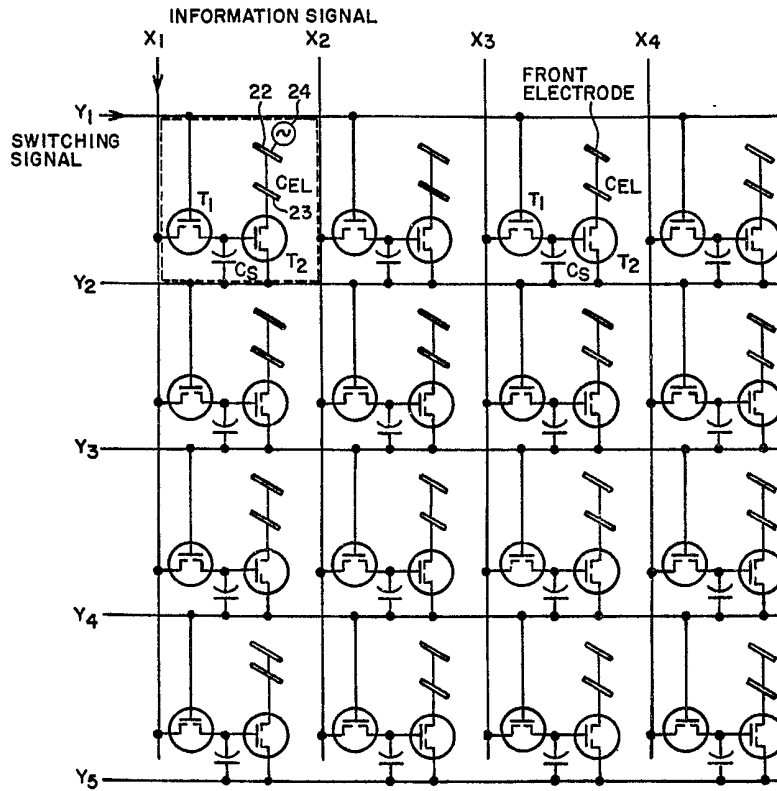


FIG. 3

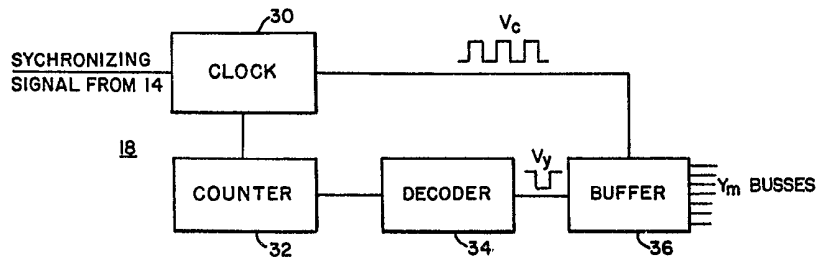


FIG. 4