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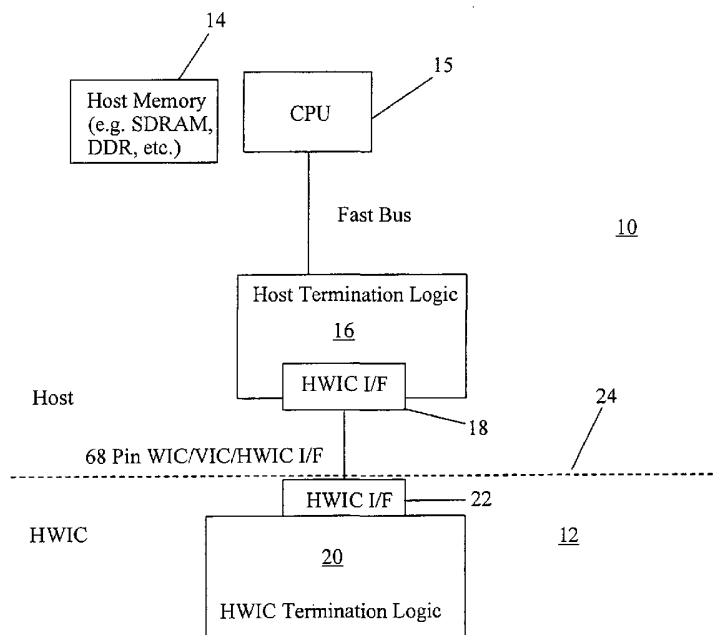
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(54) Title: BACKWARD-COMPATIBLE PARALLEL DDR BUS FOR USE IN HOST-DAUGHTERCARD INTERFACE



(57) Abstract: A host-daughtercard interface is pin compatible with a legacy interface but redefines a subset of pins to implement a high-bandwidth double data-rate (DDR) bus. By inspecting a cookie on the daughtercard, the host platform determines whether the daughtercard supports the DDR bus or the legacy interface, and then configures the subset of pins to implement the legacy interface or the DDR bus.

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INTERNATIONAL SEARCH REPORT

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A. CLASSIFICATION OF SUBJECT MATTER
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B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 U.S. : 710/11

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 6598109 B1 (MCALISTER et al.) 22 July 2003, col. 4, lines 9-24	1-11
Y	US 2002/0144074 A1 (WU et al.) 3 OCT 2002, paragraph 18	1-11
Y	US 5805833 A (VERDUN) 16 JAN 1996, col. 3, lines 50-56	1-5, 10
Y	US 2003/0093607 A1 (MAIN et al.) 15 MAY 2003, paragraph 173	1-5, 10
Y	US 5675807 A (ISHWANDI et al.) 7 June 1995, col. 49, lines 54-59	3
Y,E	US 6883171 B (BITTNER et al.) 19 Apr 2005	3, 10
Y,P	US 6772249 B1 (LADA et al.) 3 Aug 2004	5

Further documents are listed in the continuation of Box C. See patent family annex.

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C. (Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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Y,E	US 6904506 B2 (WU) 7 Jun 2005, col. 3, lines 55-66	1-11
Y	US 5249280 A (NASH et al.) 28 Sep 1993, col. 1, lines 60-64; col. 2, lines 1-5	3,10