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Hsu

(54) **COMPLEMENTARY RESISTIVE MEMORY STRUCTURE**

(76) Inventor: **Sheng Teng Hsu**, Camas, WA (US)

Correspondence Address:
SHARP LABORATORIES OF AMERICA, INC.
C/O LAW OFFICE OF GERALD MALISZEWSKI
P.O. BOX 270829
SAN DIEGO, CA 92198-2829

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(52) **U.S. Cl.** **257/2**; 257/E47.001

(57) **ABSTRACT**

A complementary resistive memory structure is provided comprising a common source electrode and a first electrode separated from the common source electrode by resistive memory material; and a second electrode adjacent to the first electrode and separated from the common source electrode by resistive memory material, along with accompanying circuitry and methods of programming and reading the complementary resistive memory structure.

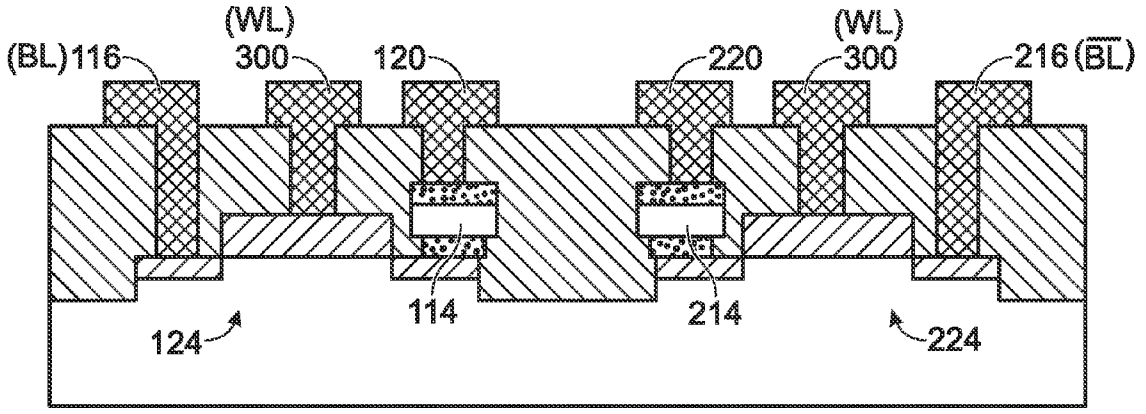


Fig. 1

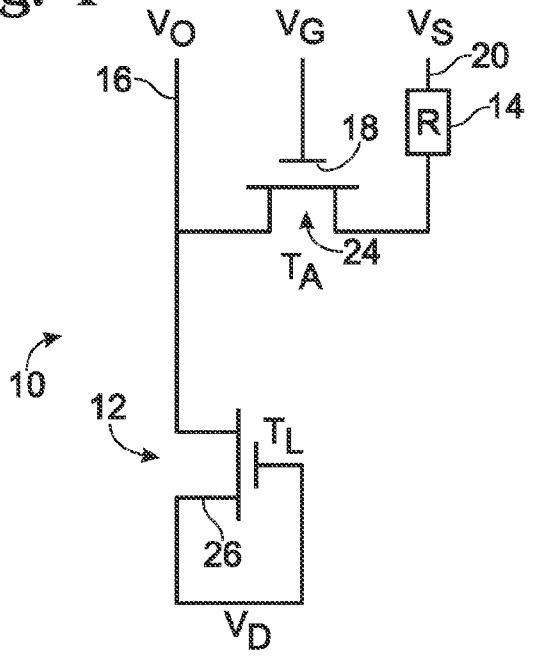

V_O
V_G
V_S
16
20
R
14
18
24
T_A
10
12
T_L
26
V_D

Fig. 2

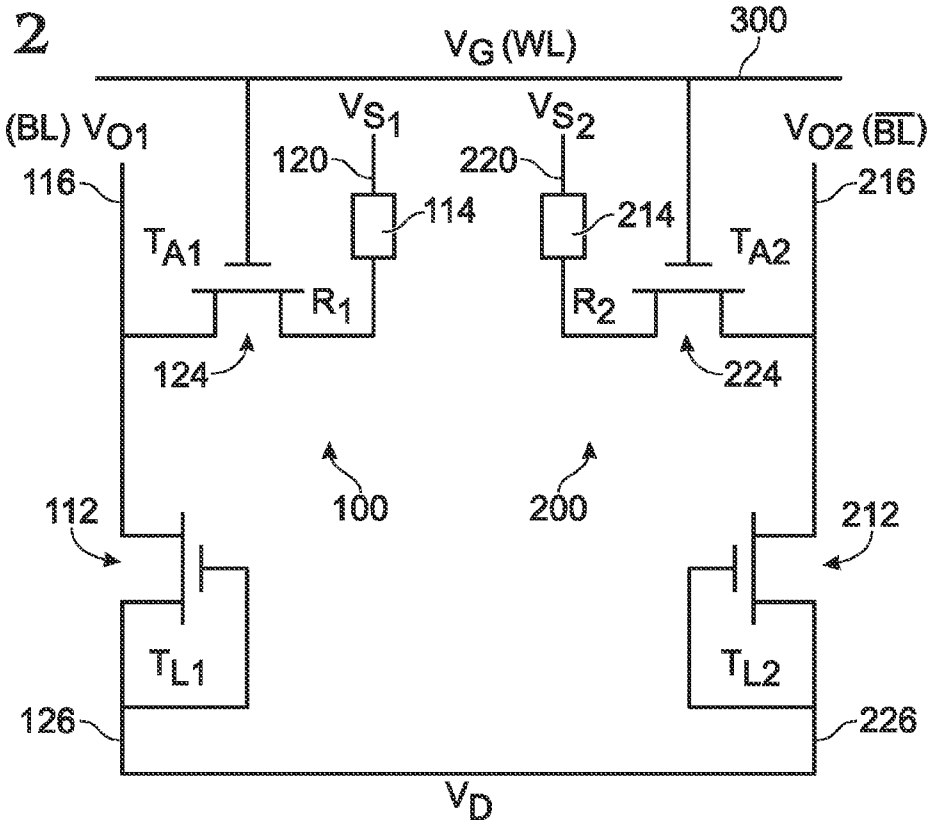

V_G (WL)
300
(BL) V_{O1}
V_{S1}
V_{S2}
V_{O2} ($\overline{BL}$)
116
120
220
216
114
214
T_{A1}
T_{A2}
R_1
R_2
124
224
100
200
112
212
T_{L1}
T_{L2}
126
226
V_D

Fig. 3

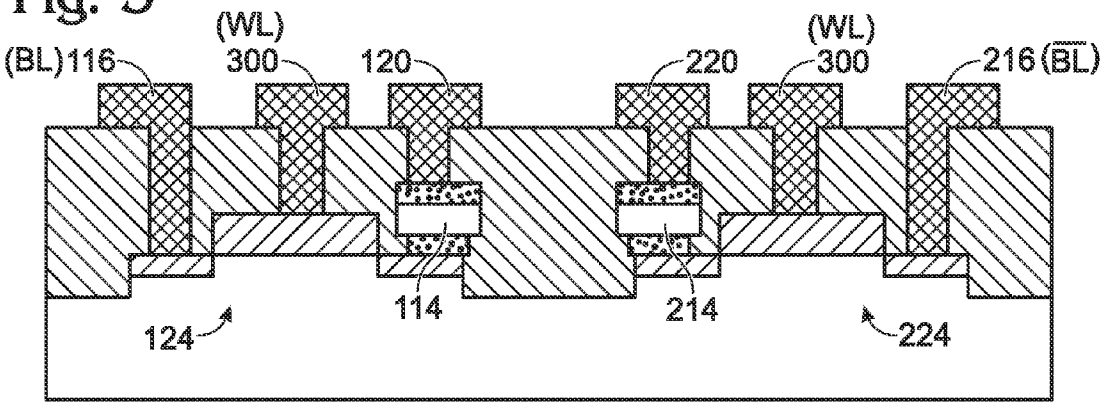


Fig. 4

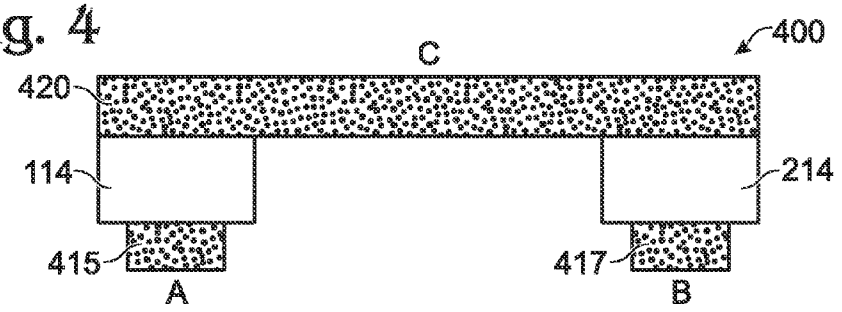


Fig. 5

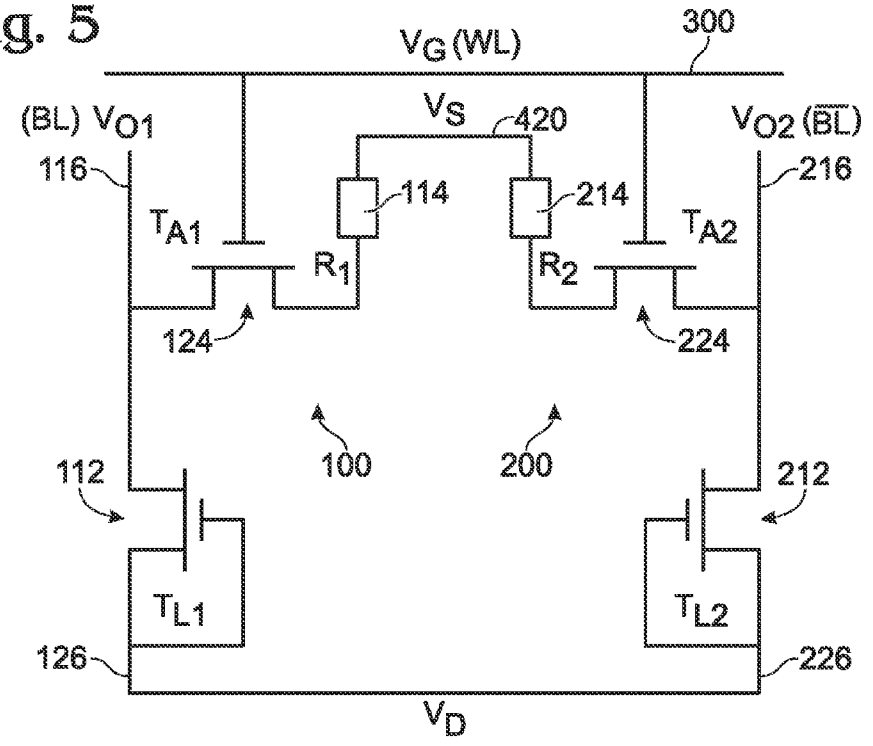


Fig. 6

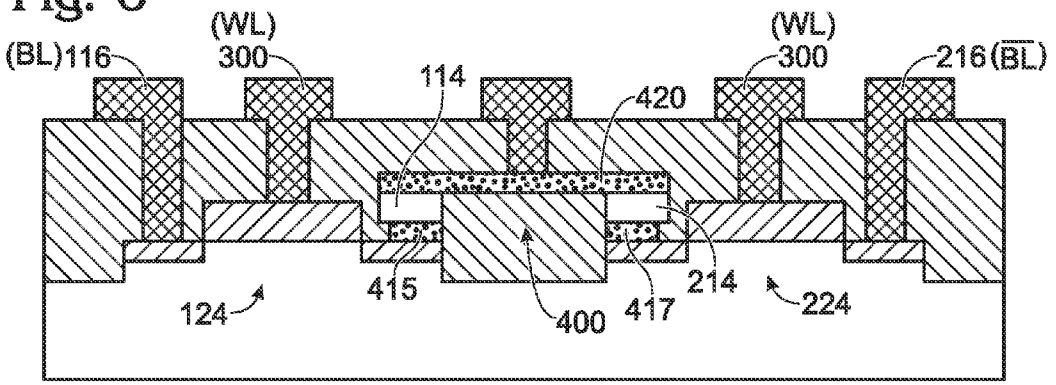


Fig. 7

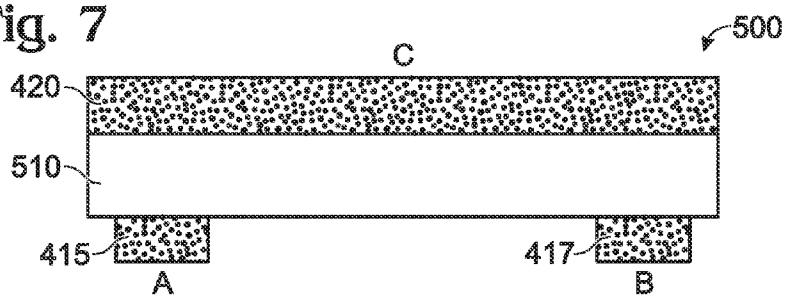


Fig. 8

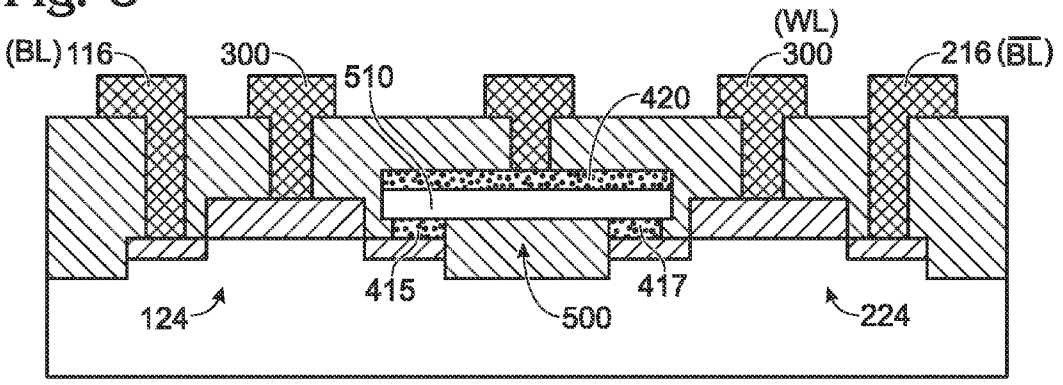
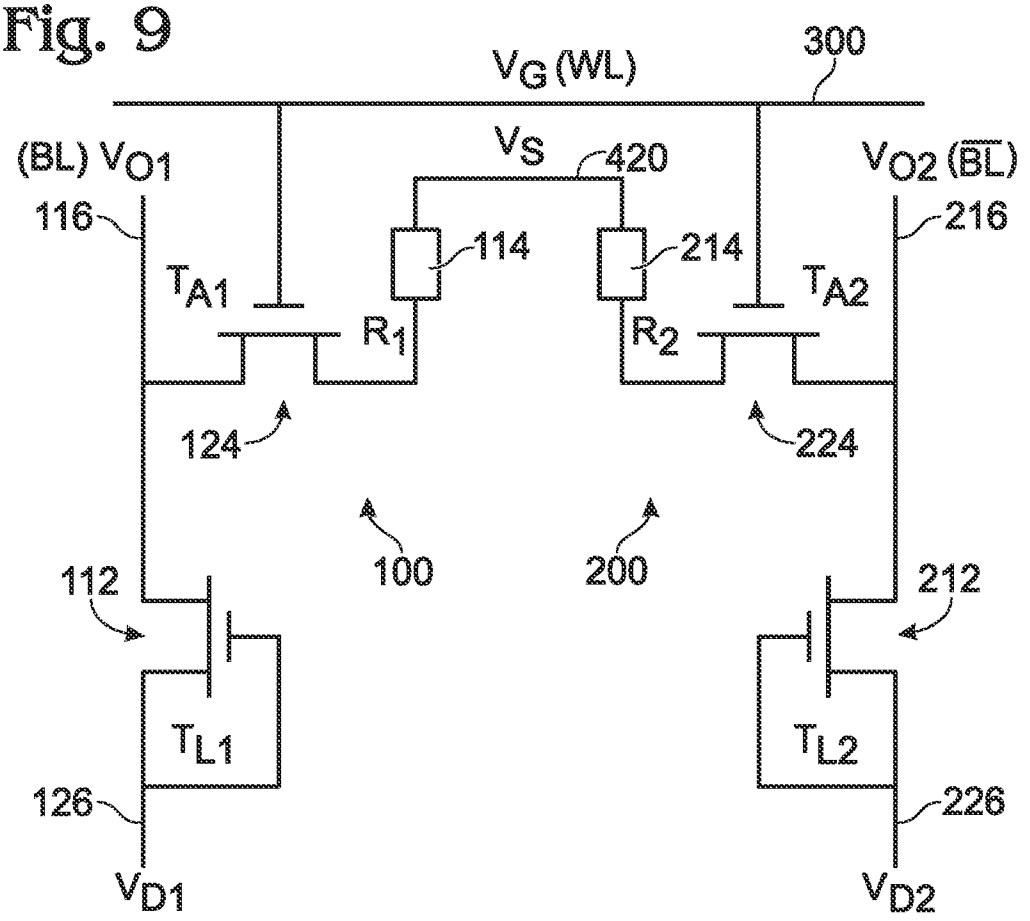


Fig. 9


V_G (WL)
300
(BL) V_{O1}
V_S
420
V_{O2} ($\overline{BL}$)
116
114
214
216
T_{A1}
T_{A2}
R_1
R_2
124
224
100
200
112
212
T_{L1}
T_{L2}
126
226
V_{D1}
V_{D2}

COMPLEMENTARY RESISTIVE MEMORY STRUCTURE

RELATED APPLICATIONS

[0001] This application is a Divisional Application of a pending patent application entitled, COMPLEMENTARY OUTPUT RESISTIVE MEMORY CELL, invented by Sheng Teng Hsu, Ser. No. 10/957,298, filed Sep. 30, 2004, Attorney Docket No. SLA0792, which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

[0002] The present device structures relate generally to resistive memory devices and more specifically to a complementary output memory cell.

[0003] A complementary memory cell has two bits capable of being programmed and of outputting a complementary output such that when the first bit is 0; the second bit is 1, and when first bit is 1; the second bit is 0. Complementary memory cells often require a large cell size and the programming process may be complicated and slow.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] FIG. **1** is a schematic view of a unit resistive memory cell.

[0005] FIG. **2** is a schematic view of a complementary resistive memory cell employing two unit resistive memory cells as provided in FIG. **1**.

[0006] FIG. **3** is a cross-sectional view of a resistive memory structure for implementing the complementary resistive memory cell of FIG. **2**.

[0007] FIG. **4**. is a cross-sectional view of a resistive memory structure for implementing an alternate embodiment of the complementary resistive memory cell.

[0008] FIG. **5** is a schematic view of a complementary resistive memory cell.

[0009] FIG. **6** is a cross-sectional view of a resistive memory structure for use in a complementary resistive memory cell shown in FIG. **5**.

[0010] FIG. **7** is a cross-sectional view of a resistive memory structure for implementing another embodiment of the complementary resistive memory cell.

[0011] FIG. **8** is a cross-sectional view of a resistive memory structure for implementing the complementary resistive memory cell utilizing the resistive memory structure of FIG. **7**.

[0012] FIG. **9** is a schematic view of a complementary resistive memory cell corresponding to the memory structures with separated power supplies associated with each bit.

DETAILED DESCRIPTION OF THE INVENTION

[0013] Certain embedded memory applications require a complementary digital output, that is a 0 for bit A and a 1 for bit B, or vice versa. Accordingly, a complementary, resistive memory device is provided.

[0014] FIG. **1** is a schematic view of a unit, resistive memory cell **10** with a gated diode load (V_D) provided by the load transistor (T_L) **12**. A memory resistor (R) **14** is written to a high-resistance state by applying ground to an output (V_O) **16**, applying a programming voltage (Vp). also referred to herein as gate voltage (V_G), to a gate **18** of an active transistor (TA) **24**, and applying a programming pulse voltage to the memory resistor (R) at a voltage source (V_S) **20** and floating the drain **26** of the load transistor The programming voltage (Vp) is larger than the amplitude of the minimum programming pulse voltage by at least 1 V.

[0015] The memory resistor (R) **14** is written to a low-resistance state by setting the source voltage (Vs) to ground at the voltage source **20**, setting the gate voltage (V_G) to a programming voltage (Vp) at the gate **18**, and applying a programming pulse voltage to a drain **26**. Again, the programming voltage (Vp) is larger than the amplitude of the minimum programming pulse voltage by at least 1V. Again the drain voltage of the load transistor, V_D is not biased.

[0016] The memory resistor (R) **14** may be read by setting the voltage source (V_S) to ground at the source **20**, setting the gate voltage (V_G) at the gate **18** and the drain voltage (V_D) at the drain **26** to a read voltage (V_A), and monitoring the output voltage (V_O) at the output **16**. When the memory resistor (R) **14** is at the high-resistance state the current is very small, and the output voltage (V_O) at the output **16** is nearly equal to the drain voltage (V_D) at the drain **26**. When the memory resistor (R) **14** is at the low-resistance state the output voltage (V_O) at the output **16** is nearly equal to the source voltage (V_S) at the source **20**, which is being held at ground. This property is illustrated by the following equations:

$$I_D = \left(\frac{W}{2L}\right)\mu C_o(V_G - V_T - IR)$$
$$= \left(\frac{E}{2L}\right)\mu C_o(V_D - V_T - V_O)^2$$
$$R \approx 0 \quad V_G - V_T = V_D - V_T - V_O \quad V_O = V_D - V_G$$
$$R \approx \infty \quad I_D \approx 0 \qquad V_O \approx V_D - V_T$$

In these calculations, it is assumed that the active transistor (T_A) and the load transistor (T_L) are identical. The geometry of these two transistors can be adjusted to improve memory device performance.

[0017] FIG. **2** is a schematic view of a complementary resistive memory cell employing a first unit resistive memory cell **100** and a second unit resistive memory cell **200** similar to that provided in FIG. **1**. The complementary resistive memory cell has a first memory resistor (R_1) **114** connected between a first voltage source (V_{S1}) **120** and a first active transistor (TAI) **124**. A first load transistor (T_{L1}) **112** is connected between the first active transistor **124** and a first drain **126** connected to a drain voltage (V_D). A first output (V_{01}) **116**, also identified as bit line (BL) is connected between the first active transistor **124** and the first load transistor **112**.

[0018] The complementary resistive memory cell has a second memory resistor (R_2) **214** connected between a second voltage source (V_{S2}) **220** and a second active transistor $_{(TA2)}$ **224**. A second load transistor $_{(TL2)}$ **212** is connected between the second active transistor **224** and a second drain **226** connected to the drain voltage (V_D). A second output (V_{02}) **216** is connected between the second active transistor **224** and the second load transistor **212**. A gate voltage (V_G) is applied along a word line (WL) **300**, which is connected to the gates of both the first active transistor **120** **124** and the second active transistor **224**.

[0019] The first unit resistive memory cell **100** and the second unit resistive memory cell **200** can have their respective memory resistors **114** and **214** programmed to a high-resistance state, and a low-resistance state respectively. With the first memory resistor **114** in the high-resistance state, the

first output **116** will have its output voltage (V_{01}) equal to about V_D; while the second memory resistor **214**, which is in the low-resistance state, will have its output voltage (V_{02}) equal to about V_{S2}. This corresponds to a complementary output of 1 and 0, respectively.

[0020] FIG. **3** illustrates a layout cross-section of a portion of the complementary resistive memory cell shown in FIG. **2**, but does not show the load transistors. The item numbers in FIG. **3** correspond to the item numbers in FIG. **2** for ease of reference to like components. The memory resistors **114** and **214** are formed using a resistive memory material. The resistive memory material is a material capable of having its resistivity changed in response to an electrical signal. The resistive memory material is preferably a perovskite material, such as a colossal magnetoresistive (CMR) material or a high temperature superconducting (HTSC) material, for example a material having the formula $Pr_{1-x}Ca_xMnO_3$ (PCMO), such as $Pr_{0.7}Ca_{0.3}MnO_3$. Another example of a suitable material is $Gd_{1-x}Ca_xBaCo_2O_{5+5}$, for example $Gd_{0.7}Ca_{0.3}BaCo_2O_{5+5}$. The resistive memory material can be deposited using any suitable deposition technique including pulsed laser deposition, rf-sputtering, e-beam evaporation, thermal evaporation, metal organic deposition, sol gel deposition, and metal organic chemical vapor deposition.

[0021] The complementary resistive memory cell shown and described in connection with FIGS. **2** and **3** is somewhat complicated to program and it may be possible to program each of the memory resistors into either the high-resistance state or the low resistance state at the same time, which would defeat the purpose of having a complementary memory cell.

[0022] A simpler complementary resistive memory cell may be achieved by taking advantage of certain resistive memory material properties. FIG. **4** shows a portion of a resistive memory cell **400**, focusing on the arrangement of the memory resistors **114** and **214**. A common electrode (C) **420**, which corresponds to a common source connection is shown. A first electrode (A) **415** and a second electrode (B) **417** are provided.

[0023] Due in part to the effect of the field direction and pulse polarity on the resistive state of a resistive memory material, when a voltage pulse is applied to A relative to B, while C is left floating, the resistance of A and B will change in opposite relation. For example, when a positive programming pulse is applied to A with B grounded and C floating, the resistance between A and C is at a low-resistance state, while the resistance between B and C is at a high-resistance state. The same result would be achieved if a negative programming pulse were applied to B with A grounded and C floating.

[0024] Alternatively, when a negative programming pulse is applied to A with B grounded and C floating, the resistance between A and C is in a high-resistance state, while the resistance between B and C is at a low-resistance state. The same result would also be achieved if a positive programming pulse were applied to B with A grounded and C floating.

[0025] FIG. **5** shows a schematic view of a complementary resistive memory unit that takes advantage of the phenomenon described above in connection with FIG. **4**, and has a common voltage source/electrode (Vs) **420**, instead of first voltage source **120** and second voltage source **220**, shown in FIG. **3**.

[0026] A cross-sectional view of a portion of the complementary resistive memory unit of FIG. **5** is provided in FIG. **6**. Common voltage source **420** is shown.

[0027] The use of a common voltage source **420** simplifies programming of the complementary resistive memory unit as compared to the embodiment shown in FIGS. **2** and **3**, without a common source. The word line **300** is biased with the programming voltage V_P, while the common source **420** is allowed to float. When the first output **116** (V_{01}) is grounded and the second output **216** (V_{02}) is allowed to float, applying a positive programming pulse at the drain voltage VD, which is connected to the first drain **126** and the second drain **226**, causes a positive pulse to be applied to the second memory resistor **214** with respect to the first memory resistor **114**. Therefore, if the second memory resistor **214** is programmed to the low-resistance state, the first memory resistor **114** will be programmed to the opposite high-resistance state. Similarly, when the second output **216** is grounded and the first output **116** is allowed to float, applying a positive programming pulse at the drain voltage V_D cause the first memory resistor **114** and the second memory resistor **214** to have the opposite complementary state, such that if the first memory resistor **114** is programmed to the low-resistance state, the second memory resistor **214** will be programmed to the high-resistance state.

[0028] As fabricated the resistance state of memory resistors **114** and **214** are unknown. The memory array has to be programmed before any application.

[0029] FIG. **7** illustrates another embodiment of a complementary resistive memory structure **500**. The common electrode (C) **420**, which corresponds to a common source connection is shown, along with the first electrode (A) **415** and the second electrode (B) **417**. A single region **510** of resistive memory material is provided. Due to the properties of the resistive memory material and because the distance between A and C, or B and C, are shorter than the distance between A and C, this single resistive memory layer behaves similarly to that of the structure shown in FIG. **4**. Any change in resistance between A and B caused by applying programming pulses is negligible compared to the changes in resistance occurring between A and C or B and C. This enables the single resistive memory material layer **510** having a first electrode **415** and a second electrode **417** on one side with a common electrode **420** on the other to act as two resistors between A and C, and between B and C, comparable to resistors **114** and **214** discussed above, and appearing the schematic view.

[0030] Accordingly, just as in the case described in connection with FIG. **4**, when a voltage pulse is applied to A relative to B, while C is left floating, the resistance of A to C and B to C will change in opposite relation. For example, when a positive programming pulse is applied to A with B grounded and C floating, the resistance between A and C is at a low-resistance state, while the resistance between B and C is at a high-resistance state. The same result would be achieved if a negative programming pulse were applied to B with A grounded and C floating.

[0031] Alternatively, when a negative programming pulse is applied to A with B grounded and C floating, the resistance between A and C is in a high-resistance state, while the resistance between B and C is at a low-resistance state. The same result would also be achieved if a positive programming pulse were applied to B with A grounded and C floating.

[0032] FIG. **8** illustrates a cross-section utilizing the resistive memory structure **500**, shown in FIG. **7**, having a single resistive memory region **510** and a common voltage source **420**.

[0033] The schematic for FIG. **5** corresponds to the structure shown in FIG. **8** as well as that of FIG. **6**. When using the programming process described above, there is a large current flow through the load transistor corresponding to whichever output is grounded, the power consumption during programming may be relatively high.

[0034] When the power supply of the load transistors is separated, as shown in FIG. **9**, the programming power may be significantly reduced. The first load transistor (T_{L1}) **112** has drain **126** connected to a first drain voltage (V_{D1}), while the second load transistor (T_{L2}) **212** has drain **226** connected to a second drain voltage (V_{D2}). To program this embodiment, the word line **300** is biased with the programming voltage Vp, while the common voltage source **420** is allowed to float. When the first output **116** (V_{01}) is grounded and the second output **216** (V_{02}) and the drain **126** are allowed to float, applying a positive programming pulse to drain voltage V_{D2} at drain **226** causes a positive pulse to be applied to the second memory resistor **214** with respect to the first memory resistor **114**. Therefore, if the second memory resistor **214** is programmed to the low-resistance state, the first memory resistor **114** will be programmed to the opposite high-resistance state. Since power is not applied to the first drain, the first load transistor (T_{L1}) draws a relatively insignificant amount of power, significantly reducing power consumption during programming.

[0035] In an alternative power-saving, programming process, the power consumption of the load resistors is significantly reduced by allowing the drain voltage (V_D) to float during the programming operation. This may be accomplished by grounding the first output **116** and biasing the word line **300** with the programming voltage Vp, while the common source **420** and the drain voltage V_D at the first drain **126** are allowed to float, and a programming pulse is applied to the second output **216**, which will cause a positive pulse to be applied to the second memory resistor **214** with respect to the first memory resistor **114**. Therefore if the second memory resistor **214** is programmed to the low-resistance state, the first memory resistor will be programmed to the opposite state, in this case the high-resistance state. Note that the drain voltage V_D may be allowed to float whether there is a single drain voltage V_D, or separated drain voltages V_{D1} and V_{D2} with both floating. Similar to the processes described above, this programming sequence can be modified by applying a negative pulse to the second output **216**, or by grounding the second output **216** and applying the either a positive or negative programming pulse to the first output **116**.

[0036] For one embodiment of the present complementary resistive memory unit, the process of reading the complementary resistive memory unit is achieved by applying ground to the voltage source of both sources V_{S1} and V_{S2}, and applying a read voltage at the gate voltage V_G through the word line **300** and to the drains **126** and **226** through a single drain source V_D. The output voltage V_{01} at the first output **116** and the output voltage V_{02} at the second output **216** will be complementary such that when V_{01} is 1, V_{02} is 0; and when V_{01} is 0, V_{02} is 1.

[0037] For another embodiment of the present complementary resistive memory unit, the process of reading the complementary resistive memory unit is achieved by applying ground to the common source voltage Vs at common voltage source **420**, and applying a read voltage at the gate voltage V_G through the word line **300** and to the drains **126** and **226** through a single drain source V_D. The output voltage V_{01} at the first output **116** and the output voltage V_{02} at the second output **216** will be complementary such that when V_{01} is 1, V_{02} is 0; and when V_{01} is 0, V_{02} is 1.

[0038] For another embodiment of the present complementary resistive memory unit having separated power supplies, the process of reading the complementary resistive memory unit is achieved by applying ground to the common voltage source Vs at common source **420**, and applying a read voltage at the gate voltage V_G through the word line **300** and to each drain **126** and **226** through the drain electrodes V_{D1}, and V_{D2}. The output voltage V_{01} at the first output **116** and the output voltage V_{02} at the second output **216** will be complementary such that when V_{01} is 1, V_{02} is 0; and when V_{01} is 0, V_{02} is 1.

[0039] Although embodiments, including certain preferred embodiments, have been discussed above, the coverage is not limited to any specific embodiment. Rather, the claims shall determine the scope of the invention.

1-8. (canceled)

9. A complementary resistive memory structure comprising:

a common source electrode;

a first electrode separated from the common source electrode by a resistive memory material; and

a second electrode adjacent to the first electrode and separated from the common source electrode by the resistive memory material.

10. The memory structure of claim **9**, wherein the first memory resistor comprises a colossal magnetoresistance (CMR) material.

11. The memory structure of claim **9**, wherein the first memory resistor comprises $Pr_{1-x}Ca_xMnO_3$ (PCMO).

12. The memory structure of claim **9**, wherein the first memory resistor comprises $Gd_{1-x}Ca_xBaCo_2O_{5+5}$.

13. The memory structure of claim **9**, further comprising:

a first active transistor connected between the first electrode and a first load transistor; which is connected between a drain voltage and the first active transistor at a first active transistor drain; and a first output connected at the first active drain;

a second active transistor connected between the second electrode and a second load transistor; which is connected between a drain voltage and the second active transistor at a second active transistor drain; and a second output connected at the second active drain; and

a word line connected to a first gate of the first active transistor and to a second gate of the second active transistor.

14-18. (canceled)

* * * * *