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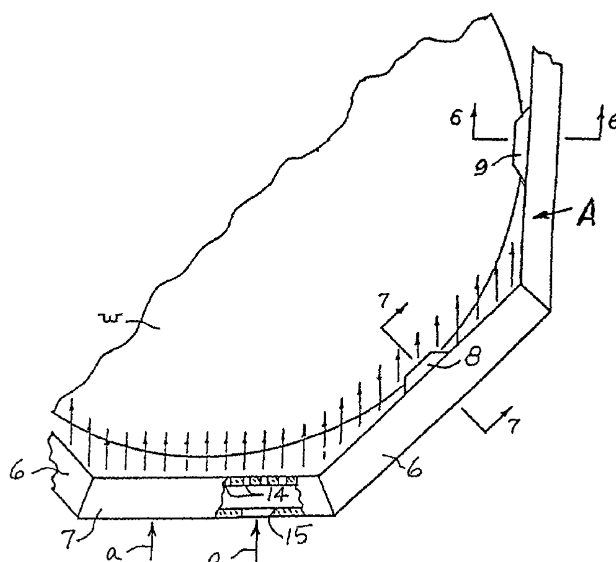
(54) Title: PROCESS AND APPARATUS FOR CLEANING SILICON WAFERS



(57) Abstract: An effective electropurge process and apparatus for wet processing of semiconductor wafers applies electrical charges to the wafer surface with an ample voltage sufficient to provide an effective field intensity which can substantially eliminate intolerable sub-0.05 micron "killer" defects when making highly advanced microchips with a feature size or line width less than 0.15 micron. The process can be used with frequent voltage reversal for automated wet-batch cleaning operations using cassettes that hold 10 to 50 wafers at a time and in various other operations involving megasonic transducers, mechanical brush scrubbers, laser cleaners and CMP equipment. The electropurge process is primarily intended for Fab plants where large wafers with a diameter of 200 to 400 mm require 250 to 350 steps including many dry layering, patterning and doping operations and at least 30 wet processing steps.

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Process and Apparatus for Cleaning Silicon Wafers

The invention as shown and described herein relates to processes and apparatus for cleaning semiconductor wafers in the manufacture of microprocessors, integrated circuits, and other sophisticated electronic devices. The invention involves the discovery of a seemingly simple and very effective cleaning system that can remove or substantially eliminate sub 0.1 micron particles during the fabrication and processing of semi-conductor wafers.

One embodiment of the invention relates to a simple and unique cleaning apparatus comprising a special shaped receptacle designed for a single silicon wafer and having generally flat vertical walls parallel to the wafer that provide a narrow space for vertical flow of cleaning liquid. The cleaning is enhanced by charging the wafer, applying a relatively low voltage insufficient to damage or degrade the delicate circuitry.

Another embodiment of the invention relates to a process and apparatus for wet cleaning of silicon wafers wherein at least twenty wafers are supported in a wafer carrier or cassette and electrically charged by induction to provide an effective field intensity during wet processing. The voltage applied to the wafers is periodically reversed to remove contaminant particles from both faces of each wafer.

The invention may seem simple in retrospect but is revolutionary in nature because it provides solutions to boundary layer problems that have mystified and plagued the semiconductor industry for decades. It involves a breakthrough in wet processing technology that should have tremendous value in the manufacture of the most advanced microchip devices.

INTRODUCTION

In the fabrication of microchips and other microelectronic devices the control of contamination is of utmost importance. As device geometries continue to shrink and die sizes grow, microcontaminants such as particles and metallic and organic impurities have an ever-increasing impact on device yields. Keeping wafer surfaces scrupulously clean throughout the wafer processing cycle is, therefore, an essential prerequisite to obtaining high yields in the fabrication of microelectronic devices.

Every wafer-processing step is a potential source of contamination. Only wet-chemical processing, or wet cleaning, between processing steps can reduce the number of particles on the surface of silicon wafers. Wet cleaning also removes metallic and organic contaminants as well as obstructive native-oxide films, which are not really a contaminant.

Wafer cleaning chemistry has remained essentially unchanged over the past 30 years, the most prevalent method in the industry still being hydrogen peroxide-based wet-chemical process -- most notably the RCA Standard Clean, where wafers are immersed in several chemicals sequentially to remove particles, metallics, organics, and native oxides. The advent of smaller geometries and contamination-sensitive features forced the industry to seek new methods of wet chemical processing or more expensive alternatives.

Background of the Invention

The RCA Standard Clean developed by Werner Kern and other RCA scientists in the late 60's is extremely effective in removing contamination from silicon surfaces of semiconductor wafers and is today and has been the defacto industry standard for more than a quarter of a century.

The rapid progress in the semiconductor industry, due in large part to the effectiveness of RCA clean (i.e., SC1/SC2), is described in detail in Werner Kern's 1993 book "Handbook of Semiconductor Wafer Cleaning" (680 pages). This progress is also discussed in "Microchip Fabrication: A Practical Guide to Semiconductor Processing" (Second Edition, 1990) by Peter Van Zant.

Unless the context or logic suggests otherwise, the terminology, abbreviations and/or jargon employed herein is intended to have a meaning consistent with the usage set forth in these Kern and Van Zant books as would be understood by those skilled in the semiconductor art.

The industry currently plans to reduce the circuit image size (also known as the line width or feature size) from 0.35 micron (um) to 0.25 micron. The leading industry group, SEMATECH, has set forth a detailed proposal for the 0.25 Micron Process which calls for around 360 process steps including more than 50 wet cleans. The detailed specifications (Steps 1 to 362) are set forth on pages B-3 to B-14 of the special printed SEMATECH publication, Technology Transfer No. 95042802-ENG. A large number of cleaning steps involve SC1, SC2 or other RCA

clean features, most or all of which could be modified in accordance with my invention to permit effective removal of extremely small or colloidal-size silica particles with a diameter of 0.05 to 0.1 micron or less which cannot be removed with current technology.

The 360-step wafer fabrication process described above involves only four basic operations. They are (1) layering, (2) patterning, (3) doping, and (4) heat treatments. A detailed overview of the wafer-fabrication process is set forth in Chapter 5 of the 1990 Van Zant book which is incorporated herein by reference. Pages 95 to 99 describe 11 basic steps employed in the formation of an MOS metal-gate transistor structure.

Cleaning steps 175, 212, 248, 284, and 320 of the aforesaid 362-step fabrication scheme shown on pages B-3 to B-14, described as Clean Post CMP, are critically important and pose a difficult problem.

The industry currently plans to reduce the circuit image size (also known as the line width or feature size) from 0.35 micron (um) to 0.25 micron or less where a particle with a minute size, such as 0.03 to 0.05 micron, create serious problems and may be considered a "killer defect".

Prior to the invention, proposed improvements in wet cleaning and dry cleaning techniques offered no real hope of eliminating significant contamination by sub 0.1 micron silica particles. Therefore, killer defects were expected and could prevent the semiconductor industry from achieving its optimistic defect goals for high volume manufacturing. The national

SEMATECH road map has set forth model defect density (and, by inference, yield) requirements by technology generation. Table 1 is a portion of such road map related to defect density goals.

Table 1 Defect Goal Trends

DRAM equiv.	16 Mb		64 Mb		256 Mb		1 Gb	
Min. dimension	0.50 μm		0.35 μm		0.25 μm		0.18 μm	
Defects/cm² (%Yield)	0.1 (87%)		0.05 (90%)		0.03 (90%)		0.01 (95%)	
	# of defects	defect size	# of defects	defect size	# of defects	defect size	# of defects	defect size
Killer defects per 200 mm wafer*	28	0.10 μm	14	0.07 μm	9	0.05 μm	3	0.03 μm

In recent years chemical-mechanical planarization (CMP), makes it possible to employ smaller and smaller line widths which may approach 0.1 micron in the near future. Unfortunately CMP involves colloidal polishing that tends to promote excessive contamination with particles of aluminum oxide, silica and the like.

In today's submicron integrated circuit technology, 0.05-micron-diameter particles can be major sources of circuit failure. Particles as small as 0.02 to 0.03 micron could become an issue soon, perhaps within the next 5 years.

Summary of the Invention

The present invention relates to unique processes and apparatus for wet processing of semiconductor wafers in which the wafers are electrically charged and more particularly to a special wafer cleaning system that is effective in removing colloidal- or sub 0.1-micron size particles that cannot be removed effectively by any known prior-art process.

The RCA-type wafer cleaning methods that have been standard in the semiconductor industry for more than a quarter of a century have been improved substantially during the last decade by use of megasonic transducer means, mechanical scrubbers or other means that helps dislodge and remove the contaminating particles. Strong or violent agitation has been provided by rotating brushes, sonic energy beams, laser beams, water jets and/or other suitable impact means. Such wet-processing techniques have made possible effective removal of contaminants with a particle size less than 0.2 micron. Improved megasonic cleaning means can remove particles as small as 0.15 micron. However, wet cleaning techniques of the type mentioned above with the latest improvements may not be effective in the future in removing sub 0.1-micron particles (e.g., those with a particle size below 0.07 micron).

Heretofore the semiconductor industry was convinced that wet cleaning methods would never be effective in removing adhered colloidal-size contaminant particles. The best scientific minds grappling with the problem assumed, with good reason, that the tremendous van der Waals adhesive forces

acting on colloidal-size particles at the wafer surface could not be overcome and that elimination of such particles by a simple wet cleaning operation was virtually impossible. The experts were convinced that the only real hope for success was a breakthrough or major improvement in dry wafer cleaning technology, perhaps a sophisticated laser technique.

The present invention provides the needed breakthrough and eliminates the need for a drastic switch from the usual wet cleaning systems to a unique dry system. It involves the amazing discovery that colloidal-size particles bonded to a wafer surface containing delicate microcircuits can easily be removed and repelled when the wafer is negatively charged in a suitable manner by applying a relatively small or limited voltage, such as 2 to 60 volts or more, insufficient to damage or degrade vulnerable portions of the microcircuits or significantly reduce the yield of top-quality microchips.

The process and apparatus of the present invention are designed for use in the fabrication of microelectronic devices on semiconductor wafers where delicate microcircuits are formed on the front face of the wafer by 250 to 350 steps or more including many layering, patterning and doping operations and a large number of wet processing steps. The preferred process of this invention is characterized in that the front face of each process wafer is provided with a suitable negative electric charge, such as 0.4 volt to 40 volts or more during wet processing and an effective field intensity, such as 0.01 volts or more per millimeter, sufficient to dislodge

and remove colloidal-size or sub 0.1-micron particles. The invention also contemplates reversing the charge on the wafer periodically for specific applications.

The provision of an electric charge on each wafer in accordance with this invention is appropriate for batch-type wet processing operations, for example, in which 20 to 40 or more silicon wafers are treated simultaneously in one wafer carrier or cassette (e.g., see Figures 13 and 14) and also for other operations where the wafers are treated one at a time. The invention is particularly well suited to water rinsing operations and to RCA-type wet cleaning operations including those with special modified sequences as mentioned in U.S. Patents Nos. 5,637,151 and 5,679,171, for example.

In carrying out the electropurge wafer cleaning process of this invention, it may be advantageous to employ megasonic transducer means for directing sonic pressure waves in a direction generally parallel to the face of each wafer thereby enhancing particle removal. In some applications it may also be appropriate or desirable to provide means for rotating the wafer(s) during wet processing.

Major advantages of the present invention can be obtained when using the preferred embodiment wherein a single wafer is subjected to wet processing in a flattened receptacle as in Figures 1 to 7 hereof. For example, a quartz glass receptacle, A, can be provided with a narrow internal cavity (e.g. of a size to receive one 200 mm, 300 mm or 400 mm wafer) having flat parallel glass wall spaced a short distance from

the flat wafer faces. An aqueous solution or DI water would be caused to flow from the bottom to the top of the receptacle while the surface of the wafer was electrically charged. A desired negative charge is preferably induced by employing a positively charged metal plate, layer or coating at the flat outer surfaces of the receptacle as shown in Figures 6 and 7, for example.

One wet cleaning operation commonly involves RCA-type wet cleans with acid and alkaline treatments and a plurality of DI water rinses followed by IPA drying, spin drying or other final drying step. During all or most of the wet cleaning operations, the silicon wafer can be electrically charged in accordance with the present invention to a predetermined limited voltage, such as 2 to 60 volts. A substantially higher voltage may sometimes be tolerable, but charging the face of the wafer to a voltage of 100 volts or more can be risky and is usually unnecessary or undesirable.

An excessive voltage is undesirable, if not foolish, because of possible adverse effects on quality, uniformity and process yields and the increased risk of degrading the more delicate portions of the microcircuits.

In the semiconductor industry, one of the current target goals in microchip fabrication is to reduce the defect density to less than 0.03 defects per square centimeter (See Table 1). An object of the present invention is to reach that goal in a simple and effective manner by substantially eliminating "killer particles" and minimizing the number of troublesome

particles (e.g., those with a particle size more than 10 percent of the minimum line width or feature size) which are detrimental or highly undesirable.

The term "killer defect" is used herein in the broad sense to cover an unacceptable or intolerable defect in the microelectronic circuits of a semiconductor device or microchip caused by a contaminant particle trapped or embedded in the device during the fabrication process. A defect can be considered intolerable or unacceptable if it degrades the electronic circuits substantially or to such a degree that the electronic device has limited utility or is unacceptable to most customers.

The term "killer defect" is used in a narrow sense in Table 1 on page 5 of this specification to describe trapped or embedded particles with a particle size that is at least about 20 percent of the minimum line width or feature size (identified in the table as "Min. dimension"). That table from the SEMATECH road map indicates that one of the goals is to obtain a 90-percent yield of advanced (0.25 um) wafers with no more than 0.03 killer defects per square centimeter.

The term "killer defect", when used herein in the narrower sense, does not include colloidal-size particles with a size of 0.01 micron or less and does not cover very small microscopic particles (e.g., those with a particle size of from about 5 to about 10 percent of the minimum line width) that are detrimental or highly undesirable and could affect the quality, reliability and useful life of the device.

Wafer Cleaning Technology

Surface contamination is considered to be a major problem in the semiconductor, aerospace, and pharmaceutical industries. The adhesion of contaminants to silicon substrates is largely responsible for the yield loss in the manufacturing of VLSI and ULSI devices. Many methods for removing particles from silicon surfaces are currently used but the most common techniques are the wet chemical processes based on the hydrogen peroxide/ammonium hydroxide mixtures (SC1 or APM). The addition of megasonic energy during these processes has been proven to enhance particle removal.

Historically, SC-1 solutions were based on highly concentrated mixtures of ultrapure de-ionized water (DIW), ammonium hydroxide (NH_4OH), and hydrogen peroxide (H_2O_2), in a volume ratio of 5:1:1 (5 DIW: 1 H_2O_2: 1 NH_4OH). Typically; wafers are immersed in these cleaning baths at 70-85°C for 10 minutes. Higher temperatures are not recommended in order to minimize thermal decomposition of hydrogen peroxide and evaporation of ammonium hydroxide. Wafer rinsing in DI water is usually conducted in intermediate and final steps.

During a SC-1 cleaning process, a cooperative and compensating action exists between the two chemical components. H_2O_2 oxidizes the silicon and forms a chemical oxide; the formation of this oxide is limited by the diffusion of the oxidizing species. Ammonium hydroxide, conversely, slowly etches this chemically grown oxide. The result of these two processes is that a chemical oxide layer will

continually be generated and removed. Particles are thus removed by this etching and undercutting action. Particle removal efficiency can be increased by increasing the etch rate of SiO_2. The etch rate, in turn, can be increased by using greater concentrations of NH_4OH or by elevating the process temperature.

The continually increasing integration of advanced IC manufacturing requires tighter process control and specifications. In addition, more stringent environmental requirements are being mandated to reduce chemical and water consumption and waste. The use of megasonic energy has been applied to many wafer surface cleaning procedures as a means to enhance particle removal, reduce chemical concentrations, and shorten process times. The acoustic waves needed for cleaning are about 0.7 to 1.5MHz and are generated from piezoelectric transducers.

The RCA Standard Clean, developed by W. Kern and D. Puotinen in 1965 and disclosed in 1970 [1] is extremely effective at removing contamination from silicon surfaces and is the defacto industry standard [2]. The RCA clean usually consists of two sequential steps: the Standard Clean 1 (SC-1) followed by the Standard Clean 2 (SC-2). The SC-1 solution, consisting of a mixture of ammonium-hydroxide, hydrogen-peroxide, and water, is a most efficient particle removing agent.

Wafer rinse stages are an integral part of the chemical processes necessary in semiconductor device manufacturing. As

an important stage in an integrated process, rinsing plays a central role in device yield, cost of ownership and environmental issues which continue to have increasing importance for the semiconductor industry. Because of these considerations, there are significant benefits to developing optimized rinsing processes, including better device performance, reduced water consumption, shorter cycle times, higher tool utilization and higher throughputs -- all leading to lower cost of ownership.

Environmental and economic considerations are now significant when discussing rinsing processes. For example, in the front end of line (FEOL), through the first contact cut, approximately 20 separate cleaning sequences are needed to provide sufficient surface quality and to isolate each step from the others. A typical sequence may include, 4 cleaning baths, 4 rinses, and a drying step. For 20 FEOL cleans this is 80 rinses. Given the number of rinses and current deionized water (DIW) use, this is 1,000 liters of DIW per wafer, just for FEOL. If one also considers back end of line (BEOL) and losses in the deionization system, over 3,700 liters of incoming water per wafer is required to meet current needs. With 5,000 wafer starts per week, this is 70 million liters of incoming water per month, just for rinsing.

Hydrofluoric Acid Solutions

Mixtures of concentrated hydrofluoric acid (49 wt% HF) and DI water have been widely used for removal by etching of silicon dioxide (SiO_2) films and silicate glasses (e.g.,

phosphosilicates, borophosphosilicates) that were grown or vapor deposited on semiconductor substrate wafers. The chemical dissolution reactions have been identified and described in the literature.

The thin layer of native oxide on silicon, typically 1.0 to 1.5 micron (um) thick, is removed by a brief immersion of the wafers in diluted (typically 1:50 or 1:100) ultrapure filtered HF solution at room temperature.

Sulfuric-Acid/Hydrogen-Peroxide Mixtures

Removal of heavy organic materials from silicon wafers, such as photoresist patterns and other visible gross contaminants of organic nature, can be accomplished with mixtures of 98% H_2SO_4 and 30% H_2O_2. Volume ratios of 2 - 4:1 are used at temperatures of 100°C and above. A treatment of 10 - 15 min at 130°C is most effective, followed by vigorous DI water rinsing to eliminate all of the viscous liquid.

Conventional RCA-Type Hydrogen Peroxide Mixtures

These are the most widely used and best established cleaning solutions for silicon wafers. They are made up of ultra-filtered, high-purity DI water, high-purity "not stabilized" hydrogen peroxide, and either electronic-grade ammonium hydroxide or electronic-grade hydrochloric acid. These mixtures, used in two process steps, have become known as RCA standard cleans (SC-1 and SC-2). The treatment is usually preceded by the preliminary cleaning.

The first step uses a mixture (SC-1) of 5:1:1 by volume of DI water, H_2O_2 (30%, "not stabilized"), and NH_4OH (29 w/w%

as NH_3) at 70°C for 5 min. followed by quench and rinse with cold ultra-filtered DI water. This deceptively simple procedure removes any remaining organics by oxidative dissolution. Many metal contaminants (group IB, group IIB, Au, Ag, Cu, Ni, Cd, Co, and Cr) are dissolved, complexed, and removed from the surface.

The solution temperature should be 70°C for sufficient thermal activation, but must not exceed 80°C to avoid excessively fast decomposition of the H_2O_2 and loss of NH_3.

The second step in the conventional RCA cleaning procedure uses a mixture (SC-2) consisting of 6:1:1 volume of DI water, H_2O_2 (30%, "not stabilized"), and HCl (37 w/w%). A solution temperature of 70°C for 5-10 minutes is used followed by quenching and rinsing as in the SC-1 treatment. SC-2 removes alkali ions, NH_4OH-insoluble hydroxides such as Al $(OH)_3$, Mg $(OH)_2$, and any residual trace metals (such as Cu and Au) that were not completely desorbed by SC-1.

An optional etching step with dilute HF solution can be used between the SC-1 and SC-2 treatments of bare silicon wafers. Since the hydrous oxide film from the SC-1 treatment may entrap trace impurities, its removal before the SC-2 step should be beneficial. A 15-second immersion is 1% HF-H_2O (1:50) solution is sufficient to remove this film.

Each of the chemical cleaning and rinsing operations described above using alkaline or acid solutions and pure water (e.g., using SC-1 or SC-2 solutions or the like in RCA-type sequences) can be enhanced by applying to each

semiconductor wafer a predetermined limited voltage, such as 2 to 60 volts or more, in accordance with the invention as described hereinafter. Providing an adequate or ample electric charge on the wafer during wet processing in a receptacle of the type shown in Figures 1 to 7, for example makes possible remarkably effective removal of sub 0.1 micron contaminant particles.

Ultrasonics and megasonics are commonly used particle removal techniques for silicon wafer cleaning. In ultrasonic cleaning, sonic energy in the range of 20-40kHZ is applied to a liquid within which the wafers are immersed. The force required to remove a particle in a sonic field, in the absence of any cavitation is: $F_r = ma$ where m is the mass of the particle and $a=4\pi^2f^2A_m$. A_m is the amplitude and f the frequency of the sonic vibration.

In most commercial megasonic cleaners, it is this force, combined with the force created by cavitation that is generally considered important in the removal of particles.

Future Needs

Particle removal in the sub 0.1 micron regime is a key requirement for advanced cleaning technologies and is essential when making modern microchips with a line width of 0.25 micron. Unfortunately megasonic cleaning technology is inadequate or ineffective in removing silica particles of such small size.

The simple fact is that current wet cleaning technology does not provide a satisfactory answer to the microcontamina-

tion problem and may not permit reduction in line widths to 0.13 micron or below, the industry goal.

The aforesaid 1993 Kern handbook confirms the inadequacy of wet cleaning technology and indicates that dry cleaning processes will have to be used in the future to obtain the ultrapurity needed for the next generation of microchips.

Excessive costs have always been a major problem in semiconductor manufacture. Wafer cleaning costs during manufacture of microchips are extremely high and can be justified only because of the critical need to obtain adequate process yields.

The various factors that determine process yields are discussed in chapter 6 of the 1990 Van Zant textbook, and Figures 6.2, 6.6 and 6.8 on pages 107, 113 and 114 are particularly pertinent with respect to cum yield.

Frequent wet cleans are essential during wafer processing to achieve satisfactory yields. In the 362-step manufacturing process previously described, more than 50 wet cleans would be employed. Wet benches are commonly used for wet cleaning operations and may employ robotic means for automatically advancing silicon wafers 25 to 40 at a time from one station to the next. A wet-bench set up is illustrated, for example, on page 138 of Kern's 1993 handbook.

When using RCA standard cleans (SC-1 and SC-2), a typical wet bench includes 5 or 7 recirculation immersion tanks, such as the tank shown in Patent No. 5520205, in which liquid is continuously pumped into the bottom of the tank and caused to

overflow. Liquid cleaning, rinsing and drying steps in a typical wafer processing sequence (MOS gate oxidation) are shown by cross hatching in Figure 3 (Kern page 281). A 5-tank wet bench could, for example, start with an HF strip and DI rinse followed by SC-1, DI rinse, SC-2 and DI rinse. Megasonic cleaning means would typically be used in the SC-1 bath but could also be used in the SC-2 bath and/or the rinse baths. A 7-tank wet bench could include a final HF bath followed by another DI rinse.

Needless to say, very large amounts of deionized (DI) water are required for the typical cleaning system. The water is extremely pure with a typical resistivity of 18 mega ohms. The DI water is usually dumped after use but can sometimes be cleaned and recirculated.

A 5-tank or 7-tank wet bench of the type described above could, for example, be employed for each of the wet clean steps 2, 5, 23, 35, 37, 63, 68, 70 and 108 of the 362-step manufacturing process previously described. It will be understood that the semiconductor wafers being processed must be dried at the conclusion of each wet clean before the next dry process step. A spin rinse dryer or IPA dryer is commonly used for this purpose.

The specific 362-step fabrication process of the SEMATECH publication, pages B-3 to B-14 includes the lithographic (patterning-doping) sequence of described steps 14-22 and seven other lithographic sequences 25-34, 72-81, 82-92, 110-118, 119-128, 135-143 and 144-153 that are basically the same

as the sequence 14-22, except for added inspection steps 31, 87, 124 and 149. Note also that there are slight differences at the ion implantation steps 78, 79, 89 and 90. Two other lithographic sequences 41-51 and 178-187 are quite similar but omit the implant step (20) and include added etching steps 48, 49 and 185.

The aforesaid fabrication process also includes the previously described layering-patterning sequences 195-204 and 214-224 involving metal or oxide deposits, steps 195 and 214, and chemical-mechanical polishing, step 211. It also includes three sequences 233-242, 269-278 and 335-344 that are basically the same as the described sequence 195-204 and three sequences 247-260, 283-296 and 314-331 that are basically the same as the described sequence 211-224.

The 362-step fabrication process includes more than 50 wet cleaning or wet processing operations that can be modified and improved in accordance with my invention as by inducing a substantial electric charge in each silicon wafer. These include eleven RCA-type wet cleaning operations (such as described steps 2, 5 and 23) including steps 35, 37, 63, 68, 70, 108, 129 and 154; four HF cleans, steps 65, 93, 103 and 133; five post CMP cleans, (such as described step 212) including steps 175, 248, 284 and 320; nine NMP cleans (such as described step 209) including steps 227, 245, 263, 281, 299, 317, 334 and 347; ten resist-strip with NMP (such as described steps 204 and 224) including steps 242, 260, 278, 296, 331, 344, 356 and 362 and fourteen resist-strip with H_2SO_4

(such as described steps 13 and 22) including steps 34, 51, 62, 81, 92, 105, 118, 128, 143, 153, 161 and 187.

Proposed Laser-boil Cleaning System

In recent years a hybrid laser cleaning system has been proposed for use in cleaning semiconductor wafers. In this system a wafer is wetted and covered with a water film. A laser beam directed against the liquid film causes violent localized boiling that helps remove particulate contamination.

Planarization and Post CMP Cleaning

Successful mass production of the advanced microchips used in today's computers became possible because of the development of a number of planarization techniques used to offset the effects of varied wafer topography. The techniques of multilayer resist processing, planarization layers, reflow, and chemical-mechanical polishing (CMP) are collectively known as planarization techniques.

The planarization methods do not guarantee an absolutely flat wafer surface ideally suited for subsequent lithographic operations. The only process that provides a global planarization of an entire wafer face is CMP, the same basic process used to flatten and polish the wafers sliced from the silicon crystal after crystal growing. Unfortunately the abrasive material used for polishing (i.e., silica or aluminum oxide) creates a major particulate contamination problem.

In a typical CMP polishing operation the wafers are mounted upside down on a holder and rotated in the other direction as in the SpeedFam CMP-V system shown and described

in "Semiconductor International", May 1993 (Figure 10.16 of the 1993 article is a picture). An alkaline slurry of silica (glass) or aluminum oxide suspended in a mild etchant, such as potassium or ammonium hydroxide, is caused to flow between the wafer and the polishing pad.

The removal of particulate contaminants from semiconductor wafers during post CMP cleaning operations is a most difficult and perhaps the most important of all wet processing operations in the fabrication of advanced microchips.

At the present time mechanical wafer surface scrubbers are considered the most practical when particulate removal is critical as in post CMP processing. The scrubbers usually hold the wafer on a rotating vacuum chuck. While being firmly held, a rotating brush is brought in near contact with the rotating wafer while a stream of deionized water (often with a detergent) is directed onto the wafer surface. This creates a high-energy cleaning action at the wafer surface. The liquid is forced into a small space between the wafer surface and the brush ends where it achieves a high velocity, which improves the cleaning action.

For the last 30 years the most competent scientists have been convinced that the primary force binding a colloidal-size particle to a wafer surface is van der Waals attraction which is universal and dominating when separation distances between a particle and a surface are extremely small (e.g., below 5 namometers). The forces of attraction increase as the

particle size decreases so that it appears virtually impossible to overcome the van der Waals forces when the particle size is 0.01 micron or less.

On this basis foremost experts, such as Werner Kern, concluded that wet cleaning processes could not provide a satisfactory way to remove colloidal-size particles when manufacturing the most advanced microchips and that new dry methods would have to be developed.

Attempts were made to improve the effectiveness of wet wafer cleaning processes by causing strong or violent agitation of the liquid as by providing concentrated bursts of energy from lasers or megasonic transducers or by providing continuous mechanical agitation by rotating scrub brushes. However, such methods were not expected to be adequate for removal of sub 0.05-micron particles. Heretofore, more sophisticated dry cleaning methods seemed to provide the only real hope for minimizing particulate contamination when manufacturing advanced microprocessors with a minimum feature size or line width of 0.15 micron or less.

The universally accepted theories of the best scientific minds have turned out to be major impediments to progress in the wafer cleaning field. The present invention demonstrates serious flaws in those theories, particularly with respect to the nature and importance of van der Waals forces. Prior to the invention, the semiconductor industry had no reason to suspect that simple electrical equipment could provide a

tremendous improvement in the effectiveness of wet cleaning processes.

Definitions and Terminology

The language used in the present disclosure should present no problem to persons skilled in the art of which the present invention pertains. The language should be construed in a reasonable and logical manner consistent with the context and normal usage in the art. Generally the technical terms and jargon can be construed to be consistent with the language or terminology employed in the textbook "Microchip Fabrication" (3rd Edition, 1997) by Peter Van Zant.

For example the terms angstrom, wafer boat, capacitor, CMP, CVD, CUM yield, DI water, die, dopant, DRAM, feature size, integrated circuit, ion implantation, killer defect, layering, lithograph, LSI, patterning, passivation, photoresist, quartz, RTP, rinse, ULSI, VLSI, wafer and yield are defined briefly in the Glossary (pages 587 to 605) of said textbook.

The term "semiconductor wafer" is used herein to describe a wafer of the type commonly used in the semiconductor industry.

The term "feature size" or "line width" is used herein in the usual sense to indicate the minimum width of pattern openings or spaces in a microelectronic device or microchip.

The term "megasonic" is used herein to describe energy waves generated from piezoelectric transducers in the 750- to 1500-kilohertz (kHz) range.

The term "field intensity" indicates the strength of an electric field. An "effective field intensity" as used herein

is at least about 0.01 volts per millimeter.

The term "charge density" indicates the degree of charge or current-carrier concentration in a region (e.g., coulombs/cm^2).

The term "electrode" is used herein to describe a silicon plate or wafer or a similar metal or metal-coated plate or device that can be electrically charged and employed to induce or create an electrical charge in a process wafer in accordance with the present invention.

A DC power source or power supply can be a direct current generator or battery or other source, such as a transformer-rectifier-filter arrangement.

The terminology used in the patent claims hereof should be construed in a reasonable manner in the light of the description and common usage. Unless the context suggests otherwise the terms are intended to be broad in scope rather than to have an unnecessary limited meaning.

Unless the context or common sense shows otherwise parts or percentages are by weight rather than by volume.

Description of the Drawings

Figure 1 is a front elevational view on a reduced scale showing a unique wafer cleaning means A in the form of a flattened quartz glass receptacle 10 having a narrow internal cavity that receives a single semiconductor wafer w;

Figure 2 is a fragmentary elevational view on a larger scale with the flat front wall 2 of the receptacle omitted and a portion of the marginal tube being shown in section, the

vertical flow of liquid from the tube 5 being shown by the arrows;

Figure 3 is an enlarged fragmentary sectional view of the inclined tube portion 6;

Figure 4 is an enlarged fragmentary sectional view of the marginal tube 5;

Figure 5 is a fragmentary top view of tube portion 6;

Figure 6 is an enlarged fragmentary sectional view taken on the line 6-6 of Figure 2;

Figure 7 is an enlarged fragmentary sectional view similar to Figure 4 but taken on the line 7-7 of Figure 2;

Figures 8 to 12 are schematic views illustrating modified forms of apparatus that could be employed in the practice of this invention;

Figure 8 is a schematic foreshortened vertical sectional view on an enlarged scale showing a modified form of split glass receptacle (20) which may be opened for insertion or removal of the wafer;

Figure 9 is a schematic side elevational view of the receptacle (20) on a reduced scale;

Figure 10 is an enlarged fragmentary vertical sectional view similar to Figure 8 showing a modified glass receptacle suitable for wet cleaning of flat panel displays and/or field emission displays and including electrical means for charging the panel or wafer;

Figure 11 is a side view of the receptacle of Figure 10 similar to Figure 9;

Figure 12 is a schematic vertical sectional view showing another modified form of wafer cleaning apparatus.

Figure 13 is a schematic side elevational view drawn substantially to scale with parts broken away and parts in section showing a preferred embodiment of the invention wherein 25 silicon wafers are electrically charged in a tank during wet cleaning; and

Figure 14 is a schematic top view of the cleaning apparatus of Figure 13 on the same reduced scale.

Description of Preferred Embodiments

One of the embodiments of the present invention is illustrated in Figures 1 to 7 and employs a flattened wafer holder and receptacle 10 designed to receive a single semiconductor wafer w. This embodiment and other embodiments of a similar nature using single-wafer receptacles or the like are believed well suited for modern fabrication systems, particularly those that employ silicon wafers with diameters of 200 mm or more. When smaller wafers are employed, it may be preferable to employ other embodiments of this invention wherein 20 to 40 or more wafers mounted on a wafer carrier or cassette are cleaned and rinsed while being electrically charged.

Such wet-batch cleaning apparatus (e.g., of the type shown in Figures 13 and 14) or a single-wafer apparatus (e.g., of the type shown in Figures 1 and 2) can be modified using sonic energy, laser energy, scrubbing means or other means which may be appropriate in some applications. Modified

versions of the apparatus can, for example, include megasonic transducer means for directing sonic pressure waves in a direction generally parallel to the wafer face (e.g., see U.S. Patents No. 4,869,278; 4,998,549 and 5,037,481).

Figures 1 to 7 illustrate an embodiment of the present invention wherein a wafer carrier formed of glass, silicon or other suitable material has a narrow internal cavity that receives a single silicon semiconductor wafer and has means for charging the wafer to a small voltage during wet processing operations. These figures provide a simple schematic illustration of apparatus particularly well suited for use in the practice of the invention and are intended to facilitate a ready understanding of the invention and the various ways the apparatus can be used in a high-tech microchip fabrication plant, for example in a typical 300-plus step manufacturing process that involves 40 to 50 or more wet processing steps.

While these drawings are to some extent schematic and omit features which may be considered valuable or important, they include the basic elements needed for practice of the invention and are drawn substantially to scale to provide an example of a simple quartz glass receptacle that would be suitable for commercial use as is or with simple modifications but probably would be improved greatly before use by a large manufacturer.

As shown, a wafer carrier A is provided in the form of an open-top quartz glass receptacle with top surfaces 1 and a

pair of identical parallel flat glass walls 2 and 3 preferably spaced apart a distance of several millimeters, usually at least twice the thickness of the silicon wafer. The front and rear glass walls have flat vertical surfaces at opposite sides that are welded to the flat surfaces of straight vertical side bars 4 of rectangular cross section.

A quartz glass tube assembly 5 of semihexagonal shape is welded to the lower margins of the plates 2 and 3 which have an identical semihexagonal shape. It will be understood, of course, that the assembly 5 and the plates 2 and 3 could be semicircular, if desired, to conform more closely to the shape of the circular semiconductor wafer w. A modern wafer used for manufacture of advanced microchips can have a diameter of 200 to 400 millimeters.

The glass tube assembly 5 has two oppositely inclined straight portions 6 welded to a straight horizontal portion 7. The flat surface 13 of tube portion 6 is welded to the flat inclined bottom surfaces of the plates 2 and 3 at opposite sides of a row of regularly spaced vertical openings 12 that direct liquid vertically in the direction of the arrows b (Figure 3). The horizontal tube portion 7 has a similar flat upper surface welded to the flat horizontal bottom surfaces of plates 2 and 3 on opposite sides of a row of closely spaced vertical openings 14 as shown in Figure 4. The tube sections 6 and 7 can have the same cross section throughout the length of tube assembly 5 so as to provide an unobstructed passage

for flow of liquid between the two side bars 4 and access to all of the multiplicity of openings 12 and 14.

The liquid pumped into the bottom inlet openings 15 of tube portion 7 as indicated by the arrows a is directed vertically from those openings at a multiplicity of regularly or closely spaced locations as indicated by a multiplicity of vertical arrows in Figure 2. The water or cleaning liquid can be pressurized by the pump P, as in the embodiment of Figures 8 and 9, and caused to flow rapidly from the openings 12 and 14 as water jets or separate vertical streams, but this is not essential. The tube assembly 5 is designed to provide substantially uniform upward flow of liquid across the full diameter of the wafer so that laminar flow will occur and unwanted eddy currents will be minimized or substantially eliminated. This assures rapid removal of all chemicals when changing from an acid to an alkaline wash or vice versa or changing to a DI water rinse.

The glass receptacle A of Figures 1 and 2 is open at the top edge 1 to permit vertical movement of the wafer w into and out of the narrow internal cavity 16 defined by the flat glass walls 2 and 3 and the marginal members 4, 6 and 7 (The large top opening is unnecessary in the embodiment of Figures 8 and 9 because the receptacle is split in half). The top edge portion at 1 provides a weir for overflow of liquid and can be flat or serrated. If the liquid overflows into a tank it can be filtered and recirculated, if desired.

Means are provided for holding and supporting a single semiconductor wafer in a vertical position midway between and parallel to the glass walls 2 and 3. If desired such means can be designed to permit or facilitate rotation of the wafer during the cleaning operation. As shown such means comprises a plurality (e.g., 3 to 5 or more) of wafer guide means 8 and 9 welded to or adhered to the marginal means 4, 6 or 7 and having grooves 11 that received and substantially fit the rounded circumferential edge portion of the wafer w. Such grooves can be shaped to maintain each wafer in the desired vertical position and can permit rotation of the wafer as by water pressure, sonic energy or mechanical means (e.g., see U.S. Patents Nos. 5,286,657 and 5,698,038).

In the practice of the present invention electrically-conductive plates, layers or coatings are provided at or near the surface of the glass receptacle to permit charging of the wafers and thereby effect removal of submicron particles adhering to the wafer surface. If a conductive metal coating is employed, it is preferably applied at the outer surface of the plate 2 or 3. However, a layer or coating of silicon metal could be employed at the inner surface. In fact the plates 2 and 3 could be formed of silicon metal to minimize the distance from the charged plate to the wafer surface, thereby increasing the field intensity at a given voltage.

As shown herein a flat conductive metal charge plate or electrode 10 is mounted on the flat outer face of each plate 2 and 3. The plate is circular and has a diameter at least

equal to and not substantially less than that of the wafer w, but other shapes and sizes may be appropriate or acceptable (e.g., when the wafer is rotated).

In order to obtain the desired uniformity it is desirable to divide the charge plate 10 or other charging means into a large number of sections so that independent computer control of the electric charge can be provided for each section. As shown the plate 10 is divided into more than 50 square sections to permit such computerized control of the charge density at each section.

In one embodiment of my invention, purging or cleaning of a semiconductor wafer can be carried out using wet cleaning means B of the type shown in Figures 8 and 9 comprising a flattened wafer holder and receptacle 20 formed of high-purity quartz glass having parallel flat circular wall portions 21 and 22 of uniform thickness and integral bottom and top portions 23 and 24 suitably connected to bottom inlet and top outlet pipes 44 and 45. A pump P is provided to cause the desired upward flow of DI rinse water or an aqueous cleaning solution through the receptacle 20.

The receptacle 20 can be split to form two halves 20a and 20b that fit together to form an airtight or watertight seal at the vertical split line 38. Optionally the receptacle may be divided into upper and lower sections with a seal at a horizontal split line. Suitable means may be provided to clamp or hold the two halves of the receptacle together and to maintain the desired seal. For example, some type of

releasable clamping or holding means 39 can be provided to hold the halves 20a and 20b together during the wet cleaning operation and perhaps during a subsequent spin drying operation. Optionally, a series of very small glass projections or spacers 50 or other suitable holding means can be provided to locate or hold the wafer 30 or to hold it in a fixed position.

The unique quartz glass receptacle 20 is shaped to provide a shallow flat circular cavity 25 of uniform width with very shallow portions 26 and 27 of narrow cross section and uniform width at the opposite faces 31 and 32 of the wafer. Optionally the receptacle can be formed in one piece or welded to join opposite halves, but this would require a narrow slot or opening at the top to permit a wafer to be lowered into and raised out of the cavity 25. Robotic means could be provided to lower, raise, and/or hold the wafer during wet cleaning and drying.

The cavity 25 of the receptacle 20 is shaped to assure laminar flow of liquid over the flat front and rear surfaces 31 and 32 of the silicon wafer 30, whose circular marginal surface 33 is preferably rounded. The wafer may, of course, have a notch or flat portion at the margin to assure proper positioning during manufacture. The inlet and outlet portions 23 and 24 of the glass receptacle are provided with smooth curved surfaces 23a and 24a, respectively, shaped to assure laminar flow free of eddy currents or turbulence as the aqueous liquid flows into or out of the narrow cavity 25.

The cavity 25 is shown as being generally circular and can have a uniform horizontal width preferably from about 2 to about 5 times the thickness (or horizontal width) of the silicon wafer 30 (e.g., a conventional 200 mm or 300 mm wafer). As shown the cavity width may be 3 or 4 times the wafer thickness so that the narrow spaces 26 and 27 between the wafer surfaces 31 and 32 and the glass surfaces 21a and 22a have a width of only a few millimeters, typically about 2 to 4 millimeters. The thickness of the vertical wall portions 21 and 22 is usually from about 2 to about 5 mm.

The RCA clean system (SC-1 and SC-2, etc.) or a similar system suitable for modern wafer cleaning is preferred when carrying out the process of my invention using the single-wafer glass receptacle and also in the embodiment of Figures 13 and 14. The efficiency in removing submicron particles can, of course, be improved by employing megasonic energy. For example, optional megasonic cleaning means can be provided with an array of piezoelectric transducers near the outer marginal portions of the wafer 30 (at 60, Figure 9). Such means is located to cause the sonic pressure waves to travel through the liquid (from location 60) in a direction parallel to the vertical wafer surface. The impact of these pressure waves on contaminating particles with a diameter greater than 0.1 micron may be sufficient to dislodge them, but may not be effective in removing smaller particles. Megasonic cleaning means are disclosed, for example, in Verteq Patents No. 4,869,278; 4,998,549 and 5,037,481 and 5,286,657.

The wafer cleaning apparatus B of Figures 8 and 9 is designed to receive flat discs or wafers 30 of circular shape but could be modified as in Figure 11 for wet cleaning of rectangular discs or wafers with or without the use of megasonic energy (at 60). The wet cleaning process and apparatus of my invention was designed primarily for use during the manufacture of microchips from circular silicon wafers, but is also important for use during the manufacture of rectangular flat panel displays (FPDs) and field emission displays (FEDs). The majority of FPDs are the color-active matrix liquid-crystal displays (AMLCD) most often seen as laptop computer screens.

Both color and noncolor LCD displays are manufactured using microchip-fabrication technology comparable to that described herein. However, the microelectronic devices, transistors, etc. are formed on relatively large rectangular glass plates rather than on a silicon wafer. The typical glass plate of an FPD has a width of at least one foot (300 mm) and is a borosilicate glass. Unlike a silicon wafer, the glass plate (e.g., plate 30′) is nonconductive and cannot readily be charged by induction like the silicon wafer 30 of Figure 1. For this reason it is desirable to employ apparatus of a type specially designed for cleaning the rectangular FPD plate as shown in Figure 10, for example.

The cleaning means B′ of Figures 10 and 11 is generally equivalent to the apparatus B of Figures 1 and 2 (except for the location of the glass plate 30′ against or almost in

contact with the flat wall portion 21′ of the quartz glass receptacle 20′) and is used in the same way (e.g., with the RCA clean sequences).

As shown the cleaning means A comprises a flattened quartz glass receptacle 20′ having flat wall portions 21′ and 22′ of uniform thickness and integral curved bottom and top portions connected to inlet and outlet pipes 44 and 45. The receptacle is formed in two (non-symmetrical) halves that fit together at the vertical split line 38′ to form an air-tight or liquid-tight seal throughout the periphery of the narrow cavity 25′. The portion 27′ of that cavity between wall portion 22′ and plate 30′ has a horizontal width that is usually no more than 3 or 4 millimeters and may, for example, be the same as that of the cavity portion 27 of Figure 8 so as to function in the same way.

The shape of the two-piece glass receptacle 20′ differs from that of receptacle 20 at the inlet and outlet ends 28′ and 29′. In Figure 10, the upper and lower portions 34 and 35 of the front half (20c) of the receptacle containing wall portion 22′ is preferably symmetrical with only a slight curvature. In the rear half containing wall portion 21′, the upper and lower portions are also symmetrical (as in Figure 8) with a curvature (e.g., at 23′) comparable to that of inlet and outlet portions 23 and 24, but the inner surface at the margin of glass plate 30′ is shaped to fit the plate at its marginal edge. If desired the receptacle may be made to fit the flat narrow marginal faces of the glass plate (at 33′),

thereby eliminating a marginal gap. However, as shown in Figure 10, there is a marginal gap that's substantially filled with a narrow marginal strip 41 of generally triangular cross section. The strip extends around the entire periphery of the glass plate 30' to promote laminar flow of liquid and minimize unwanted eddy currents or the like. It can be rigid or flexible and can be formed of silicon, glass or other suitable materials.

In carrying out the process of the present invention, a small precision robot can be employed to pick up a single wafer 30 or a single FPD plate 30' and transfer it to a wet cleaning means B or B'. After the wafer or glass plate is placed in and securely located in the open half of the quartz glass receptacle 20 or 20', the receptacle is closed and held closed by clamping means or the like at 39 until the RCA or other cleaning sequence (or rinse) is completed.

The liquid flow provided by a water pump P or in other manner by a spray technique or vapor condensation is toward the outlet end from the inlet. The wafer 30 for example, can be in a substantially vertical position or in an inclined or horizontal position provided the flow is toward the outlet. If desired, one or more receptacles 20 can be spun about a vertical or horizontal axis at any desired speed to provide a centrifugal force on the liquid at the wafer surface. The desired movement of the water or other liquid over the wafer surface may be obtained with or without a pump P. It will also be understood that the DI water in the final rinse may be

displaced with isopropyl alcohol prior to spin drying or other final drying operation.

The apparatus B of Figures 8 and 9, for example, is inexpensive and well suited for laboratory research. Apparatus of this type designed for research and development work in the field of wafer cleaning happens to be convenient for use in research involving electricity. The glass receptacle 20, for example, can easily be provided with a silver coating or other conducive metal coating (e.g., at 47 and 48) as part of an electrical circuit. The simple circuit shown in Figure 10, for example, can easily be employed with the wet cleaning apparatus B or B′ to apply a positive or negative charge.

That circuit includes a battery means or DC power source D with lines 1′ and 2′ connected to the negative and positive terminals, respectively, and an on-off switch 3′. The power source D can include means to adjust and measure the voltage or emf.

It has been discovered that inducing a charge in a silicon wafer, such as the wafer 30, by providing a limited voltage, such as 2 to 60 volts, at the metal plate 47 or 48, is effective to remove submicron particles from the wafer surface during microchip fabrication. A voltage insufficient to harm or damage a modern microchip with a line width of 0.15 micron can be sufficient to provide efficient removal of "killer" particles in the sub 0.1 micron range which

heretofore could not be removed satisfactorily by any known wet cleaning method.

The embodiment of Figure 12 includes a thin rectangular quartz glass tank, vessel or receptacle and a plurality of permanently-mounted oxide-coated silicon wafers that serve as positive electrodes on opposite sides of each semiconductor wafer lowered into the vessel. If the vessel is designed to receive 2, 3 or 5 silicon semiconductor wafers (30), then the required number of positive silicon electrodes would, of course, be 3, 4 and 6, respectively. It could be feasible to clean 10 or 20 semiconductor wafers at a time in a tank 5 or 10 times the size of the one shown (which is designed to receive only one such wafer). However, the system illustrated in Figures 13 and 14 would be more appropriate.

In the apparatus of the embodiment of Figure 12, DI water or other liquid is pumped into the bottom of the vessel and allowed to overflow at a weir or exit to an outlet pipe (not shown). The system could be fully automated. A small precision robot would pick up a single semiconductor wafer from a 25-wafer cassette or wafer carrier and insert this one wafer into the liquid bath midway between and parallel to the two outer positive-electrode silicon wafers.

The outer silicon-wafer electrodes of Figure 12 (and also Figures 4, 6, 7 and 8) can be connected in a suitable manner to the positive side of a power supply. They would be carefully and gradually charged to a positive emf of say 2 to 30 volts while the semiconductor wafer being processed is

charged inductively to a comparable negative emf.

It may be preferable to employ silicon wafers as electrodes when they are immersed in the aqueous bath as shown. All of the silicon surfaces of such electrode wafers will be completely oxidized prior to use so that substantial electrolysis will not occur in the bath. In the case where exposed conductor surfaces exist as IC components, the electrode voltages may be controlled at a low enough level to preclude destructive electrolysis.

Figures 13 and 14 illustrate a preferred embodiment of the present invention wherein wet processing operations are carried out while a row of 20 or more aligned, parallel, regularly spaced, vertically-oriented silicon wafers w is supported on a conventional type of wafer carrier or cassette. A suitable type of cassette having parallel slotted vertical side walls to hold a row of rotatable wafers is shown and described in U.S. Patent No. 5,698,040 together with an overflow tank and associated equipment for circulating a cleaning liquid.

As shown, an array W of 25 aligned vertical wafers w is supported and held in position on a wafer carrier or holder H comprising a rigid assembly 50 of quartz glass rods or bars that are integrally connected, as by welding. The assembly includes a bottom pair of slotted circular rods 51, an upper pair of similar slotted rods 52, a series of regularly spaced curved support arms 53 connected between the rods 51 and 52 at opposite ends of the holder H, and a pair of horizontal connecting rods or bars 54 at opposite sides of the holder adjacent to the end wafers of the array W.

A shorter horizontal connecting rod or bar 55 extends between each pair of rods 51, and a pair of inclined rods or bars 56 are connected to the rods 52 and to a short circular lifting member 57 located near the end wafers of array W and the common horizontal axis of the 25 wafers. A small diameter stud portion 58 or similar means projecting outwardly from member 57 can be engaged by the lift hook of a robot to support the holder H and the wafer array W as they are raised or lowered.

The crude wafer holder H is not conventional and is shown for convenience of illustration, it being understood that additional means, such as the slotted vertical wall means of Patent No. 5,698,040 or the slotted member 9 of Figure 2, can be employed to help locate the wafers and hold them in the desired vertical positions or allow them to rotate, if desired.

In Figure 13, portions of the row of axially aligned wafers are broken away to expose the second wafer w-2 next to the end wafer w-1, the third wafer w-3, and the adjacent fourth wafer w-4. The rectangular vertical side wall 62 of the overflow tank T and the thin flat circular metal sheet forming the electrode or charge plate 100 are also broken away to show the wafer carrier H. The conductive metal sheet can have a thickness of 1 to 3 mm or less.

A substantially rectangular overflow vessel T formed of quartz glass or other suitable non-conductive material is provided to receive the wafer carrier and the 20 or more

silicon wafers of the array W. The wafers may be standard 200 mm or 300 mm wafers. The vessel comprises a thin-wall tank 60 in the form of a box (which could be modified, if desired, to serve as a cassette) having a flat horizontal bottom wall 61, parallel flat vertical side walls 62, and similar vertical end walls 63. The top edge 64 of the tank 60 is higher than the top portions of the wafers so that the array can be completely submerged in the DI water or cleaning liquid filling the tank.

A pair of horizontal quartz glass feed tubes 65 are welded to or attached to the end walls 63 near the bottom of the tank and are aligned with narrow horizontal slots 66 in the end walls 63 to facilitate rapid flow of liquid from the tube 65 to the interior of the tank. Each end wall can have a single slot 66 with a width of 1 to 2 mm and a length of about 150 to 170 mm or more or a plurality of slots with a comparable total length, such as 150 mm or more.

During normal wet cleaning operations, water or other liquid is fed to the inlet 68 of each to be 65 by a pump P or other suitable feed means. The liquid fills the tank 60 and continually overflows at the top edge 64.

Megasonic transducer means may be provided to direct sonic wave energy upwardly to assist in removal of the contaminant particles from the wafer surfaces. As shown such means includes 12 transducers m fitting together side-by-side and bonded to the bottom wall 61 of the tank as shown in Figure 13. Each transducer m can have a width of one inch and extend parallel to the rods 51 and 52 a distance of 6 or 7

inches, preferably corresponding to the width of the wafer array W (e.g., about 150 mm).

A flat circular electrode or charge plate 100 with a diameter about the same as or somewhat smaller than the diameter of the wafers is mounted at the outside face of each tank side wall 62 usually within 20 mm of the end wafer w. The plate is connected to a suitable electric power source by electric lines 101 or 102 (e.g., as in Figure 10). The electrode can be formed from a sheet of aluminum foil, stainless steel or silicon metal and is charged by applying a positive or negative voltage, such as 2 to 40 volts, sufficient to induce an effective charge at the outer surface of each and every wafer in the array W. The voltage at lines 101 and 102 is controlled and periodically reversed so that a positive charge is provided in the plate 100 at the front side of tank 60 whenever a negative charge is provided in the plate 100 at the rear side and vice versa.

In this system the front faces of the silicon wafers containing the microcircuits are charged by induction and will repel contaminant particles while negatively charged. The charge on the rear face of each wafer in the array W will be positive and may attract negatively charged particles during the time the front face of that wafer is negatively charged (i.e., by induction).

When a DC power source is provided, suitable switch means can be used to reverse polarity at suitable intervals (e.g., 1 to 10 reversals per second). The reversals from positive to negative should be controlled so that the front faces of the

wafers with the microcircuits are negatively charged at least half and preferably most of the time (e.g., 60 to 90 percent of the time) to assure adequate particle removal. An important advantage of voltage reversal is the ability to clean both the front and rear faces of each wafer and to limit the number of particles deposited on the rear faces. The invention also contemplates charging of the wafers during cleaning by means of a conventional type of alternating current source (perhaps 20 to 30 cycles per second or more).

In the manufacture of microelectronic devices or the like by the 362-step fabrication process of the aforesaid SEMATECH publication, pages B-3 to B-14, contamination by sub 0.1-micron "killer" particles can be minimized by applying to each process wafer a predetermined limited voltage, such as 2 to 60 volts, during the various wet cleaning or processing operations while the wafer is within the glass receptacle (10) of Figures 1 and 2. For example, the desired negative or positive electric charge can be applied to the wafer (w) during each of the necessary wet processing operations including the RCA-type wet cleans, such as steps 2, 5, 23, 129 and 154; HF cleans, such as steps 65, 93 and 133; post CMP cleans, such as steps 175, 212, 248 and 320; and resist strips with H_2SO_4, such as steps 13, 22, 62, 105, 143, and 187.

In carrying out the preferred wafer cleaning process of the present invention as herein described, the front face of the flat semiconductor wafer is negatively charged to a limited voltage, such as 2 to 60 volts, insufficient to create

a substantial risk of harm or damage to any of the delicate microcircuits on that face. The negative charge on the wafer surface at that face is associated with a substantial charge density and an effective field intensity (preferably at least 0.01 volts/mm) sufficient to achieve or assure effective removal of contaminant colloidal-size and sub 0.05 micron particles that are bonded to or adhere to the wafer surface because of van der Waals forces and other bonding forces. A variety of bonds may be involved including covalent, coulombic, ionic, electrostatic, dipole-dipole and hydrogen bonds.

While the negative charge can be obtained by use of an electric circuit that connects the silicon wafer to the negative terminal of a battery or other suitable DC power supply, it is often preferable to obtain the necessary charge by induction as by placing a positively charged conductor or electrode near the wafer as shown in the drawings. If the electrode is spaced 1 to 5 millimeters away from the wafer, an adequate field intensity (e.g., preferably at least 0.01 volts per mm) can be obtained, even with a relatively low voltage, such as 1 to 2 volts.

The repulsive force exerted on a colloidal-size particle bonded to the wafer surface at a certain point when the surface is electrically charged at that point is directly proportional to the field intensity at that point. When such electrical charge is induced by a charged electrode nearby, the field intensity can easily be calculated. It is directly

proportional to the voltage at the electrode, inversely proportional to the dielectric constant of the liquid filling the space between the electrode and the wafer surface, and inversely proportional to the distance between the electrode and said point on the wafer surface.

The dielectric constant, commonly identified as epsilon (ϵ), is more than 70 when the liquid is water and can be reduced to about 50 when chemicals, such as ammonium hydroxide, are added to the water (e.g., as in RCA SC-1).

Assuming that the electrode is a flat metal plate parallel to the front face F of the wafer, spaced 5 millimeters from such face, and having a charge of 3 volts, that the wafer is submersed in an aqueous liquid cleaning solution having a dielectric constant of 50, and that the charge density is substantial, the field intensity at any point on said front face spaced 5 mm from the electrode would be 3 divided by 250 (50x5) or 0.012 volts per mm. Such field intensity at a point on the wafer surface containing a bonded sub 0.1-micron particle or a colloidal-size particle would be adequate and effective to dislodge and remove such a particle in the practice of the present invention.

In the fabrication of advanced microcircuits where the feature size or minimum line width is reduced below 0.15 micron, it is necessary to limit the voltage to avoid damage to the circuitry. However, a substantial voltage, perhaps from 20 to 60 volts or more, may be desirable and tolerable if applied gradually.

If the voltage applied to the wafer surface is relatively low (e.g., in the range of 0.4 volt to 1.5 volts, for example), the distance from the wafer surface to the electrode may have to be less than 3 mm (e.g., in the range of 1 to 2 mm) in order to achieve the desired field intensity (e.g., adequate to assure effective removal of sub 0.1-micron or colloidal-size particles).

The charge density at the wafer surface is preferably maintained substantially uniform and should, of course, be substantial and more than adequate to achieve effective electropurging of the wafer(s).

Reducing the distance from the electrode to the wafer surface results in an increase in the field intensity. Such a reduction is easily accomplished in the embodiment of Figure 8. If the distance is greater than 4 mm because of the need for a glass wall near the wafer surface, it might be desirable to provide a silicon-metal layer or coating on the inner liquid-engaging face of the quartz glass wall (e.g., wall 21 or 22). In this way the distance from the positively-charged metal layer (electrode) to the wafer surface can be reduced to 1 or 2 mm. It will be understood that the spacing between the positive electrode and the wafer surface can likewise be reduced to a few millimeters in other embodiments of the invention to increase the field intensity.

In carrying out the electropurge process of the present invention, it is necessary to provide the surface of the wafer with the desired charge and an effective field intensity. It

will be readily apparent to those skilled in the art from the present specification and the schematic drawings how much charge can be provided and what electrical means could be employed for that purpose. It will be understood that such details or specifics are not needed for an understanding of the invention, that substantial portions of the complete electrical system that might be desired are not and need not be described herein (e.g., switch means to reverse voltage from positive to negative).

Zeta potential is important and the simplest potential of the colloid system to measure. By applying an electric field across a region of the liquid and measuring the resulting drift velocity of the colloid, the colloid mobility and potential (the zeta potential) can be determined.

Zeta potential generally depends on the ionic concentration of the liquid in which the surface is immersed, although the exact interaction is surface and ion specific. In aqueous systems, the zeta potential varies with pH as shown, for example, in Figure 11 on Page 173 of Kern's 1993 handbook. Increasing the concentration of OH makes the zeta potential more negative, and vice vera.

Zeta Potential and Particle Deposition

While Figure 10, page 171 of Kern, illustrates the potential and charge distribution surrounding a spherical particle, the same description applies to a silicon wafer surface immersed in a liquid. It too is typically charged by the simple act of bath immersion. As indicated in the Kern

handbook, when the zeta potential of the particle and the wafer are both negative, a repulsive force exists that creates a barrier to particle diffusion to the wafer surface.

As explained in the Kern handbook, a negatively charged colloidal particle is repelled from a negatively charged wafer surface by the charges absorbed on the surfaces of each. If these repulsive forces dominate the interaction between the colloid particles and the surface, colloid deposition will not occur. This interaction is called electrostatic double layer repulsion (EDR).

Figure 14 on page 175 of Kern's handbook shows that colloid deposition on a hydrophilic wafer surface exhibits a dependence on pH very similar to zeta potential. According to Kern, at the pH of deionized water, silicon wafers and silicon particles exhibit negative zeta potentials, and EDR effectively resists the deposition of the particles on the charged wafer surface. However, negative zeta-potential particles can deposit on the negative wafers. For example, it is known that such particles can deposit on the wafer from the water film that adheres to the wafer as it is withdrawn from the bath. For hydrophobic wafers, those prepared with an HF-last chemical clean, no adhering film remains during wafer withdrawal.

Because the deposit of particles on the wafer from the water film can be a significant problem, it is desirable to treat each wafer with isopropyl alcohol or other suitable alcohol or nonpolar organic compound (e.g., ethyl alcohol, 1-

methoxy-2-propanol or di-acetone alcohol before the wafer is dried (e.g., see U.S. Patent No. 4,911,761).

According to Kern's 1993 handbook, the effectiveness of EDR as a mechanism for shielding hydrophilic wafers and retarding colloid deposition becomes marginal if that zeta potential of the colloid is about -10 millivolts (Kern page 178). In other words, for EDR to retard colloid deposition (e.g., deposition of contaminant particles), the voltage applied to the charged wafer should be at least -10 millivolts or -0.01 volt. A negative voltage of only 0.05 volt could possibly be useful in the practice of the present invention.

It may often be desirable to provide a small positive charge at the wafer surface (e.g., by applying 2 to 60 volts) during the acid cleaning step (e.g., when using hydrochloric or hydrofluoric acid as in DHF (dilute HF), HPM or an RCA-2-type wet clean). A megasonic transducer can be provided to supply sonic energy to assist in the electropurge cleaning of negatively charged wafers. The megasonic assist can also be employed when the wafer is positively charged as described above. The use of megasonic transducers during RCA SC-1 and SC-2 cleans is standard practice today to assist in removing sub-micron particles and is desirable but not necessary when employing the electropurge process of the present invention.

It will be understood that the wet cleaning operations described above using a positive or negative charge on the wafer (or reversing the charge periodically as in the embodiment of Figure 13 and 14) can be carried out using a

single-wafer receptacle, such as one of the general type shown in the drawings hereof, made of a suitable material, such as quartz glass or Teflon. The electric charge applied to the wafer surface being cleaned would be such as to provide an effective field intensity (e.g., preferably at least 0.01 volts/mm and more preferably at least 0.02 volts/mm).

As indicated on page 125 of the aforesaid Kern handbook, typical RCA clean sequences include use of sulfuric acid (SPM) and hydrofluoric acid before the SC-1 and SC-2 cleans. Original RCA standard cleans employed substantial amounts of ammonium hydroxide and hydrochloric acid in the SC-1 and SC-2 recipes. A typical recipe was 29%NH_4OH:30%H_2O_2:DI water (1:1:5 by volume) or 37%HCl:30%H_2O_2:DI water (1:1:5). More dilute RCA-type cleaning solutions can be used.

It will be understood that the electropurge wafer cleaning process of this invention is preferably carried out using conventional cleaning liquids or conventional RCA-type cleaning systems and that megasonic transducer means are desirable (e.g., particularly when cleaning the wafers with an ammoniacal hydrogen peroxide solution, such as SC-1) to set up high pressure waves in the cleaning solution. The transducers can be made of a suitable piezoelectric material, such as lead zirconate titanate or other commonly used material, and perform well at frequencies of 850 to 900 kHz, for example.

The use of megasonic transducers to improve the conventional RCA-type wet processing operations is described by Werner Kern in an article at pages 81 to 105 of the March

1985 issue (Volume 46, Number 1) of RCA Review, a well-known technical journal that was published quarterly by RCA Laboratories, Princeton, New Jersey. The transducers made it possible to use lower temperatures, such as 40°C to 50°C, during SC-1 cleaning instead of the usual temperatures of 70° to 75°C. The megasonic RCA-type cleaning methods described in this 1985 article can, of course, be employed in the practice of my invention using a single-wafer cleaning system of the type disclosed in connection with Figures 1 to 7 or a batch-type cleaning system as disclosed in connection with Figures 13 and 14.

Excellent results can, for example, be obtained with a process and apparatus of the type described in connection with Figures 13 and 14 using standard 5-tank or 7-tank wet benches of the type previously described herein with the standard or commonly used cleaning sequences. A typical 5-tank wet bench can start with an HF strip and DI water rinse followed by SC-1, DI rinse, SC-2 and DI rinse. A 7-tank wet bench used during the practice of this invention (e.g., to clean the 25-wafer array W) could include a final HF bath followed by another DI rinse for a few minutes before the final drying operations.

For example, when using a tank comparable to the tank 60 of Figures 13 and 14 and provided with electrode means, such as the flat electrodes 100, to charge the wafers, the tank could be filled with an RCA SC-1 solution with a high pH of at least about 10 or higher when using the usual 5:1 volume ratio of DI water and ammoniom hydroxide. If the cleaning process

is carried out with the assistance of megasonic transducers m, the temperature of the SC-1 solution could be in the range of 45° to 60°C and the total time in the tank could be about 8 to about 10 minutes. If the megasonic assist is omitted, a higher temperature, such as 65° to 70°C could be advantageous to limit the time to 10 minutes or less.

As the feature size or line width of advanced microchips is reduced below 0.15 micron, the concentration of the wet cleaning solutions can be very important. It becomes important to obtain a clean and smooth or atomically flat silica wafer surface (e.g., with surface roughness values preferably under 2 Angstroms). In order to avoid excessive etching and unacceptable surface roughness, dilution of the RCA-type cleaning solutions may be desirable.

The progressive reduction of MOS transistor dimensions will soon require ultrathin gate oxides less than 30 Angstroms thick and low rms interface roughness (e.g., below 2 Angstroms). In order to minimize interfacial microroughness for 15- to 30- Angstrom gate oxides, the wet cleaning or wet etching solutions should be diluted with substantial amounts of DI water. For example, a solution of 49%HF:98%H_2SO_4:H_2O (1:0.5:30) has been found suitable for wet chemical etching of the sacrificial SiO_2 layer. In order to reduce the objectionable surface roughening effect of SC-1 solutions, a dilute solution can be used, such as NH_4OH:H_2O_2:H_2O (1:8:64).

When employing a dilute or ultra-dilute RCA SC-2 clean recipe for wet cleaning (e.g., after an SC-1 clean), it is not

necessary to employ hydrogen peroxide. The dilute or ultra-dilute RCA clean can employ a 100:1 or 1000:1 dilution of 37%HCl in water at 45°C, for example. Metal removal efficiency of this solution is very high with or without the assistance of megasonic energy, particularly when the dilute solution is employed in the electropurge process of this invention (e.g., with a wafer charge of 2 to 60 volts and a field intensity of at least 0.02 volts/mm).

In the practice of the present invention electropurge cleaning with limited wafer charges, such as 2 to 60 volts, can be effective with the dilute RCA and ultra-dilute RCA (SC-1 and SC-2) cleans with or without the assistance of megasonic energy.

The need for ultrathin gate oxides to improve MOS device performance imposes stringent requirements on the silicon/gate oxide interface roughness to satisfy yield criteria and provide device reliability. Interface roughness not only degrades device performance by reducing the channel mobility, but may also affect reliability and yield by introducing asperities which act as electrical punctures. Even if the oxide is conformal, an asperity is an electric weak point due to the field lines associated with that topography. Therefore, it is important to consider the various contributions to roughness during device fabrication and employ methods which tend to minimize problems, especially when using ultrathin gate oxides with a thickness in the range of 15 to 30 Angstroms.

Advanced microchips are becoming more delicate and increasingly vulnerable as the feature sizes and line widths are progressively reduced. At the same time the industry performance standards for microelectronic devices are increasing to satisfy the need for better and more reliable devices. It is becoming more difficult to obtain satisfactory yields of advanced microchips with the quality, reliability and longevity meeting those high standards and the demands of consumers.

As the feature size is reduced, there is an increase in the number or frequency of imperfections, defects and potential problems areas, such as the electric weak points referred to above. In order to meet the reliability and yield requirements and avoid known and unknown hazards, there is reason to disapprove questionable or risky procedures which might be unsafe or detrimental.

For these and other reasons, the electric charge applied to the silicon wafers in the practice of this invention should be limited and may be relatively small (e.g., from 1 to 60 volts). Excessive voltage should be avoided to minimize the risk of harm or damage to the delicate or sensitive microcircuits. A voltage of 100 volts or more is usually unnecessary or disadvantageous and might be imprudent for the more highly advanced microchips because of the potential detrimental, degrading or undermining affects on the more vulnerable or sensitive portions of the delicate microcircuits.

In order to help in the removal of sub-micron particles from the wafer surface, the surface should be charged with an effective negative voltage (e.g., preferably at least about one volt) to provide an effective field intensity (e.g., preferably at least about 0.01 volts/mm) at said surface. Such field intensity can be at least 0.02 volts/mm and sufficient to cause or permit effective removal of sub 0.1-micron particles but insufficient to create a substantial risk of adverse affects or harm to the more vulnerable portions of the microcircuits.

The use of low voltages in the range of 2 to 60 volts is prudent and often preferred, particularly during BEOL wet processing where there are more problems and difficulties and the risk of harm or loss due to excessive voltage is much greater. Such low voltages provide a higher degree of safety and can be remarkably effective in dislodging, removing and repelling sub 0.05-micron and colloidal-size contaminant particles which cause "killer defects" in advanced microchips, such as those having feature sizes of from 0.10 to 0.15 micron.

The present invention is a godsend to the semiconductor industry, which heretofore had no practical and effective way to eliminate "killer" particles of sub 0.1-micron size or to reach target defect-density goals, such as those set forth in TABLE 1 on page 5 hereof. That table describes the SEMATECH yield model and equipment defect goals based on the model for pilot line and high-volume manufacturing. The table is taken

from a printed SEMATECH publication dated July 31, 1994 and entitled "Contamination-Free Manufacturing Handbook" (Identified as 94062428A-TR). That publication provides information that covers most, if not all, aspects of contamination control methodology for semiconductor equipment and processes.

That publication points out that random particles represent a substantial and significant portion of yield loss, especially in the back end (BEOL) of a process, and that any systematic defect-reduction program needs to establish defect goals and then strive to achieve them. The most widely used approach for determining defect goals has been to take particle per wafer pass (PWP) numbers for next generation design rules. However, as pointed out in the SEMATECH publication, this approach is inadequate because it does not indicate or consider which particle goals are the first-order drivers of yield improvement.

The publication includes a footnote below TABLE 1 that reads as follows:

> "Since killer defect density is derived from yield and different process levels having varying sensitivities, defect size is not precise (± 100%). However, this size is often used for PWP goals as if it were precise and therefore causes problems in setting realistic detection and reduction goals."

The more recent National Technology Roadmap for Semiconductors as published by Semiconductor Industry

Association (SIA) was reproduced in SEMICONDUCTOR INTERNATIONAL (January 1998), pg. 40 (and Table 1) of which is incorporated herein by reference for all purposes. The SIA Roadmap estimates process-specific defect densities for future 0.25-micron (um) to 0.05-micron devices (up to the year 2012) and proposes defect targets for future generations of devices based on 60% yield for initial production.

Reaching such defect goals will be less difficult because of the many advantages provided by the present invention. One major advantage, exemplified by the wafer cleaning systems described previously in connection with Figures 1 to 7 and Figure 8, is the unique ability to clean both the front and back faces of each silicon wafer simultaneously (e.g., when the wafer is located between two positive electrodes to induce a negative charge in both faces).

As previously disclosed in connection with a modification of Figure 8, that major advantage can also be achieved (e.g., when treating 10 to 20 or more silicon wafers at one time as in Figure 14) by providing a suitable positively-charged metal electrode plate or disk between each adjacent pair of wafers. For example, when employing a wafer carrier (H) to support a single row of 25 regularly-spaced vertical metal disks or plates (like the array W), 12 of those disks could be silicon wafers with microcircuits being formed on the front faces and the other 13 could be positively-charged electrodes formed of a suitable conductive metal, such as stainless steel, aluminum

or silicon (i.e., a bare unpatterned silicon wafer functioning as the positive electrode).

The electrical apparatus used to charge the positive electrodes to the desired voltage in the embodiments just described can, of course, include a conventional DC power source with suitable switch means or the like to provide for reversals of polarity, if desired. An AC power source can be used instead to provide periodic voltage reversals (e.g., 10 to 30 or more cycles per second). The AC voltage curve or wave profile can, for example, be controlled in such manner that a positive voltage is provided during 80 to 90 percent of each cycle and a negative voltage is provided during the other 10 to 20 percent.

Such a special AC electrical system could be particularly advantageous in the specific embodiment of Figures 13 and 14 (where the front and back faces are oppositely charged) to reduce or minimize the redeposit of particles on the wafer faces during the brief time that they are positively charged, thereby reducing the need for megasonic assistance. The 12 transducers m at the bottom wall could then be omitted, if desired.

It will be understood that the above description is by way of illustration rather than limitation and that variations and modifications of the specific processes and devices disclosed herein may be made without departing from the spirit of the invention.

I claim:

1. In the preparation of semiconductor wafers or microelectronic devices wherein delicate microcircuits are to be formed on the front face of a flat silicon wafer having a diameter of at least 200 mm by more than 200 steps including many layering, patterning and doping operations and at least 30 wet processing steps, the improvement wherein each semiconductor wafer is electrically charged during wet processing to provide an effective field intensity.

2. A process according to claim 1 wherein the field intensity at the wafer surface is sufficient to facilitate removal of sub 0.1 micron particles.

3. A process according to claim 1 wherein a wafer is charged to a voltage of from about 2 to about 60 volts during wet processing operations.

4. A process according to claim 1 wherein a wet processing operation includes chemical mechanical polishing with colloidal-size abrasive particles and subsequent chemical cleaning of each wafer to remove such particles while the wafer is charged to a voltage sufficient to facilitate removal of sub 0.1-micron and colloidal-size particles.

5. A wafer cleaning process according to claim 1 wherein a wet processing operation includes treatment of each wafer with a dilute high-purity acid solution while the wafer surface is electrically charged.

6. A process according to claim 1 wherein the wet processing operation includes treatment of each wafer by a non

polar compound, such as isopropyl alcohol, 1-methoxy-2-propanol or di-acetone alcohol, before drying the wafer.

7. A process according to claim 1 wherein particulate contaminants are removed from at least one face of a wafer by applying a negative voltage of from about 2 to about 60 volts while providing a field intensity of at least about 0.01 volts/mm at the wafer surface.

8. A wet cleaning process wherein a semiconductor wafer is cleaned by thorough rinsing in DI water characterized in that the wafer is charged during rinsing to a voltage of at least 50 volts in such manner that detrimental colloidal-size and submicron killer particles bonded to the front face of the wafer containing the microcircuits are effectively removed.

9. A process for economical wet cleaning of semi-conductor wafers during the fabrication of microelectronic devices wherein a single flat wafer is mounted in a fixed position in a narrow shaped receptacle having flat walls parallel to the front and back faces of the wafer and spaced therefrom a short distance, and wherein a sequence of several wet cleaning operations is performed on said wafer while it is held in the desired position in said receptacle.

10. A process according to claim 9 wherein the semiconductor wafer is subjected to RCA wet cleaning operations, and megasonic energy is directed over the surfaces of said wafer during such operations.

11. A process according to claim 9 wherein an SC-1 cleaning operation is employed using a solution of water,

hydrogen peroxide, and ammonium hydroxide including from about 10 to about 30 percent by weight of an alcohol.

12. A process according to claim 9 wherein at least one face of the semiconductor wafer is charged to a limited but effective voltage, such as 2 to 60 volts, during a wet cleaning operation in said receptacle.

13. A process according to claim 9 wherein a flat electrode with a diameter or width comparable to or larger than that of the semiconductor is provided at the outer face of the glass receptacle to induce the desired electrical charge at the wafer surface during wet cleaning.

14. A process according to claim 3 wherein the front face of one thin plate or wafer containing the delicate microelectronic devices is subjected to a series of wet cleaning steps while that plate is mounted in a fixed position in the internal cavity of a flattened quartz glass receptacle.

15. A process according to claim 1 wherein at least one face of an unpatterned wafer is charged to a voltage of at least 40 volts sufficient to facilitate elimination of detrimental sub 0.05-micron particles.

16. Apparatus of the character described for wet cleaning of semiconductor wafers comprising a shaped receptacle having a cavity for receiving at least one semiconductor wafer, means for admitting a liquid to said cavity, and means for charging said wafer with a limited voltage effective to facilitate removal of sub 0.1-micron particulates.

17. Apparatus according to claim 16 for wet cleaning of wafers during the fabrication of microelectronic devices comprising a shaped receptacle with a narrow cavity of a size to receive a single flat wafer, said receptacle having a flat wall portion parallel to the wafer and spaced from the wafer a distance of from about 1 to about 5 mm to cause uniform flow over the entire face of the wafer.

18. Apparatus according to claim 17 wherein a process wafer is mounted in said cavity and exterior means are provided to induce an electric charge of at least 2 volts at the face of said wafer during wet cleaning.

19. Apparatus according to claim 16 wherein means are provided to support a row of at least 10 or 20 axially aligned silicon wafers with a diameter of from about 200 to 400 millimeters, electrode means are provided at opposite ends of said row for simultaneously charging the delicate front faces of all of the wafers with a negative voltage of at least 2 volts, and means are provided for reversing the voltage periodically to clean the back faces of the wafers.

20. In a process for wet cleaning of flat silicon semiconductor wafers wherein at least one face of each wafer is treated with a high-purity aqueous liquid to remove submicron contaminant particles and thereafter dried, the improvement wherein the particle removal at the liquid-covered face of the wafer is accelerated and intensified by charging that face to a voltage no less than 10 volts effective to purge and eliminate detrimental sub 0.1-micron particles.

21. A process of the character described for fabrication of microelectronic devices on silicon wafers wherein microcircuits are formed on the front face of a wafer by a plurality of layering, patterning, doping and heating operations and the wafer is wetted and repeatedly subjected to cleaning, rinsing and drying operations to remove contaminants, characterized in that said front face of the process wafer is artificially charged during wet processing by applying a negative voltage sufficient to facilitate removal of detrimental sub 0.1 micron contaminant particles bonded to the wafer surface.

22. A process according to claim 21 wherein the front face of the process wafer is subjected to wet CMP polishing with colloidal silica or alumina particles having an average particle size of from 0.01 to 0.03 microns and is thereafter subjected to chemical cleaning and DI rinsing operations while said front face is negatively charged to a voltage sufficient to facilitate effective removal of sub 0.05-micron contaminant particles bonded to the wafer surface.

23. A process for fabrication of microchips having a minimum line width or circuit image size less than 0.15 microns wherein the front face of each wafer is subjected to the wet CMP polishing with colloidal silica or alumina particles and is thereafter subjected to a wet cleaning operation for about 0.5 to about 5 minutes while said front face is negatively charged to a substantial voltage of at least about 2 volts sufficient to remove colloidal or sub 0.05

- micron contaminant particles, the voltage and rate of charge of the wafer surface being controlled during said wet cleaning operation in such manner as to minimize or limit degradation or alteration of the delicate microcircuitry.

24. In a process for forming delicate microcircuits on the front face of a semiconductor wafer wherein the wafer is subjected to a large number of layering, patterning and doping operations and many wet processing steps to remove organic, metallic and particulate contaminants, the improvement in which at least one face of the wafer is provided with a limited electric charge during wet processing steps insufficient to degrade the microcircuits, the charge being sufficient to provide a field intensity at the wafer face effective to facilitate removal of sub 0.1-micron particles bonded at the wafer surface.

25. A process according to claim 24 wherein said field intensity is at least 0.02 volts/mm and sufficient to achieve effective removal of colloidal-size particles.

26. A process according to claim 25 wherein the front face of the wafer is charged to a voltage of from about 1 to about 60 volts.

27. A process according to claim 26 wherein a single silicon wafer with a diameter of at least about 200 mm having a front face with microcircuits having a feature size or line width less than 0.18 micron is wetted and cleaned by charging said front face to a voltage of from about 2 to 40 volts,

thereby causing sub 0.1-micron particles to be dislodged, released and removed.

28. A process according to claim 27 wherein the front face of the wafer is positively charged to a field intensity of at least about 0.02 volts/mm during washing of the wafer in a highly dilute acid solution.

29. In the manufacture of advanced microchips, a process for forming delicate microcircuits on the flat face of a semiconductor wafer in which the wafer is subjected to a large number of layering, patterning and doping operations and many wet cleaning steps with acid and alkaline solutions and pure water to remove intolerable contaminants, characterized in that the wafer face containing said microcircuits is electrically charged to a limited voltage to provide an effective field intensity that promotes removal of sub 0.1 micron particles bonded at the wafer face.

30. A process according to claim 29 wherein said wafer face is negatively charged to a voltage of from about 2 to 60 volts sufficient to achieve effective removal of harmful particles with a particle size of from 0.01 to 0.1 micron.

31. A process according to claim 29 wherein said wafer face is provided with a limited electric charge of at least 10 volts during said wet cleaning steps to minimize particulate contamination.

32. A process according to claim 29 wherein said wafer face is charged to a negative voltage of at least 50 volts during wet cleaning sufficient to dislodge and remove

particles with a particle size of from 1 to 2 microns without the help of megasonic transducers, brush scrubbers or other auxiliary agitating means.

33. A process according to claim 29 wherein a row of at least 10 or 20 axially aligned silicon wafers with a diameter of from about 200 to about 400 mm is supported in a receptacle, the delicate front faces of all of the wafers in said row are charged by induction to a negative voltage of at least about 2 volts to facilitate removal of contaminant particles, and the induced charge on said front faces is periodically reversed to provide the back faces of the wafers with a negative charge that repels contaminant particles during wet cleaning operations in said receptacle.

34. A process according to claim 33 wherein megasonic energy is employed to assist in the removal of the contaminant particles, and the voltage applied to the wafer surfaces is frequently reversed, at least 5 cycles per second.

35. In the manufacture of advanced microchips from flat semiconductor wafers having delicate microcircuits formed on one face, an RCA-type wet cleaning process wherein a single wafer is treated in an aqueous alkaline solution containing hydrogen peroxide and thereafter treated in an acidic solution, rinsed in pure water and dried, the improvement wherein the wafer surface containing said delicate microcircuits is electrically charged during the wet cleaning process to cause effective removal of sub 0.05 micron particles that are strongly bonded to the wafer face.

36. A wafer cleaning process according to claim 35 wherein megasonic energy is employed to assist in the removal of the contaminating particles during the treatment in the alkaline solution and said wafer surface is charged to a negative voltage of from about 2 to 60 volts during the cleaning and rinsing steps.

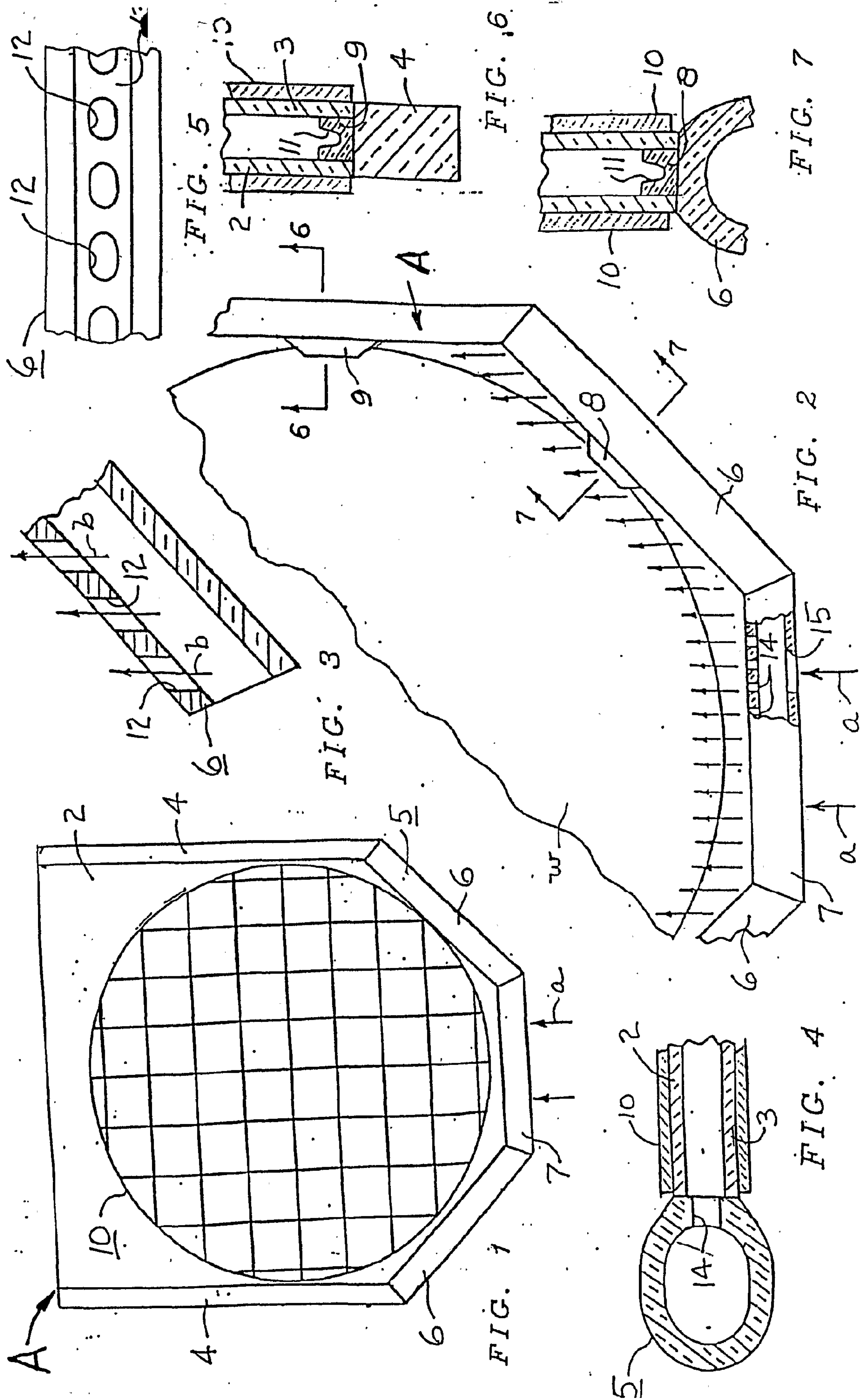
FIG. 1
FIG. 2
FIG. 3
FIG. 4
FIG. 5
FIG. 6
FIG. 7

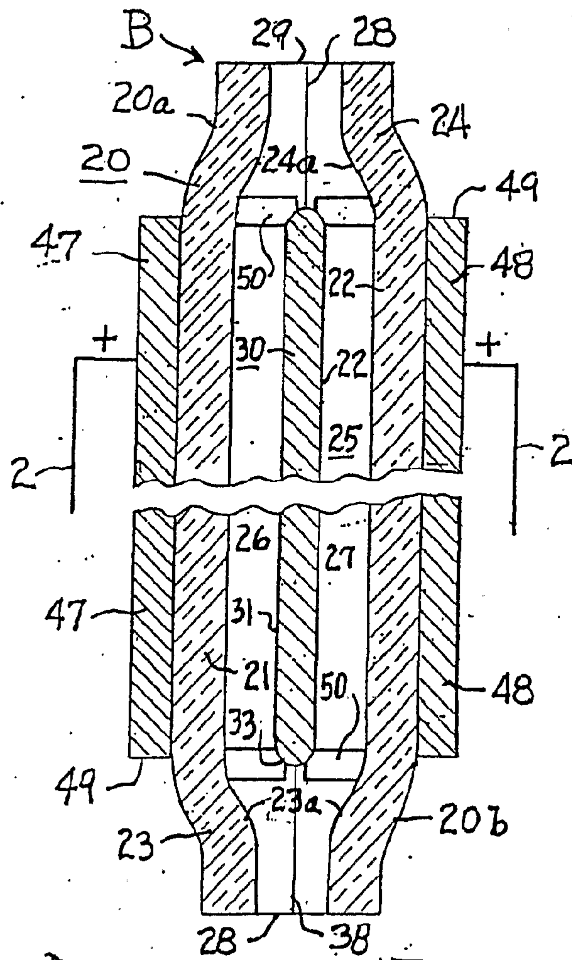

FIG. 8

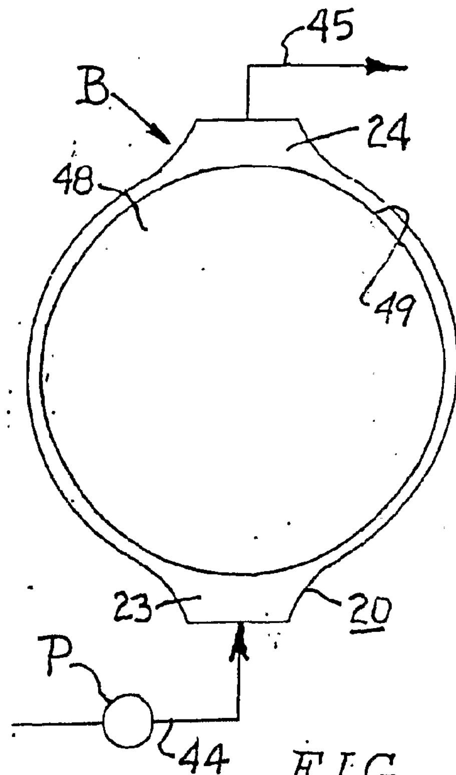

FIG. 9

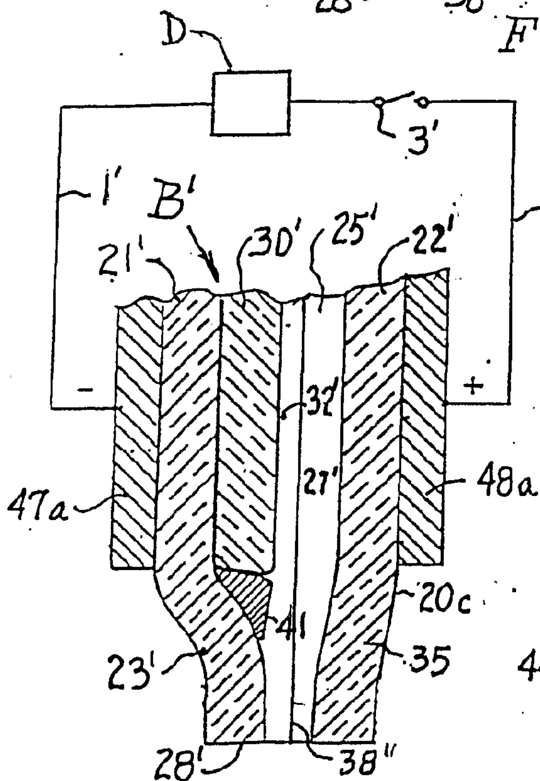

FIG. 10

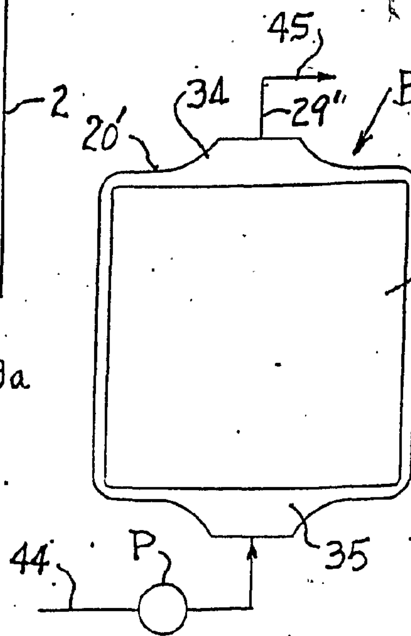

FIG. 11

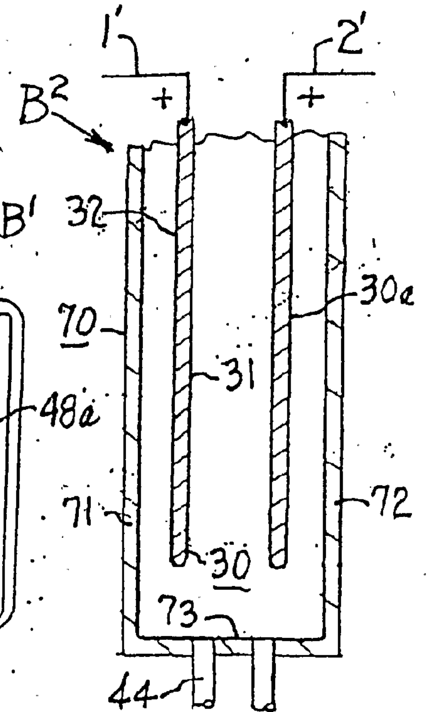

FIG. 12

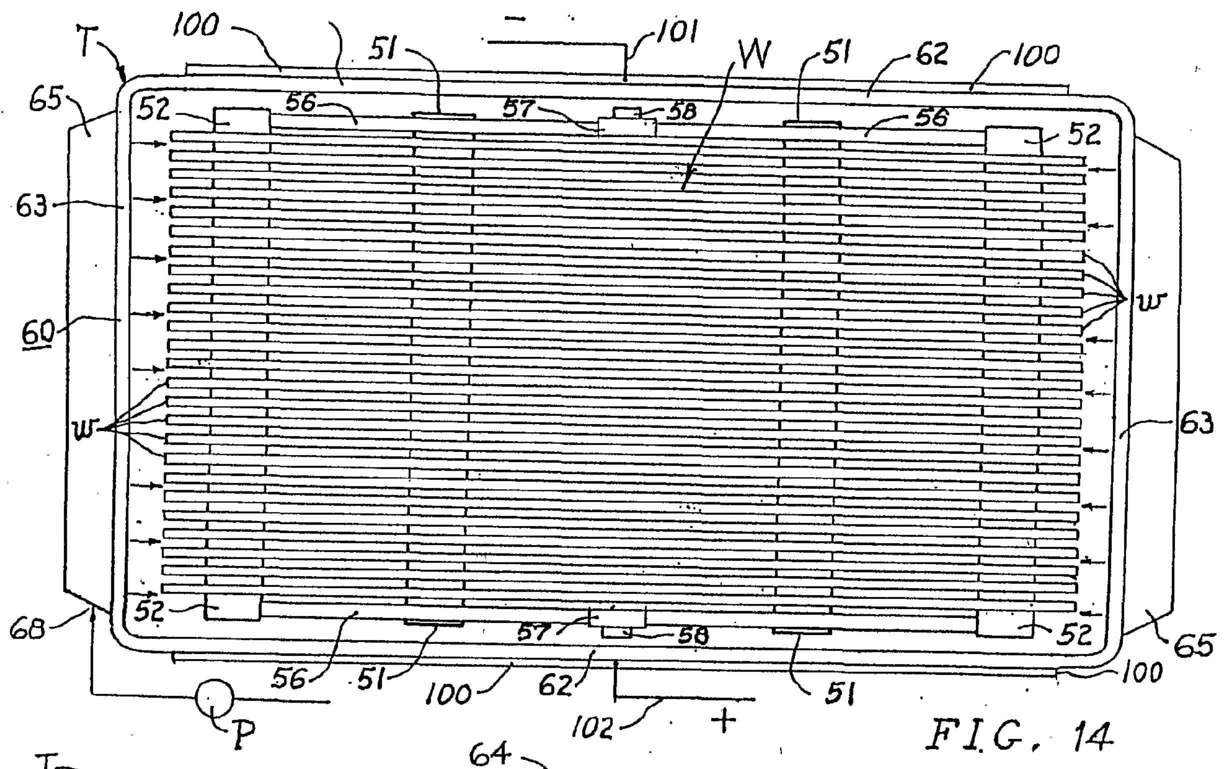

FIG. 14

FIG. 13