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ONLINE: WPI, EPODOC, JAPIO

(54) Abstract Title
Method of fabricating a semiconductor device

(57) A method for fabricating a semiconductor device, including the steps of: forming a contact hole (208, Figure 2c) so as to cause the etching stopper 205 on the substrate 201 to be exposed; removing an exposed etching stopper 205 on the substrate; filling the contact hole 208 to form a contact plug 210; removing a film [209, Figure 3b] that is deposited on the interlayer insulation film 206, so as to expose the contact plug 210; etching the interlayer insulation film 206 and removing the etching stopper 205 on the gate electrode 203; forming an interlayer insulation film 211; etching the interlayer insulation film 211 so as to expose the etching stopper 205 on a diffusion layer [231, Figure 5a] and etching the insulation film 204 of the gate electrode 203, so as to form contact holes [213, Figure 5a] on the diffusion layer 231 and gate electrode 203; removing the etching stopper 205 exposed on the diffusion layer 231; and, filling the contact hole 213, so as to form the contact plugs 215.

Fig. 6

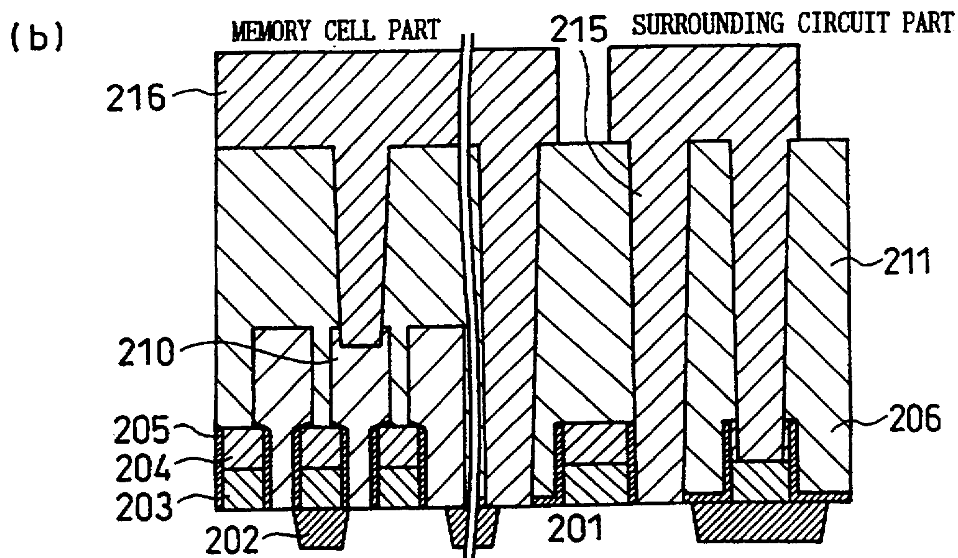

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Fig. 1

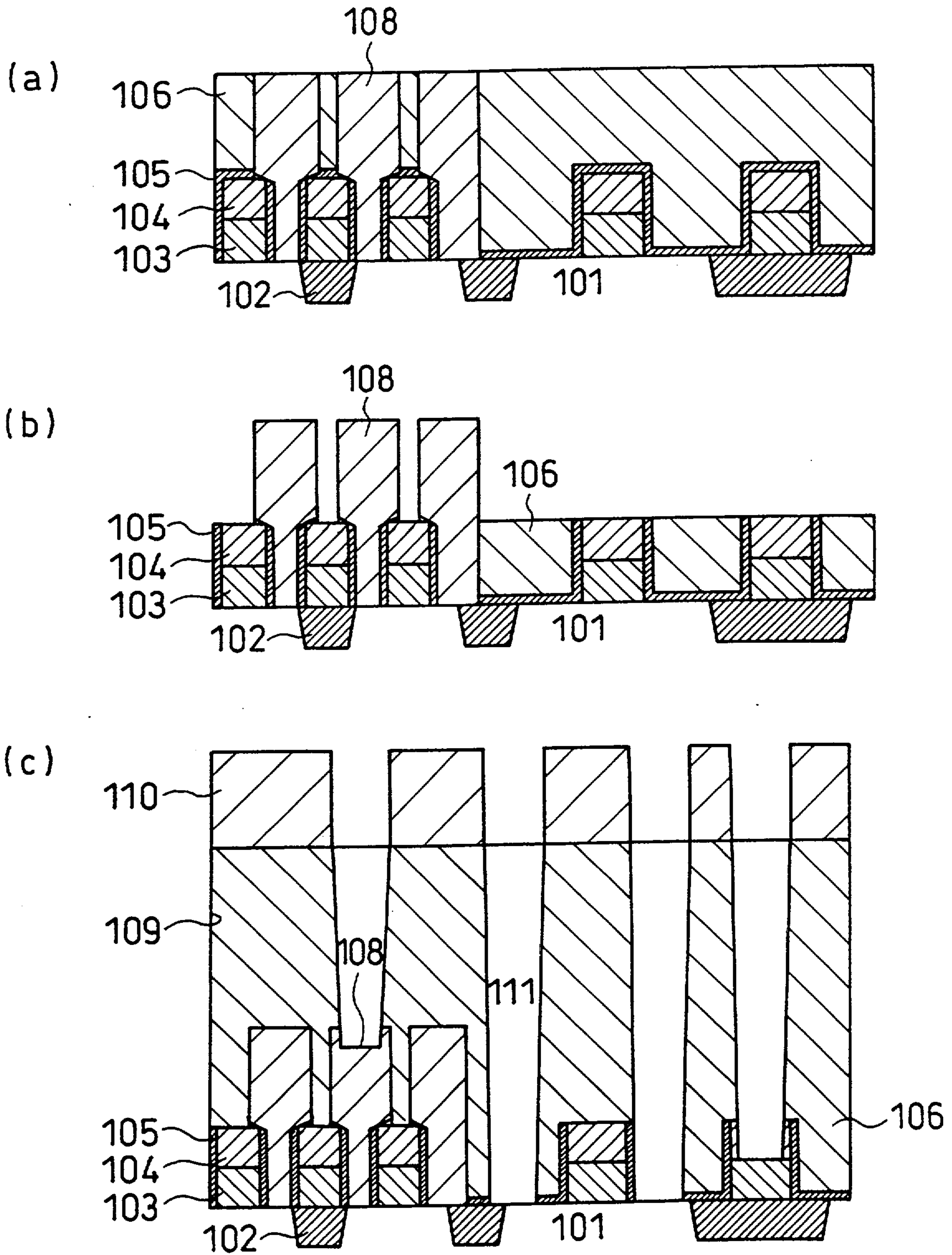


Fig. 2

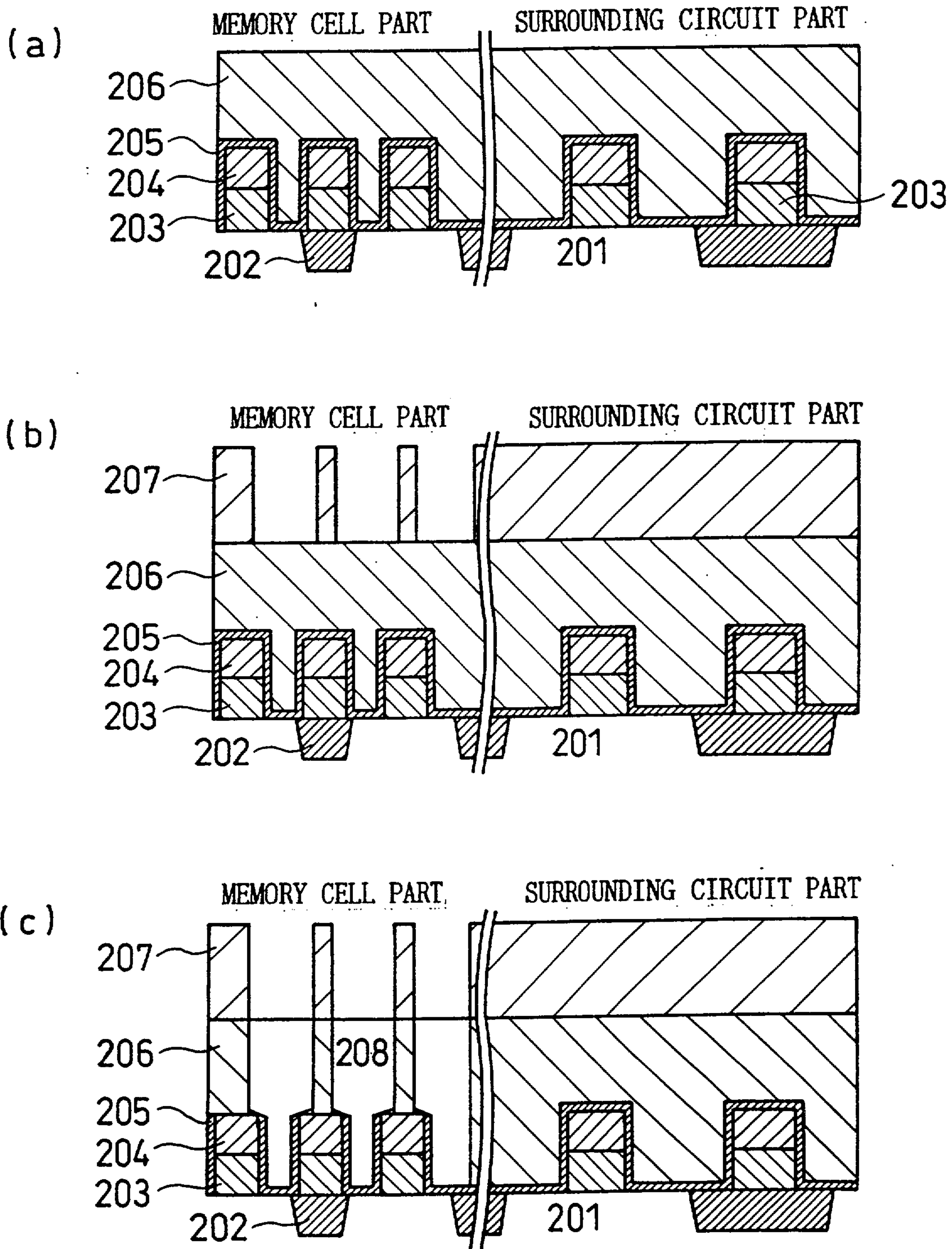


Fig. 3

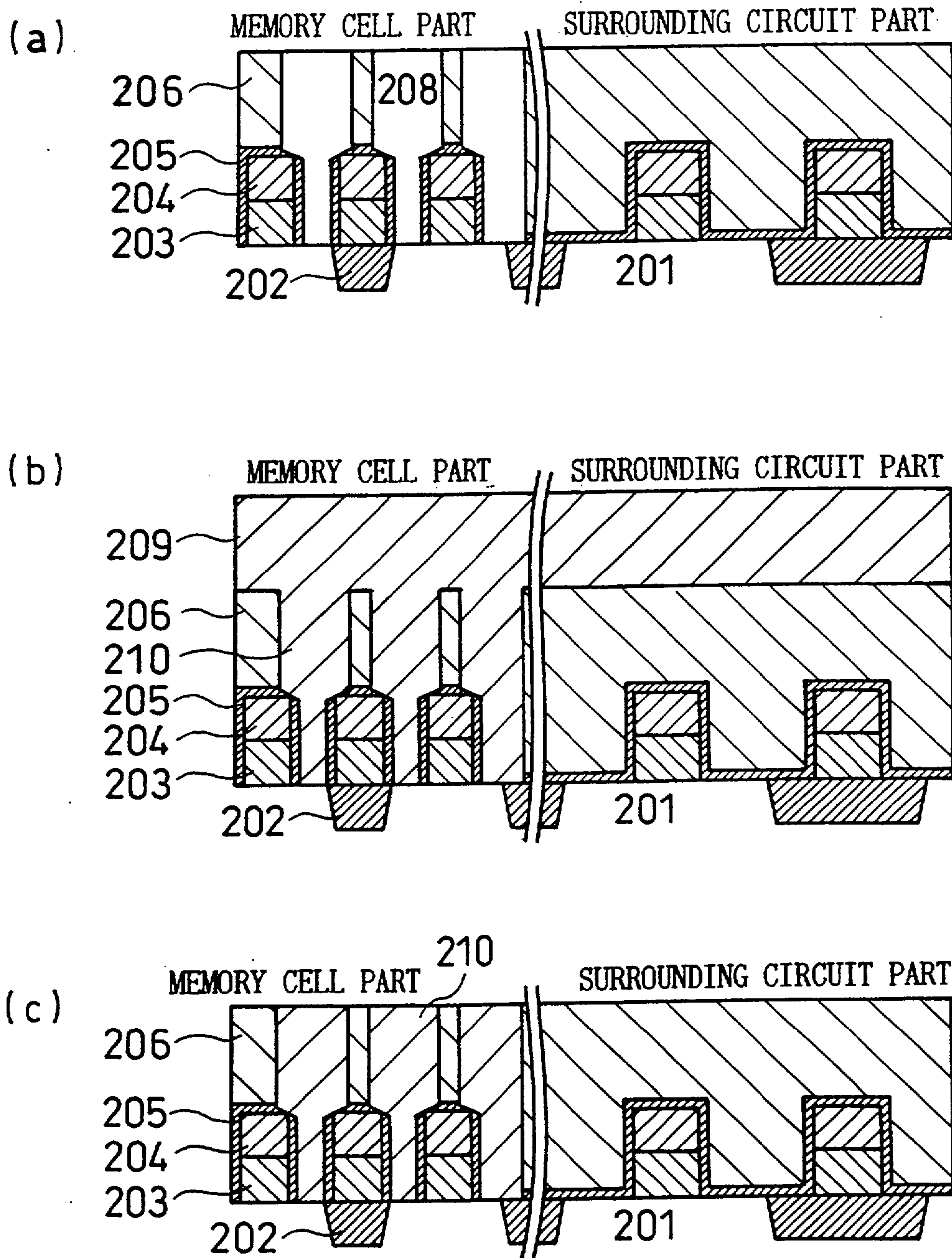
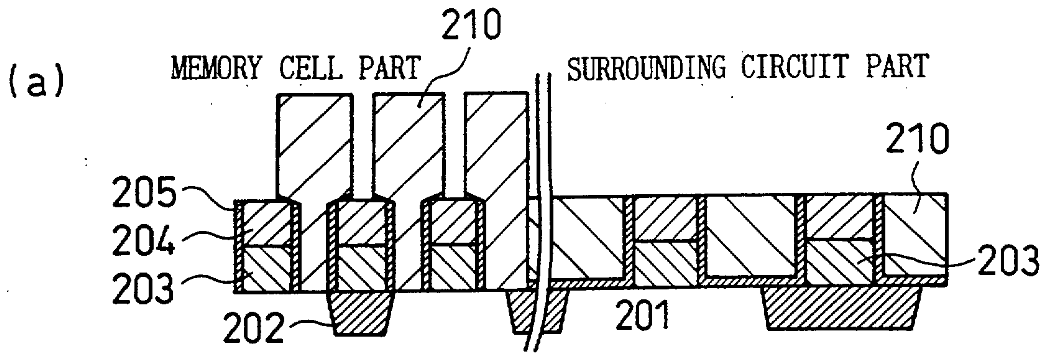


Fig. 4

(a)



(b)

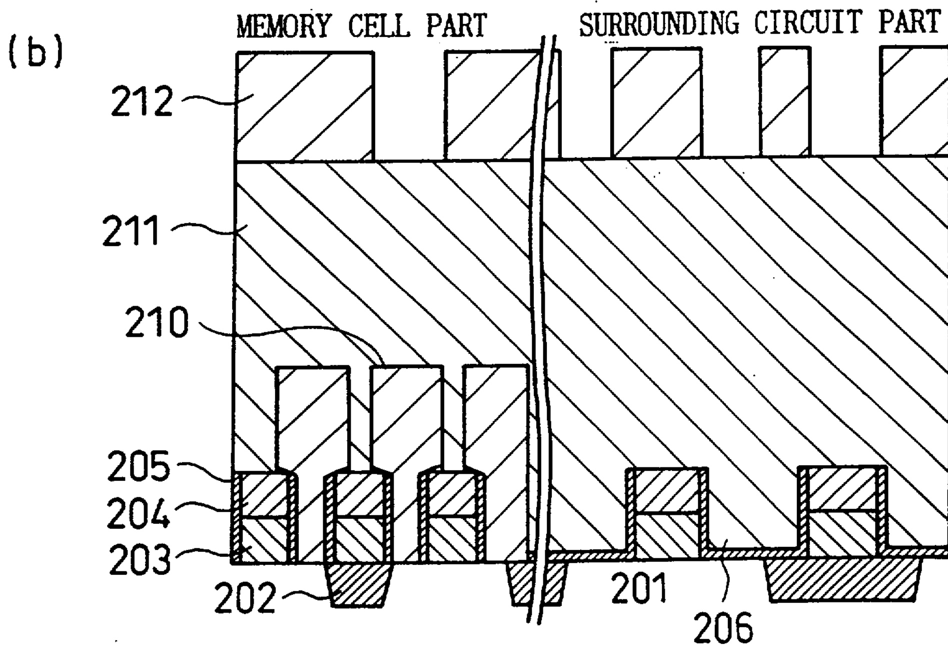
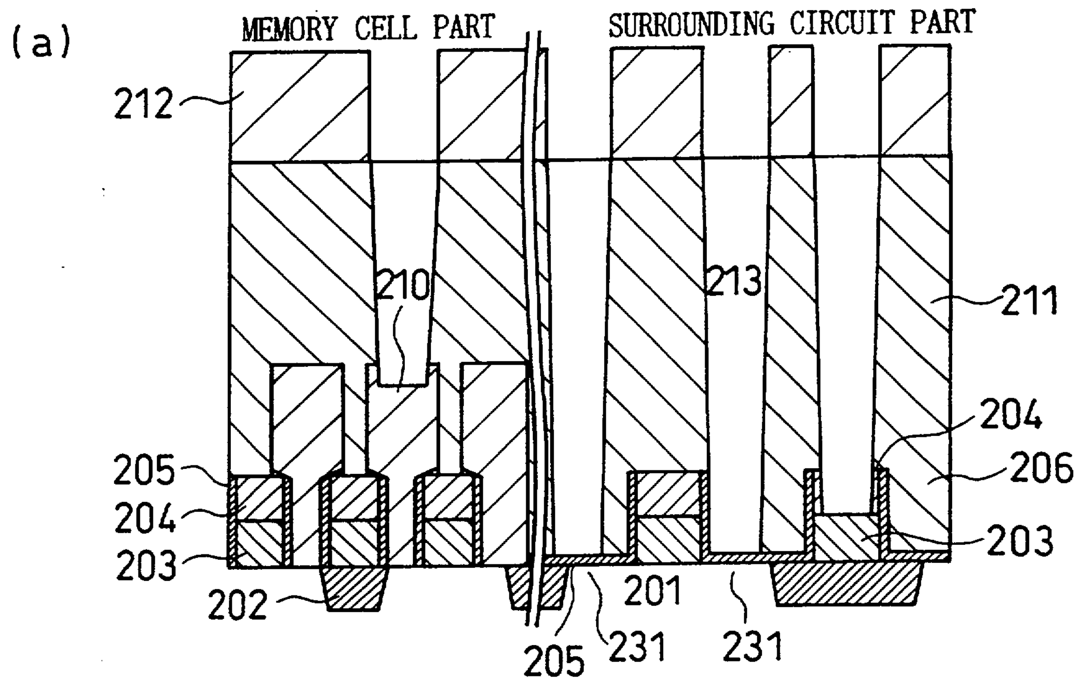


Fig. 5



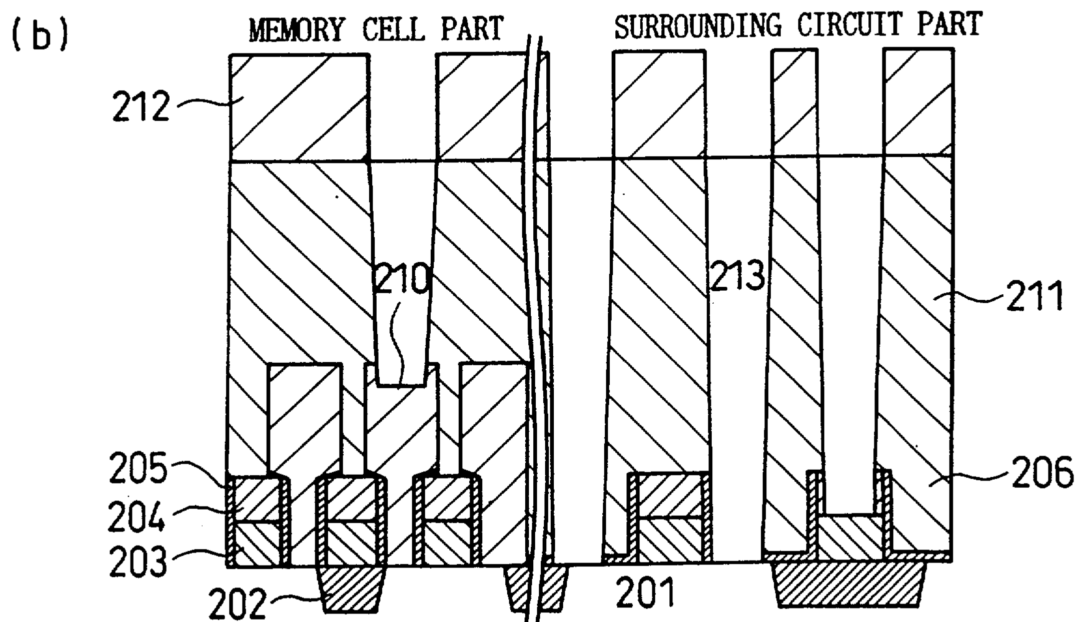
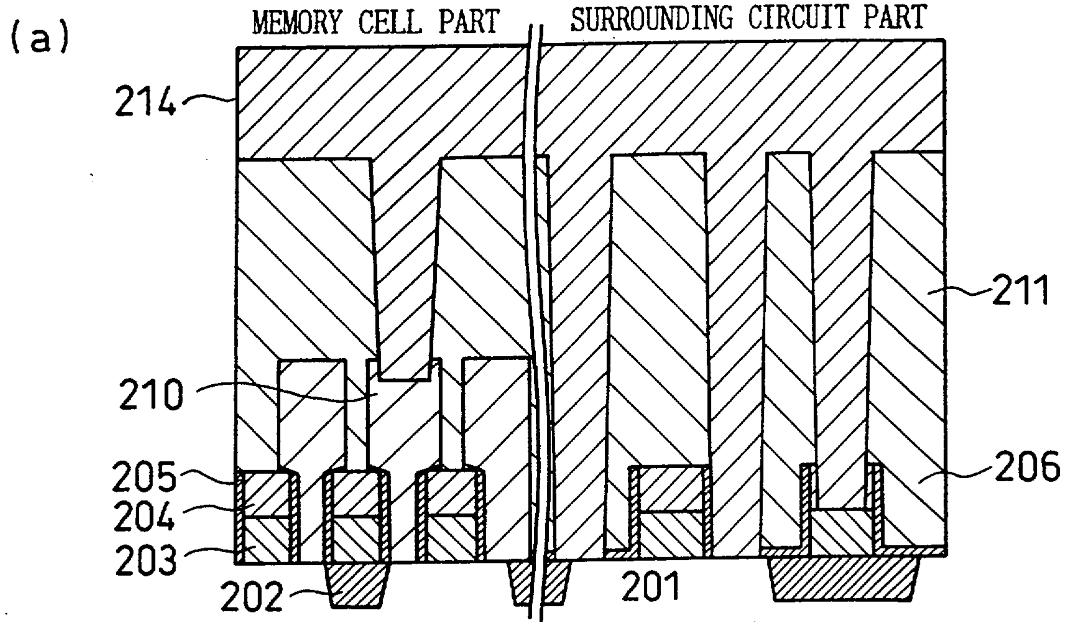


Fig. 6

(a)



(b)

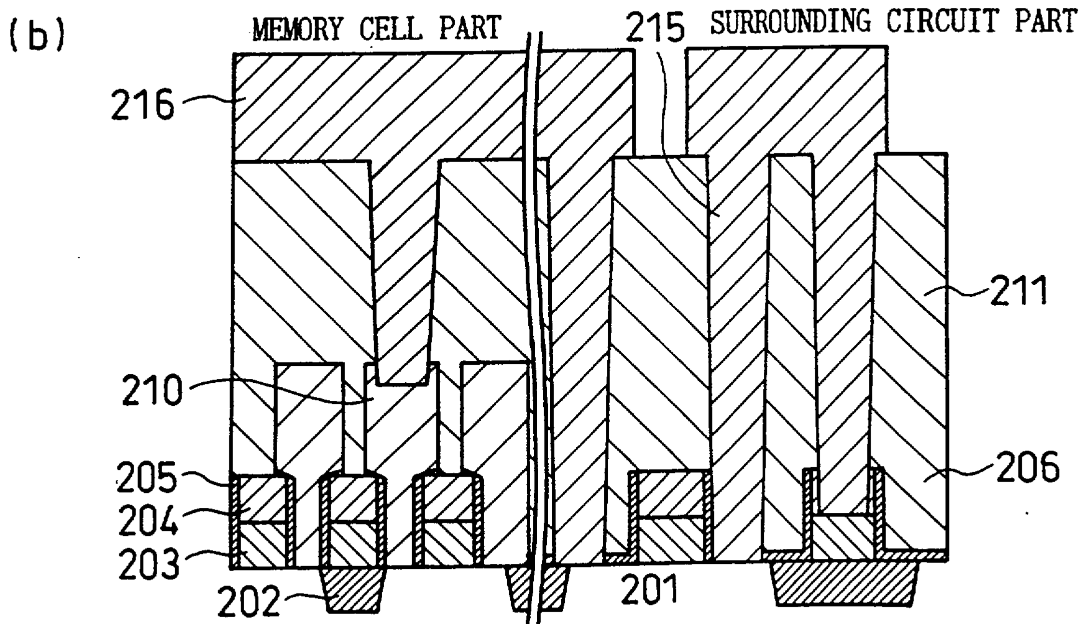


Fig. 7

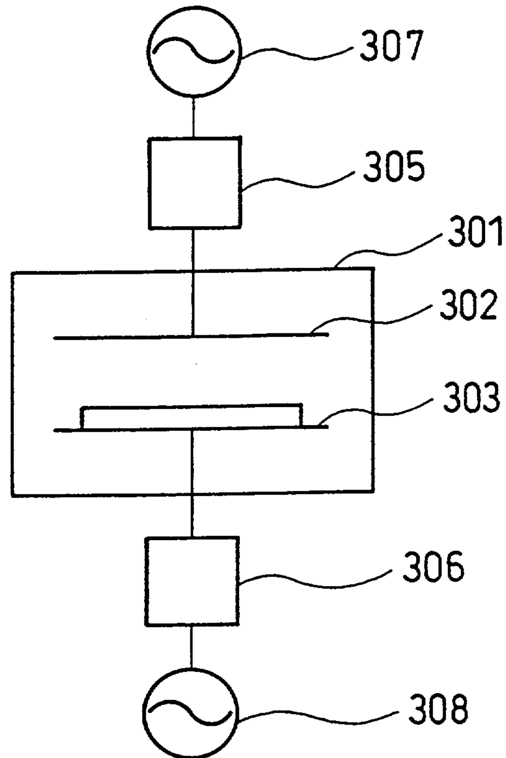
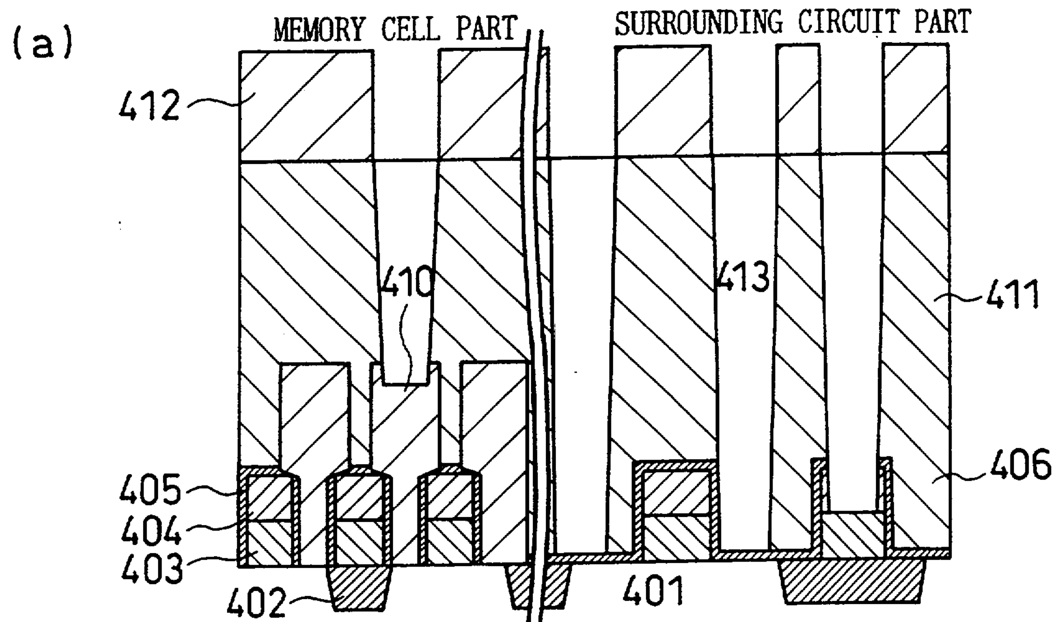


Fig. 8

PRIOR ART

(a)



(b)

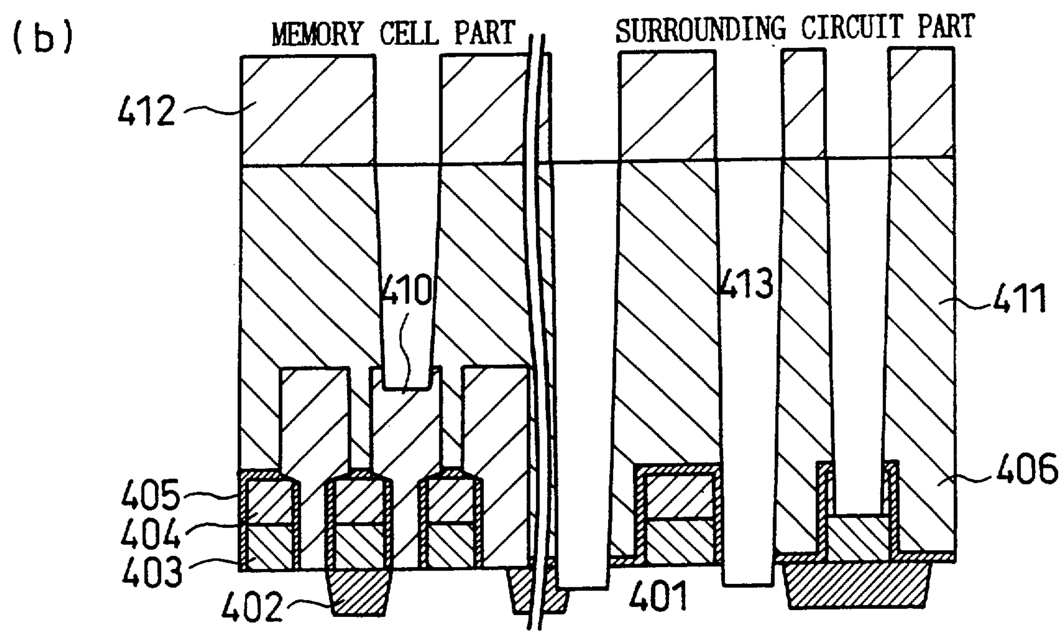
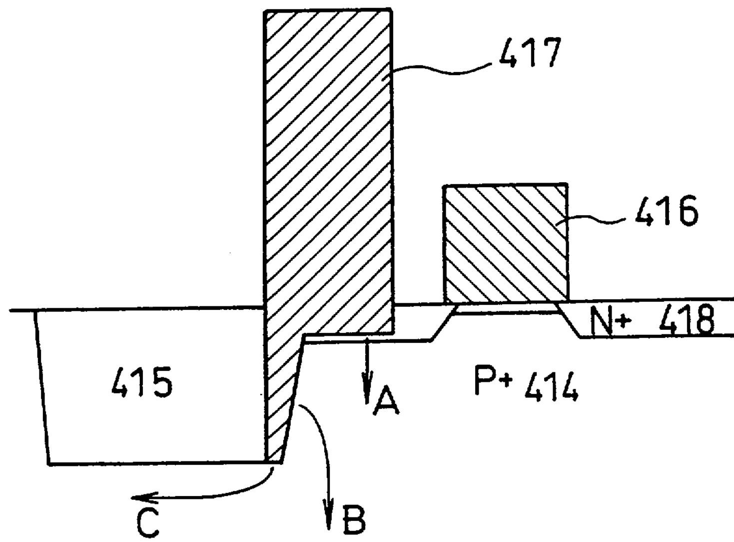


Fig. 9

PRIOR ART



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SPECIFICATION

Method of fabricating a semiconductor device

5 BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a semiconductor device and to a method of fabricating a semiconductor device, and more particularly it relates to a semiconductor device and 10 method of fabricating same which eliminates over-etching and achieves stable transistor characteristics.

2. Background of the Invention

In an interconnect technology making use of self-alignment process to form contacts in a semiconductor device, 15 and particularly a method of forming a self-aligning contact using an etching stopper made of a silicon nitride film, the following problems were encountered in the past.

Fig. 8 shows cross-section views of process diagrams illustrating the application of a general self-aligning 20 contact process to a memory device.

As shown in Fig. 8 (a), a gate electrode 403 and an insulation film 404 made of a silicon nitride film are formed on a silicon substrate 401 and an element separation region 402, and then a silicon nitride film 405 serving as an etching 25 stopper is deposited so as to cover the gate electrode and the silicon substrate. Then after forming a BPSG film 406 as an interlayer insulation film, self-aligning contact etching is done to form a contact plug 410. Then, after forming an interlayer insulation film 411 using a CVD process, a

contact pattern is formed on photoresist 412, this being used as a mask to etch the BPSG film 406.

After the above, as shown in Fig. 8 (b), the silicon nitride film 405 is etched. When doing this, if the usual
5 nitride film etching is done with a fluorocarbon gas such as CF_4, because it is not possible to achieve a selection ratio with respect to the silicon substrate, the silicon substrate 401 is simultaneously etched.

As shown in Fig. 9, which is a simplified drawing of
10 a transistor structure, each transistor on a p-type silicon substrate 414, for example, is separated by a field oxide film 415, and the transistor is formed by a gate electrode 416, an n-type diffusion layer 418 that will serve as a source and drain, and a contact electrode 417, when the n-type
15 diffusion layer made of silicon is over-etched, there is current leakage in the direction A indicated in Fig. 9, the result being that it is not possible to achieve stable transistor characteristics.

While the above applies to the case in which an
20 insulation film 404 over the gate electrode is a silicon nitride film, even in the case in which this insulation film 404 over the gate is a silicon oxide film, for the same reason as described above, the field oxide film 415 is etched, in which case there is current leakage in the direction B or
25 the direction C indicated in Fig. 9, the result being that it is not possible to achieve stable transistor characteristics.

In the Japanese Unexamined Patent Publication (KOKAI) No.H9-205185, there is a method for removing the silicon

nitride film from over the gate beforehand. This method, however, requires an extra lithography process, thereby causing the problem of an increased number of process steps.

Accordingly, in view of the above-noted prior art drawbacks, it is an object of the preferred embodiment of the present invention to provide a novel method for fabricating a semiconductor device, whereby over-etching is prevented without the need to increase the number of lithography steps, and which achieves stable transistor characteristics.

SUMMARY OF THE INVENTION

Generally, the present invention is a method for fabricating a semiconductor device having a contact plug, this method comprising the steps of: a first step of forming a polysilicon film and an insulation film on a semiconductor substrate, and then etching the polysilicon film and the insulation film to a prescribed shape, so as to form a gate electrode, after which an etching stopper is formed on an entire surface of the substrate and an interlayer insulation film is formed over the entire surface thereof; a second step of forming a contact hole that reaches the semiconductor substrate in the interlayer insulation film, so as to cause the etching stopper on the semiconductor substrate to be exposed; a third step of removing an exposed etching stopper on the semiconductor substrate; a fourth step of filling the contact hole to form a contact plug; a fifth step of removing a film that is deposited on the interlayer

insulation film when the contact plug is formed, so as to expose the contact plug; a sixth step of etching the interlayer insulation film and removing the etching stopper on the gate electrode; a seventh step of forming an interlayer
5 insulation film over an entire surface of the substrate; a eighth step of etching the interlayer insulation film so as to expose the etching stopper on a diffusion layer, and etching the insulation film of the gate electrode, so as to form contact holes on the diffusion layer and the gate
10 electrode; a ninth step of removing the etching stopper exposed on the diffusion layer; and a tenth step of filling the contact hole formed by the eighth step and the ninth step, so as to form the contact plugs.

In the sixth step, CH_4 amd CHF_3 gases may be used as an
15 etching gas.

In the sixth step, an etching rate of the interlayer insulation film and the etching stopper preferably is higher than that of the contact plug formed in the fourth step.

In the eighth step, C_4F_8, Ar, CO, and O_2 gases may be
20 used as an etching gas.

In the eighth step, an etching rate of the interlayer insulation film preferably is higher than that of the etching stopper.

In the ninth step, CHF_3, Ar, and O_2 gases may be used as
25 an etching gas.

By doing the above, because there is no etching stopper on the gate electrode, over-etching of the diffusion layer

and field oxide film are prevented when contact hole etching is done, thereby enabling the formation of a device having stable element separation characteristics.

BRIEF DESCRIPTION OF THE DRAWINGS

5 Preferred features of the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:-

Figs. 1(a) to 1(c) are drawings showing an embodiment of a method for fabricating a semiconductor device according
10 to the present invention.

Figs. 2(a) to 2(c) are cross-sectional views showing the process steps of a method of fabricating a semiconductor device according to the present invention.

Figs. 3(a) to 3(c) are cross-sectional views showing
15 process steps subsequent to those shown in Fig. 2.

Fig. 4(a) and Fig. 4(b) are cross-sectional views showing process steps subsequent to those shown in Fig. 3.

Fig. 5(a) and Fig. 5(b) are cross-sectional views showing process steps subsequent to those shown in Fig. 4.

20 Fig. 6(a) and Fig. 6(b) are cross-sectional views showing process steps subsequent to those shown in Fig. 5.

Fig. 7 is a drawing showing a simplified view of an etching apparatus according to the present invention.

Fig. 8(a) and Fig. 8(b) are drawings showing a method
25 for fabricating a semiconductor device according to the prior art.

Fig. 9 is a drawing showing a semiconductor device according to the prior art.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 2 to Fig. 6 show a method for fabricating a semiconductor device according to the present invention.

In these drawings, Fig. 2 (a) shows the first step, whereby a polysilicon film 203 and an insulation film 204 are formed on a semiconductor substrate 201, and then the polysilicon film 203 and insulation film 204 are etched to a prescribed shape, so as to form a gate electrode 203, after which an etching stopper 205 is formed over the entire surface of the substrate and an interlayer insulation film 206 is formed over the entire surface thereof.

Fig. 2(c) shows the second step, whereby a contact hole 208 is formed in the interlayer insulation film 206 that reaches the semiconductor substrate, so as to cause the etching stopper 205 on the semiconductor substrate to be exposed.

Fig. 3 (a) shows the third step, whereby the exposed etching stopper 205 on the semiconductor substrate 201 is removed.

Fig. 3 (b) shows the fourth step, whereby the contact hole 208 is filled to form a contact plug 210.

Fig. 3 (c) shows the fifth step, whereby the film 209 deposited on the interlayer insulation film 206, when the contact plug 210 is formed, is removed, so as to expose the contact plug 210.

Fig. 4 (a) shows the sixth step, whereby the interlayer insulation film 206 is etched and the etching stopper 205 on the gate electrode 203 is removed.

Fig. 4 (b) shows the seventh step, whereby an interlayer insulation film 211 is formed over the entire surface of the

substrate.

Fig. 5 (a) shows the eighth step, whereby the interlayer insulation films 211 and 206 are etched, so as to expose the etching stopper 205 on the diffusion layer 231, and the
5 insulation film 204 of the gate electrode 203 is etched, so as to form a contact hole 213 on the diffusion layer 231 and the gate electrode 203.

Fig. 5 (b) shows the ninth step, whereby the etching stopper 205 exposed on the diffusion layer 231 is removed.

10 Fig. 6 (a) shows the tenth step, whereby the contact hole 213 form by the eighth and ninth steps is filled, so as to form a contact plug 215.

The present invention is described in further detail below.

15 The method of fabricating a semiconductor device according to the present invention is illustrated in Fig. 2 to Fig. 6, which shows cross-section views of a memory device.

As shown in Fig. 2 (a), a gate electrode 203 having a
20 width of 0.2 μm and a height of 200 nm, and a 200-nm insulation layer made of a silicon oxide film, a silicon nitride film or a oxide nitride film are formed in the memory cell part on the silicon substrate 201 and the element separation region 202, with an interval of 0.2 μm. In the surrounding area,
25 a gate electrode 203 having a minimum width of 0.3 μm is formed, with an interval of 0.8 μm. A conventional CVD process is used to deposit a silicon nitride film 205 serving as an etching stopper for a self-aligning contact process, so as to cover the gate and the silicon substrate, and then a BPSG

film 206 is formed as an interlayer insulation film. When this is done, the thickness from the surface of the silicon substrate to the upper surface of the interlayer insulation film is, for example, 800 nm.

5 In the memory cell part shown in Fig. 2 (b), a lithographic process is used to pattern photoresist 207, and to pattern a contact hole that is 0.3 μm, which is larger than the gate electrode spacing. Then, as shown in Fig. 2 (c), an oxide film etching apparatus is used to etch a BPSG 10 film 206, after which, as shown in Fig. 3 (a), the silicon nitride film 205 on the semiconductor substrate is etched and the photoresist 207 are peeled off, thereby forming the contact hole 208.

As shown in Fig. 3 (b), a CVD process is used to deposit 15 phosphorus-doped polysilicon within the contact hole 208 and on the interlayer film 206. To remove the polysilicon on the interlayer film 206, a silicon etching apparatus using chlorine or oxygen or the like as an etching gas, is used to etch the entire surface, thereby forming the contact plug 20 210 as shown in Fig. 3 (c).

In the condition with the exposed contact plug 210, an oxygen dry etching apparatus is used to perform etching of the BPSG film and the etching stopper silicon nitride film 205, so as to expose the upper surface of the gate electrode 25 203. The dry etching apparatus is, for example, a flat-sheet type RIE apparatus, with an RF frequency of 13.56 MHz, the etching conditions being, for example, a pressure of 5 Pa, a gas flow of CF_4 and CHF_3 of 50 and 10 sccm, an electrode temperature of 50℃, and an RF power of 1200 W, under which

conditions the etching rates for a silicon oxide film, a silicon nitride film, and polysilicon are 600 nm/minute, 500 nm/minute, and 100 nm/minute, respectively. To control the amount of etching, an end-point detector that monitors the change in emitted light from the plasma is used. For example the emitted wavelength of CO of 483 nm and the emitted wavelength of CN of 388 nm are monitored to detect a change in intensity, thereby enabling etching up until the upper surface of the gate electrode 203.

By the above-noted etching, as shown in Fig. 4 (a), the nitride film is left on the diffusion layer, without any remaining nitride film 205 of the gate. Because the etching rate of polysilicon is low, the contact plug 210 remains in substantially its original shape.

The dry etching method can alternatively be that in which, after etching the BPSG film 206 under conditions for which the etching rate for the silicon oxide film is higher than the etching rate for the silicon nitride film, the silicon nitride film is etched.

After the above, as shown in Fig. 4 (b), a BPSG film is formed by a CVD process, and thermal treating is done in a nitrogen atmosphere, so as to cause reflow, thereby forming an interlayer insulation film 211. Then, a photoresist 212 is applied and a lithographic process is used to form a contact pattern on the contact plug 210, the gate electrode, and the diffusion layer.

Then, for example, as shown in Fig. 7, an etching apparatus having two opposing electrodes, an upper electrode 302 and a lower electrode 303, in a chamber 301 having a gas

supply mechanism at the top and a gas exhaust mechanism at the bottom, with the electrodes connected to RF sources 307 and 308 via respective matching boxes 305 and 306, is used to, as shown in Fig. 5 (a), etch the BPSG films 211 and 206,
5 and the silicon oxide film 204. When this is done, the RF frequencies in the etching apparatus are 27 MHz at the upper electrode and 800 kHz at the lower electrode, the RF powers being 2000 W at the upper electrode and 1400 W at the lower electrode, the pressure being 25 mTorr, the gas flows for
10 C_4F_8, Ar, CO, and O_2 being, 20, 300, 100, and 10 sccm, respectively, and the lower electrode temperature being -20℃. Under these conditions, the etching rates for the BSPG film and the silicon nitride film are 600 nm/minute and 50 nm/minute, respectively. If this etching rate difference is
15 used, it is possible to stop the etching at the silicon nitride film 205 on the silicon substrate 201.

Next, for example, using the etching apparatus of Fig. 7 with etching conditions such as an RF power of 1500 W and 1400 W at the top and bottom parts, a pressure of 50 mTorr,
20 gas flows of CHF_3 , Ar, and O_2 of 30, 200, and 10 sccm, respectively, and a lower electrode temperature of -20℃, the silicon nitride film 205 is etched, so as to expose the silicon substrate 201 as shown in Fig. 5 (b). When this is done, it is possible to perform control so that over-etching of the
25 silicon substrate 201 does not occur, and it is possible to prevent worsening of the element separation characteristics and contact leakage.

After peeling off the photoresist, as shown in Fig. 6 (a), sputtering of a barrier metal is done, and a CVD process

is used to deposit a film of tungsten 214, thereby forming a contact plug.

After the above, as shown in Fig. 6(b), interconnect patterning and etching are performed to form the contact plug 215 and metal interconnect layer 216, thereby electrically connecting the gate electrode, the contact plug, and the diffusion layer.

In the above embodiment, no restriction on the materials cited and the values given in the description thereof is intended.

By adopting the above-described construction, a method for fabricating a semiconductor device according to the present invention prevents over-etching of the diffusion layer and field oxide films on the silicon substrate without the need to increase the number of photolithography process steps, thereby achieving a device with superior stability and no contact leakage.

Each feature disclosed in this specification (which term includes the claims) and/or shown in the drawings may be incorporated in the invention independently of other disclosed and/or illustrated features.

The text of the abstract filed herewith is repeated here as part of the specification.

A method for fabricating a semiconductor device includes the steps of: forming a contact hole 208 so as to cause the etching stopper 205 on the substrate 201 to be exposed; removing an exposed etching stopper 205 on the substrate; filling the contact hole 208 to form a contact plug 210; removing a film 209 that is deposited on the interlayer insulation film 206, so as to expose the contact

plug 210; etching the interlayer insulation film 206 and removing the etching stopper 205 on the gate electrode 203; forming an interlayer insulation film 211; etching the interlayer insulation film 211 so as to expose the etching
5 stopper 205 on a diffusion layer 231 and etching the insulation film 204 of the gate electrode 203, so as to form contact holes 213 on the diffusion layer 231 and gate electrode 203; removing the etching stopper 205 exposed on the diffusion layer 231; and, filling the contact hole 213,
10 so as to form the contact plugs 215.

What is claimed is:

1. A method for fabricating a semiconductor device having a contact plug, said method comprising the steps of:

a first step of forming a polysilicon film and an insulation film on a semiconductor substrate, and then etching said polysilicon film and said insulation film to a prescribed shape, so as to form a gate electrode, after which an etching stopper is formed on an entire surface of said substrate and an interlayer insulation film is formed over said entire surface thereof;

a second step of forming a contact hole (that reaches said semiconductor substrate) in said interlayer insulation film, so as to cause said etching stopper on said semiconductor substrate to be exposed;

a third step of removing an exposed etching stopper on said semiconductor substrate;

a fourth step of filling said contact hole to form a contact plug;

a fifth step of removing a film that is deposited on said interlayer insulation film when said contact plug is formed, so as to expose said contact plug;

a sixth step of etching said interlayer insulation film and removing said etching stopper on said gate electrode;

a seventh step of forming an interlayer insulation film over an entire surface of said substrate;

an eighth step of etching said interlayer insulation film so as to expose said etching stopper on a diffusion layer, and etching said insulation film of said gate electrode, so as to form contact holes on said diffusion layer and said

gate electrode;

a ninth step of removing said etching stopper exposed on said diffusion layer; and

a tenth step of filling said contact hole formed by said
5 eighth step and said ninth step, so as to form said contact plugs.

2. A method for fabricating a semiconductor device according to claim 1, wherein in said sixth step, CH_4 and CHF_3 gases are used as an etching gas.

10 3. A method for fabricating a semiconductor device according to claim 1, wherein in said sixth step, an etching rate of said interlayer insulation film and said etching stopper is higher than that of said contact plug formed in said fourth step.

15 4. A method for fabricating a semiconductor device according to claim 1, wherein in said eighth step, C_4F_8, Ar, CO, and O_2 gases are used as an etching gas.

5. A method for fabricating a semiconductor device according to claim 1, wherein in said eighth step, an etching
20 rate of said interlayer insulation film is higher than that of said etching stopper.

6. A method for fabricating a semiconductor device according to claim 1, wherein in said ninth step, CHF_3, Ar, and O_2 gases are used as an etching gas.

25 7. A method for fabricating a semiconductor device having a contact plug, the method being substantially as herein described with reference to and as shown in Figures 1(a) to 7 of the accompanying drawings.

Application No: GB 0007279.3
Claims searched: all

Examiner: Claire Williams
Date of search: 24 August 2000

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.R): H1K (KDEG, KDES, KDEX, KHAE, KGFX, KLEXX)

Int Cl (Ed.7): H01L (21/3065, 21/3105, 21/311, 21/60, 21/768, 27/108)

Other: ONLINE: WPI, EPODOC, JAPIO

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
A	GB 2289984 A	(HYUNDAI) in particular page 6 lines 26 to 31 and page 7 lines 21 to 26.	
A	EP 0337109 A1	(INTERNATIONAL BUSINESS MACHINES) whole document	
A, P	WO 99/16118	(ADVANCED MICRO DEVICES) in particular claim 1	

15

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.