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Fischer

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[54] **DIRECT CURRENT ELECTROLUMINESCENT PANEL USING AMORPHOUS SEMICONDUCTORS FOR DIGITALLY ADDRESSING ALPHA-NUMERIC DISPLAYS**

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[73] Assignee: **The United States of America as represented by the Secretary of the Army,** Washington, D.C.

[22] Filed: **Nov. 28, 1973**

[21] Appl. No.: **419,827**

Related U.S. Application Data

[62] Division of Ser. No. 310,736, Nov. 30, 1972, Pat. No. 3,807,036.

[52] **U.S. Cl.** ..... **340/324 M;** 340/166 EL

[51] **Int. Cl.²** **G06F 3/14**

[58] **Field of Search**... 340/324 A, 324 AD, 166 EL, 340/168 SR; 357/2, 24

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Attorney, Agent, or Firm—Max L. Harwell; Nathan Edelberg; Robert P. Gibson

[57] **ABSTRACT**

An alpha-numeric display panel with a matrix of amorphous semiconducters mounted on a substrate. Each of the semiconductors comprises a vitreous material layer contiguous with an electroluminescent material layer. Metal electrodes with small metal islands positioned in the center of the electrodes and isolated therefrom are vapor deposited through a photoetched mask on each side of the vitreous material, or vitreous switching layer. The electrodes and islands are in exact registration on opposite sides of the vitreous switching layer. An electrically conductive layer is vapor deposited on one side of a glass substrate. The electroluminescent layer is contiguous with one side of the vitreous switching layer on one side and is contigous with the electrically conductive layer on the opposite side. The matrix of amorphous semiconductors are connected to a voltage source, ground, and to bucket brigade shift registers, such that a display is generated according to video information transmitted to the read-out and matrix.

The electrodes on the rear of the vitreous switching layer are connected to a positive direct current voltage source. The electrically conductive layer is connected to ground. The rear metal islands are connected to row shift registers, and the front metal islands are connected to the column shift registers. The column shift register has an overriding video signal thereon. The vitreous layer is biased close to, but less than, the amount required for conduction such that an increased voltage potential across the vitreous layer provided by the combination of the shift register and video signals causes the amorphous semiconductor to conduct and, therefore, the electroluminescent layer to luminesce providing a display at that element. Horizontal and vertical clock pulses, from the column and row shift registers, synchronously switch voltages to the rear and front metal islands until the entire panel has been scanned. The electroluminescent layers remain "on", thus displaying an alpha-numeric read-out, until the direct current voltage source is removed from the rear electrode.

7 Claims, 3 Drawing Figures

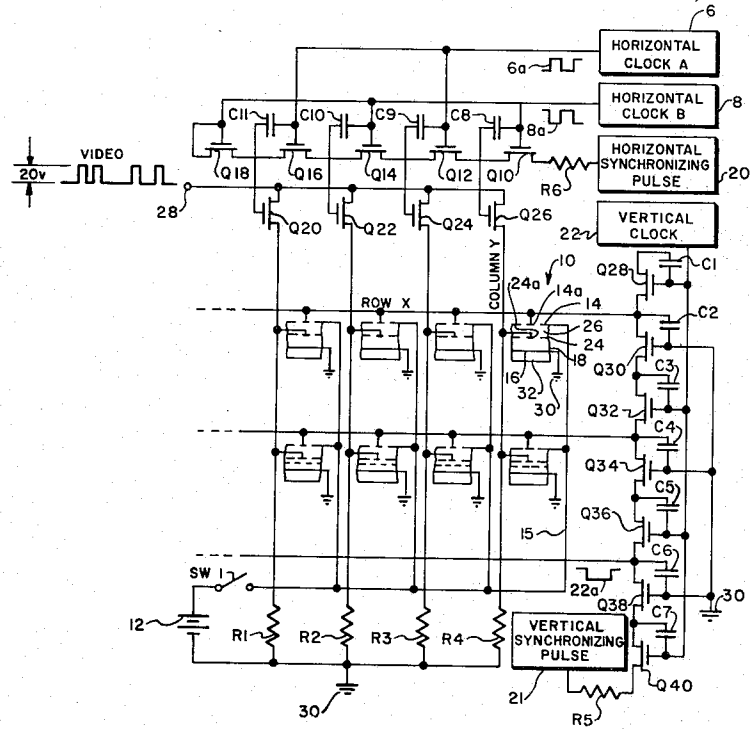


FIG. 1

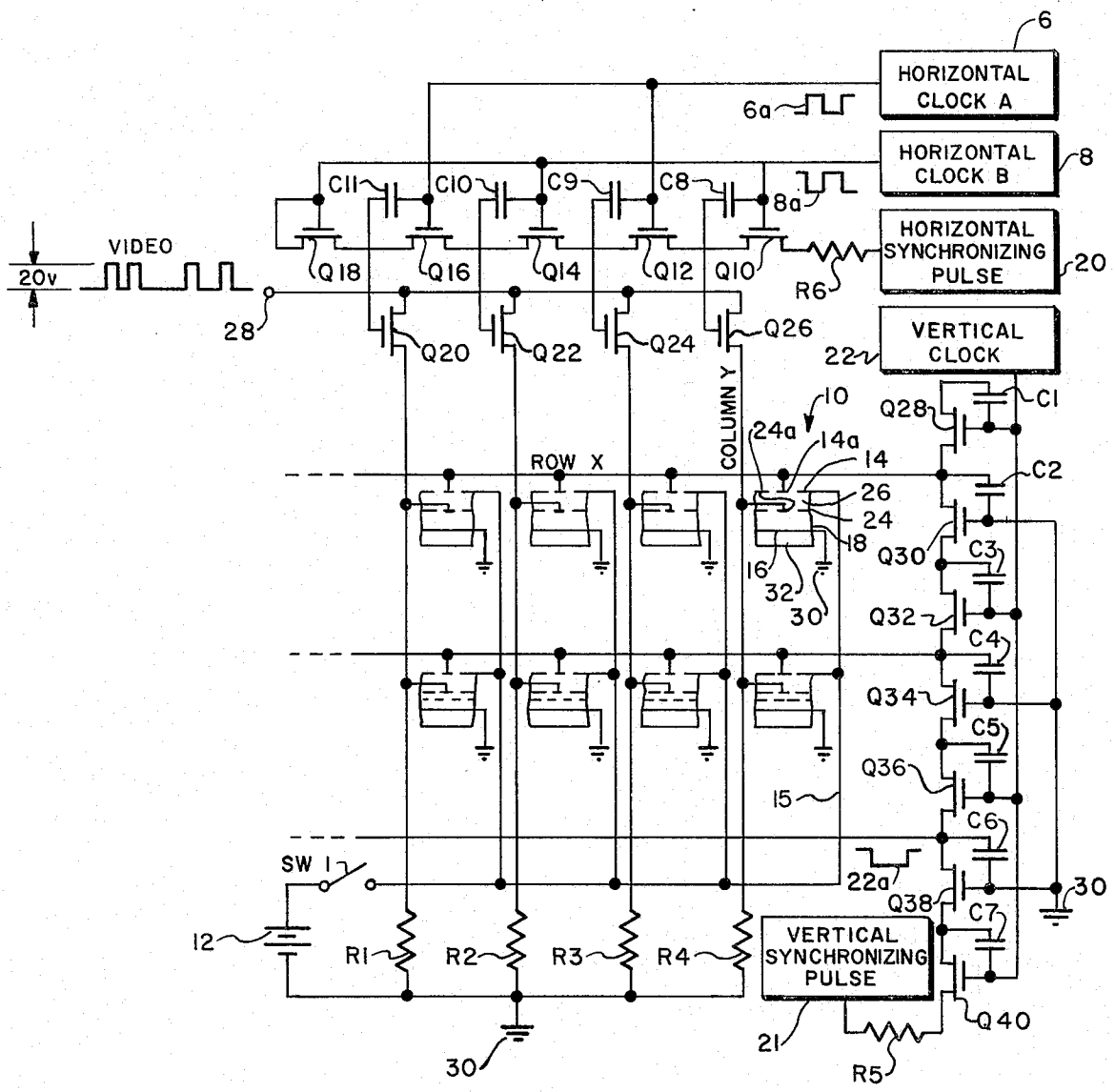

6
HORIZONTAL CLOCK A
6a
HORIZONTAL CLOCK B
8
8a
C11
C10
C9
C8
HORIZONTAL SYNCHRONIZING PULSE
20
VIDEO
20v
Q18
Q16
Q14
Q12
Q10
R6
28
Q20
Q22
Q24
Q26
VERTICAL CLOCK
22
COLUMN Y
10
24a
14a
14
ROW X
C1
Q28
C2
26
24
18
Q30
C3
16
32
30
Q32
C4
Q34
C5
Q36
15
C6
SW 1
22a
Q38
30
C7
12
R1
R2
R3
R4
VERTICAL SYNCHRONIZING PULSE
Q40
21
R5
30

FIG. 2

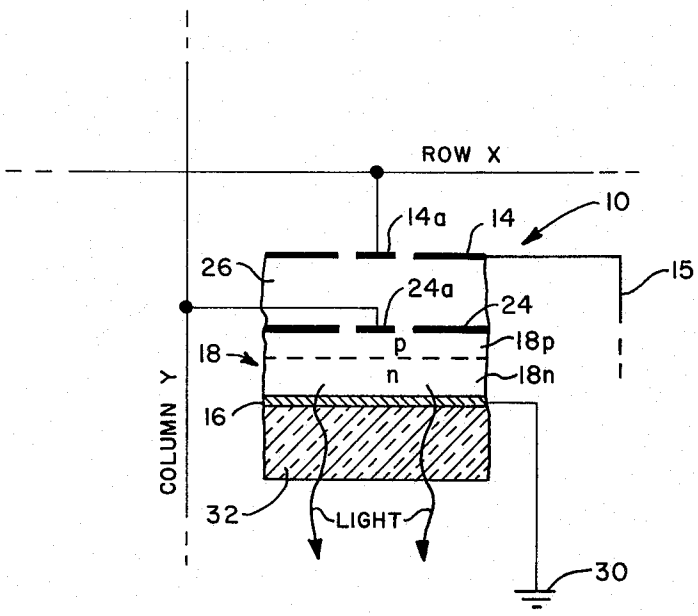
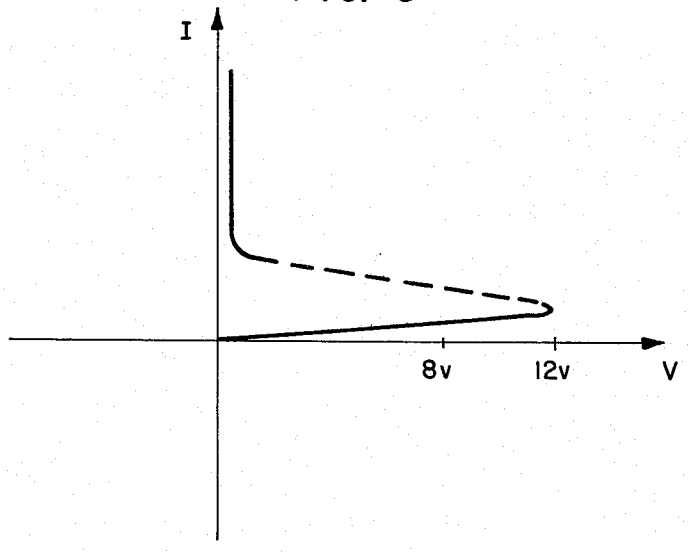

ROW X
14a
14
10
26
24a
24
15
18
p
18p
n
18n
COLUMN Y
16
32
LIGHT
30

FIG. 3


I
8v
12v
V

DIRECT CURRENT ELECTROLUMINESCENT PANEL USING AMORPHOUS SEMICONDUCTORS FOR DIGITALLY ADDRESSING ALPHA-NUMERIC DISPLAYS

This is a divisional of prior application Ser. No. 310,736, filed 30 Nov. 1972, now U.S. Pat. No. 3,807,036.

BACKGROUND AND SUMMARY OF THE INVENTION

This invention is in the field of large flat panel electroluminescent diode read-out displays using amorphous semiconductors with vitreous material for switching video signals across electroluminescent elements.

Previously, the development of display panels was directed toward gas discharge elements, solid breakdown voltage devices, etc. which were triggered by alternating current (a.c.) voltage. More recently, display panels using miniaturized electroluminescent elements for transmittal of light are used wherein the elements are turned "on" by a d.c. voltage.

The present invention comprises a predictable and efficient breakdown amorphous semiconductor having a vitreous switching layer that switches "on" by coincident voltages at the rear and front metal islands on each side thereof. These coincident voltages are produced as horizontal and vertical clock pulses at the output of shift registers. A positive d.c. voltage source is applied to the rear electrode on the vitreous switching layer and sets up an electric field in the vitreous and electroluminescent layers between the positively charged rear electrode and a grounded electrically conductive layer, which is contiguous with the electroluminescent layer and the glass substrate. When output clock pulses from both shift registers are coincident at their respective islands in any one element, the vitreous switching layer will break down in the area between the metal islands and start conducting current therethrough if a video signal is also present. The electric field provided by the d.c. voltage source applied to the rear electrodes will sustain conduction in the vitreous and electroluminescent layers, thus holding the electroluminescent layer in a luminescent condition even after the video signal is removed, and can only be stopped by removal of the d.c. voltage source. For the panel to accept a subsequent display, the d.c. voltage source is simply switched off for removal of the alpha-numeric display and switched back on again to establish the electric field for the subsequent display.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a schematic circuit showing bucket-brigade type scanners, feeding rows and columns of the amorphous semiconductor electroluminescent elements;

FIG. **2** is a diagrammatic illustration of a single element amorphous semiconductor electroluminescent element; and

FIG. **3** is a V-I curve of the electrical characteristics of the vitreous switching element within the amorphous semiconductor.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. **1** illustrates a partial schematic of a multi-element electroluminescent display panel. A typical element **10** (shown in the upper right) is biased by d.c. voltage source **12** when switch SW1 is closed, thus placing an electric field across element **10.** Element **10** is addressed by clock pulses from column and row bucket brigade shift registers, respectively, arriving on column Y and row X. The column bucket brigade shift register is comprised of horizontal clocks A and B, represented by numerals **6** and **8,** and horizontal synchronizing pulse generating circuit **20.** The row bucket brigade shift register is comprised of vertical clock **22** and vertical synchronizing pulse generating circuit **21.** Horizontal clocks **6** and **8** produce square waves **6***a* and **8***a* that are 180° out of phase with each other. Square waves **6***a* and **8***a* are applied to alternate gates of column shift register MOSs to "hand off", in a bucket brigade manner, the horizontal synchronizing pulses from circuit **20** along the column shift register MOSs **Q10, Q12, Q14, Q16, Q18,** and others (not shown). The outputs from the column shift register MOSs are applied to the gates of video MOSs **Q20, Q22, Q24, Q26,** and others (not shown) totalling the number of columns in the matrix. Video signals are applied to terminal **28.** Terminal **28** is connected to all of the source terminals of the video gate MOSs **Q20, Q22, Q24, Q26,** etc. When a video signal is present at terminal **28** and the video MOSs are gated on by display information from horizontal clocks **6** and **8,** the video signal will be transmitted to islands **24***a* of elements **10.** This display information present at clocks **6** and **8** may be transmitted on a high frequency carrier wave, such as a laser beam or a VHF channel, into the horizontal clocks of the column bucket brigade shift register. Similarly, display information present at vertical clock **22** "hands off" the vertical signal pulses from circuit **21** along row shift register MOSs **Q40, . . . , Q28,** and others (not shown) totalling the number of rows in the matrix. This display information is first received, amplified, and decoded using circuitry similar to a television receiver (with such circuitry not being a part of this invention) and is produced as digitalized information at the output of the column and row shift registers. The shift registers operate similar to deflected coils of a television, while the video gate MOSs operate as modulation devices. When there is coincidence of the digitalized information, the video signal addresses an electroluminescent element **18.** The horizontal shift register operator typically at 5 kilocycles for an element **18** addressing time of 200 microseconds.

Referring to FIG. **2,** a typical display element **10** of this invention is shown. Element **10** is an amorphous semiconductor that comprises a vitreous switching element layer **26,** an electroluminescent element **18** made of layered *p–n* material, an electrically conductive layer **16,** and a glass substrate **32.** Rear electrode **14** and rear metal islands **14***a* are vapor deposited on the rear side of layer **26.** Front electrode **24** and front metal island **24***a* are vapor deposited on the front side of layer **26.** An external d.c. voltage source **12** is connected to rear electrode **14** when switch SW1 is closed. Layer **16** is connected to ground terminal **30.** Electrical leads from a column and a row, represented as column Y and row X, are shown connected to front metal island **24***a* and rear metal island **14***a*, respectively. Islands **14***a* and **24***a* are positioned directly opposite each other on layer **26.** Also, rear electrode **14** and front electrode **24** are positioned directly opposite each other on layer **26.** Opera-

tion of the amorphous semiconductor will be explained in more detail later with reference to FIG. **2.**

The display panel is prepared by the process as explained hereinbelow. Starting with glass substrate **32,** an electrically conductive layer **16** of transparent material, such as tin oxide, is evaporated on one side thereof. A direct current electroluminescent layer **18** is then vapor deposited on conductive layer **16.** Layer **18** may be a polycrystalline heterjunction sandwich structure made of group II–VI materials, or alternately a layer composed of many single crystalline light emitting diodes. In either case, layer **18** will become operative at a few volts and milliamperes of d.c. power, e.g., 8 volts at 1 milliamperes. Typically, an embodiment of a panel made in this manner has 250,000 elements in a panel having 500 rows and 500 columns. If layer **18** is polycrystalline heterjunction sandwich structure, metallized square electrodes **24** and small metal islands **24***a* enclosed by and insulated from electrodes **24** are vapor deposited through a photoetched mask onto the back side of electroluminescent layer **18.** In further developing element **10** for use as a display element, electrodes **24** and islands **24***a* are separated by an insulator material, which is deposited by photoresist techniques, such that electrodes **24,** but not front islands **24***a*, are insulated from column leads. The insulator material may be aluminum oxide. These column leads are deposited over the insulator material and are connected to each of the front islands such that the column leads are insulated from front electrode **24.** However, the remainder of front electrode **24** not insulated from the column lead is in intimate contact with layer **18.** The column leads are connected at their opposite end to the drain terminal of the various video MOSs **Q20, Q22, Q24, Q26,** etc. Vitreous switching layer **26** is deposited over the electroluminescent layer **18,** the insulator material layer, and the column leads deposited thereon. Layer **26** is from 1 to 10 microns in thickness. Layer **26** may be vacuum deposited, rf sputtered, etc. A great variety of materials are known to exhibit the switching effect needed for layer **26.** Some of these materials are germanium, sulfur, selenium silicon oxide, aluminum oxide, etc. On top of this vitreous material layer **26** are deposited the rear electrodes and rear islands in the same manner that the front electrodes and front metal islands were deposited on layer **18,** i.e., by vapor depositing through a photoetched mask. The electrodes and islands deposited on each side of layer **26** are in exact registration. A layer of insulator material is deposited by photoresist techniques such that the rear electrodes **14,** but not the rear metal islands **14***a*, are insulated from row leads. The row leads are connected to the rear metal islands. Rear electrode **14** is in intimate contact with layer **26.** Lead wires from all of the rear electrodes **24** are connected to power supply **12.** The row leads are connected to the rear metal islands at one end and to the bucket brigade vertical shift register MOSs **Q28, Q30, Q32, Q34, Q36, Q38, Q40,** etc., at the other end. With pulses on row leads from the bucket brigade vertical shift register MOSs and pulses on the bucket brigade horizontal shift register MOSs connected, respectively, to rear metal islands and front metal islands, the vitreous switching layer **26,** which these islands are connected across, conducts through the area between the particular metal islands **14***a* and **24***a* being pulsed. The conducting area between islands **14***a* and **24***a* forms a generally cylindrical aisle through layer **26.** The cylindrical aisles extending through the electroluminescent layer may simply be the electroluminescent layer **18** left uncovered, or grooves etched all the way through to conductive layer **16.** These grooves are needed for optical separation such that light from one element cannot be scattered into the next element. The grooves may also be filled with black resin by simply rubbing the resin therein. A typical I–V characteristic curve for the vitreous material of layer **26** is shown in FIG. **3.** These characteristics are discussed below with reference to the voltages existing between electrodes **14** and **24.**

FIG. **1** illustrates a partial schematic of the overall scanning system with the matrix of amorphous semiconductor attached to voltage source **12** and to the various column and row leads. When switch **SW1** is closed, the positive terminal of voltage source **12** is connected to rear electrodes **14** on all the semiconductors, establishing a potential gradient through all of the elements between rear electrode **14** and layer **16** that is connected to ground **30.** Front electrode **24** is, therefore, at some floating potential between the positive voltage from voltage source **12** and the ground potential on layer **16.** The voltage differential between electrodes **14** and **24** is close to, but under, the amount needed to initiate conduction through the area of the vitreous switching layer **26** that is between rear electrode **14** and front electrode **24.** When layer **26** conducts there is also conduction through layer **18** between front electrode **24** and layer **16,** thus causing electroluminescent layer **18** to luminesce. Scanner voltages from horizontal clocks A and B, represented by pulses **6***a* and **8***a*, respectively, apply positive pulses to the gate electrodes of alternate horizontal shift register MOSs **Q10, Q12, Q14, Q16, Q18,** etc., and others (not shown). The horizontal shift register MOSs alternally gated "on", the horizontal synchronizing pulse from circuit **20** is passed along the horizontal shift register MOSs in bucket brigade "hand off" fashion. These "hand off" horizontal synch pulses are applied to the gates of video MOSs **Q26, Q24, Q22, Q20,** and others (not shown). When pulse **6***a* from clock **6** is positive, pulse **8***a* from clock **8** is negative, and vice versa. Video information, applied at terminal **28** is connected to the source terminals of the video MOSs. Electrical leads from the drain terminals of the video MOSs are connected to column leads which are, in turn, connected to metal islands **24***a* of the semiconductors. In operation, a horizontal synchronizing pulse circuit, represented by block **20,** produces synchronous pulses that are "moved along" the bucket brigade horizontal shift register MOSs **Q10, Q12, Q14, Q16,** and **Q18** by alternate pulses **6***a* and **8***a*. Vertical clock **22** applies positive voltage pulses to alternate gates of the bucket brigade vertical shift register MOSs **Q28, Q30, Q32, Q34, Q36, Q38,** and **Q40.** A vertical synchronizing pulse produced, through resistor **R5,** at the output of vertical synchronizing pulse circuit **21** is also "moved along" the bucket brigade vertical shift register MOSs. More specifically, video information is stored in one of the two storage registers, or horizontal clocks A and B, represented by blocks **6** and **8,** while the vertical shift register **22** discharges its previously stored information into all elements of one column simultaneously. Storage and discharge of the registers are out of phase with each other as shown by the output waves **6***a* and **8***a* therefrom in FIG. **1.** The video input signals to the ma-

trix at terminal **28** is the actual source of information that is displayed on the various electroluminescent elements of the matrix. The bucket brigade vertical shift register MOSs gate the various video MOSs "on" such that when the video information is present at the source terminal of the video MOSs the information is passed to the drain terminal and on to the islands **24***a* of the elements.

In the shift register addressing method, the column scanner is a slow shift register that scans, say for example, the right column. During the time that the slow register scans this one column, the fast register scans all of the rows in a sequential manner. Therefore, while the extreme right column has a voltage applied to the middle metal islands **24***a*, all of the vertical synchronizing pulses from **21** are applied to the rear metal islands **14***a*. Only at the addressing coincidence of the column Y and row X elements **10** along this extreme right column will the video signal, present at terminal **28** and at the source terminal of the video MOSs, switch the vitreous layer **26** "on", causing luminescence of that element. Instantaneously, only the element **10** in the extreme upper right has the full voltage applied across the rear metallic island **14***a* and the middle metallic island **24***a*. If the video signal is present at the video input terminal **28,** this signal switches the element which has the voltages coincidence thereacross and the element — in this case element **10** — will luminesce. The slow column scanner will then switch to the next column and the fast scanner will switch on all the rows sequentially before the slow column scanner switches again. The video signal has a larger voltage peak than the column and row scanner voltages, and consequentially switches the coincidence address elements "on". After the entire panel has been scanned, the scanners may be switched off and the image retained. The image may be erased by opening switch SW1 to the external d.c. voltage source **12.** The panel may then be readdressed. An important alternative to erasing the image over the entire panel is that of erasing one line at a time by inserting a switch in each line (row and column) and selectively opening these switches after the entire panel has been scanned. Also, selective erasure of single lines of the alpha-numeric read out on the panel may be controlled from the broadcasting station by coded signals to which the receiver is sensitive.

In operation, assume that the extreme right column is pulsed, the strongly positive pulse video signal, at the source terminal of video MOS Q**26,** is passed through MOS Q**26** to front metal island **24***a* of element **10.** The video signal sets up a high electric field in the small area between the rear metal island **14***a* and front metal island **24***a*. The video signal voltage is greater than the threshold voltage that has been established across layer **26** by applying d.c. voltage source **12** to rear electrode **14.** Therefore, when the video signal is applied the small area of layer **26** that is between islands **14***a* and **24***a* will break-down and begin conducting. The differential voltage between the positive d.c. voltage applied to electrode **14** and the floating voltage on electrode **24** is sufficient to break-down the entire area of layer **26** when the area between islands **14***a* and **24***a* has broke-down. Conduction is sustained through layer **26** by d.c. voltage source **12** even after the video signal has been removed. That is, the unswitched vitreous material of layer **26** has high impedance until the video signal is applied and the low impedance after the video signal is applied. After the column and row shift registers have scanned the entire panel, the alpha-numeric read-out will remain on the display panel until the panel is readdressed. When conduction begins through layer **26** this conduction extends through layer **18** and into layer **16.** The electroluminescent material in layer **18** will luminesce when conduction is taking place therein.

I claim:

1. An electroluminescent display panel comprising:

a light translucent substrate;

a transparent electrically conductive layer contiguous with one side of said substrate;

a layer of electroluminescent material contiguous with said transparent electrically conductive layer;

a plurality of metallized front electrodes and front islands with said front electrodes contiguous with said layer of electroluminescent material, said front electrodes and said front islands insulated from each other;

a plurality of column leads connected to said plurality of front islands;

a layer of vitreous material contiguous with said plurality of metallized front electrodes and front islands and said layer of electroluminescent material;

a plurality of metallized rear electrodes and rear islands contiguous with said layer of vitreous material;

a plurality of row leads connected to said plurality of rear islands;

a positive direct current power supply, said power supply connected to said plurality of metallized rear electrodes for establishing a voltage differential across said layers of vitreous material and electroluminescent material such that the voltages differential between said rear and front metallized electrodes is close to the breakdown voltage of said layer of vitreous material;

a bucket brigade column shift register having two horizontal clock pulse circuits and horizontal synchronizing circuit as inputs and a plurality of column shift register metallic oxide semiconductors as outputs;

a bucket brigade row shift register having a vertical clock pulse circuit and vertical synchronizing circuit as inputs and a plurality of row shift register metallic oxide semiconductors as outputs wherein said two horizontal clock pulse circuits and said vertical clock pulse circuit are adapted for receiving display information;

a video terminal;

a plurality of video metallic oxide semiconductors having a gate electrode, a drain electrode, and a source electrode wherein said video terminal is connected to said source terminal of the plurality of video metallic oxide semiconductors and wherein the outputs of said plurality of column shift register metallic oxide semiconductors is connected to said gate terminal of the video metallic oxide semiconductors for switching video invormation through the video metallic oxide semiconductors to the rear metal islands for breaking down said layers of vitreous material and electroluminescent material to provide a display on said electroluminescent material according to the input display information to said column and row shift registers.

2. An electroluminescent display panel as set forth in

claim 1 wherein said light translucent substrate is glass.

3. An electroluminescent display panel as set forth in claim 1 wherein said transparent electrically conductive layer is tin oxide.

4. An electroluminescent display panel as set forth in claim 1 wherein said layer of vitreous material is germanium.

5. An electroluminescent display panel as set forth in claim 1 wherein said layer of vitreous material is sulfur.

6. An electroluminescent display panel as set forth in claim 1 wherein said layer of vitreous material is selenium silicon oxide.

7. An electroluminescent display panel as set forth in claim 1 wherein said layer of vitreous material is aluminum oxide.

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