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(71) Applicant
PMJH Electronic Consultants Limited,
(Great Britain),
792 Halifax Road,
Liversedge,
W. Yorks,
WF15 8HG
(72) Inventors
M. J. Hampshire,
Dr. J. Parkes
(74) Agent and/or address for service
M. J. Hampshire,
Electrical Engineering Department,
University of Salford,
Salford,
Lancs.
M5 4WT

(54) **Electronic control means**

(57) The invention relates to the field of electronic microprocessor control equipment. The application describes a computer containing a resident high level language interpreter which provides for easy programming. The computer contains read-write memory (RAM) 4 and non-volatile programmable read-only memory (PROM) 8 and means to burn programmes into the read-write memory without the necessity for any external circuitry or equipment. The computer will, on power-up, search and find the area of contiguous RAM and will then execute a valid programme instruction starting in a specific address of PROM and so provide a turn-key operation by entering automatically the control mode of the system. If a valid programme is, however, not found the computer enters the command mode of the system and communicates with an external terminal.

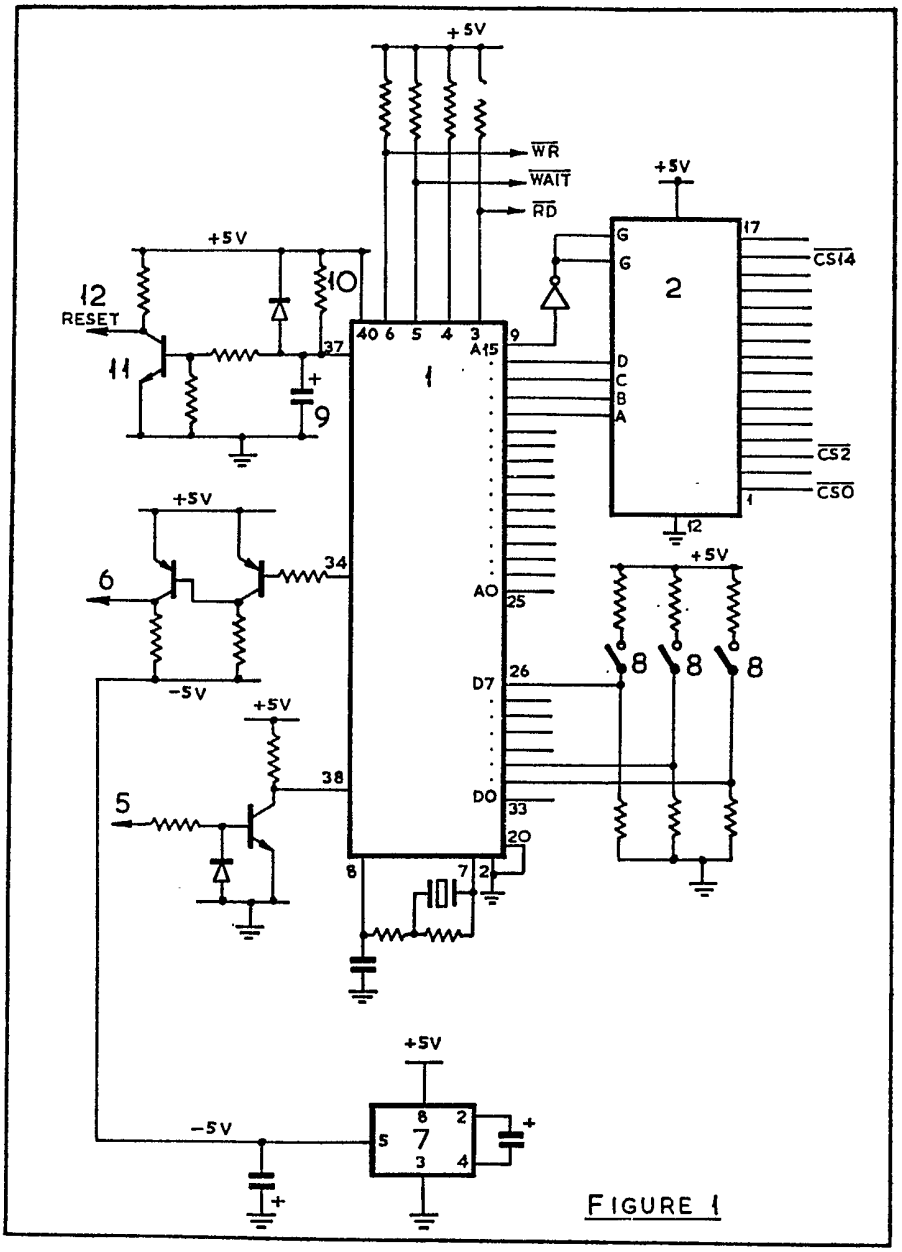

FIGURE 1

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The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

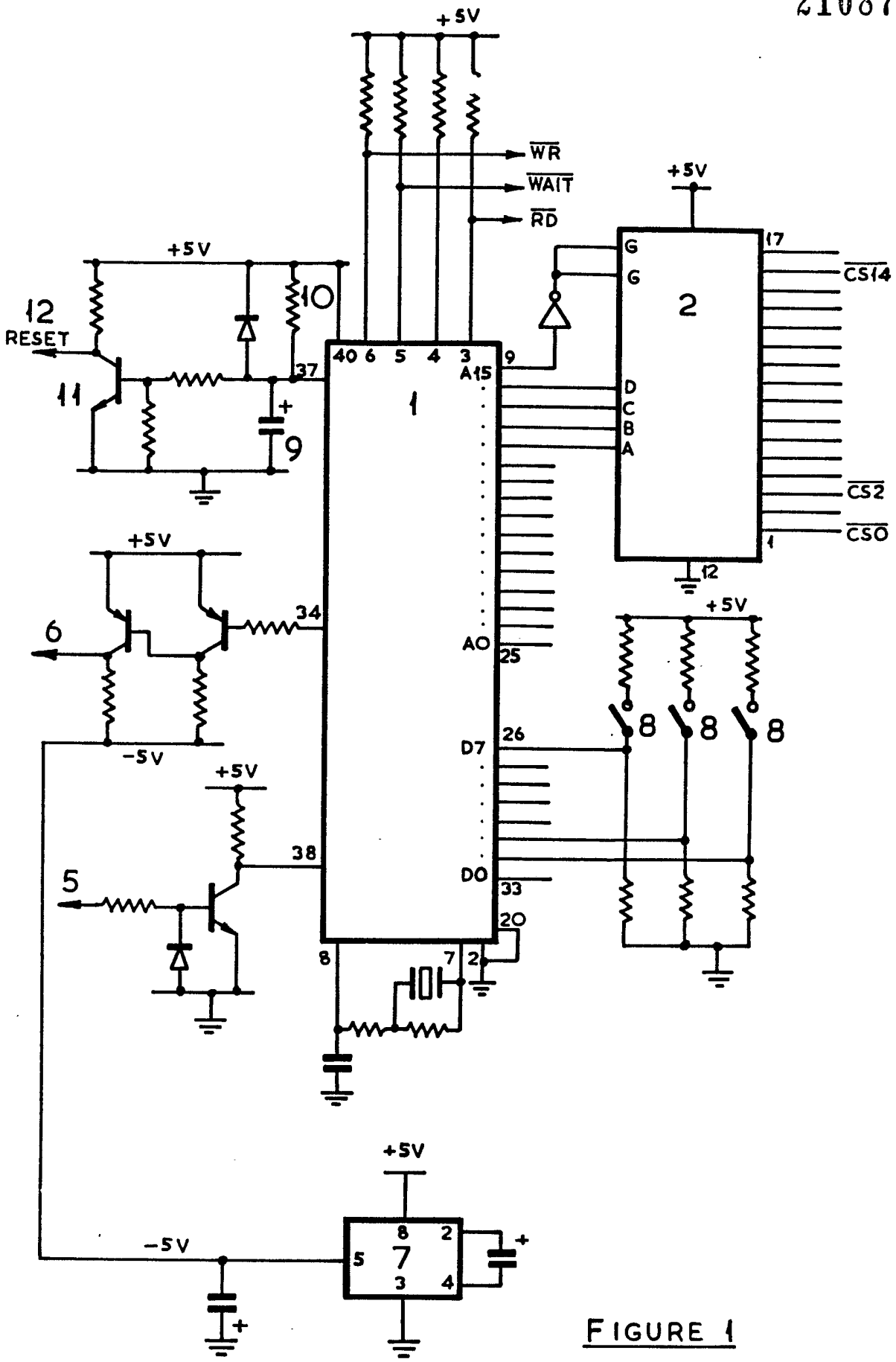
+5V
WR
WAIT
RD
+5V
12
RESET
11
10
9
37
40 6 5 4 3
A15
AO
25
D7
26
DO
33
20
8
7
2
38
34
6
5
1
+5V
G
G
2
17
CS14
D
C
B
A
CS2
CS0
1
12
+5V
8
8
8
+5V
-5V
+5V
-5V
8
2
5
7
3
4

FIGURE 1

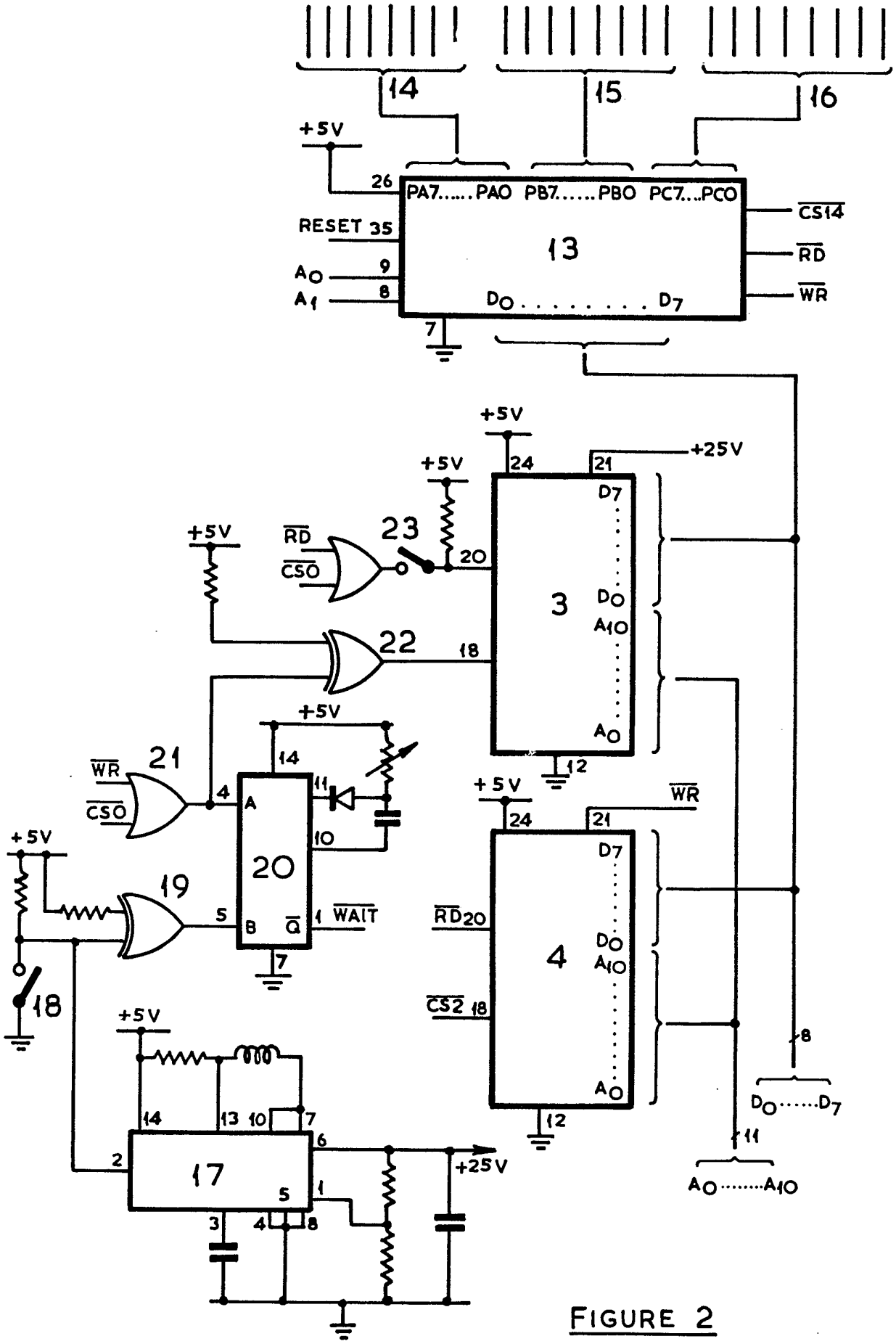
14
15
16
+5V
26
PA7.....PA0
PB7.....PB0
PC7...PC0
RESET 35
13
$\overline{CS14}$
$\overline{RD}$
$\overline{WR}$
A0 9
A1 8
D0 . . . . . D7
7
+5V
+5V
24
21
+25V
D7
+5V
$\overline{RD}$
$\overline{CS0}$
23
20
3
D0
A10
22
18
A0
12
+5V
14
$\overline{WR}$
21
$\overline{CS0}$
4
A
11
20
10
+5V
19
5
B
$\overline{Q}$
1 $\overline{WAIT}$
7
+5V
18
+5V
24
21
$\overline{WR}$
D7
$\overline{RD20}$
4
D0
A10
$\overline{CS2}$ 18
A0
12
8
D0.....D7
11
A0.....A10
+5V
14
13
10
7
6
2
17
5
1
+25V
3
4
8

FIGURE 2

SPECIFICATION

Electronic means for control of machinery

The present invention relates to electronic means for controlling and/or monitoring machinery or any system requiring complex logic with or without arithmetic capabilities.

For some time programmable logic controllers and computer systems have been available and have been used to control systems, or more specifically machinery, requiring complex logic, timing delays and arithmetic operations. The problem has been that the electronic system has required considerable programming skill if machine code were used. If a high-level language were used, then the electronic system carries a high cost penalty in that it is necessary to provide means to interpret the language or to compile it. Turn-key systems, which are necessary in many control and monitoring applications, are usually achieved by holding the operating programme in a non-volatile memory. Any variable data would normally be loaded manually from a keypad input into a volatile memory and this operation would be necessary each time the system was powered-up. Any changes in the operating software of firmware would usually be achieved by using a separate development system, which had the capability of burning PROM, EPROMS or EAROMS. Consequently, unless they are expensive and sophisticated present systems are not especially versatile and do not find application in the general area of control and monitoring of cheaper machinery and systems. The present invention proposes a simple, cheap method of controlling machinery using a high-level language where the means for permanently burning a programme into a non-volatile memory are included in the control system. Consequently, the system is versatile in that variable data can be tried and then permanently committed to non-volatile memory when satisfactory. Similarly, programme changes can be achieved within the proposed system and again committed to permanent memory when satisfactory, changed and tested without the requirement of a separate development system or PROM burning unit.

According to the present invention, there is provided a volatile read-write memory, a non-volatile normally read-only memory, circuit means for writing to the non-volatile memory, and a processor for controlling the transfer of data from the volatile memory to the non-volatile memory using the circuit means for writing to the non-volatile memory, said processor having means to run a programme stored in the non-volatile memory so providing a resident control mode for the system, and means to communicate with an external terminal so providing an external interactive command mode for the system, which also includes circuit means for determining whether the system is in the said resident control mode or the said interactive command mode.

A preferred embodiment of the apparatus may comprise one or more of the following advantageous features:—

(a) The system comprises permanent memory containing a programme to interpret a high level language.

(b) The system comprises means to handle one or more input/output lines which provide control and/or monitoring capability.

(c) The system comprises a serial input line and a serial output line for the purpose of providing communication with a VDU (visual display unit with keypad) or similar device such as a keypad and/or a printer.

(d) The system comprises electrical lines and connectors which will provide for expansion of the system. Such expansion may include one or more of the following:—

(1) extra memory
(2) extra input/output lines
(3) A/D and/or D/A channels
(4) module for switching power
(5) arithmetic (number-crunching) circuit means
(6) real-time clock and/or calendar
(7) keypad
(8) visual display means
(9) extra microprocessor

(e) The system comprises switching means to enable a number of programme alternatives to be selected.

(f) The system comprises a microprocessor, which on power-up will check that ROM exists at a specified address and, if so, execute the programme starting there, if not will interact with and receive instructions from, an external terminal.

(g) The system comprises switching means to enable or disable the ROM resident at the specific address referred to in (f) above so that the system will operate a programme starting at the specific address, if the ROM is enabled, or, if disabled, will interact with an external terminal in an interactive command mode.

In order that the invention may be more clearly understood an embodiment of the invention will now be described with reference to the accompanying figures.

Figure 1 illustrates the circuit containing a microprocessor with power-up reset, together with address decode logic and means for generating RS232 serial communication.

Figure 2 illustrates a circuit containing RAM, EPROM together with a circuit for writing to the EPROM and including a programmable I/O circuit providing three, 8 bit parallel I/O ports.

Referring to figure 1, there is a microprocessor, 1, which is a National Semiconductor device number 8073 which contains a Tiny Basic Interpreter specifically intended for control application. On power-up this processor does an automatic search of the memory space and finds the area containing RAM giving great flexibility as to the location and amount of RAM which is included in the design. After the memory search

the processor will execute any Basic programme starting in ROM at address location 8000 Hex. The decoder chip, 2 is enabled at address 8000 H by the highest address line and $\overline{CS0}$ selects the 2K×8 EPROM chip, 3, in figure 2. The chip select line $\overline{CS2}$ is used to enable a 6116 which is a 2K×8 CMOS RAM chip, 4, which could readily be made non-volatile by battery back-up although this feature is not shown.

Referring again to figure 1, the circuit provides a serial input line 5 which is capable of receiving RS232 signals. Similarly, line 6, provides RS232 serial transmission, the –5V supply being derived from a 7660 chip, 7. The three switches, 8, enable three logic ones or three logic zeros or any of the eight possible combinations onto the data lines and provided the data bus is not being driven by any of the chips, the three digit binary number can be read by the microprocessor. This provides for the selection of any one of eight possible options which reside in the Basic Interpreter, and selects amongst other things, the baud rate of the serial communication. The resistors connecting the switches to +5V must be at least less than

$$\frac{1}{3}$$

of the value of the resistors connecting the other pole of each switch to ground. Also both resistors must be large enough so that any chip can drive the data bus high or low irrespective of the state of any of the switches, 8.

Figure 1 shows a reset circuit, which is activated when the system is powered up. The capacitor, 9, is charged through the resistor 10 and whilst pin 37 is held low the processor, 1, is reset. The transistor, 11, inverts the signal and provides an active high reset, 12, which is used to reset the programmable I/O chip, 13, which provides three parallel 8 bit I/O ports 14, 15 and 16 (see Figure 2). The I/O chip shown is the 8255 and is memory mapped being selected from $\overline{CS14}$ generated by the decode chip, 2, in figure 1.

The EPROM 3, shown in Figure 2 requires a 25V supply for programming which is generated from a standard TL497 switching regulator chip, 17. The regulator is enabled on closing the switch, 18 and through the exclusive OR gate, 19 connected as an inverter the monostable, 20, is also enabled. When the processor 1 generates a low write enable pulse, and a low zeroeth chip select, $\overline{CS0}$ and $\overline{WR}$ are both active low and through the OR gate, 21, the monostable 20 is triggered producing an active low $\overline{WAIT}$ pulse for fifty milliseconds. During this time the appropriate data required to write to the EPROM, 3, is held on the data bus. The PD/PGM signal (pin 18, chip 3) which is normally active low in the read mode, is inverted by the exclusive OR gate, 22, connected as an inverter to provide the correct level for programming. After programming is complete, verification is possible with the 25V level still enabled by performing a read on the EPROM, and comparing the data with the original information to be programmed. With switch 18 open the regulator chip 17 is disabled and has the feature that the 25V supply falls to just below 5V which is supplied to pin 21 of the EPROM 3. This 5V level is necessary for the normal read only operation of the EPROM.

Instead of activating the programming of the EPROM by a switch, 18, it is possible to connect the active side of the switch to one bit of an output port say, 14. In this way the programming of the EPROM could be totally initiated by software.

The following programme is written in BASIC and provides the software initially necessary to move programmes from RAM to EPROM and vice versa, giving the hardware described a very high degree of versatility:—

```
10 N=£8000
20 M=£19100
30 FOR I=0 TO 99
40 @(N+I)=@(M+I)
50 NEXT I
```

The above programme is by way of example and moves a hundred bytes of data stored from address M, in the above case 9100 Hex upwards, which is located in RAM in the specific embodiment described here, and moves the data sequentially one byte at a time to address 8000 Hex upwards which is the start of the EPROM memory space. Provided that the programming switch 18 is closed then this movement of data results in the permanent storage of the data into a virgin EPROM.

On power-up the microprocessor, 1, will check that PROM exists at 8000 Hex, and if so, will execute the programme resident there. The system is then in the resident control mode. If the switch, 23 in figure 2 is opened then on power-up the microprocessor, 1, will find no PROM exists at 8000 Hex because the switch, 23 has disabled the EPROM containing that address by not permitting the read pin 20 to be pulled low. Under these conditions the processor goes into command mode and will interact with external instruction input through the serial RS232 port. In this command mode it is possible to move programmes, modify them, to test them and to permanently commit them to EPROM as outlined above.

Claims (Filed on 28 April 1982)

1. A system comprising, volatile read-write memory, mono-volatile normally read-only memory, circuit means for writing to and programming the non-volatile memory, switching means to enable the aforesaid circuit means, a processor, means to execute a programme of instructions stored in memory, means to communicate to an external terminal, means to provide a resident control mode, means to provide a command mode interactive with the external terminal and means on power-up to determine

whether the control mode or the command mode is entered.

2. What is claimed in 1 where the means to execute a programme of instructions is a high level language interpreter.

3. What is claimed in 2 where the high level language is BASIC.

4. What is claimed in 1 and 2, where the high level language interpreter is stored in the processor.

5. What is claimed in 1 where the switching means enabling the circuit means for writing to and programming the non-volatile memory comprises a means responsive to a two-state logic voltage level.

6. What is claimed in 5 where the two state logic voltage level is generated by a mechanical switch.

7. What is claimed in 1 where the circuit means for writing to and programming the non-volatile memory comprises a monostable.

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