Office de la Propriété Intellectuelle du Canada
Un organisme d'Industrie Canada

Canadian Intellectual Property Office
An agency of Industry Canada

CA 2388792 A1 2003/11/30

(21) 2 388 792

(12) DEMANDE DE BREVET CANADIEN
CANADIAN PATENT APPLICATION

(13) A1

(22) Date de dépôt/Filing Date: 2002/05/31

(41) Mise à la disp. pub./Open to Public Insp.: 2003/11/30

(51) Cl.Int.^{7}/Int.Cl.^{7} H04L 29/02, H04L 12/56

(71) Demandeur/Applicant:
CATENA NETWORKS CANADA INC., CA

(72) Inventeurs/Inventors:
ETEMADI, REZA, CA;
FEELEY, MARK, CA;
GAZIER, MIKE, CA;
MAGNUSSON, MIKE, CA;
NEUDORF, KEN, CA

(74) Agent: OGILVY RENAULT

(54) Titre : SYSTEME ET METHODE AMELIORES POUR LE TRANSPORT DE SERVICES MULTIPLES DANS UN FOND DE PANIER

(54) Title: AN IMPROVED SYSTEM AND METHOD FOR TRANSPORTING MULTIPLE SERVICES OVER A BACKPLANE

AN IMPROVED SYSTEM AND METHOD FOR TRANSPORTING MULTIPLE SERVICES OVER A BACKPLANE

BACKGROUND OF INVENTION

ATM has been used in many applications for carrying multiple services. ATM can be used to carry data, voice and video streams.
One method of reducing the number of system interfaces (physical buses and/or data links) within a system is to use only one protocol (ATM) for data transfer within the system.
This requires that all data flows that are not already in ATM format must be encapsulated into ATM format before transfer over the system interfaces. It also requires that flows must be recovered from ATM format before being processed in their native format.
This patent deals with efficient methods of transferring, and cross-connecting, TDM voice flows over a system, or multiple systems, that internally use only ATM interconnection interfaces.

This type of implementation also applies to all other methods of packetization of the TDM flows (ie in place of ATM mentioned above)

DETAILED TECHNICAL BACKGROUND:

- **What is a BLC**

Is this already described in another of our patents?
Broadband Loop Carrier

- **What is RDT**

An RDT is Remote Digital Terminal. An RDT is an intelligent network element that interfaces between customer access lines and DS1 rate facilities.

- **What is HDT and RT**

An HDT is Host Digital Terminal and an RT is Remote Terminal. An HDT subtends one or more RTs and the combination of the HDT and RT(s) is also an RDT. The HDT terminates interfaces to the DS1 rate facilities which interface to the PSTN while aggregating the traffic from one or more RTs. The RT connects to the customer loops and aggregates the analog signals by multiplexing them into a digital transport facility which could support but is not limited to a TDM, ATM or IP bearer path.

- **What is a TSI**

A TSI is a Timeslot Interchanger. A TSI provides the ability to cross connect a DS0 from one TDM stream to a DS0 of another TDM stream.

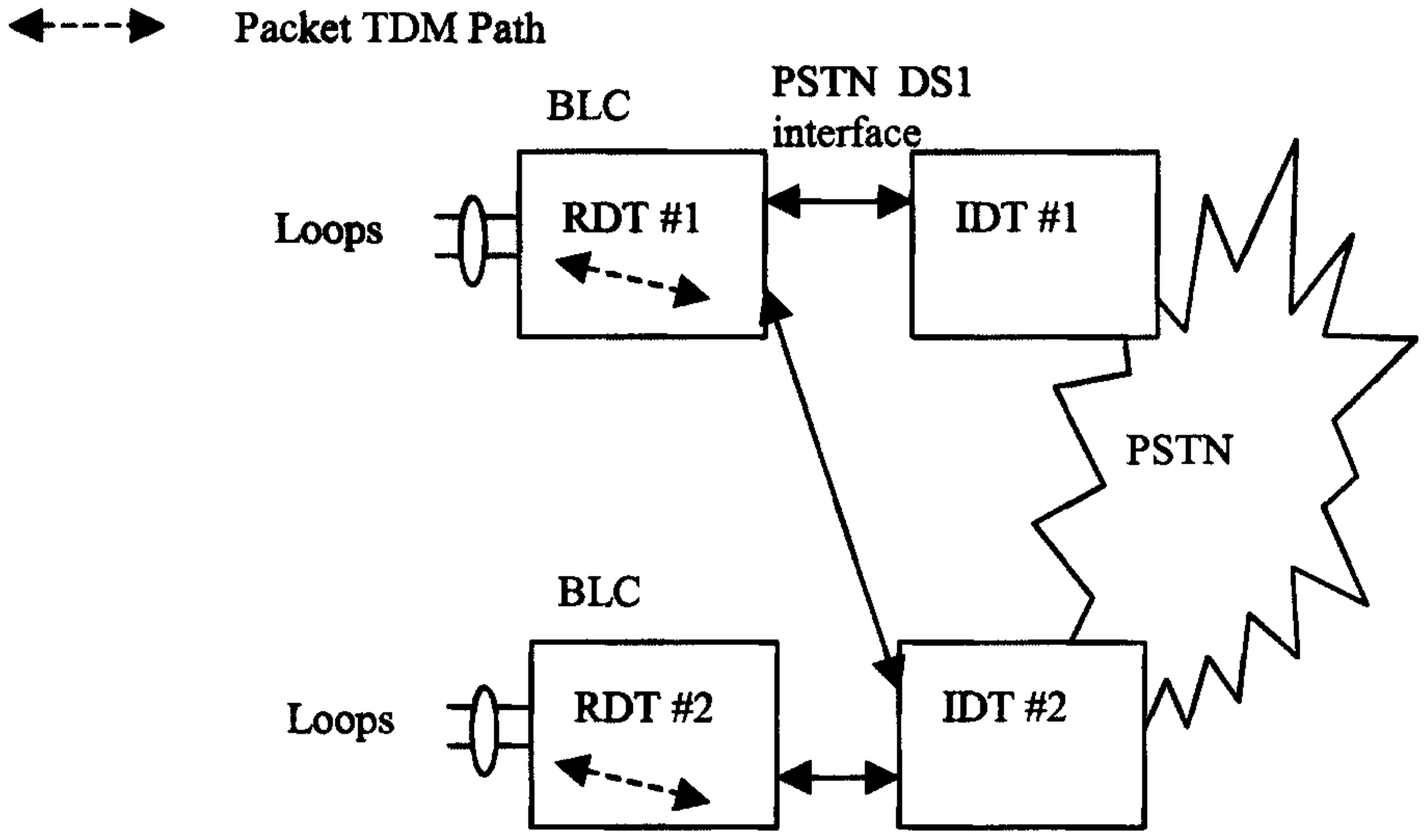

Figure 1: Integrated BLC or Digital Loop Carrier in a Traditional TDM Network

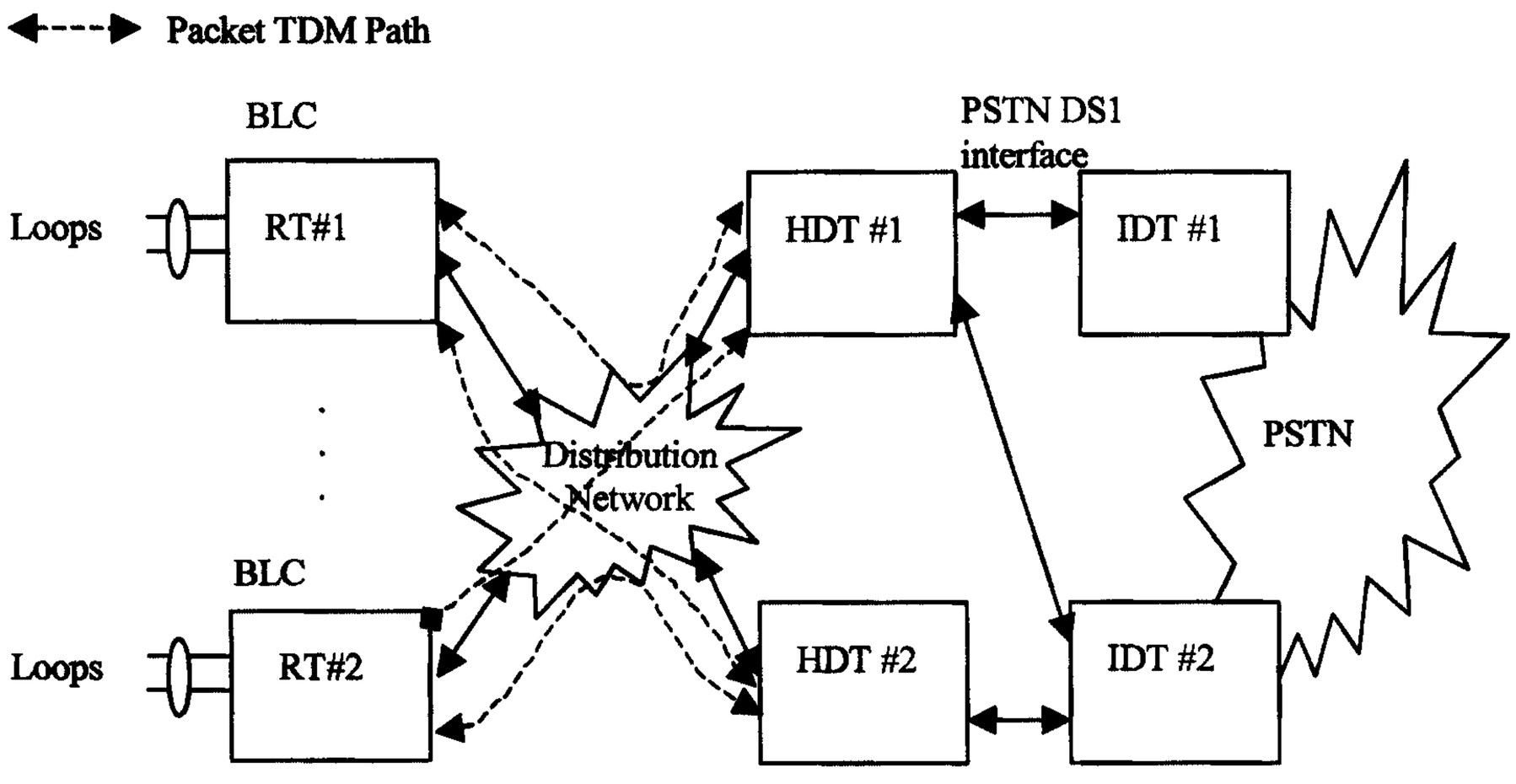

Figure 2: Distributed RDTs

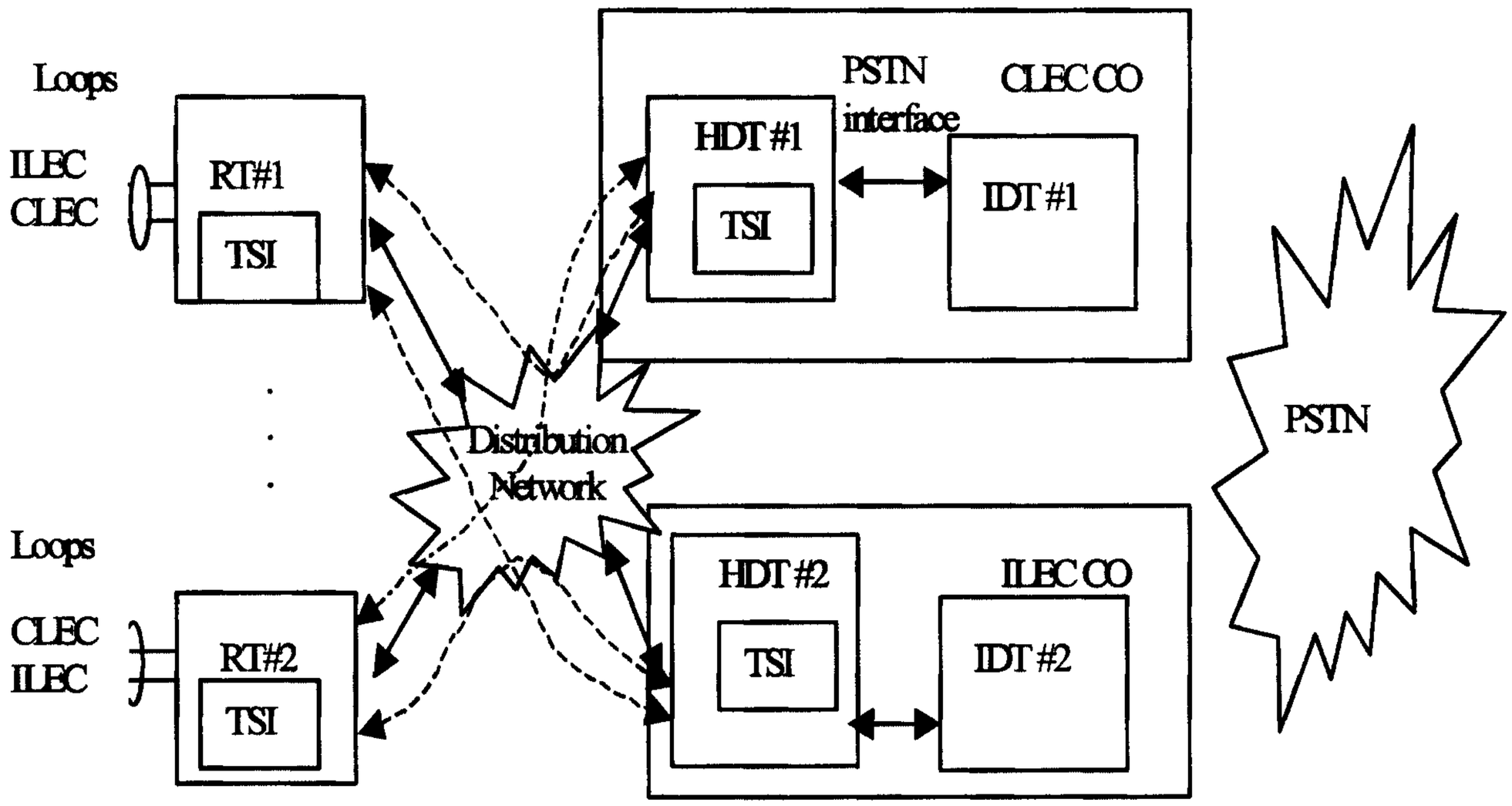

Figure 3 TSI's may be located in a RT or HDT

DETAILED DESCRIPTION OF DS0 CROSS-CONNECT FUNCTION COMBINED WITH PACKETIZED (ATM IN THIS DESCRIPTION) IMPLEMENTATION

1) Catena Network Processor is architectured to support switching TDM voice that is carried over AAL1 and processing data packets. ATM cells are identified based on VPI/VCI and either get SARed and passed to packet processing micro-engine or passed to AAL1 dedicated processing micro-engine. AAL1 micro-engine has embedded hardware co-processor that is used by micro-code to buffer DSOs and do DS0 time switch.

2) AAL1 re-assembly and segmentation is done in micro-code. DSO time switch is being done in a DS0 switch co-processor. DS0 bytes are passed from AAL1 cells to DS0 switch coprocessor through special micro-code instruction. DS0 bytes are fetched from DS0 switch co-processor using a special micro-code instruction. Read DS0 bytes are used by micro-code to construct AAL1 cells for all outgoing circuit emulation connection.

3) Catena Network Processor Supports DS0 time switch. It has special micro-code instructions to do DS0 time switch between incoming and outgoing circuit emulation connections. A circuit emulation connection can consists of up to 32 DS0s. DS0s belonging to different circuit emulation connection arrive/leave CNP as AAL1 cells. There are 4 instructions: 2 instructions for writing/reading DS0 data and 2 instructions for reading/writing signaling nibbles.

4) Catena Network Processor uses different techniques to speed-up AAL1 SAR in micro-code. These techniques are described below.

+ Upon arrival of each AAL1 cell, AAL1 hardware pre-processor identifies the cell using VPI/VCI field and fetches a 64-byte context from internal RAM and maps it to context registers which are

accessible from micro-code. The context keeps AAL1 circuit emulation connection's state that is used to do the AAL1 SAR.

+ Special micro-code instructions to do CRC-3 calculation and parity calculation required for AAL1 SAR. These instructions are executed in 1 clock cycle.

+ Cell insertion is not by AAL1 SAR micro-code and to compensate for the lost cells, DS0 time switch will insert DS0s into outgoing circuit emulations.

5) Catena Network Processor uses different techniques to speed up DS0 time switching in hardware and reducing hardware complexity. These techniques are described below.

+ Micro-code passes up to 32 DS0s to DS0 time switch in 1 clock cycle (CNP is running at 80 MHZ). DS0 time switch writes each DS0 to its corresponding FIFO queue. There are two FIFO queues for each DS0 channel. One queue is for data and the other for signaling. Micro-code passes DS0 channel number and frame number to DS0 time switch. DS0 time switch uses DS0 channel number, frame number, and circuit emulation connection number to determine the FIFO queue.

+ When timer expires for a circuit emulation connection, micro-code segmentation routine is called. Micro-code read DS0s for circuit emulation by passing DS0 channel numbers and frame numbers. Up to 32 DS0s can be read in 1 clock cycle.
DS0 time switch uses DS0 channel number, frame number, and outgoing circuit emulation connection number to identify the FIFO queue. It is using a routing table indexed by circuit emulation connection number, and DS0 channel number to find the entry in the routing table which has the FIFO queue number. Frame number is used to determine if the signaling FIFO queue or data FIFO queue should be used.

+ A FIFO queue can be provisioned to support multi-frame alignment. Each entry in the queue is 9 bits. 8 bits are used for data and 1 bit is used to indicate if DS0 belongs to the first frame of a super frame. This is bit set when DS0 is written to the queue and frame number for DS0 is 1. During read, if micro-code asks for a DS0 which does not belong to frame 1 and the next read entry in the FIFO is a DS0 which does not belong to frame 1, then DS0 time switch will return conditional data and no read will be done on FIFO. Conditional data is returned until micro-code asks for a DS0 for frame 1. If the next read entry in the FIFO is not a DS0 for frame 1, micro-code will be able to read DS0 from queue regardless of the frame number.

+ DS0 time switch will detect under-run in a queue when there is no DS0s in the FIFO. After detecting under-run, FIFO is being reset and conditional data is returned during read until there are CDV number of DS0s in the FIFO queue.

+ DS0 time switch detects if more than 6 AAL1 cells are lost on a circuit emulation, and set a flag to indicate to micro-code to re-synchronize on the next super frame.

6) AAL1 cell construction is done in micro-code and is triggered by DS0 switch co-processor.
Each circuit emulation connection has a programmable timer. DS0 switch co-processor makes a callback to the micro-code when timer expires. Micro-code reads DS0s for the circuit emulation and will send the AAL1 cell out.

7) The CNP architecture is flexible to change front-end micro-code from AAL1 to other protocols (e.g., AAL2, IP).
This can happen when back end DS0 time switch remains the same.

DESCRIPTION OF SYSTEM LEVEL IDEAS LEADING TO CLAIMS:

1. The use of packet based encapsulation for transport of TDM information streams.
   - streams may contain, data, voice, signaling etc
   - used internal to a standalone telecommunication system or between distributed nodes in a telecommunications system
     - narrow claim down to a BLC system if required
   - packet encapsulation methods may be
     - ATM AAL0, AAL2 or AAL5
     - As above but with pwe3 (MPLS) TDM encapsulation
     - As above but with 802.3xx (Ethernet) TDM encapsulation
     - As above but with xxx (IP) TDM encapsulation
     - as above but with other encapsulations…. Does this need to be elaborated?

   A specific example that we are claiming is voice and associated signaling encapsulated in ATM AAL0 or AAL1 between access cards (POTs line card, DS1 card, or other) and a network connected card. This applies to both a standalone BLC system or a distributed BLC RDT and HDT system.

2. The TDM voice being packetized into a format (ATM as one example) allows a single backplane transport technology to be used to transmit both data (such as ATM cells being transmitted on an xDSL connection connected to the same line card) and the TDM voice on a single physical media. This allows high integration and low system cost particularly compared to an implementation that has separate TDM and ATM backplane/transport as has previously been implemented especially within one system.

3. Use of multiple TDM streams, with packet encapsulation, per source in order to avoid a common DS0 cross-connect/switch function
   - ie a Line card can use two or more packet streams, one towards a distant network termination point (possibly an HDT, or multiple HDTs) and one towards a local system termination point (possibly a DS1 interface card)

4. The combination of a device which provides;
   - Termination/origination of packet encapsulated (could be encapsulated in any ATM standard, or proprietary, adaptation method – eg AAL0, AAL1, AAL2 or AAL5) TDM streams which may carry one or more TDM DS0 streams
   - Cross-connect of the TDM DS0s

   Note the fact there are no integrated chips that can do this means it is either new or new to this app. Most people build tdm based systems

   Same as #4 above but with pwe3 (MPLS) TDM encapsulation
   Same as #4 above but with 802.3xx (Ethernet) TDM encapsulation

Same as #4 above but with xxx (IP) TDM encapsulation
Same as #4 above but with other encapsulations

- this device may have packetized TDM on both sides of the Xconnect or it may have packetized TDM on one side and standard TDM on the other side of the crossconnect

5. Methods of aligning start of multi-frame signals in order to;
   - minimize signaling delays by nearly 1 full multi-frame
   - minimize the number of LSB bits corrupted due to the use of RBS signaling coming into our system and exiting our system (ensure the same frames are used for LSB RBS signaling in the incoming side as on the outgoing side of the system)

- one method of determining the line card upstream multi-frame alignment at the line card is to use a programmable time interval after the start of multi-frame time of the downstream flow

- alignment of the downstream CEM (after Xconnect) start of multi-frame slightly after the multi-frame alignment of CEM, or DS1 signals occuring before the Xconnect

- extension being to use the xDSL 8 kHz marker to get other end (IAD etc) to synch up for perfect MF u/s. Can be done with h/w sych'g or may need messaging to supplement for exact synch'ing.

6. idea of SDT AAL1 with messaging to supplement for FDL between RDT and HDT

7. idea of SDT AAL1 used from LC with separate signaling which (1) avoids any cross connect issues with the RBS / MF and (2) when sent across a network eg rdt-hdt-and even further avoid the rbs issues incured with classical dlc which is why such is important for dlc.

8. idea that with integrated pots + dlc chip (ie. the catena story) the use of aal1 is the ultimate integration and cost reducer, avoiding multiple backplanes with tdm. this claim needs careful work in order to ensure we wrap it up tightly as an extension to our general integration story.

9. same idea as related to use of aal1 from hydra to quarks

10. same idea as related to how we are implementing the onu aal0-aal1-vop cell chain

11. In the line card, prioritize the tdm voice packets with strict priority over all data in order to get absolute lowest possible TDM voice delays