(12) UK Patent Application (19) GB (11) 2586158 (13) A

(43) Date of A Publication 10.02.2021

(21) Application No: 1911357.0

(22) Date of Filing: 08.08.2019

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(51) INT CL:
H01L 29/10 (2006.01) ***H01L 29/423*** (2006.01)
H01L 29/739 (2006.01)

(56) Documents Cited:
WO 2018/034818 A1 **US 20170110562 A**

(58) Field of Search:
INT CL **H01L**
Other: **WPI, EPODOC**

(54) Title of the Invention: **Semiconductor device and method for producing same**
Abstract Title: **Planar trench IGBT cell**

(57) The device comprises a planar gate 10 and a trench gate 11 with their longitudinal directions arranged orthogonally to one another. The emitter electrode contacts a source region 7 formed in a first base region 9. An emitter electrode also contacts a further base region 8 that extends deeper than the source region and is more highly doped than the first base region 9. A lateral channel 15 between the source region and the drift region 4 is formed during device operation. Additionally, a vertical component to the device current is formed during device operation (see fig 14). The device may be configured for punch-through operation.

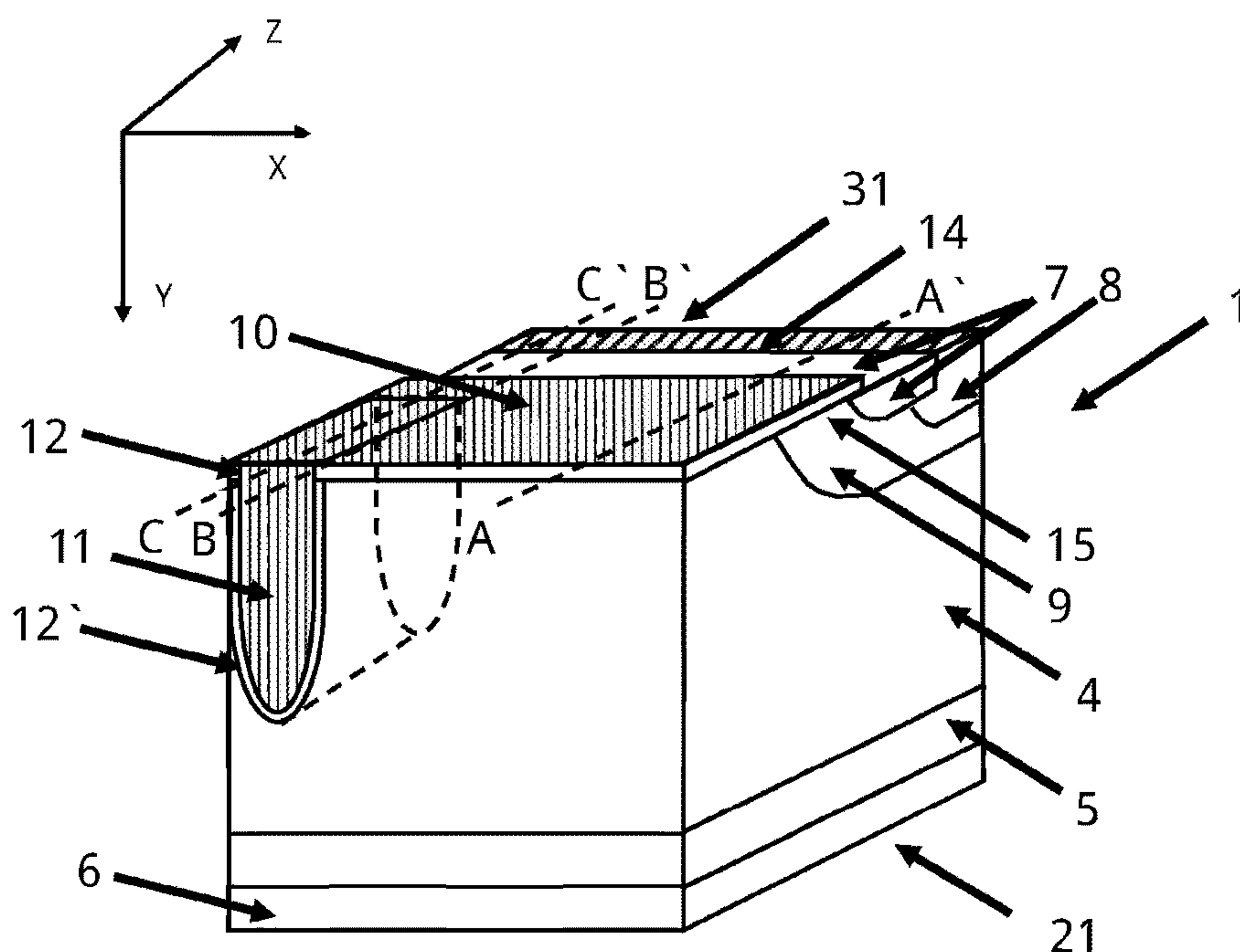

Figure (10) First exemplary embodiment of a punch-through IGBT according to the invention

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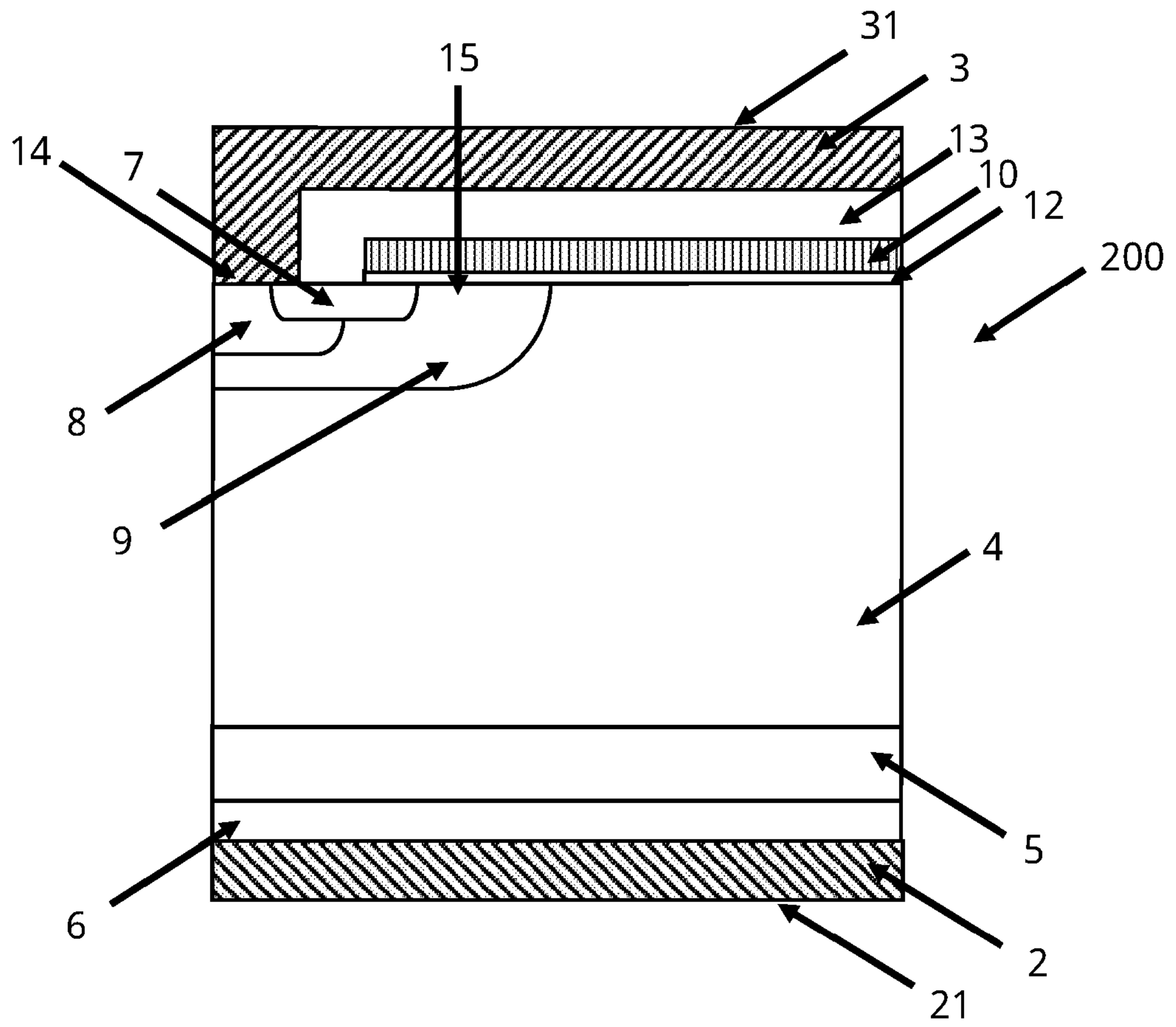

Figure (1A) Planar MOS IGBT structure (prior art).

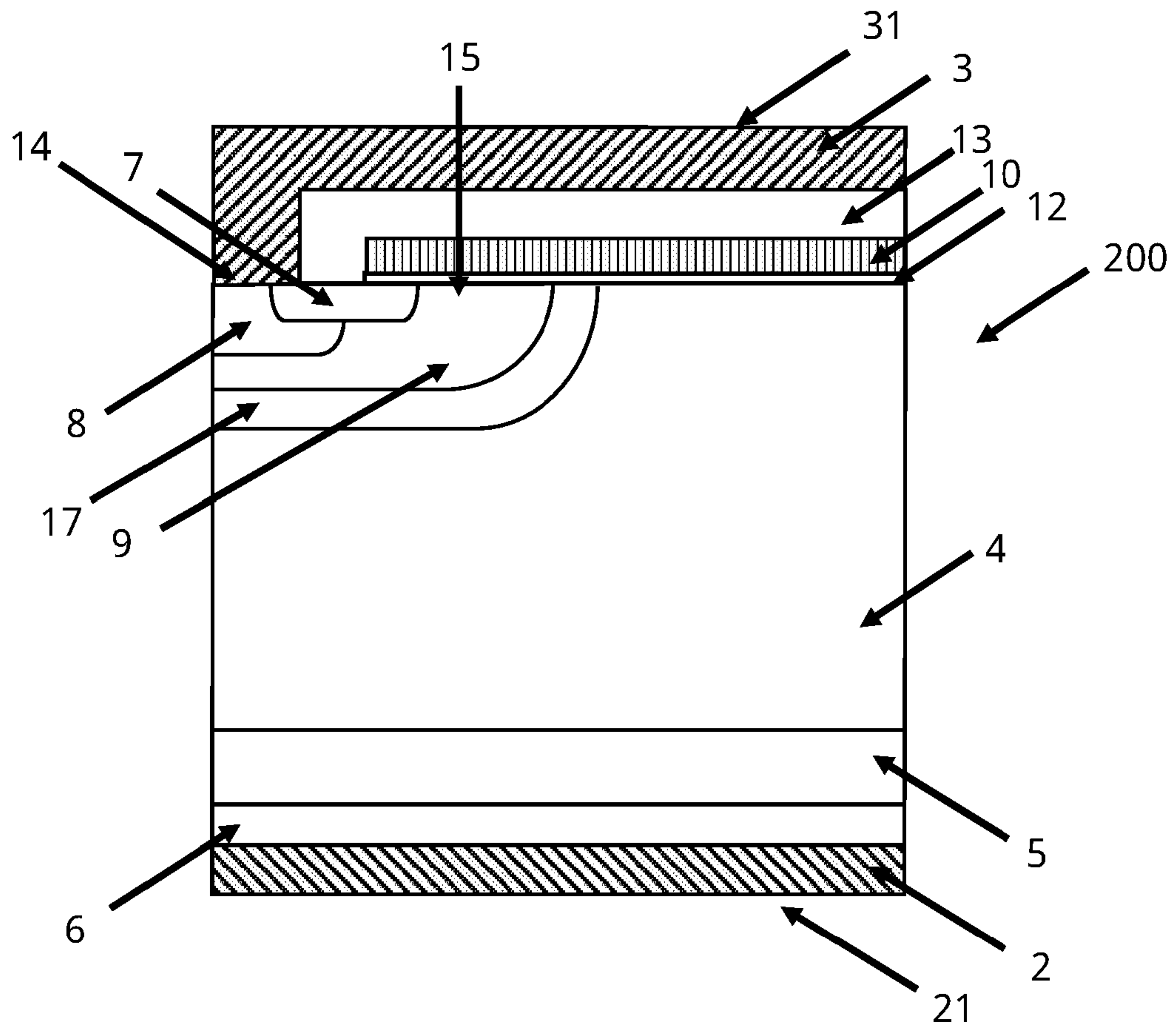

Figure (1B) Enhanced Planar MOS IGBT structure (prior art).

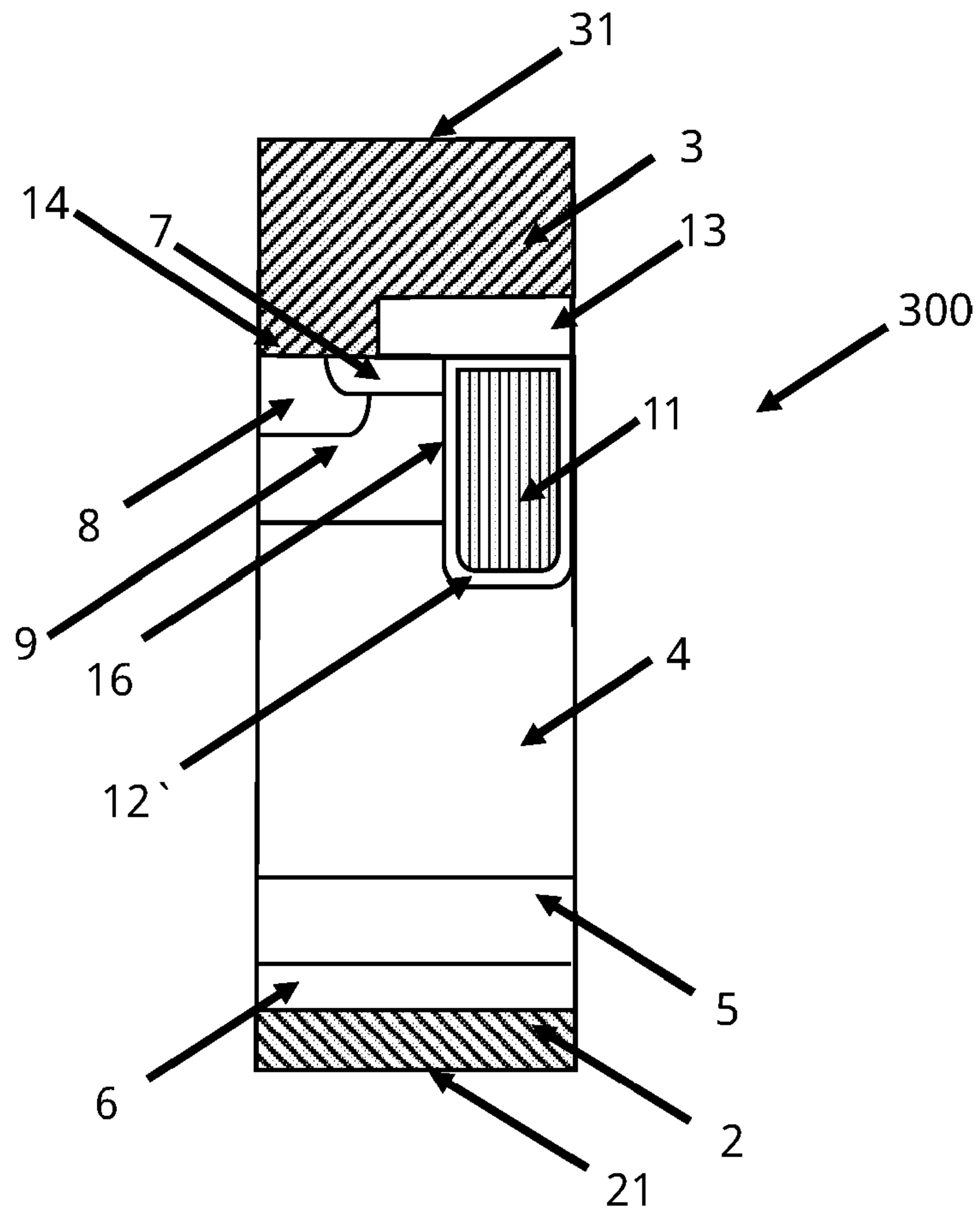

Figure (2A) Trench MOS IGBT structure (prior art).

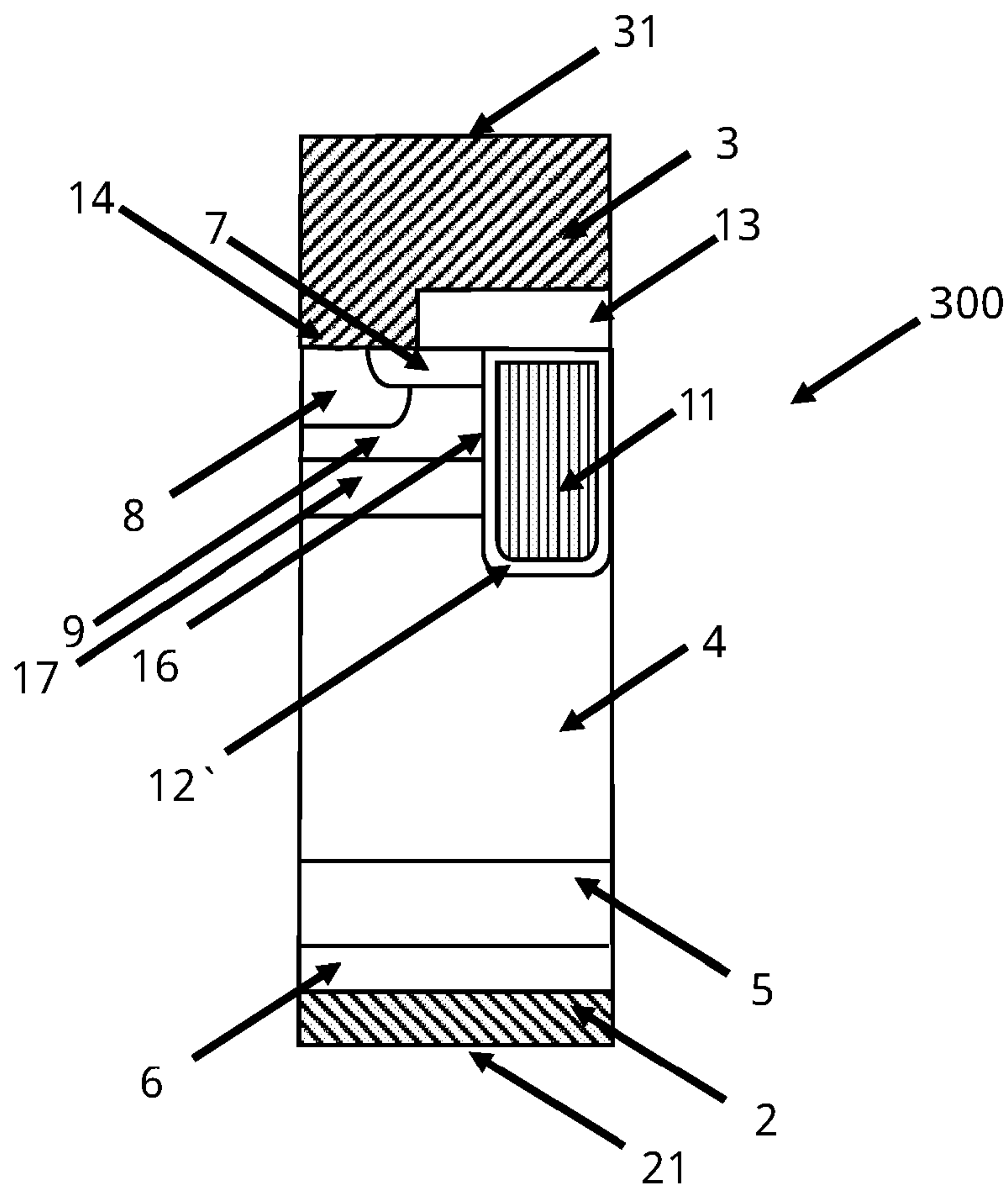

Figure (2B) Enhanced Trench MOS IGBT structure (prior art).

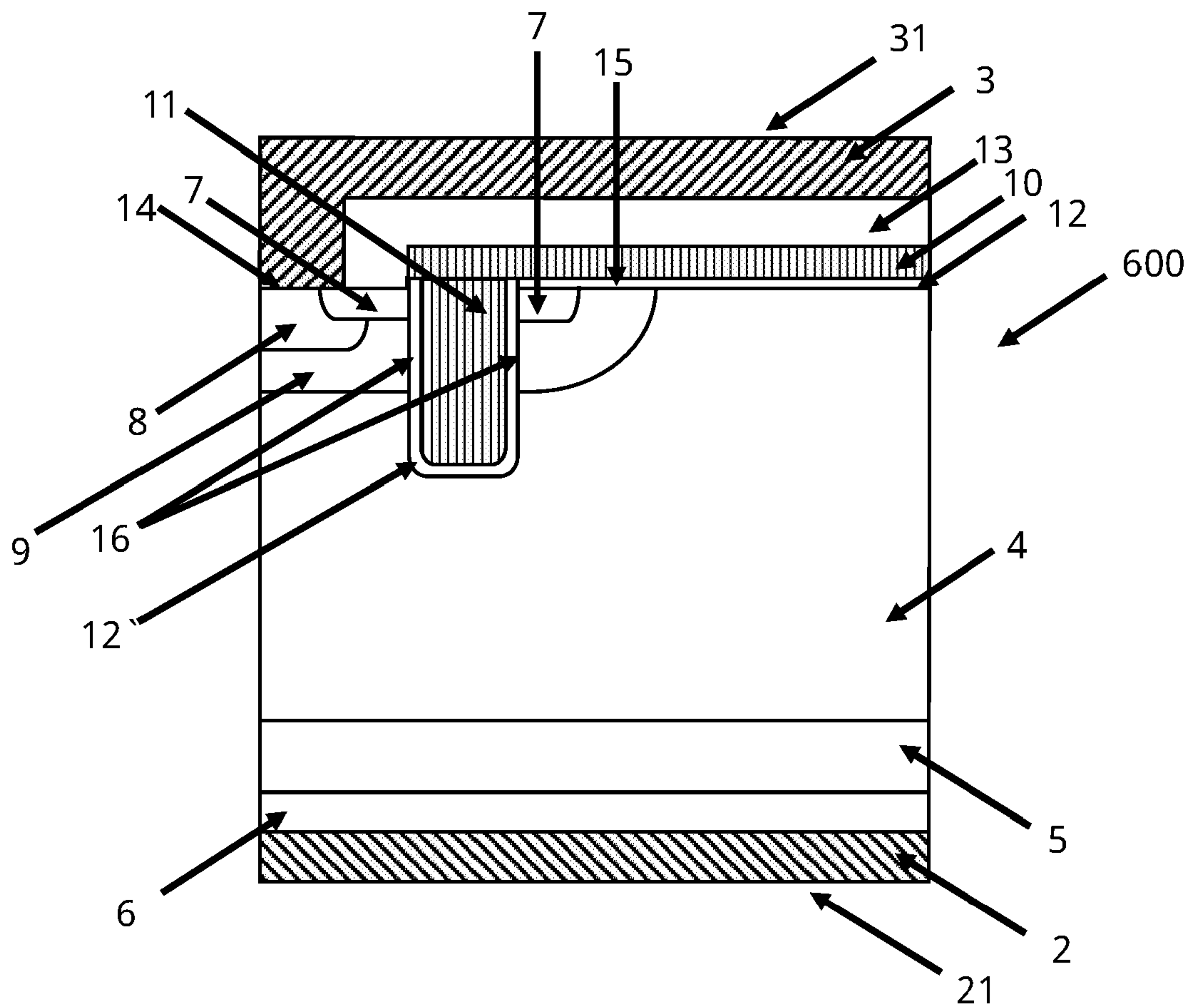

Figure (3) Trench Planar MOS IGBT structure (prior art).

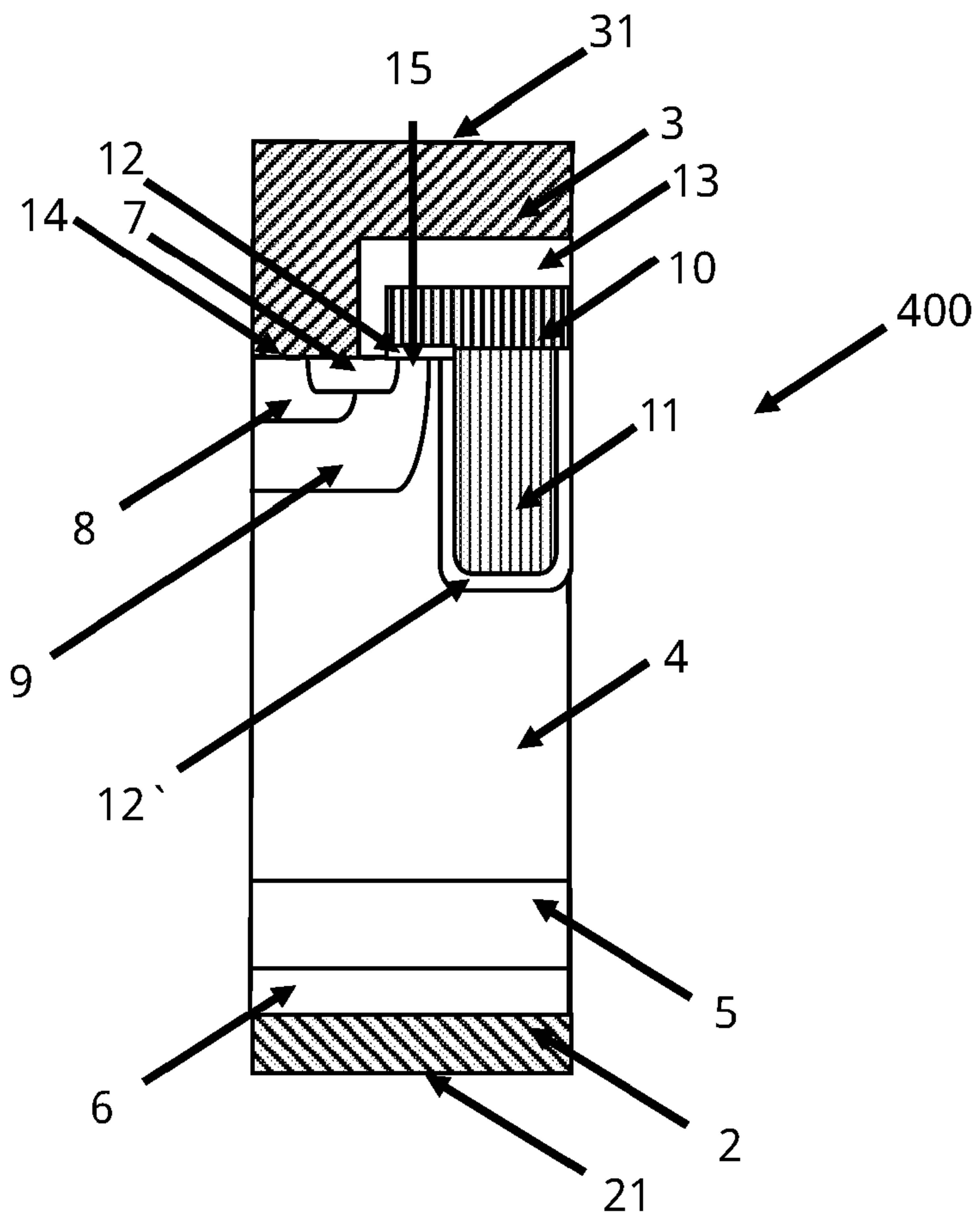

Figure (4A) Trench Planar MOS IGBT structure with Gaussian p-well profile (prior art).

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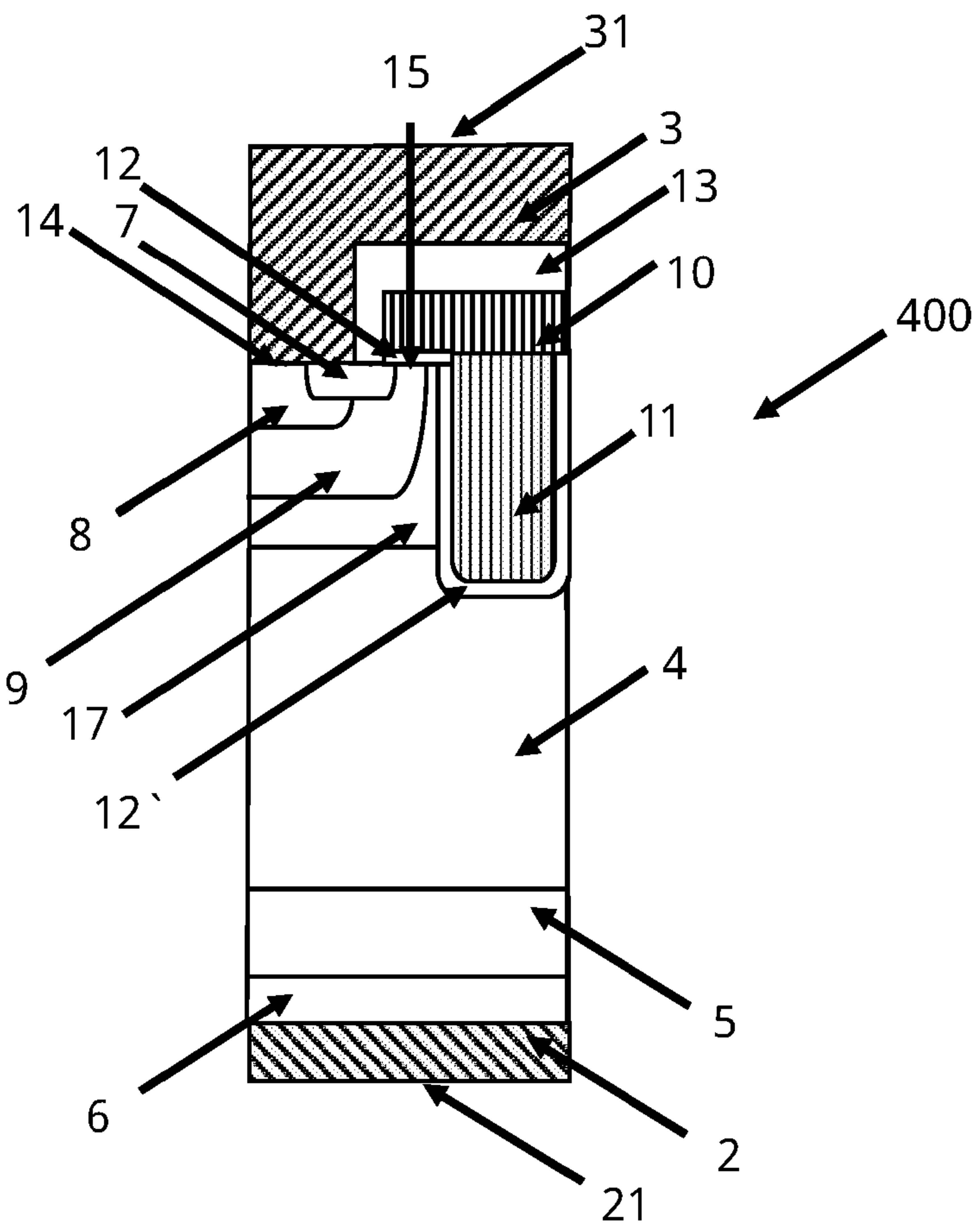

Figure (4B) Trench Planar MOS IGBT structure with Gaussian p-well profile and enhancement layer (prior art).

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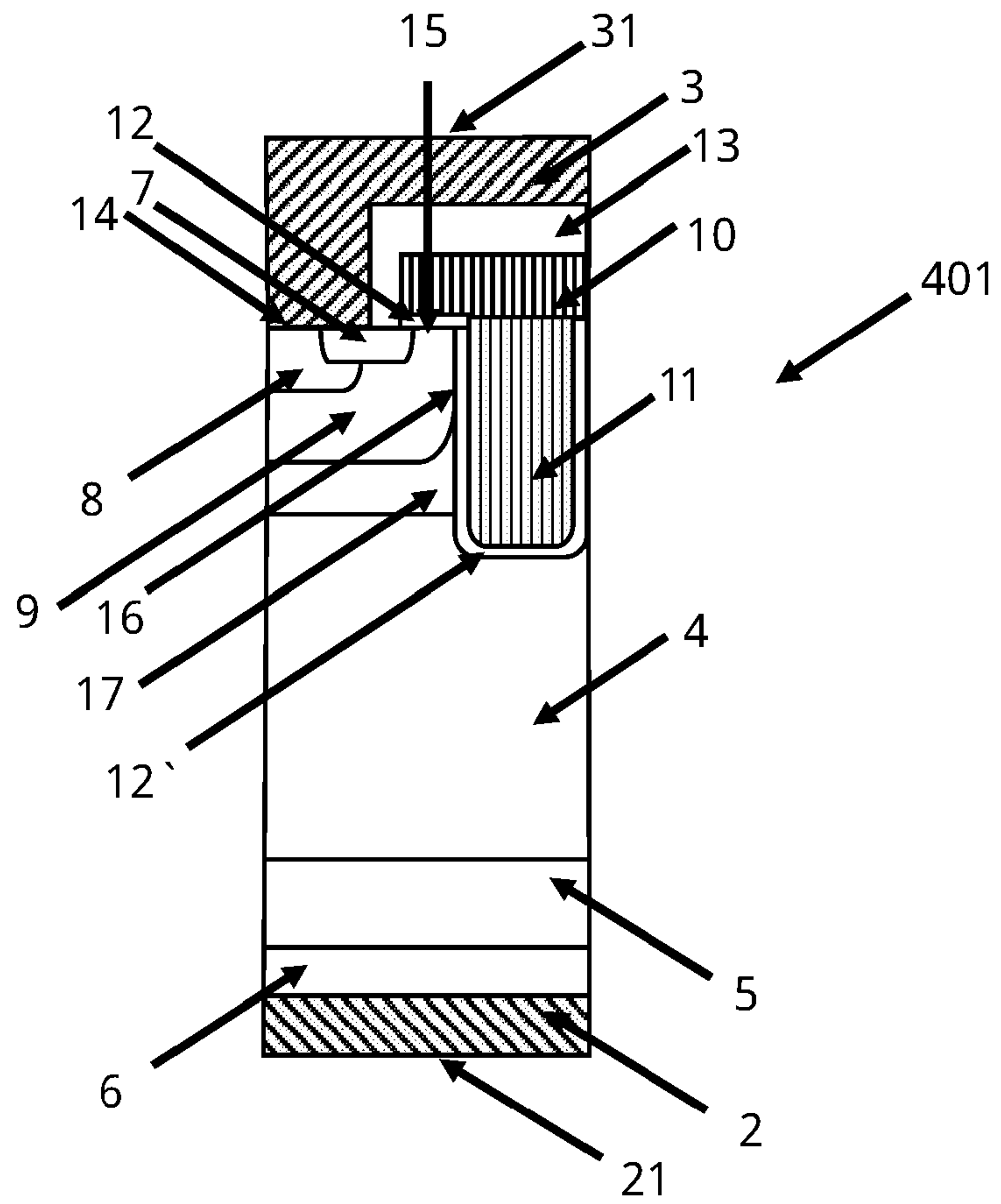

Figure (5A) Trench Planar MOS IGBT structures (prior art) with series connected planar and trench channels.

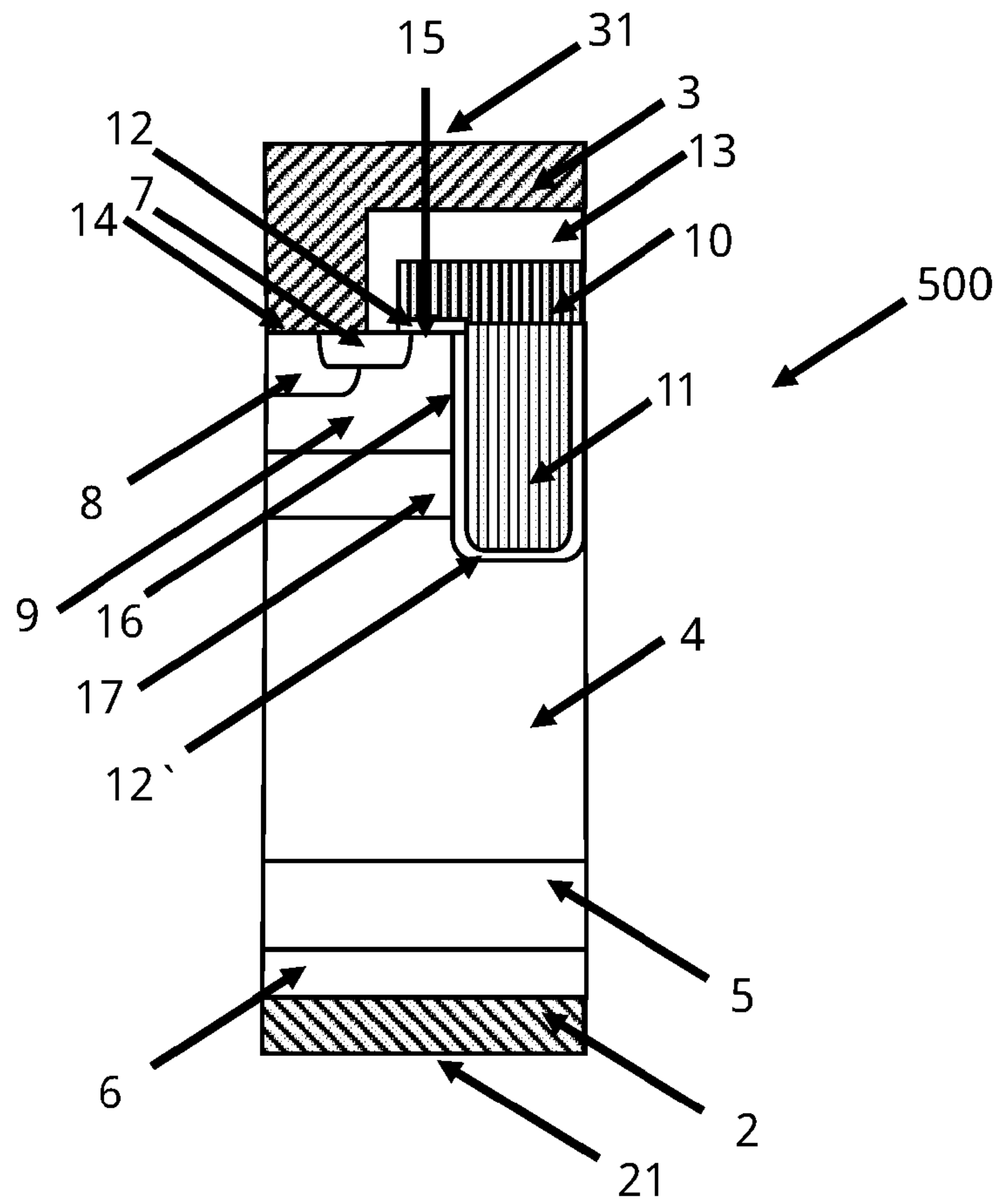

Figure (5B) Trench Planar MOS IGBT structures (prior art) with series connected planar and trench channels

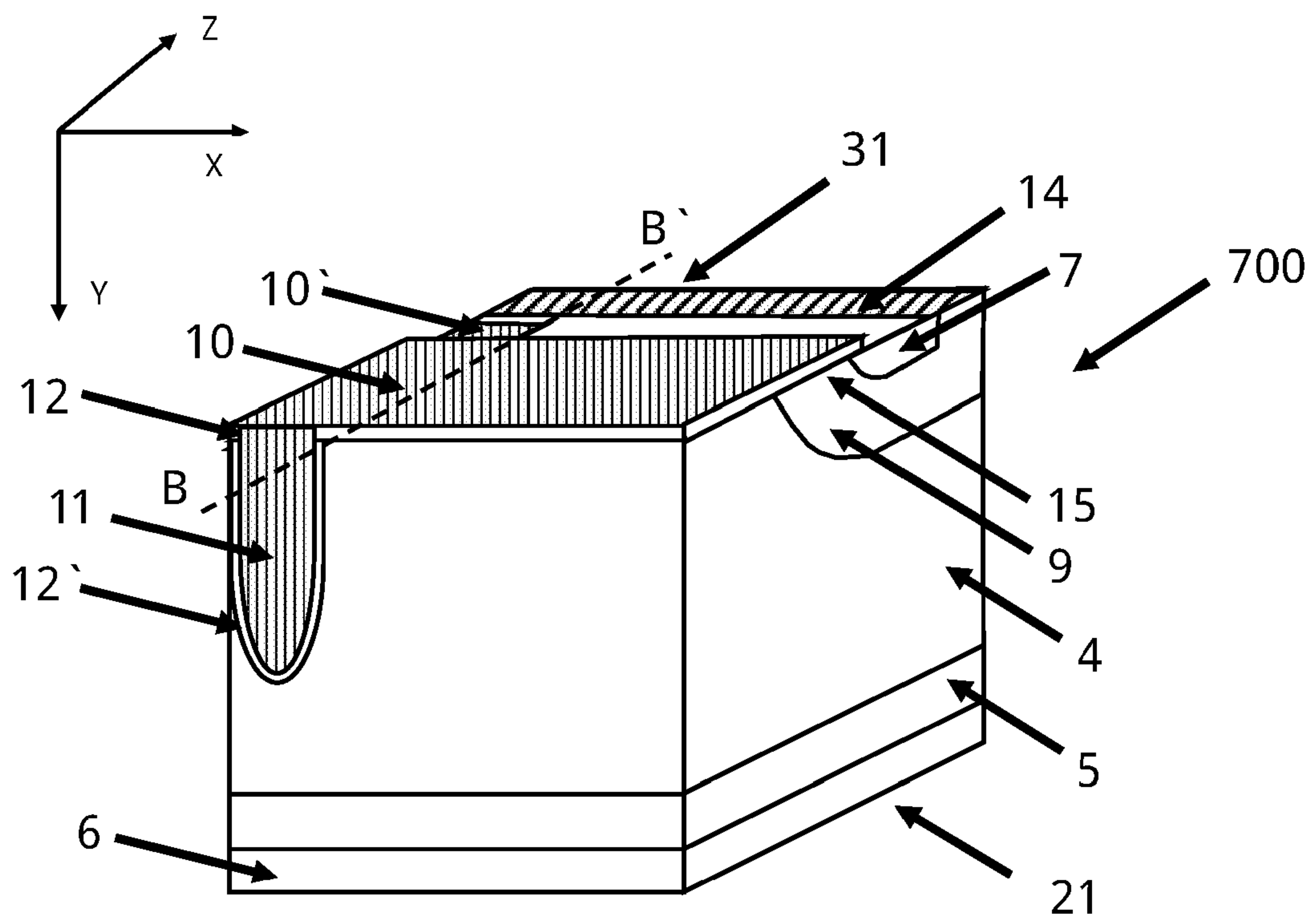

Figure (6) Three-dimensional illustration of Trench MOS cell structure with planar channel orthogonal to the trench regions (prior art).

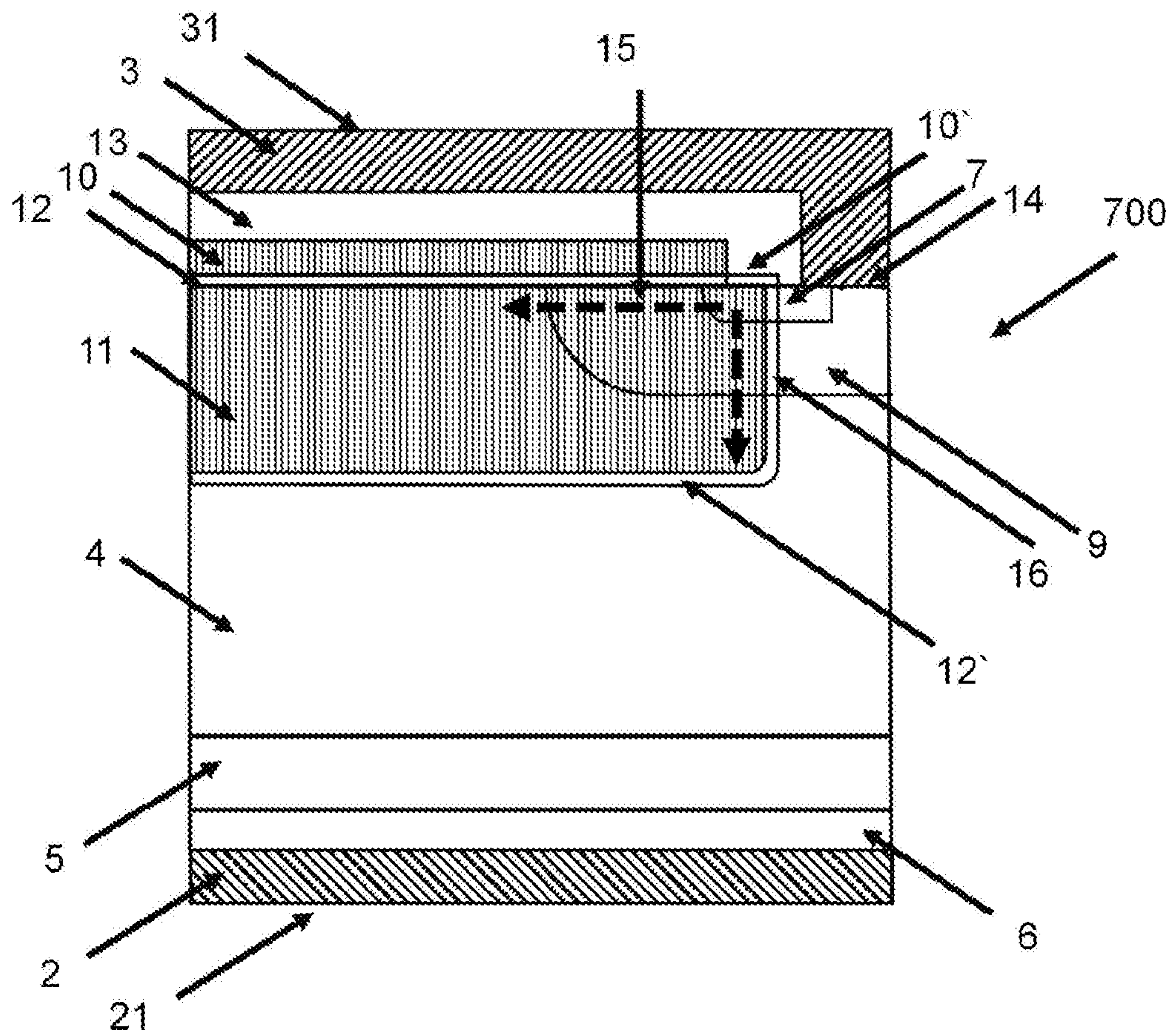

Figure (7) Cross section along B-B` of Trench MOS cell structure in FIG. (6) with planar channel orthogonal to the trench regions showing both planar and vertical MOS channels are formed (prior art).

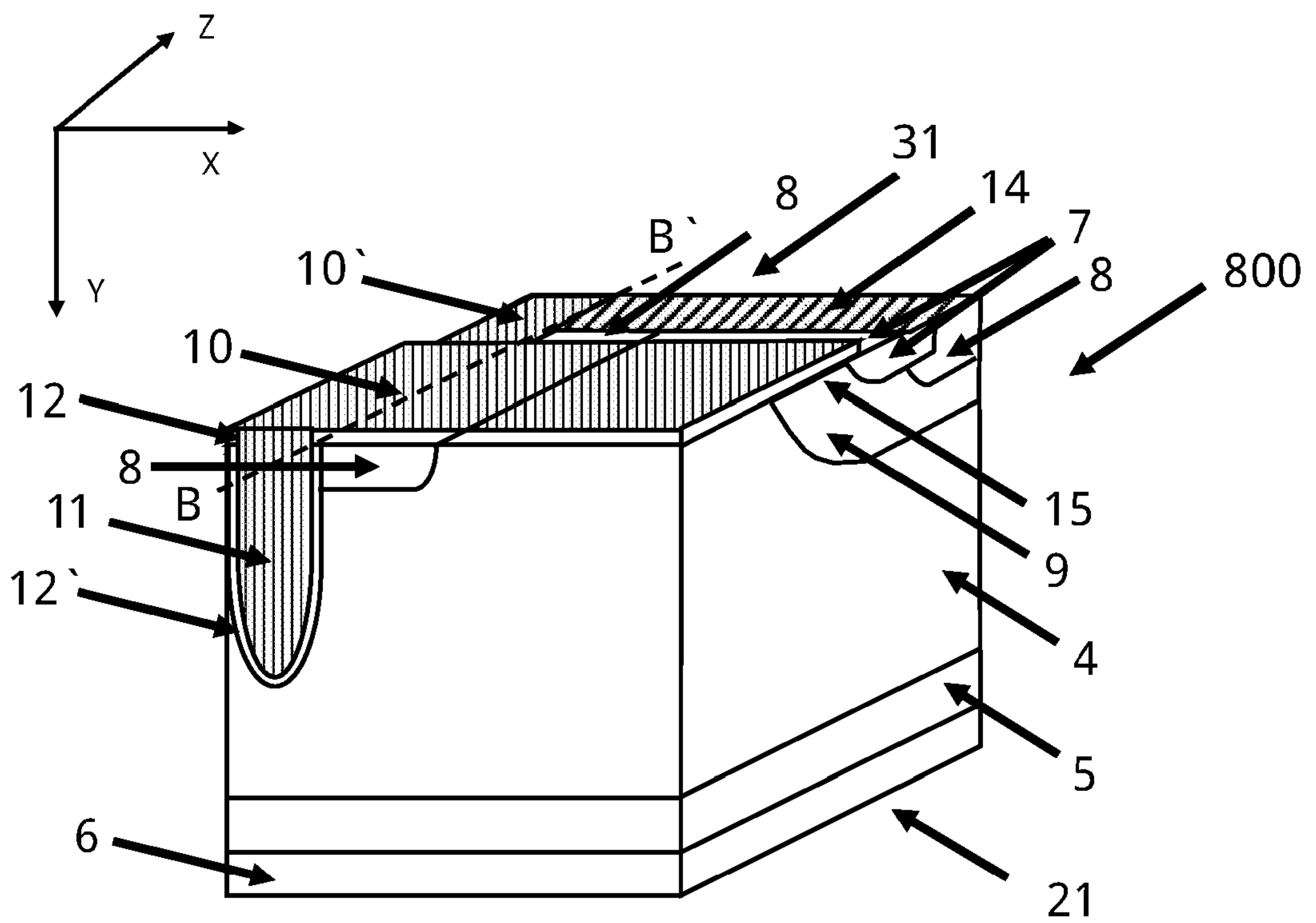

Figure (8) Three-dimensional illustration of Planar MOS cell structure with planar
5 channel orthogonal to the trench regions (prior art).

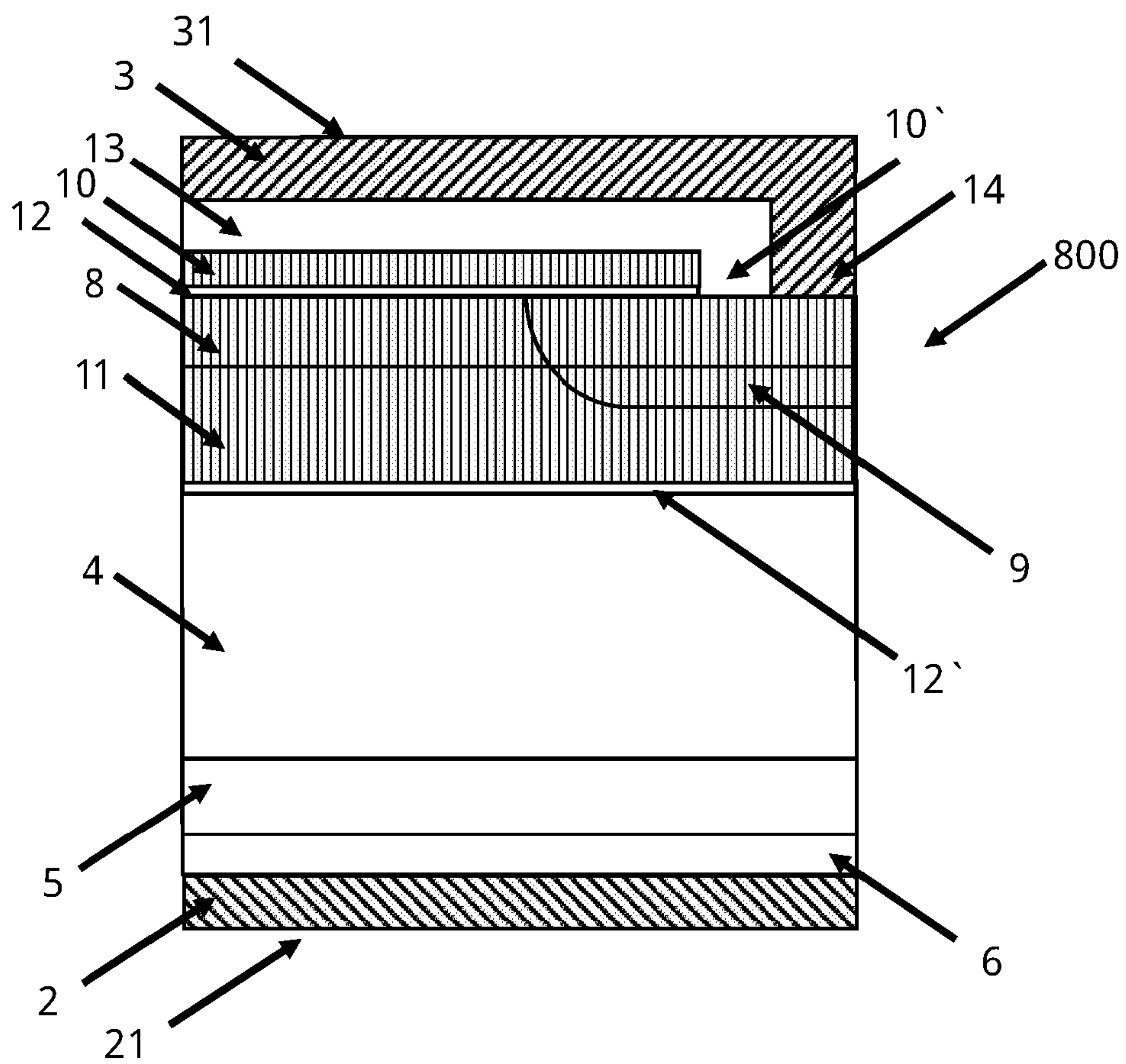

Figure (9) Cross section along B-B`of Planar MOS cell structure in FIG. (8) (prior art).

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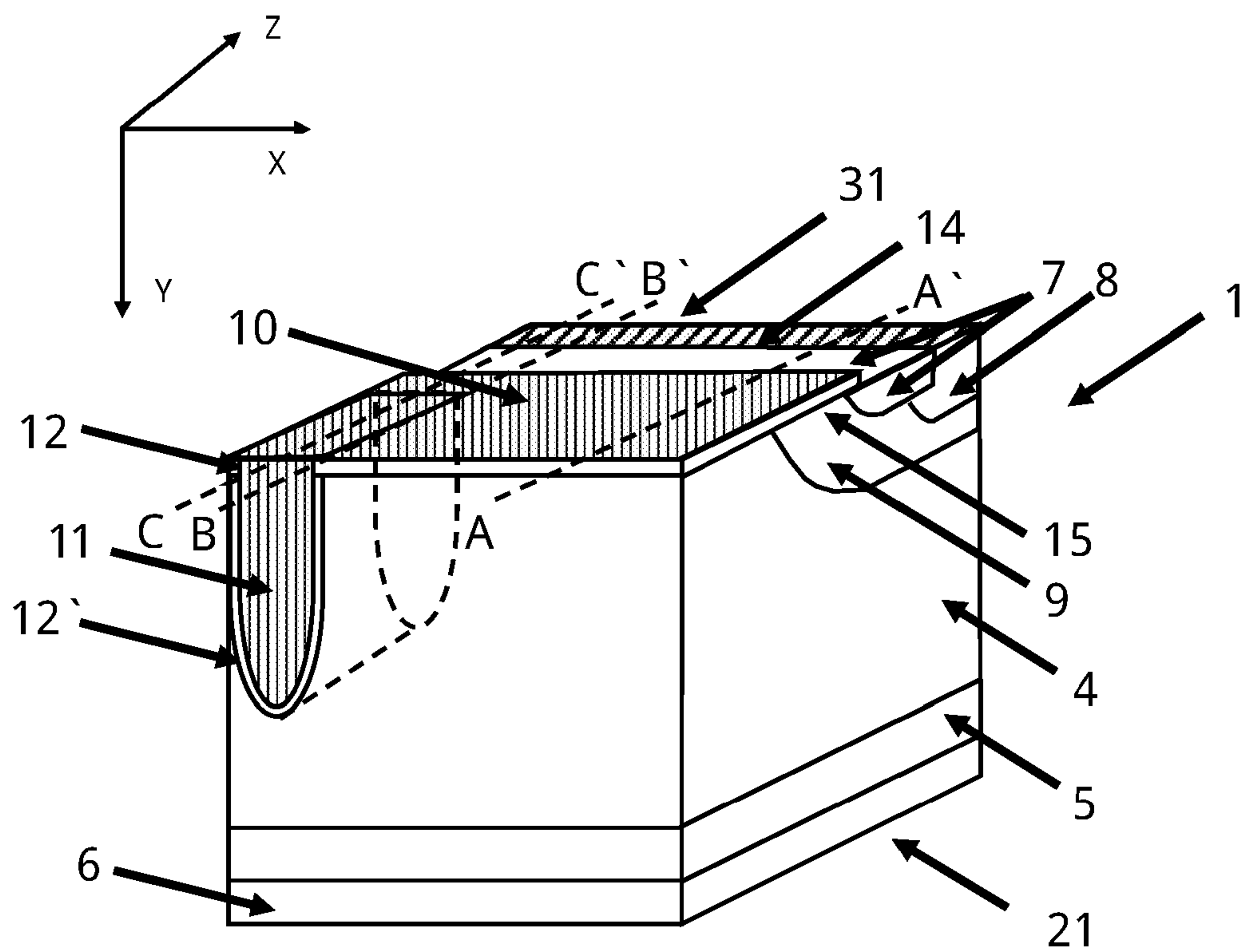

5 Figure (10) First exemplary embodiment of a punch-through IGBT according to the invention

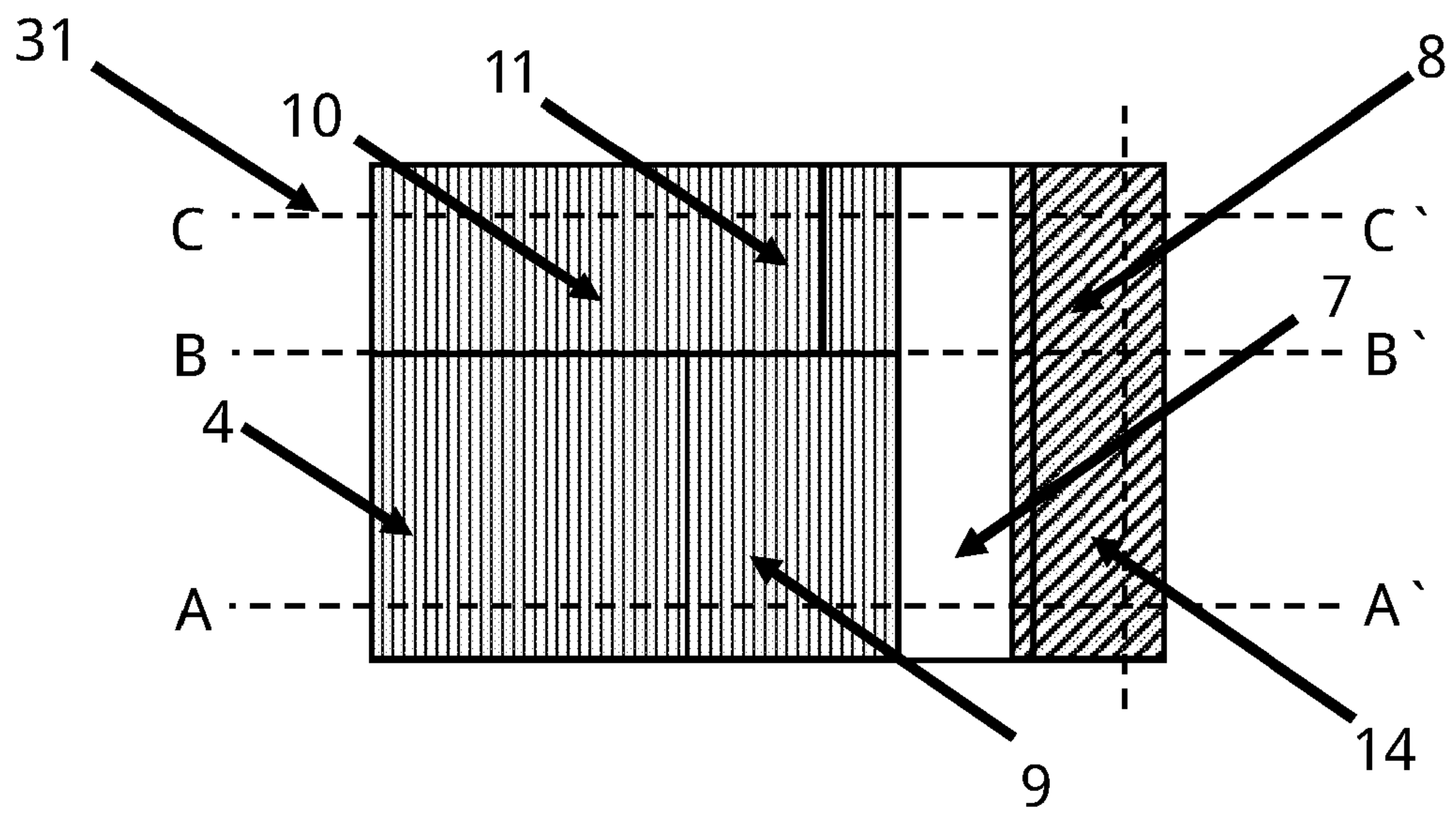

Figure (11) Top view of first exemplary embodiment of a punch-through IGBT according to the invention

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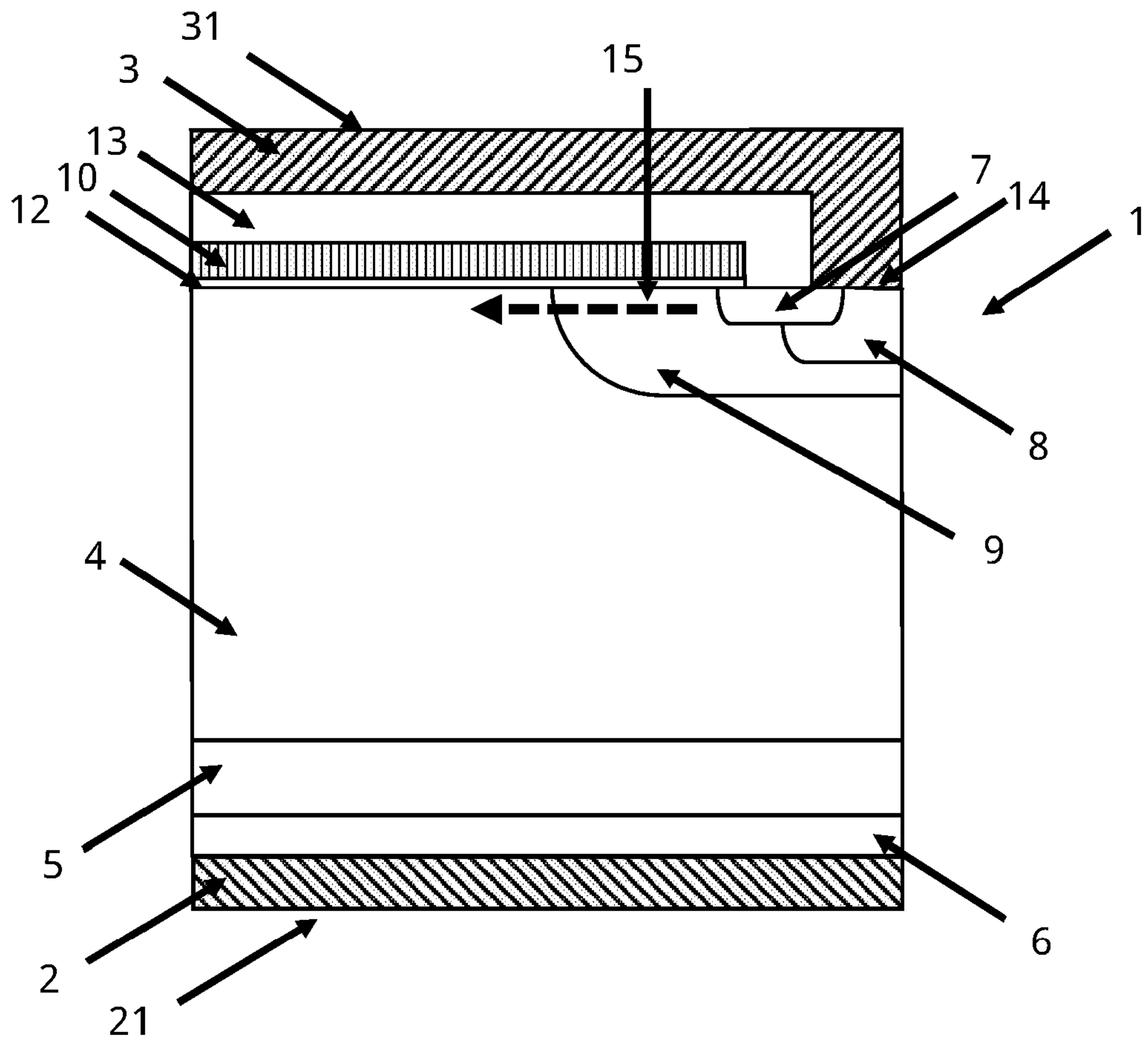

Figure (12) Cross section along A-A` of first exemplary embodiment of a punch-through IGBT according to the invention showing the planar MOS channel.

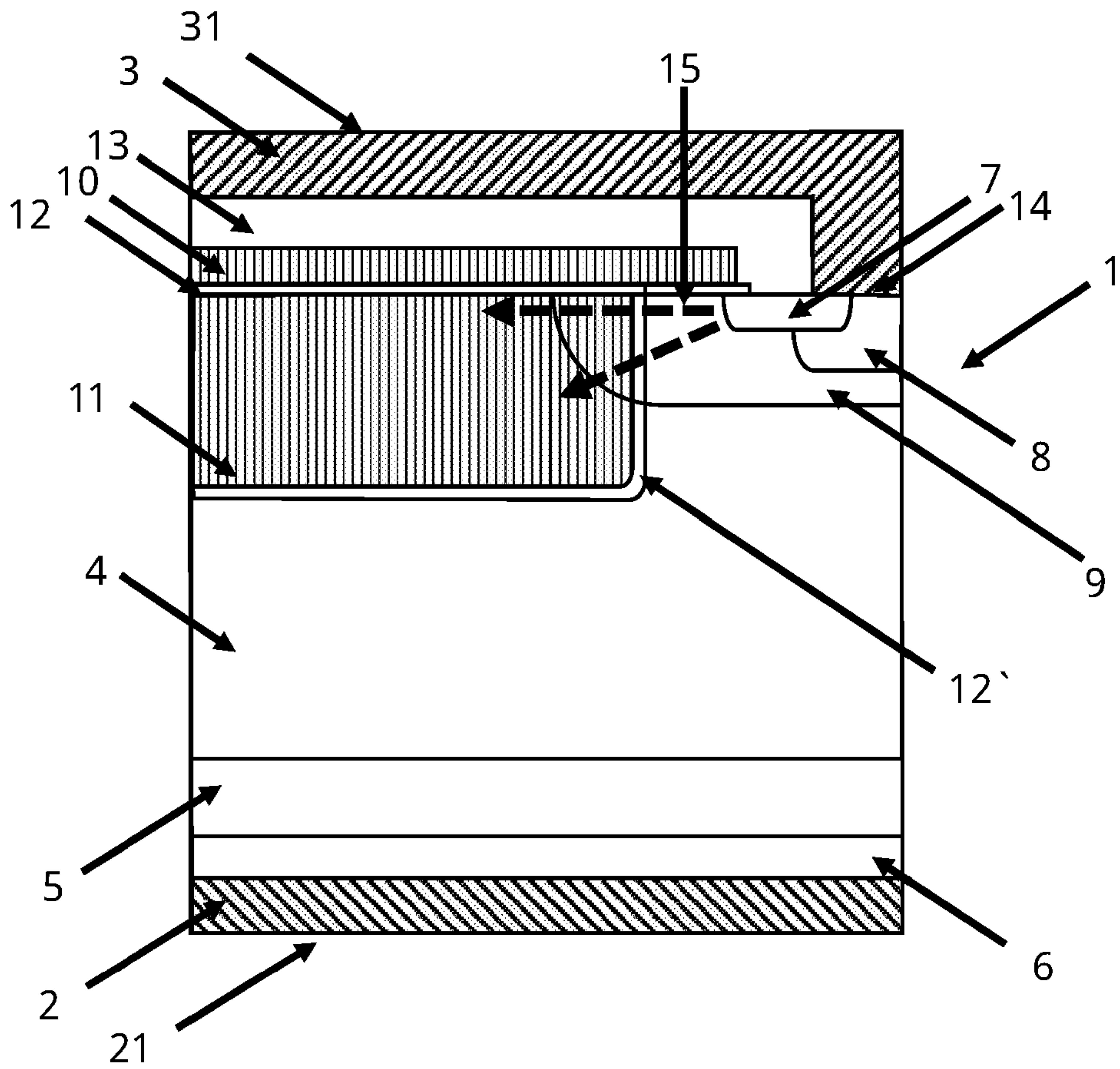

Figure (13) Cross section along B-B` of first exemplary embodiment of a punch-through IGBT according to the invention

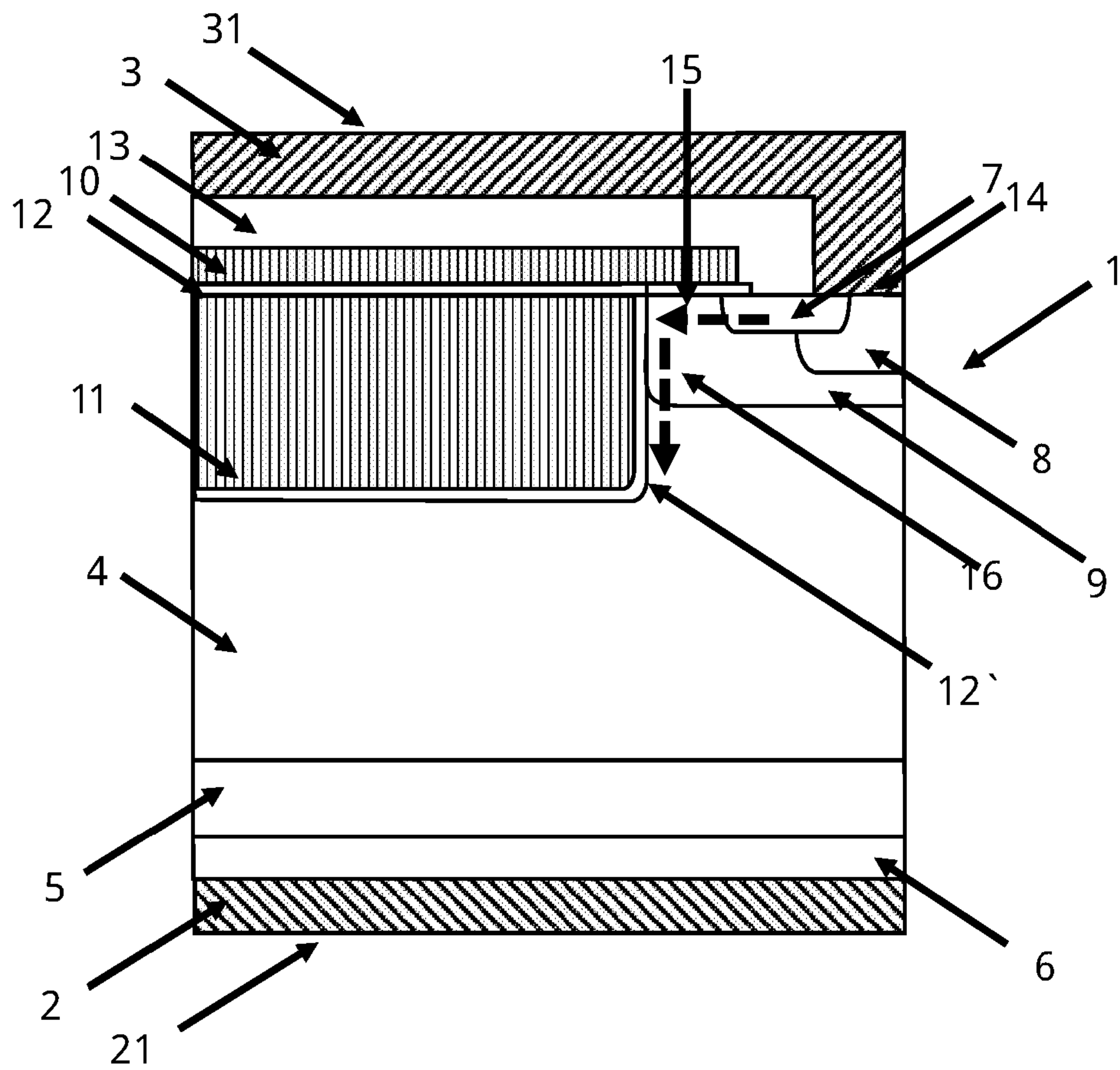

Figure (14) Cross section along C-C` of first exemplary embodiment of a punch-through IGBT according to the invention, showing series connected planar and trench channels

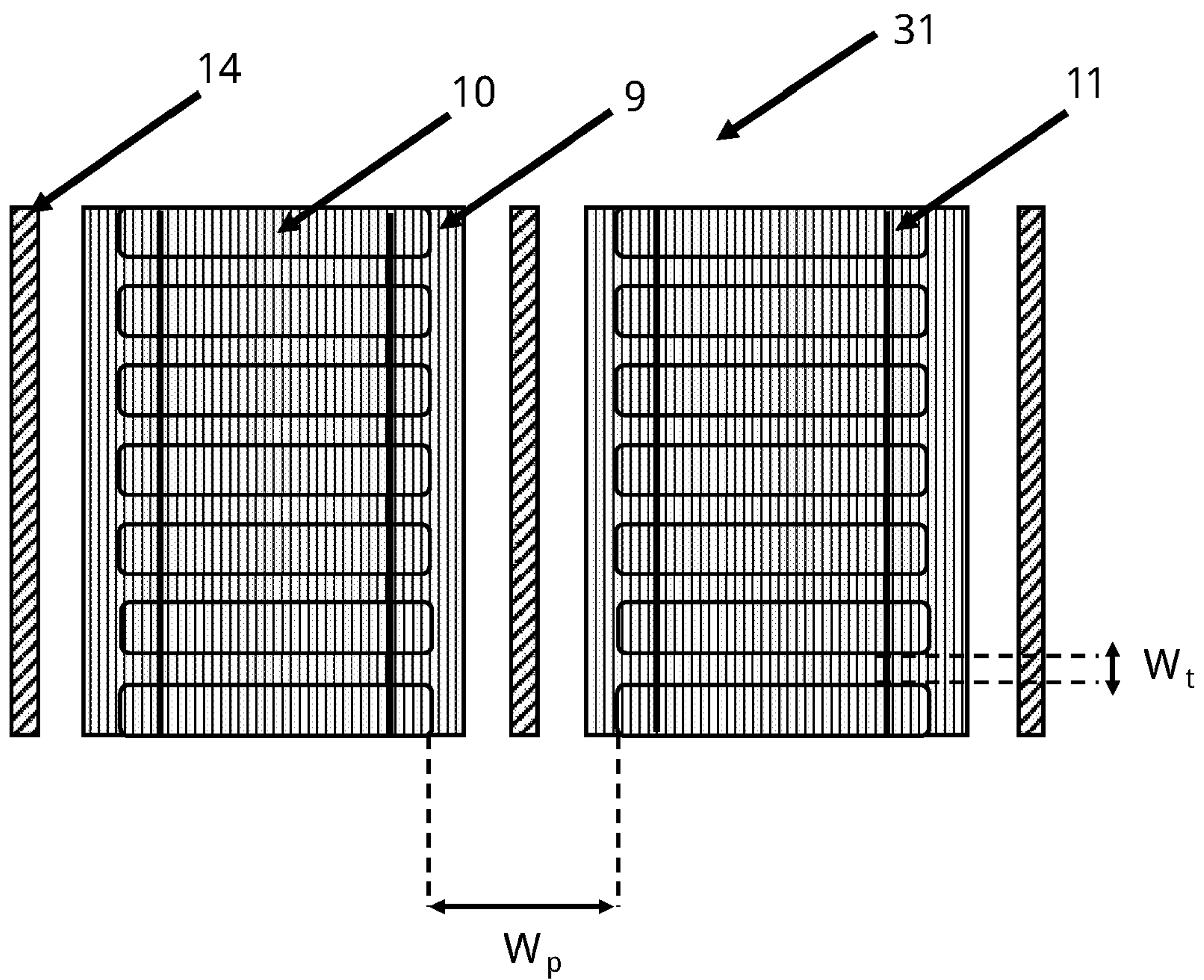

Figure (15A) A typical top view for a stripe design of first exemplary embodiment of a punch-through IGBT according to the invention with all trenches having the same length

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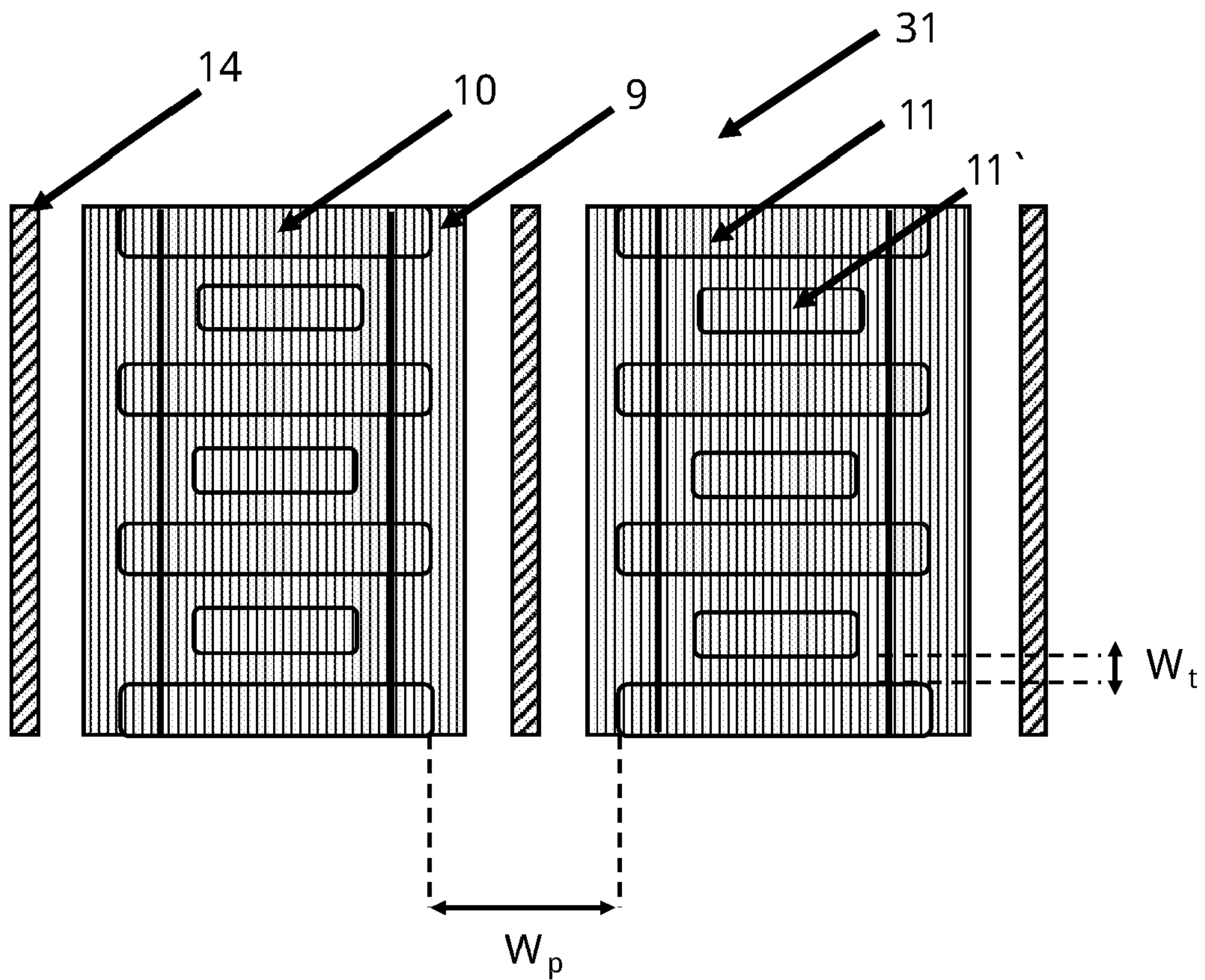

Figure (15B) A typical top view for a stripe design of first exemplary embodiment of a punch-through IGBT according to the invention where some of the trenches have different lengths

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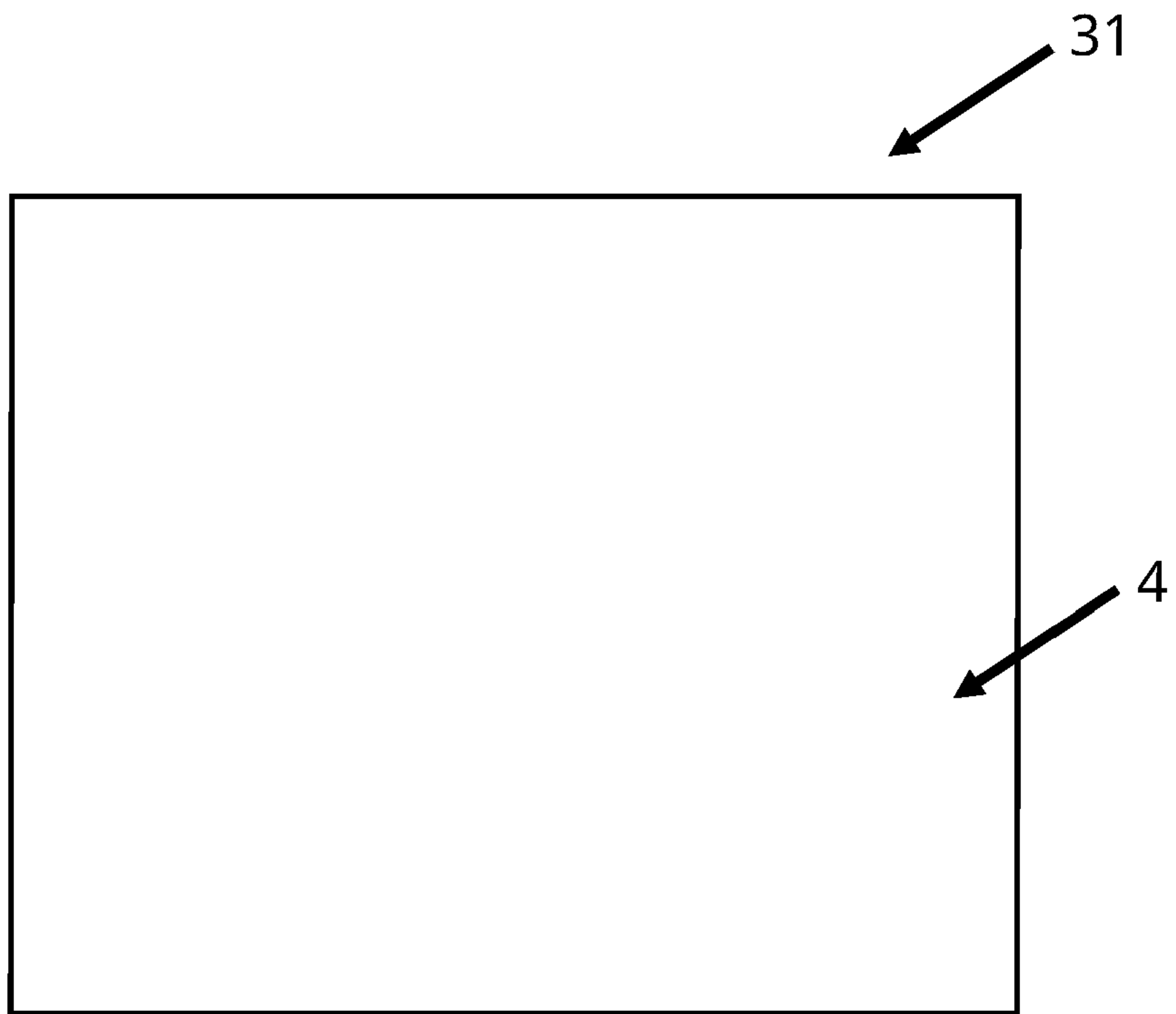

Figure (16) Method of manufacturing ‾ cross section

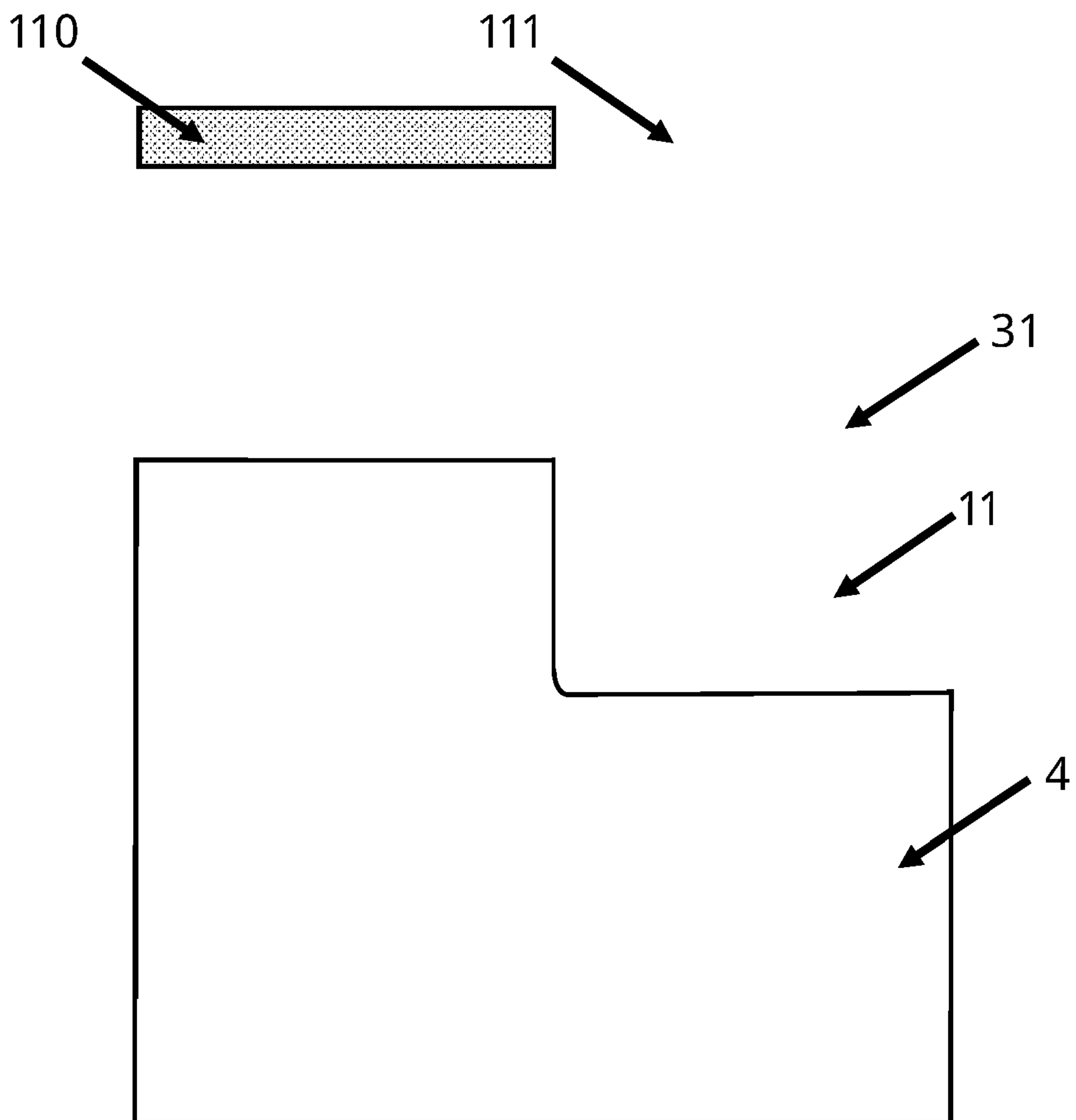

Figure (17)

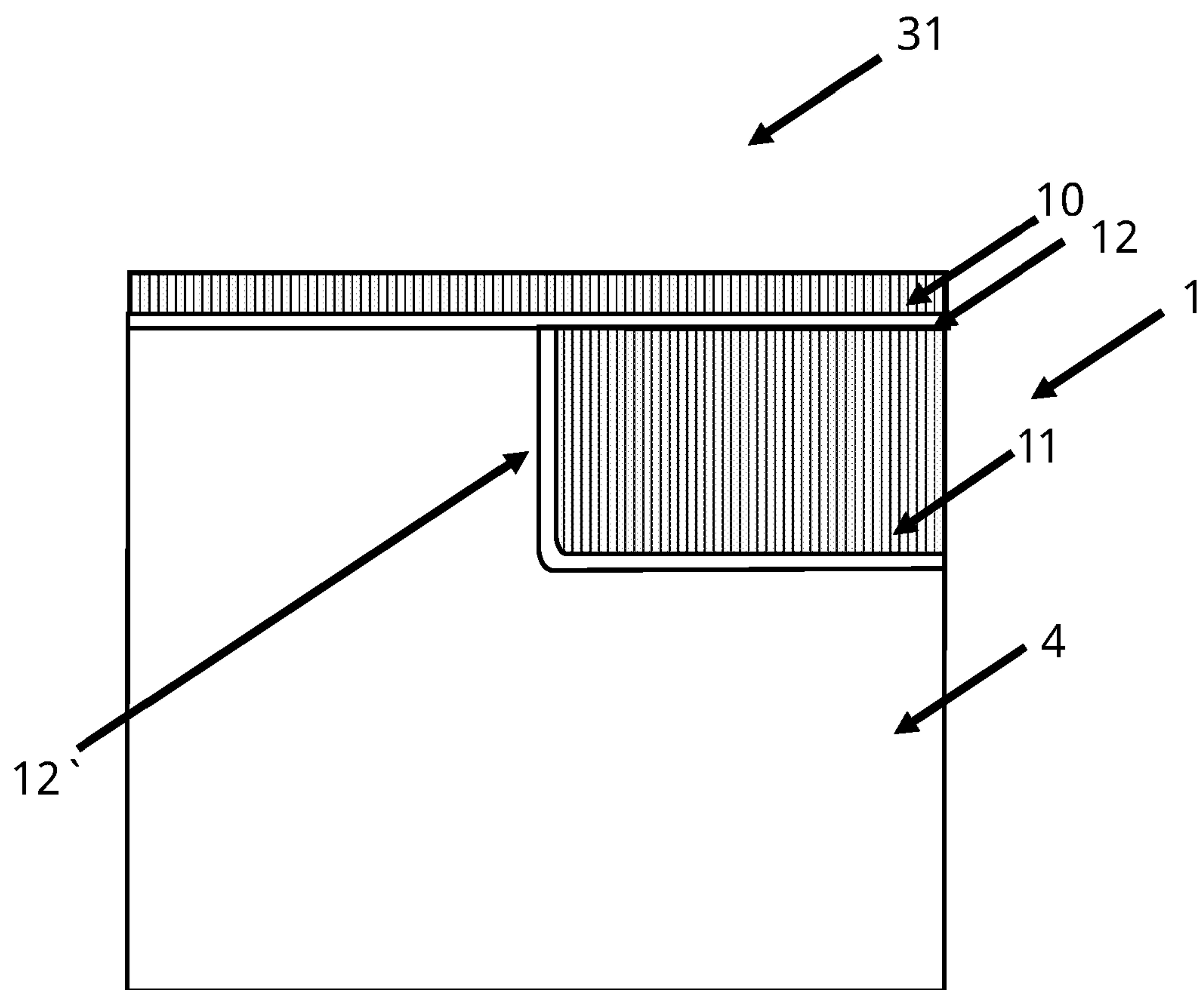

Figure (18)

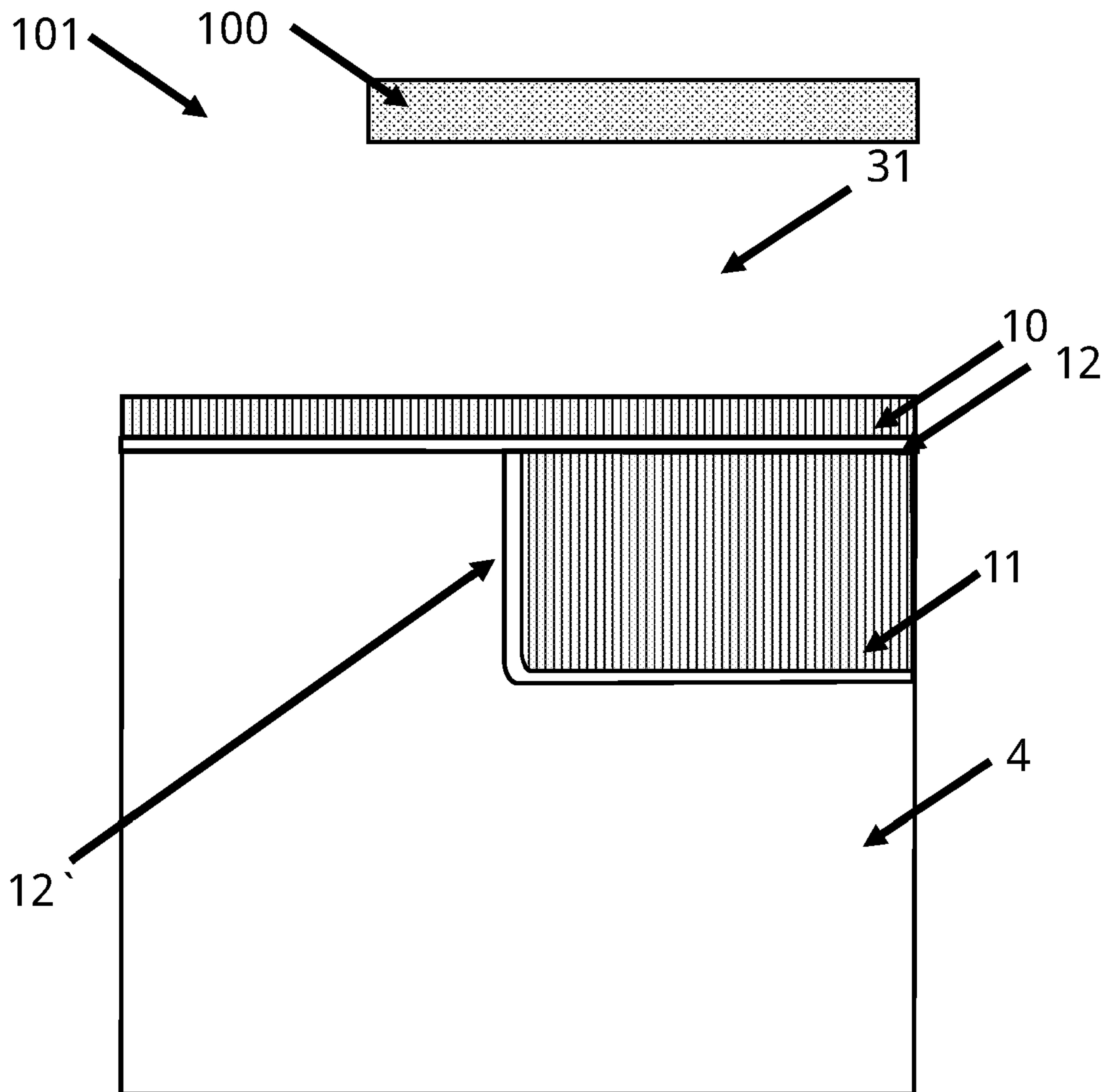

Figure (19)

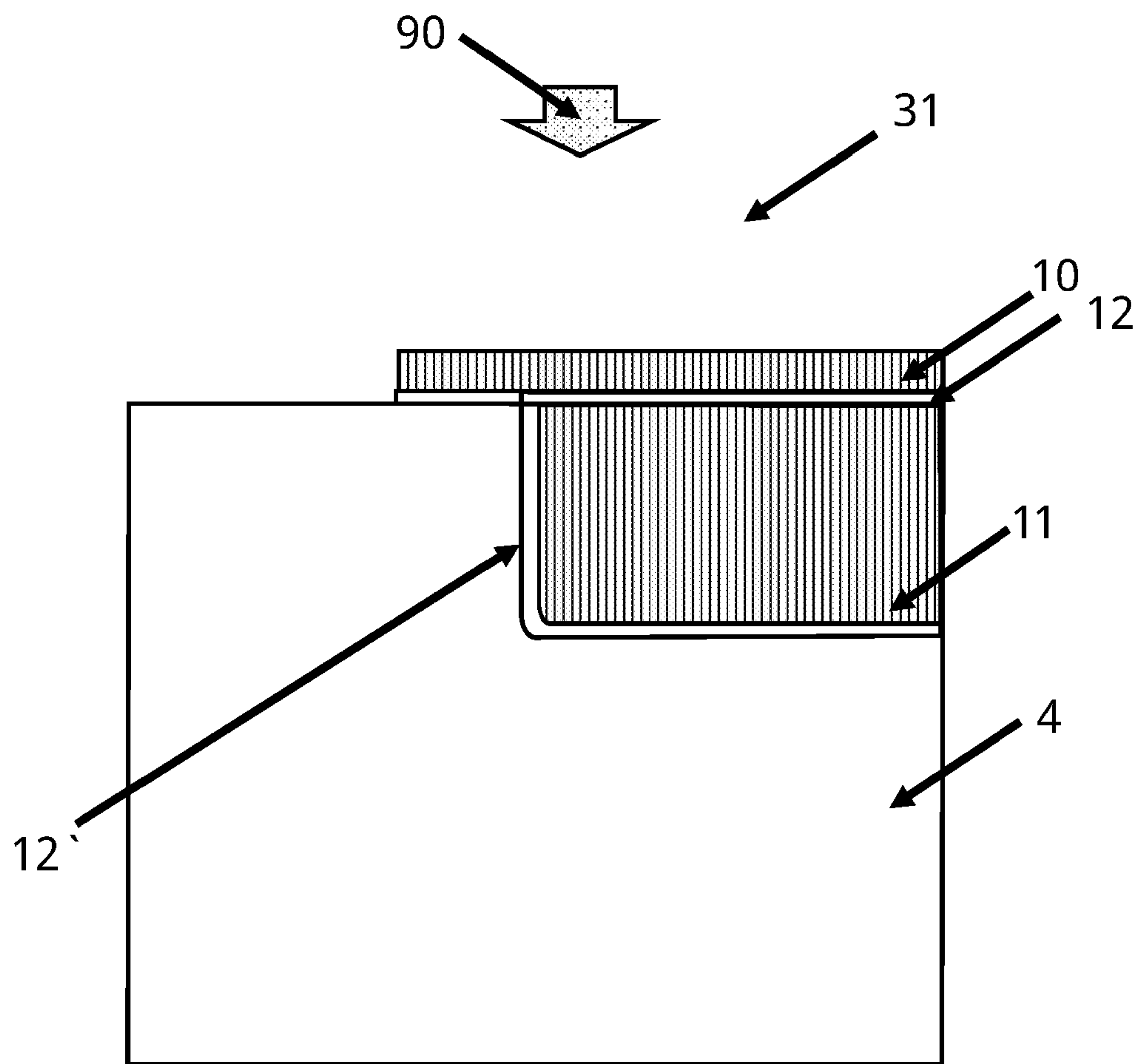

Figure (20)

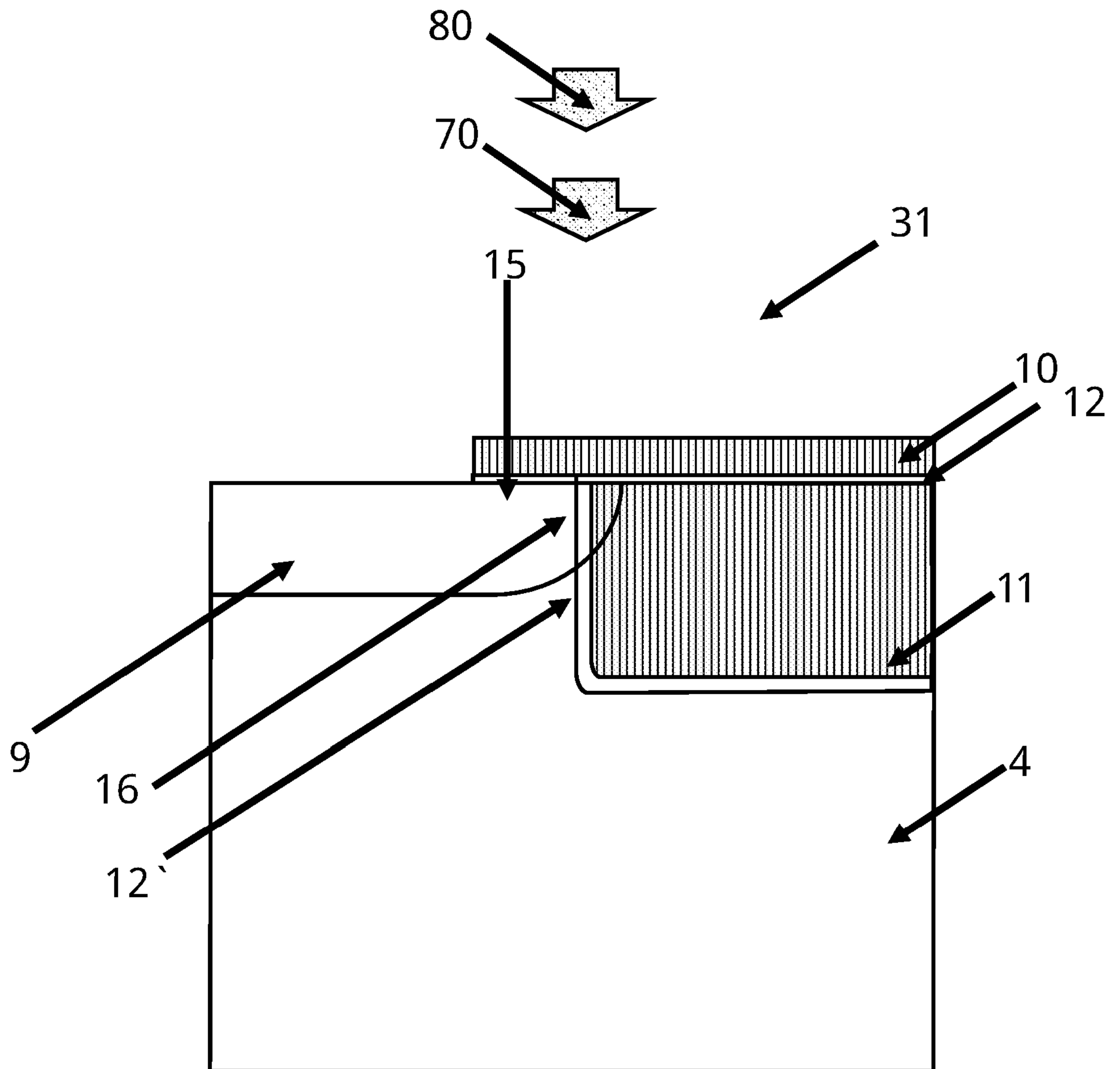

Figure (21)

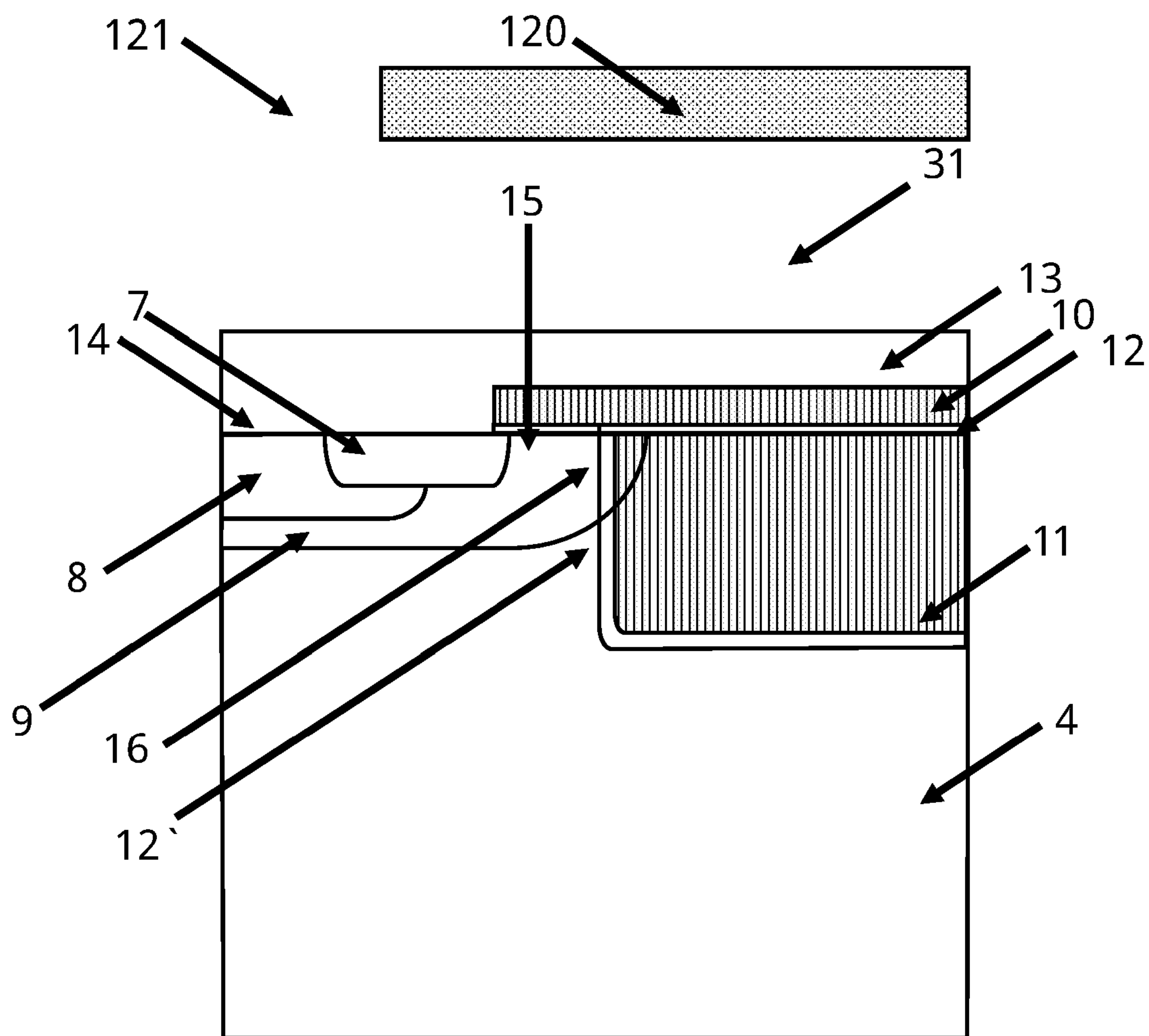

Figure (22)

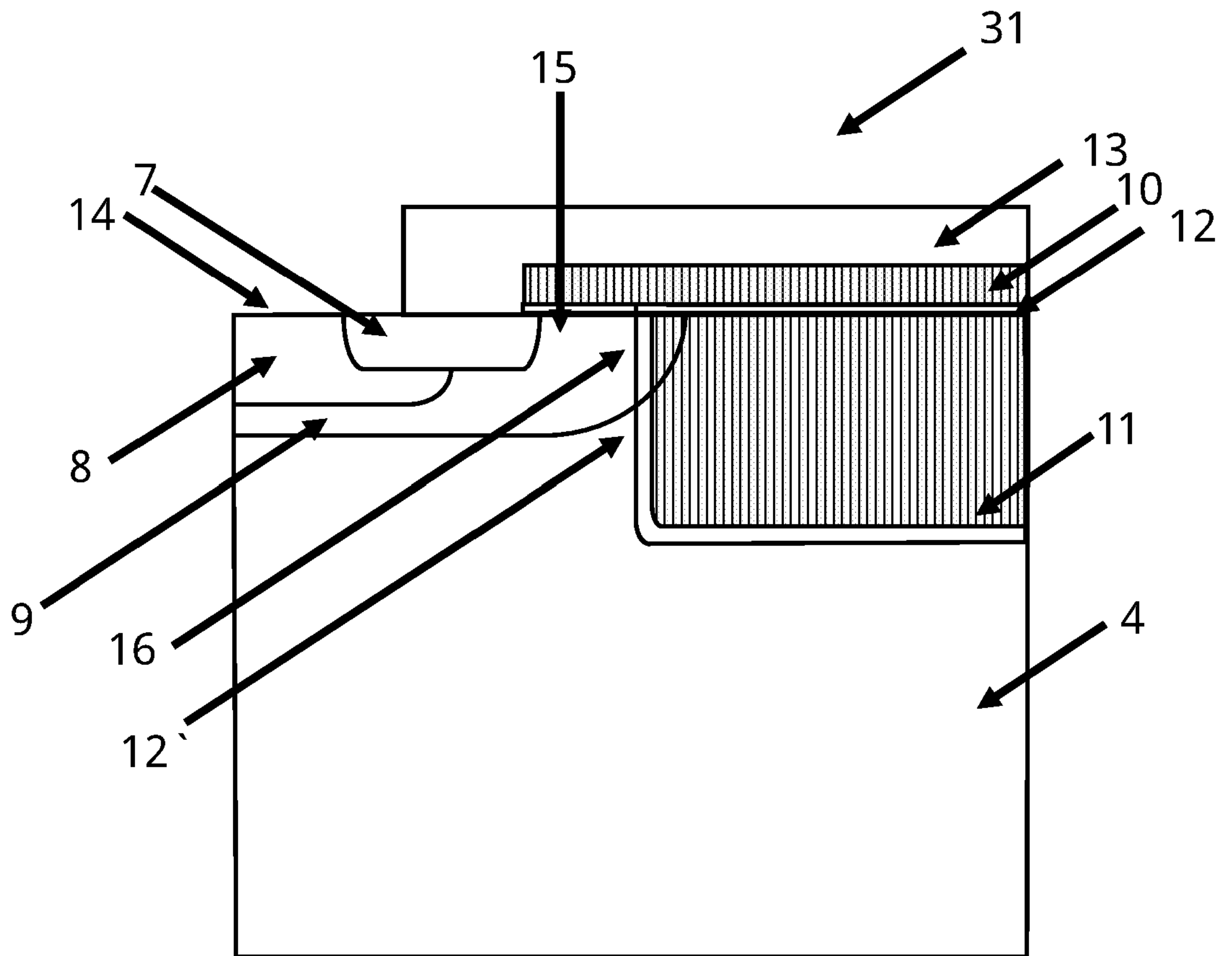

Figure (23)

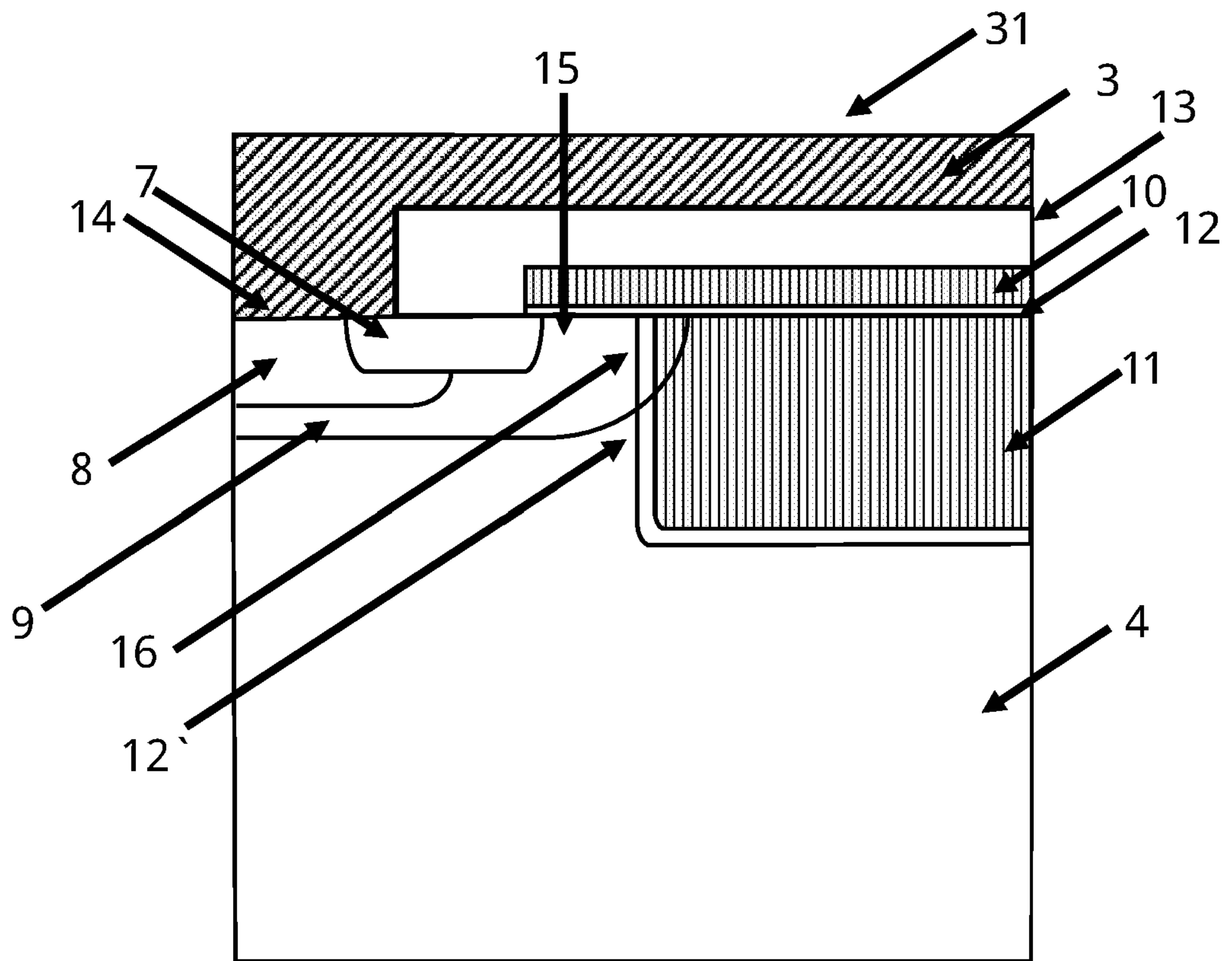

Figure (24)

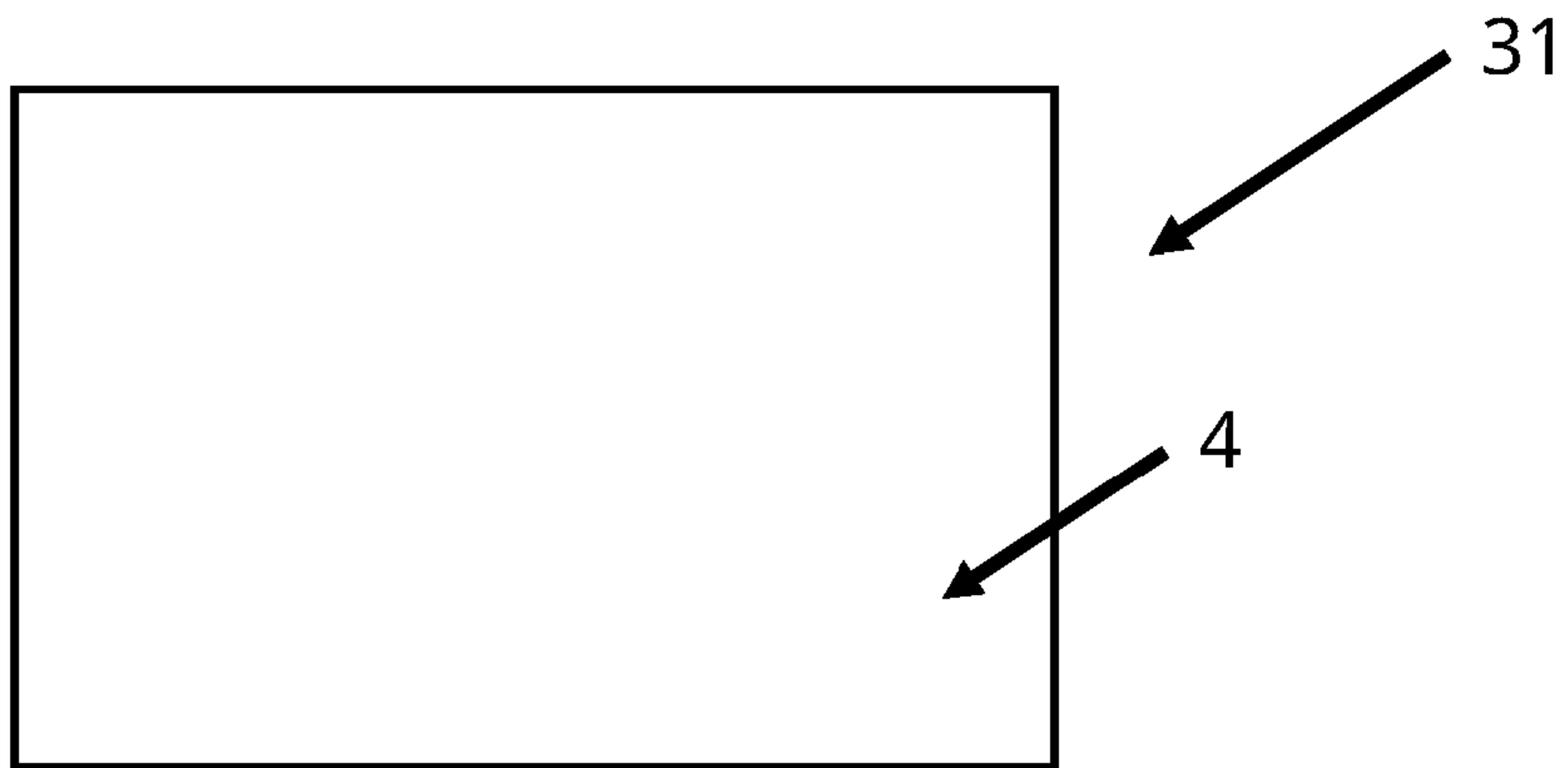

Figure (25) Method of manufacturing ‾ top view

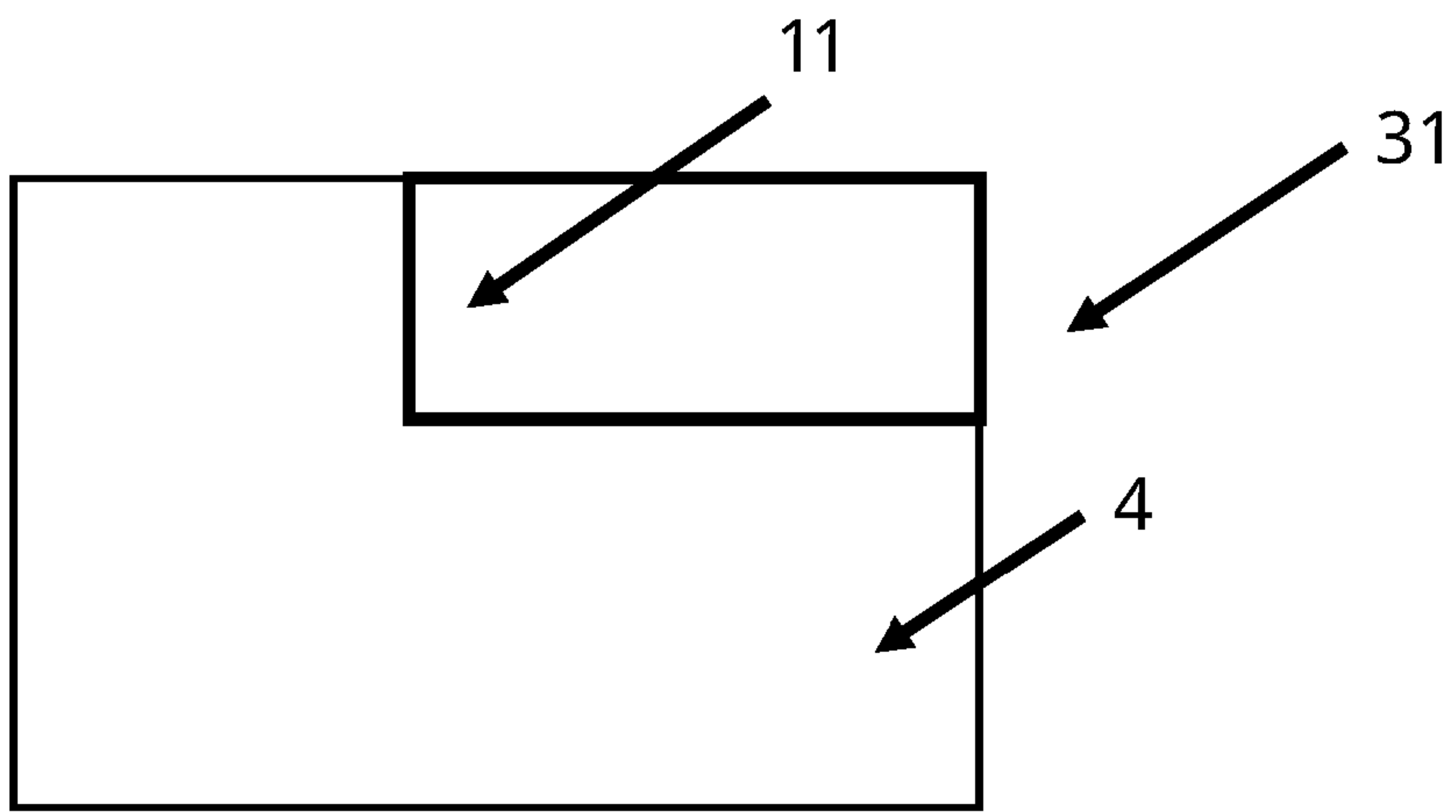

Figure (26)

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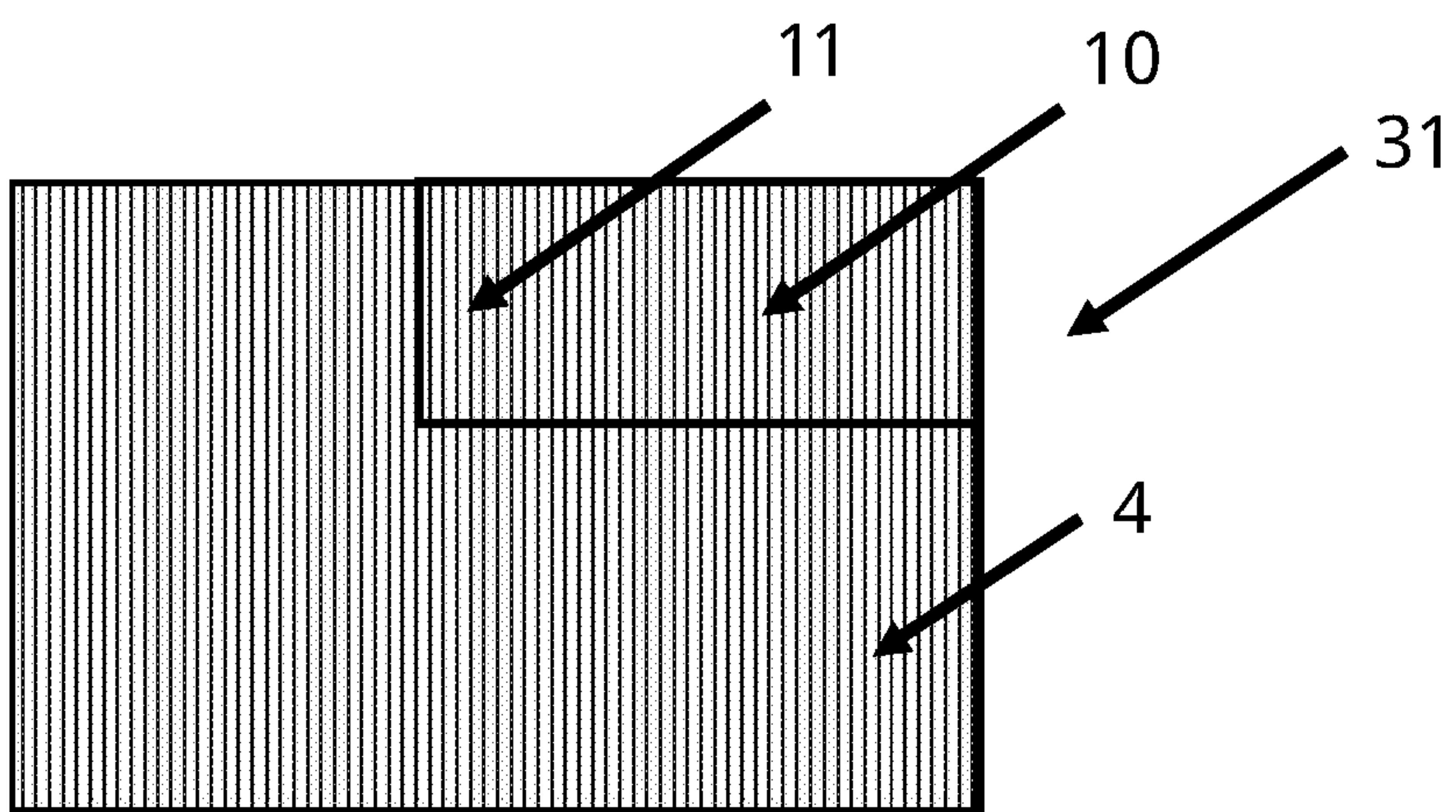

Figure (27)

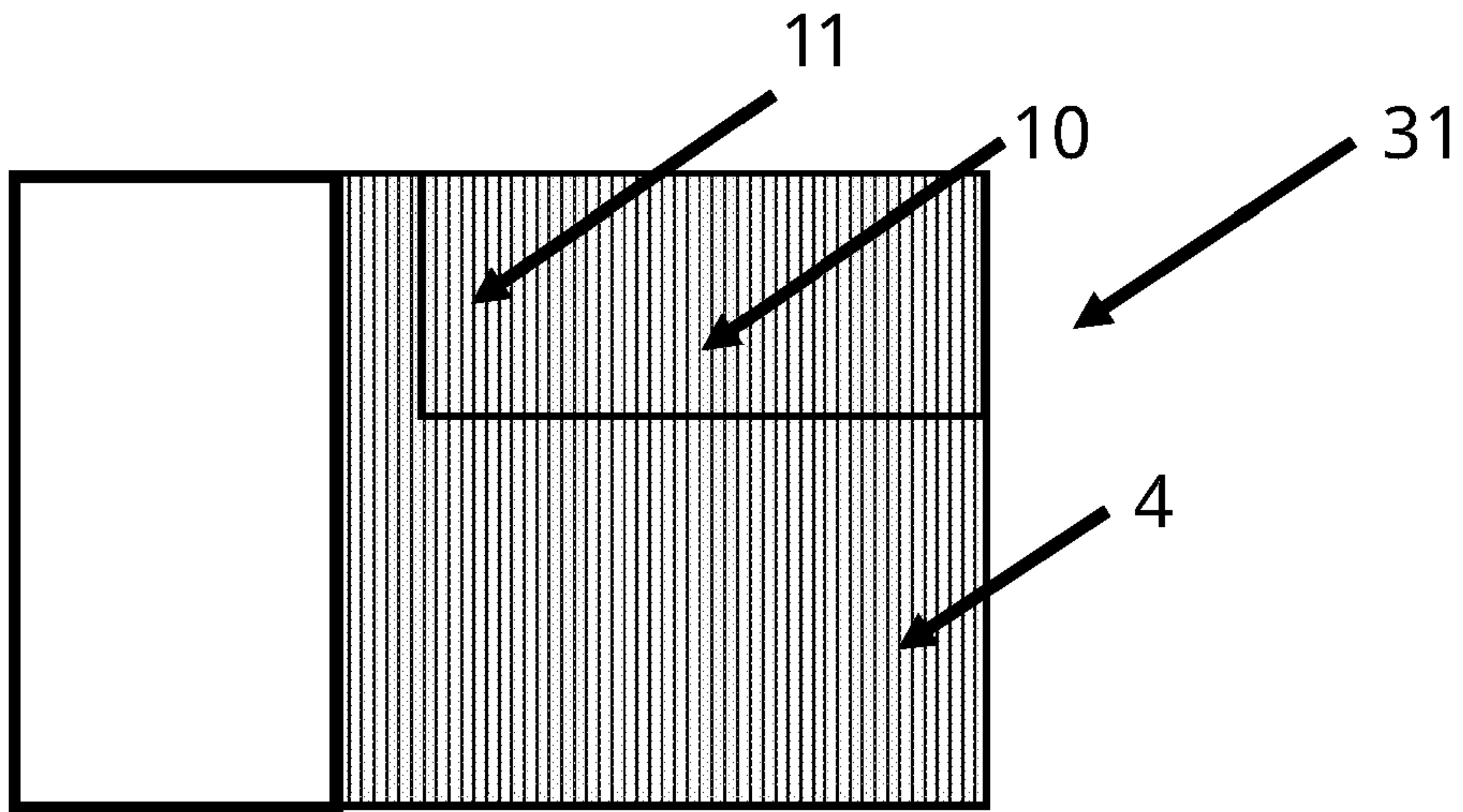

Figure (28)

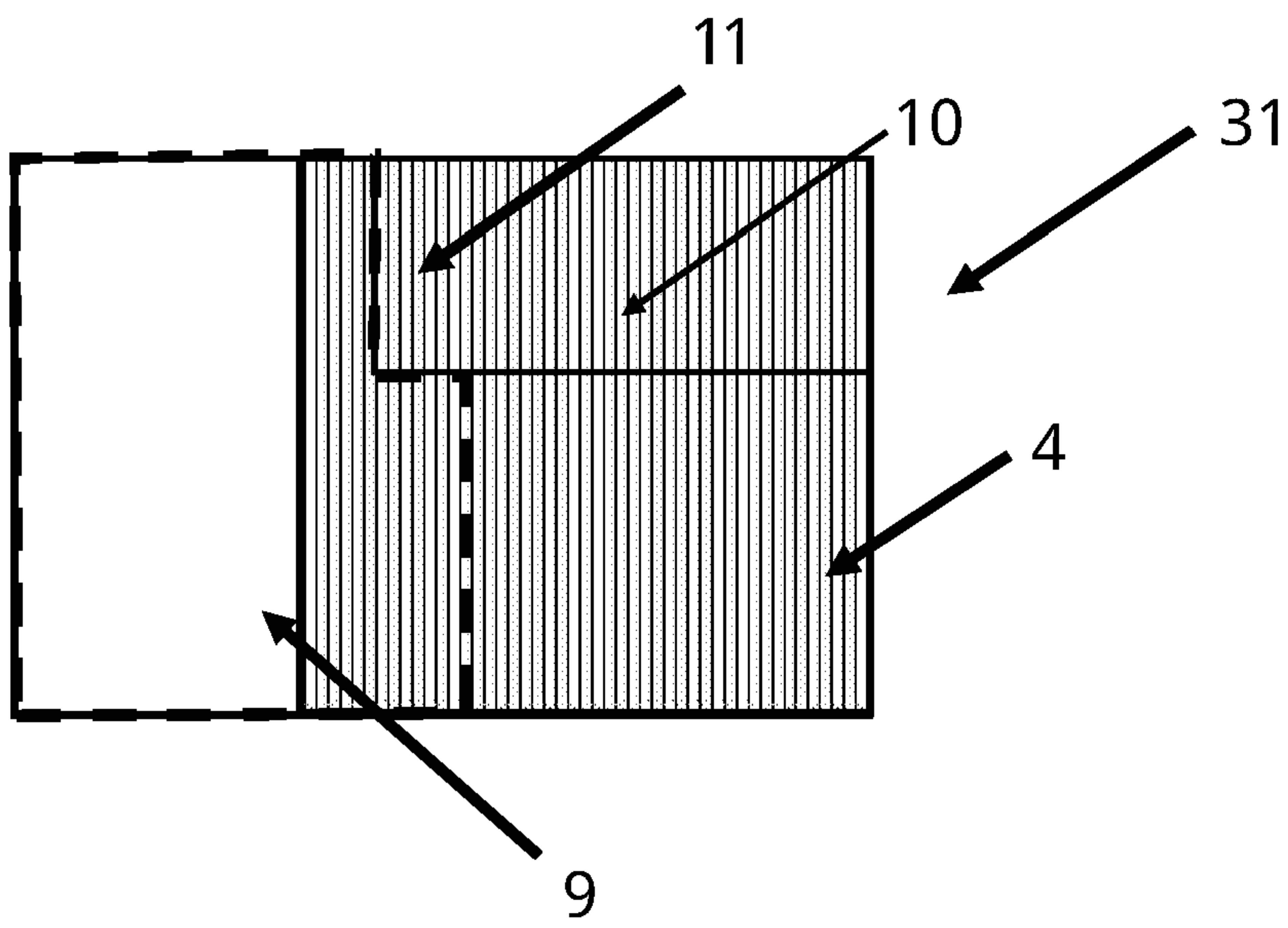

Figure (29)

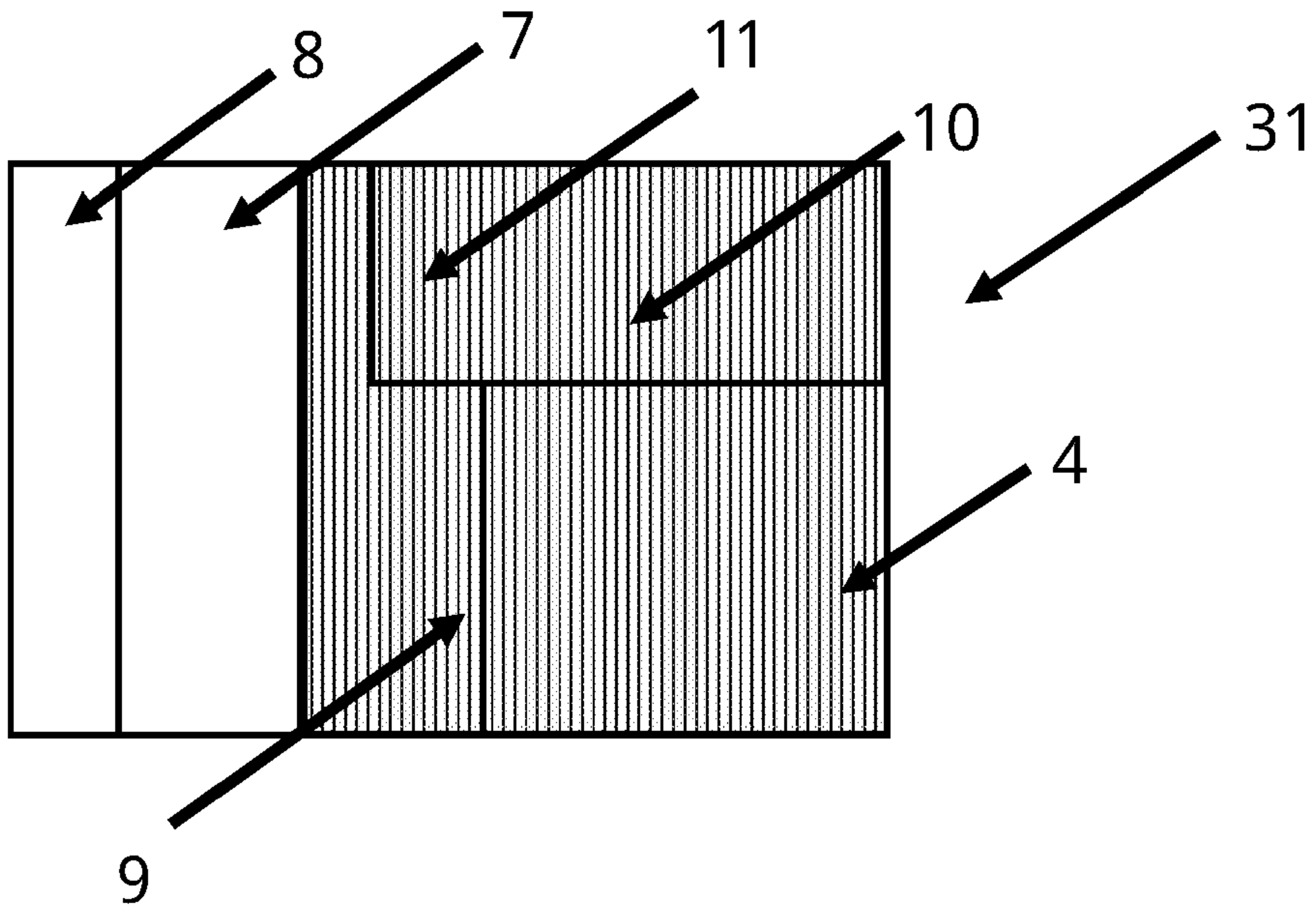

Figure (30)

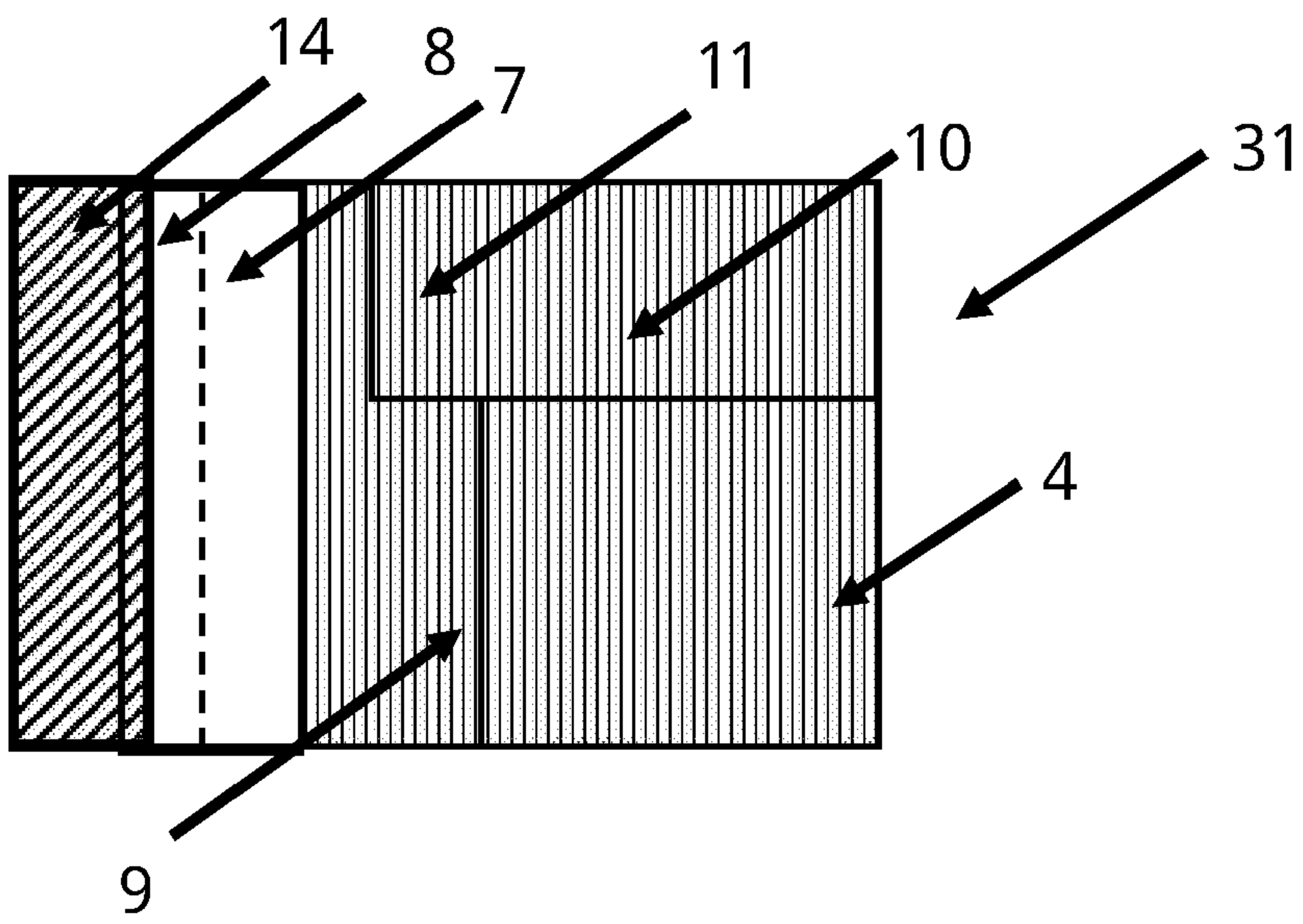

Figure (31)

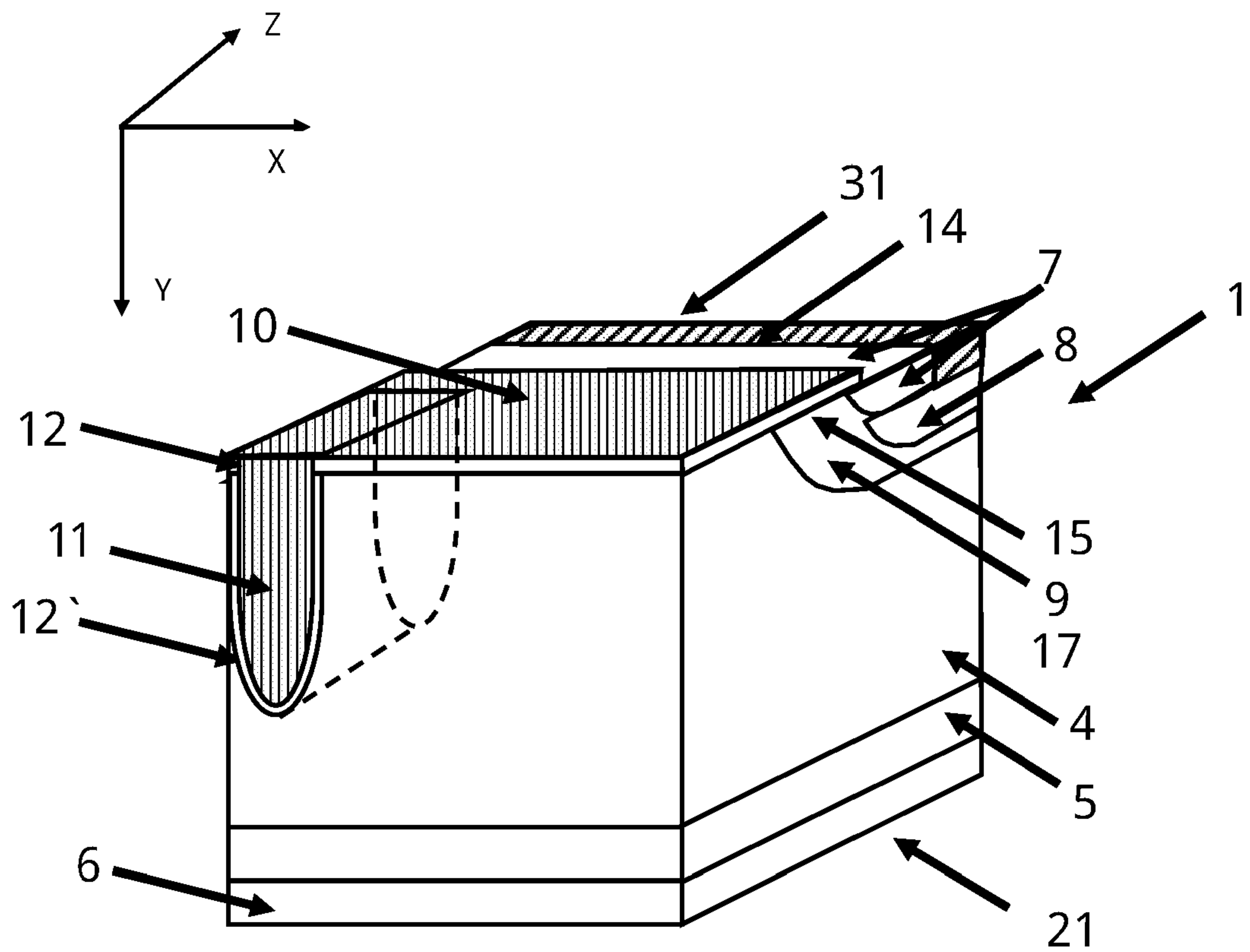

Figure (32) second exemplary embodiment of a punch through IGBT with extended second base layer under the source region and etched contact through the source region according to the invention

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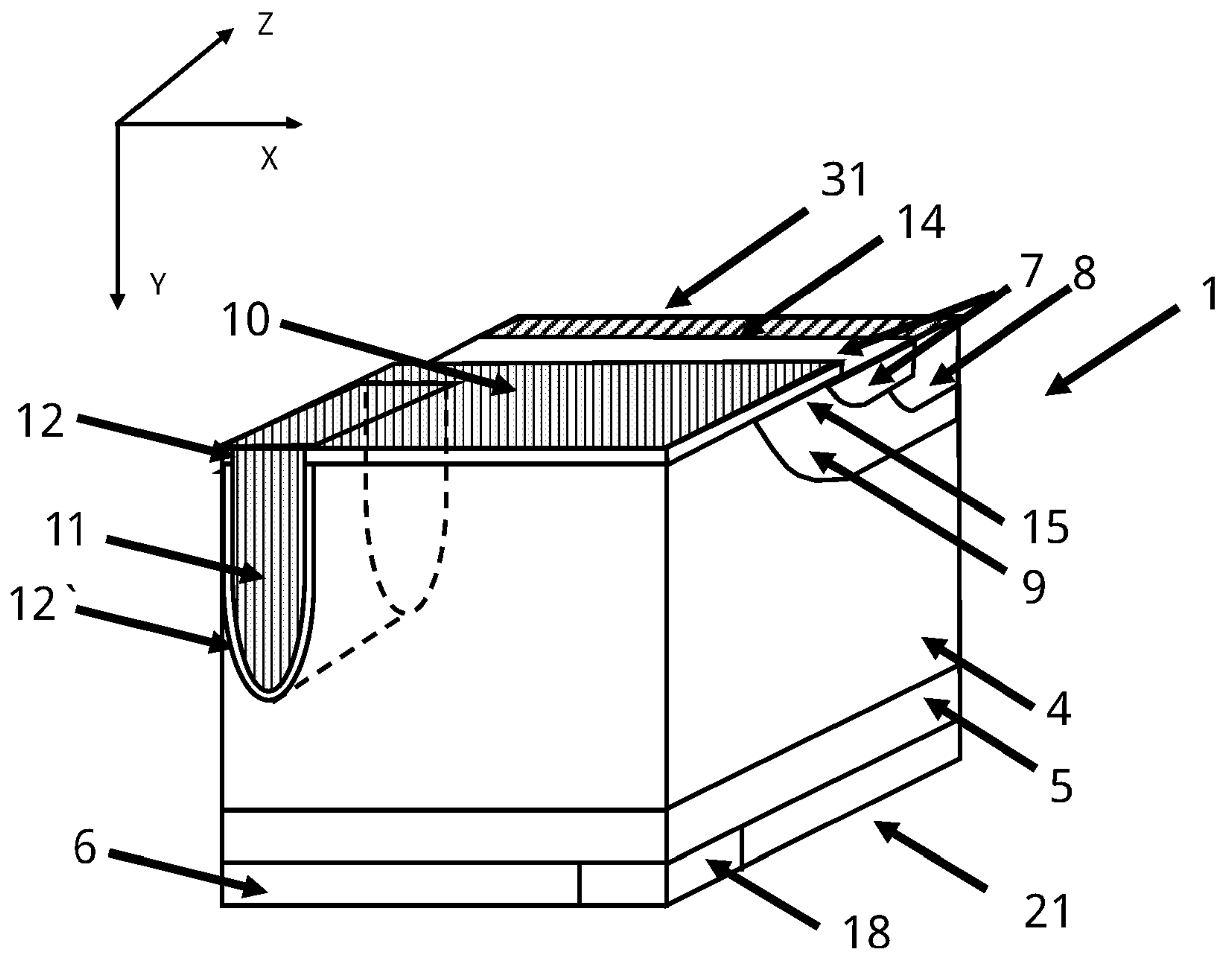

Figure (33) third exemplary embodiment of a reverse conducting IGBT according to the invention

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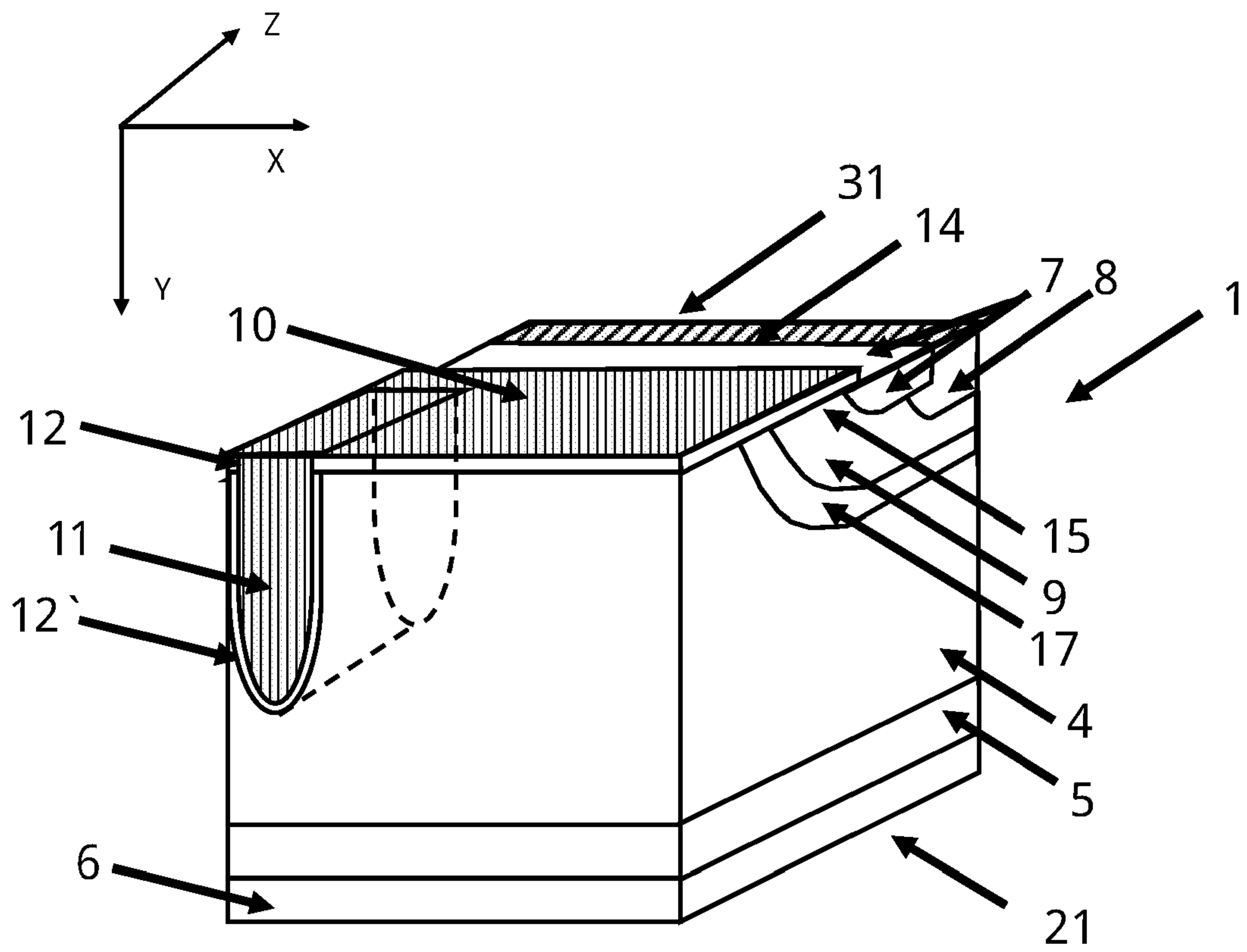

Figure (34) fourth exemplary embodiment of a punch through IGBT with n-enhancement layer according to the invention

DESCRIPTION

SEMICONDUCTOR DEVICE AND METHOD FOR PRODUCING SAME

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FIELD OF THE INVENTION

The invention relates to the field of power semiconductor devices. It relates to a power semiconductor device with layers of different conductivity types and a method for producing
10 such a semiconductor device.

TECHNICAL BACKGROUND

Planar and Trench MOS cell designs exhibit a number of advantages and disadvantages
15 for IGBT and MOSFET designs. For IGBTs, typical Planar and Trench designs are shown in FIG. 1A and 2A. Both designs can incorporate an enhancement n-type layer for improved excess carrier storage as shown in FIG. 1B and 2B.

FIG. 1A shows a prior art IGBT with planar gate electrodes. The IGBT 200 is a device
20 with a four-layer structure, which are arranged between an emitter electrode 3 on an emitter side 31 and a collector electrode 2 on a collector side 21, which is arranged opposite of the emitter side 31. An (n-) doped drift layer 4 is arranged between the emitter side 31 and the collector side 21. A p doped planar base layer 9 is arranged between the drift layer 4 and the emitter electrode 3, which planar base layer 9 is in direct electrical contact to the emitter
25 electrode 3. A planar n-doped source region 7 is arranged on the emitter side 31 embedded into the planar base layer 9 and contact opening 14 to the emitter electrode 3. In addition, a planar p doped region 8 arranged on the emitter side 31 below region 7 and embedded into the planar base layer 9 and contact opening 14 through region 7 and extending to region 8 is formed for the emitter electrode 3.

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A planar gate electrode 10 is arranged on top of the emitter side 31. The planar gate electrode 10 is electrically insulated from the planar base layer 9, the planar source region 7 and the drift layer 4 by a planar insulating layer 12. There is a further insulating layer 13 arranged between the planar gate electrode 10 and the emitter electrode 3.

The planar cell concept offers a lateral MOS channel 15 which suffers from non-optimal charge spreading (so called JFET effect) near the cell resulting in low carrier enhancement and higher conduction losses. Furthermore, due to the lateral channel design, the planar cell design suffers also from the PNP bipolar transistor hole drain effect (PNP effect) due to the bad spreading of electrons flowing out of the MOS channel. However, the accumulation layer between the MOS cells offers strong charge enhancement for the PIN diode part (PIN effect). The planar design also requires more area resulting in less cell packing density for reduced channel resistance.

On the other hand, the planar design provides good blocking capability due to low peak fields at the cell and in between. The planar design can also provide good controllability and low switching losses and the cell densities in planar designs are easily adjusted for the required short circuit currents. Due to the fact that there exist few high peak electric fields in the gate oxide regions, the planar design offers good reliability with respect to parameter shifting during operation under high voltages. Also, the introduction of enhanced layers in planar cells as shown in FIG. 1B has resulted in lower losses rivalling those achieved with trench designs as explained below.

The trench cell concept for a trench IGBT 300 shown in FIG. 2B offers a vertical MOS channel 16 which provides enhanced injection of electrons in the vertical direction and suffer from no drawbacks from charge spreading (JFET effect) near the cell. Therefore, the trench cells show much improved carrier enhancement for lower conduction losses. Due to the vertical channel design, the trench offers also less hole drain effect (PNP effect) due to the improved electron spreading out of the MOS channel. Modern trench designs adopting mesa widths (trench to trench distance) below 1mm achieve very low conduction losses since closely packed trenches can provide a strong barrier to hole drainage. Matching such a performance with less complex processes can be of a great advantage. The accumulation layer at the bottom of the trench offers strong charge enhancement for the PIN diode part.

Hence wide and/or deep trenches show optimum performance. Furthermore, the trench design offers large cell packing density for reduced channel resistance.

However, the trench design suffers from lower blocking capability near the bottom corners of the trenches due to high peak electric fields. This has also resulted in parameter shifting during operation due to hot carrier injection into the gate oxide. The trench design has also a large MOS accumulation region and associated capacitance resulting in bad controllability and high switching losses. The high cell densities in trench designs will also result in high short circuit currents. Finally, gate parameter shifts can occur under normal gate biasing stress conditions due to the trench etch process in relation to the silicon crystal orientation and the critical region at the n-source and p-base junction which is formed at the trench gate oxide 12` and defines the device MOS parameters.

Hence, optimising the trench design to overcome the above drawbacks has normally resulted in higher losses when compared to the initial loss estimations and potential of trench designs. Many trench designs have been proposed with particular focus on the regions between the active MOS cells for lowering the losses and improving the device controllability. Another approach in previous inventions combines planar and trench designs. This was proposed to obtain the advantage of the planar designs (region between the cells) and trench designs (the cell) while eliminating some of the drawbacks of the planar and trench designs.

In US 9064925B2, the Trench Planar IGBT 600 shown in FIG. 3 combines both a planar and trench MOS cells in a single design. However, both the planar channel 15 and trench channel 16 are separated. Similarly, in "Trench emitter IGBT with lateral and vertical MOS channels" (Proc. 23rd Internat. Conf. on Microelectronics MIEL 2002, 163-166) an IGBT is described, which comprises trench gate electrodes and planar gate electrodes in one device.

A Trench Planar MOSFET cell (Solid State Electronics, V38, No 4, page 821-828, 1995) represents the first publication of Trench Planar MOS cell design. A similar design was published as a Trench Planar IGBT (IEEE Electron Device Letters, Vol 20, No.11, Nov. 1999, page 580). The Trench Planar IGBT 400 design shown in FIG. 4A consist only of a planar channel and proposes a trench structure to improve carrier accumulation. The concept

proposed shallow trenches for improved blocking capability. In US 9093522B2, a similar Trench Planar design 401 with an enhancement layer 17 described with an embodiment where the channel extends to include trench section 16 as shown in FIG. 4B. The channels are formed with a gaussian doping profile with the maximum doping region near the n-source p-base junction which defines the device MOS parameter. Hence, the trench channel will be very lightly doped and will have little impact on the device operation. In US8441046B2, A Planar Trench MOS IGBT 500 with an enhancement layer was described as shown in FIG. 5. Similar to the Trench Planar NOS cell described above, the Planar Trench design includes a planar channel 15 and a trench channel 16 with the trench channel having higher doping levels compared to the Trench Planar design. US8441046B2 also describes a Trench Shielded Planar version where the trench is grounded (not connected to the gate) and in one version cuts orthogonally through the planar cell.

The majority of the above patents describe an active trench connected to the gate in combination with a planar channel in a two-dimensional arrangement.

In a closely related prior art to the present invention, US6380586B1 describes a trench IGBT 700 where planar channels 15 are orthogonally positioned in relation to the trench regions as shown in FIG. 6 for an embodiment having a discontinued trench at the emitter contact 3. A continuous trench cutting through the emitter contact 3 was also described. The main feature of this structure is the trench channel 16 which will provide electron injection in both lateral and vertical dimensions at the trench wall as shown in the cross-section B-B` as shown in FIG. 7. Such a device will have different MOS parameters such as the threshold voltage for the vertical and lateral channels. Furthermore, for the discontinued version, the trench MOS channel 16 at the trench periphery near 10` can become critical due to the sharp trench curvature in that region.

To overcome the above issues, US9640644 describes a planar cell structure 800 where the n-source regions 7 are separated from the trench by a highly doped p-region 8 which also extend along the trench orthogonal dimension for achieving higher turn-off capability as shown in FIG. 8. Hence, only a planar channel 15 is formed in this structure and no vertical channel along the trench oxide 12` is present as shown in FIG. 9 for the cross-section B-B`.

However, this device will not provide lower conduction losses and the highly doped p-regions can result in high hole drainage levels.

The structures described above also suffer from complex and critical alignment process
5 steps such as n-source 7 and p-region 8 structuring which can also increase the cost and limit the option to reduce the cell dimensions for providing lower losses.

It is desirable to find a new MOS cell design concept that can still benefit from the combination of the trench and planar MOS cell concepts while enabling simple process steps
10 and lower conduction / on-state losses.

DISCLOSURE OF THE INVENTION

It may be an object of the present invention to provide a Planar Insulated Gate Bipolar
15 Transistor IGBT with improved electrical characteristics. Furthermore, it may be an object of the present invention to provide a method for producing such a planar semiconductor device.

These objects may be met by the subject matter of the independent claims. Embodiments
20 of the invention are described with respect to the dependent claims.

It is an object of the invention to provide a power semiconductor device with reduced on-state losses, low drainage of holes, stable gate parameters, improved blocking capability, and good controllability.

25

The problem is solved by the semiconductor device with the characteristics of claim 1.

The inventive power semiconductor device has layers of different conductivity types, which layers are arranged between an emitter electrode on an emitter side and a collector
30 electrode on a collector side, which is arranged opposite of the emitter side. The layers comprise:

- a drift layer of a first conductivity type, which is arranged between the emitter side and the collector side,
- a first base layer of a second conductivity type, which is arranged between the drift layer and the emitter electrode, which first base layer is in direct electrical contact to
5 the emitter electrode,
- a source region of the first conductivity type, which is arranged at the emitter side embedded into the first base layer and contacts the emitter electrode, which source region has a higher doping concentration than the drift layer, and extends to the first and second gate electrode,
10 - a second base layer of the second conductivity type, which is arranged at the emitter side embedded into the first base layer and is situated deeper than the source region, and contacts the emitter electrode, which second base layer region has a higher doping concentration than the first base layer,
- a first gate electrode, which is arranged on top of the emitter side and the first gate
15 electrode is electrically insulated from the first base layer, the source region and the drift layer by a first insulating layer, an lateral / horizontal channel is formable between the emitter electrode, the first source region, the first base layer and the drift layer,
- a plurality of second gate electrodes, each of which is electrically insulated from the
20 first base layer and the drift layer by a second insulating layer and which second gate electrode is arranged orthogonally to the plane of the first base layer, and is discontinued in the planar channel regions and extends deeper into the drift layer than the first base layer, a vertical channel is formable between the lateral / horizontal channel, the first base layer and the drift layer,

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The inventive planar semiconductor device includes planar cells forming a lateral / horizontal channel and a plurality of trenches, which are arranged orthogonally to the plane of the planar cells and are discontinued in the planar channel regions to form lateral / horizontal planar channels in the mesa regions between the trenches, and form exceptionally
30 a series connection between a lateral /horizontal planar channel and a vertical trench channel only in the discontinued trench regions.

The inventive planar semiconductor device integrates a Trench into a Planar MOS cell in order to gain the advantages of both designs in terms of reduced on-state losses, low drainage of holes, stable gate parameters, improved blocking and good controllability.

The advantage of the planar gate design and trench design can be combined in the inventive semiconductor device while the disadvantages of the planar cell region and inter-space between trench cells are eliminated.

Due to the fact that the area in between the orthogonal gate trenches does not need to be further structured, very high-density trenches can be used with trench mesa dimensions below 100nm. This will significantly reduce the hole drainage effect as well known to those experts in the field.

In addition, for discontinued orthogonal gate trenches at the planar cell, the trench mesa dimension at the planar cell can be reduced to 1mm for further reducing the hole drainage effect while keeping the planar cell dimensions larger than 1mm.

The planar source region is formed to ensure stable gate parameters and blocking capability. However, the trenches will provide a vertical channel with improved vertical spreading.

Some or all of the plurality of second gate electrodes can be directly connected to the first gate electrodes, or can be grounded to the emitter electrode, or made floating. If the second gate electrodes gates are shorted to the emitter electrode, there is no voltage differential between the second gate electrodes and effectively no capacitance. Since the second gates do not invert the first base region, the cell containing the second gate is a passive type of cell, as opposed to an active cell controlled by the gate trenches. By controlling the number of passive cells, the input capacitance of the device can be precisely controlled.

Similarly, if the second gate electrodes are floating, resulting in a passive cell, the potential floats up to the emitter voltage so there is effectively no capacitance associated with the second gates.

Furthermore, the device is easy to manufacture, because the inventive design can be manufactured based on a self-aligned process with minimum a number of masks required.

5 The new design offers a wide range of advantages both in terms of performance (reduced losses, improved controllability and reliability), and processability (very narrow mesa design rules, reliable planar process compatibility) with the potential of applying enhanced layer structures. The inventive design is suitable for full or part stripes but can also be implemented in cellular designs.

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The inventive design is also suitable for reverse conducting structure and can be applied to both IGBTs and MOSFETs based on silicon or wide bandgap materials such as Silicon Carbide SiC.

15 The inventive method for manufacturing a power semiconductor device comprises the following steps:

- a trench region is produced by etching on the first main side of the substrate of a first conducting type
- 20 a first oxide layer is produced on a first main side of a substrate of a first conductivity type,
- a structured gate electrode layer with at least one opening is produced on the first main side on top of the first oxide layer,
- first dopants of a second conductivity type are implanted into the substrate on the 25 first main side and,
- the first dopants are diffused into the substrate, characterized in that,
- the structured gate electrode layer is used as a mask for implanting the first dopants,
- second dopants of a first conductivity type are implanted into the substrate on the 30 first main and,
- the second dopants are diffused into the substrate, characterized in that,

- the second dopants are diffused to a lower depth than the first dopants,
- the structured gate electrode layer or an additional mask is used as a mask for implanting the second dopants,
- third dopants of a second conductivity type are implanted into the substrate on the first main side and,
- the third dopants are diffused into the substrate, characterized in that,
- the third dopants are implanted and diffused to a lower depth than the first dopants,
- the structured gate electrode layer or an additional mask is used as a mask for implanting the third dopants,
- an insulating oxide layer is produced on the first main side,
- a contact opening is produced by etching through the insulating layer and by filling a resulting contact opening with metal

The inventive method for manufacturing a power semiconductor device, in particular an IGBT or MOSFET, has the advantage that the base and source layers are self-aligned by using the structured gate electrode layer as a mask.

BRIEF DESCRIPTION OF THE DRAWINGS

The embodiments of the invention will be explained in more detail in the following text with reference to the attached drawings, in which:

FIG. 1A-B: show the cross sections of Planar MOS IGBT structures (prior art).

FIG. 2A-B: show the cross sections of Trench MOS IGBT structures (prior art).

FIG. 3: show the cross section of Trench Planar MOS IGBT structure (prior art).

FIG. 4A-B: show an alternative cross-section of Trench Planar MOS IGBT structures (prior art).

FIG. 5A-B: show the cross sections of Planar Trench MOS IGBT structures (prior art).

FIG. 6: show the Trench Planar MOS IGBT structure (prior art).

FIG. 7: show the cross sections of Trench Planar MOS IGBT structure at cut B (prior art).

FIG. 8: show the Trench MOS IGBT structure (prior art).

FIG. 9: show the cross sections of Trench MOS IGBT structure at cut B (prior art).

FIG. 10: show a first exemplary embodiment of a power semiconductor device according to the invention

5 FIG. 11: Top view of first exemplary embodiment of a punch-through IGBT according to the invention

FIG. 12: Cross section along A-A` of first exemplary embodiment of a punch-through IGBT according to the invention.

FIG. 13: Cross section along B-B` of first exemplary embodiment of a punch-through 10 IGBT according to the invention.

FIG. 14: Cross section along C-C` of first exemplary embodiment of a punch-through IGBT according to the invention showing series connected planar and trench channels.

FIG. 15A: A typical top view for a stripe design of first exemplary embodiment of a punch-through IGBT according to the invention where all trenches have the same length

15 FIG. 15B: A typical top view for a stripe design of first exemplary embodiment of a punch-through IGBT according to the invention where some of the trenches have different lengths

FIG. 16 - 24: show a cross section of the different steps of the method for manufacturing a semiconductor device according to the invention.

20 FIG. 25 - 31: show a top view of the different steps of the method for manufacturing a semiconductor device according to the invention.

FIG. 32: second exemplary embodiment of a punch through IGBT with extended second base layer under the source region and etched contact through the source region according to the invention

25 FIG. 33 third exemplary embodiment of a reverse conducting IGBT according to the invention.

FIG. 34 fourth exemplary embodiment of a punch through IGBT with n-enhancement layer according to the invention

30 The reference symbols used in the figures and their meaning are summarized in the list of reference symbols. The drawings are only schematically and not to scale. Generally, alike

or alike-functioning parts are given the same reference symbols. The described embodiments are meant as examples and shall not confine the invention.

MODES FOR CARRYING OUT THE INVENTION

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FIG. 10 shows a first exemplary embodiment of a power semiconductor device 1 in form of a punch through insulated gate bipolar transistor (IGBT) with a four-layer structure (pnpn). The layers are arranged between an emitter electrode 3 on an emitter side 31 and a collector electrode 2 on a collector side 21, which is arranged opposite of the emitter side
10 31. The IGBT comprises the following layers:

an (n-) doped drift layer 4, which is arranged between the emitter side 31 and the collector side 21,

15 a p doped first base layer 9, which is arranged between the drift layer 4 and the emitter electrode 3, which first base layer 9 is in direct electrical contact to the emitter electrode 3,

a p doped second base layer 8, which is arranged between the first base layer 9 and the emitter electrode 3, which second base layer 8 is in direct electrical contact to the emitter
20 electrode 3, which second base layer 8 has a higher doping concentration than the first base layer 9, which second base layer 8 extends perpendicularly deeper than the source region while allowing the horizontal channels to form,

an n doped source region 7, which is arranged at the emitter side 31 embedded into the
25 first base layer 9 and contacts the emitter electrode 3, which source region 7 has a higher doping concentration than the drift layer 4,

a first gate electrode 10, which is arranged on top of the emitter side 31 and the first gate electrode 10 is electrically insulated from the first base layer 9, the source region 7 and the
30 drift layer 4 by a first insulating layer 12, an lateral / horizontal channel 15 is formable between the emitter electrode 31, the source region 7, the first base layer 9 and the drift layer 4,

a plurality of second gate electrodes 11, each of which is electrically insulated from the first base layer 9, and the drift layer 4 by a second insulating layer 12ˇ and which second gate electrode 11 is arranged orthogonally to the plane of the first base layer 9, and is discontinued in the planar channel regions 15 and extends deeper into the drift layer 4 than the first base layer 9, a vertical channel is formable between the lateral / horizontal channel, the first base layer 9 and the drift layer 4,

a collector layer 6 arranged between the buffer layer 5 and the collector electrode 2, which collector layer 6 is in direct electrical contact to the collector electrode 2,

a buffer layer 5 arranged between the collector layer 6 and the drift region 4,

The trench regions can be better viewed in the top cell view shown in FIG. 11 for the first main embodiment of the inventive design. The inventive design consists of a basic planar MOS cell design with active trenches 11 (connected to gate electrode 10) occupying the regions between the planar cells in the 3rd dimension or in other words orthogonal to the planar channels. FIG. 12 to FIG. 14 show the cross sections of the inventive design along the cut lines shown in FIG. 11. The inventive design provides a lateral / horizontal channel 15 in the planar regions 10 (A-A`) and a lateral / horizontal channel 15 with improved vertical spreading at the edge of the trench region 11 (B-B`), and exceptionally, a series connection between a planar lateral/horizontal channel and a vertical channel in the trench region 11 (C-C`).

Specifically, the trench extends vertically to a depth approximately in a range from about 2 ı m to about 7 ı m. The trench width may range from about 3 ı m to about 0.5 ı m.

With respect to the top views shown in FIG. 15A-B, the critical design aspects are the dimension W_t or mesa between the orthogonal trenches, as well as the dimension W_p representing the distance from the end of one trench to the adjacent trench along the planar channel. Improved carrier storage/reduced hole drainage is expected as the dimension W_t and W_p are reduced. The value of W_t may be in a range from about 5 ı m to below 0.1 ı m,

more preferably from 1 ı m to 0.1 ı m ¯ which is achievable with the proposed design because no additional structures have to be lithographically defined in between the trenches, as in prior art. Also, improved carrier storage/reduced hole drainage is expected with reducing the planar cell dimensions, or by keeping the same pitch for the planar cell part, but reducing the distance W_p by etching the adjacent trenches closer to each other. More specifically, W_p could extend approximately in a range from about 20 ı m to about 1 ı m, preferably from 5 ı m to 1 ı m, and more preferably from 2 ı m to 1 ı m. The length of the orthogonal trenches can very on the same structure as shown in FIG. 15B where the trenches with a shorter length 11` can be discontinued in the drift region 4. Other orthogonal trench design parameters can also vary on the same structure such as the width, depth or voltage bias.

The inventive method for manufacturing a planar MOS cell on an emitter side is shown in cross sections in the FIGs. 16 to 24 and corresponding top views in the FIGs. 25 to 31. The method comprises manufacturing steps as follows.

As shown in FIG. 16 (corresponding top view FIG. 25) the method is started with a lightly n doped substrate 4, which has an emitter side 31. As shown in FIG. 17 (top view FIG. 26), a trench region 11 is produced by dry etching through a mask opening 111 into the substrate 4. A first oxide layer 12 and second oxide layer 12` are produced completely covering the substrate 4 on the emitter side 31. As shown in FIG. 18 (top view FIG. 27), electrically conductive layers 10 and 11 are produced on top of the first oxide layer 12 and second oxide layer 12` respectively. The electrically conductive layers 10 and 11 cover the first oxide layer 12 and second oxide layer 12`completely. According to FIG. 19 and FIG. 20 (top view FIG. 28) an opening 101 in form of a through hole is etched in the electrically conductive layer 10, resulting in a structured gate electrode layer 10.

Afterwards, the first dopants of p conductivity type are implanted into the substrate 4 (shown by arrows 90 in FIG. 20) (top view FIG. 29) using the structured gate electrode layer with its opening as a mask, resulting in a first implant region 9. Afterwards, the implanted first dopants are diffused into the substrate 4 as shown in FIG. 21 (top view FIG. 29). The first dopants are preferably Boron ions. The first dopants are preferably implanted with an energy of 20-100 keV and / or a dose of 5 x 10^{13} / cm^2 to 2 x 10^{14} / cm^2. The first dopants

are driven into a maximum depth between 1 ı m and 5 ı m, in particular between 1 and 3 ı m and in particular between 1 and 2 ı m. As shown in FIG. 21, the first dopants are not only driven into the substrate 4 in a direction perpendicular to the surface, but they are spread out laterally as shown in top view FIG. 29, and will reach the orthogonal trenches 11 to form the series connected planar and trench channels 15 and 16, while reaching out further laterally in the mesa region between the orthogonal trenches 11 to form only the planar channel 15.

Afterwards, the second dopants of highly doped n conductivity type are implanted 70 into the substrate 4 through a mask or using the structured gate electrode layer with its opening as a mask, resulting in a second implant region 7. Afterwards, the implanted second dopants are diffused into the substrate 4. The second dopants are preferably Phosphorous or Arsenic preferably Arsenic ions. The second dopants are preferably implanted with an energy of 100 -160 keV and / or a dose of 1 x 10^{15} / cm^2 to 1 x 10^{16} / cm^2. The second dopants are driven into a maximum depth between 0.5 ı m and 1 ı m. As shown in FIG. 22 (top view FIG. 30), the second dopants are mainly driven into the substrate 4 in a direction perpendicular to the surface, but they are only slightly spread out laterally to form the critical source region under the gate oxide.

Afterwards, the third dopants of highly doped p conductivity type are implanted 80 into the substrate 4 through a mask opening or using the structured gate electrode layer with its opening as a mask, resulting in a third implant region 8. Afterwards, the implanted third dopants are diffused into the substrate 4. The third dopants are preferably Boron ions. The third dopants are preferably implanted to a higher depth than the second region with an energy of 50 -160 keV and / or a dose of 1 x 10^{15} / cm^2 to 1 x 10^{16} / cm^2. The third dopants are driven into a maximum depth between 0.5 ı m and 2.5 ı m. As shown in FIG. 22 (top view FIG. 30), the third dopants are mainly driven into the substrate 4 in a direction perpendicular to the surface, but they are only slightly spread out laterally to cover a section or all the lower part of the second region and ensure a lateral / horizontal channel can be formed in the planar cell.

Afterwards, an insulating oxide layer 13 is produced to cover the first main side 31 completely. The insulating oxide layer thickness can range between 500nm to 1500nm. A contact opening 14 is then produced by dry etching the insulating oxide layer 13 fully

through a mask opening 121 as shown in FIG. 22 to reach the third dopants region 8 as shown in FIG. 23 (top view FIG. 31). The contact opening 14 is filled with metal to produce a direct electrical emitter contact 3 to the second dopants region 7 and third dopants region 8 as shown in FIG. 24.

A second exemplary embodiment consists of a second base layer 8 extended under the source region, together with an etched contact through the source region 7 to reach the second base layer 8 as shown in FIG. 32. The advantage of the second exemplary embodiment is that it does not require the use of the additional masks to structure the source region 7 and second base region 8.

The inventive design is also suitable for a reverse conducting structure by introducing n type dopants at the collector side to produce collector shorts 18, and an internal anti-parallel diode structure as shown in FIG. 33.

An enhancement layer or fourth dopants of lightly doped n conductivity type can be implanted and diffused before the first dopants implant as shown in FIG. 34. The fourth dopants of n conductivity type are implanted into the substrate 4 using the structured gate electrode layer with its opening as a mask, resulting in a fourth implant region 17. Afterwards, the implanted fourth dopants are diffused into the substrate 4. The fourth dopants are preferably Phosphorous ions. The fourth dopants are preferably implanted with an energy of 20-100 keV and / or a dose of 5×10^{12} / cm^2 to 5×10^{13} / cm^2. The fourth dopants are driven into a maximum depth between 2 µm and 8 µm, in particular between 2 and 6 µm and in particular between 2 and 4 µm. As shown in FIG. 34, the fourth dopants are not only driven into the substrate 4 in a direction perpendicular to the surface, but they are spread out laterally.

It is possible to apply the invention to a method for the manufacturing of semiconductor devices, in which the conductivity type of all layers is reversed, i.e. with a lightly p doped substrate etc.

Reference list

1 : inventive planar MOS cell power semiconductor device

3 : emitter metallization (electrode)

31 : emitter side

2 : collector metallization (electrode)

21 : collector side

4 : drift layer, substrate

5 : buffer layer

6 : collector layer

7 : n source layer

8 : p second base layer

9 : p first base layer

10 : planar gate electrode, electrically conductive layer

10`: uncovered gate electrode

11: trench gate electrode, electrically conductive layer

11`: trench region gate electrode with different dimensions

12 : insulating gate oxide gate electrode for planar gate

12` : insulating gate oxide gate electrode for trench gate

13 : insulation layer for planar cell and trench cell

14: emitter contact opening

15 : horizontal channel for planar gate

16: vertical channel for trench gate

17: enhancement layer

18 : collector shorts

70 : source implantation step

80 : second base implantation step

90 : first base implantation step

100 : electrically conductive layer etch mask

110 : electrically conductive layer etch mask opening

111 : trench etch mask opening

120 : contact etch mask

121 : contact etch mask opening

5 200 : planar MOS cell power semiconductor device (prior art)

300 : trench MOS cell power semiconductor device (prior art)

400 : trench planar MOS cell power semiconductor device (prior art)

401 : trench planar MOS cell power semiconductor device (prior art)

500 : trench planar MOS cell power semiconductor device (prior art)

10 600 : trench planar MOS cell power semiconductor device (prior art)

700 : trench planar MOS cell power semiconductor device (prior art)

800 : planar MOS cell power semiconductor device (prior art)

C L A I M S

1. A power semiconductor, comprising:

   a drift layer of a first conductivity type, which is arranged between the emitter side and the collector side,

   a first base layer of a second conductivity type, which is arranged between the drift layer and the emitter electrode, which first base layer is in direct electrical contact to the emitter electrode,

   a source region of the first conductivity type, which is arranged at the emitter side embedded into the first base layer and contacts the emitter electrode, which source region has a higher doping concentration than the drift layer, and extends to the first and second gate electrode

   second base layer of the second conductivity type, which is arranged at the emitter side embedded into the first base layer and is situated perpendicularly deeper than the source region, and contacts the emitter electrode through a contact opening, which second base layer region has a higher doping concentration than the first base layer

   a first gate electrode, which is arranged on top of the emitter side and the first gate electrode is electrically insulated from the first base layer, the source region and the drift layer by a first insulating layer, an horizontal channel is formable between the emitter electrode, the first source region, the first base layer and the drift layer,

   a plurality of second gate electrodes, each of which is electrically insulated from the first base layer, and the drift layer by a second insulating layer and which second gate electrode is arranged orthogonally to the plane of the first base layer, and extends deeper into the drift layer than the first base layer, a vertical channel is formable between the lateral / horizontal channel, the first base layer and the drift layer ,

2. A power semiconductor according to claim 1, wherein

   - the first base is shaped with respective stripes;

   - the trenches are shaped with respective stripes in orthogonal direction to the stripes of the first base layer,

   - the stripe of the trenches is divided into rectangles spaced apart from each other by the stripes of the first base layer,

- the length of the trench rectangles can be same or some trenches can be of different length than the adjacent ones, where by means of example one trench can be etched closer of further away from the source regions than its adjacent trenches,

- the depth of the trench rectangles can be same or some trenches can be of different depth than the adjacent ones, where by means of example one trench can be etched deeper than its adjacent trenches

- the width of the trench rectangles can be same or some trenches can be of different width than the adjacent ones, where by means of example one trench can be wider than its adjacent trenches

3. A power semiconductor according to claim 1, wherein the first and second gate electrodes are electrically connected.

4. A power semiconductor according to claim 1, wherein all or some of the second gate electrodes are electrically connected to the emitter electrode.

5. A power semiconductor according to claim 1, wherein all or some of the second gate electrodes are electrically floating.

6. A power semiconductor according to claim 1, comprising:

   a buffer layer of the first conductivity type with a higher doping concentration than the drift layer, arranged between the drift layer and the collector electrode.

7. A power semiconductor according to claim 1, comprising:

   a collector layer of the second conductivity type arranged on the collector side between the drift layer and the collector electrode; or comprising:

   a buffer layer of the first conductivity type with a higher doping concentration than the drift layer, which buffer layer is arranged on the collector side between the drift layer and the collector electrode; and a collector layer of the second conductivity type, which is arranged on the collector side between the buffer layer and the collector electrode.

8. A power semiconductor according to claims 1 thru 7, wherein the first dopants are preferably boron ions and are driven into a maximum depth between 1 ı m and 5 ı m, in particular between 1 and 3 ı m and in particular between 1 and 2 ı m.

9. A power semiconductor according to claims 1 thru 8, wherein the second dopants are preferably Phosphorous or Arsenic ions and driven into a maximum depth between 0.5 ı m and 1 ı m.

10. A power semiconductor according to claims 1 thru 9, wherein the third dopants are preferably Boron ions and are driven in the wafer to a maximum depth between 0.5 ı m and 2.5 ı m, and partly or completely cover the lower part of the second region while ensuring that a lateral channel can be formed at the planar regions.

11. A power semiconductor according to claims 1 thru 10, wherein an enhancement layer of the first conductivity type is arranged between, and thereby separating, the drift layer and the first base layer.

12. A power semiconductor according to claims 1 thru 11, wherein the fourth dopants are preferably Phosphorous ions and are driven into a maximum depth between 2 ı m and 8 ı m, in particular between 2 and 6 ı m and in particular between 2 and 4 ı m.

13. A power semiconductor according to claims 1 thru 12, comprising:

    A reverse conducting type device with a collector short layer of the first conductivity type arranged at the collector side between the collector electrode and buffer layer

14. A power semiconductor according to claims 1 thru 13, wherein the distance between the second wall of the trench recess and the first wall of the adjacent trench in the lateral direction in the planar view may be in a range from about 5 ı m to below 0.1 ı m, more preferably from 1 ı m to 0.1 ı m

15. A power semiconductor according to claims 1 thru 14 wherein the distance between adjacent trenches in the longitudinal direction of the trenches in the planar view extends approximately in a range from about 20 ı m to about 1 ı m, preferably from 5 ı m to 1 ı m, and more preferably from 2 ı m to 1 ı m.

16. A power semiconductor according to claims 1 to 15 wherein the device has a stripe layout design or cellular layout design.

17. A method for manufacturing a power semiconductor, the method comprising:

    providing a lowly doped wafer of a first conductivity type having an emitter side and a collector side, forming a drift layer;

    applying a mask and etching a trench recess on the first main side of the substrate of a first conductivity type;

    forming a first oxide layer on a first main side of a substrate of a first conductivity type;

    producing a structured gate electrode layer with at least one opening on the first main side on top of the first oxide layer;

using the structured gate electrode layer on the first main side as a mask for implanting a first dopant of a second conductivity type, which is different than the first conductivity type, into the substrate on the first main side for forming a well;

diffusing the first dopants into the substrate;

5 using the structured gate electrode layer on the first main side as a mask for implanting second dopants of a first conductivity type into the substrate on the first main side;

diffusing the second dopants to a lower depth than the first dopants for forming a source contact;

10 using the structured gate electrode layer for implanting third dopants of a second conductivity type into the substrate on the first main side to a depth higher than the second dopants;

diffusing the third dopants into the substrate, characterized in that, the third dopants are diffused to a lower depth than the first dopants;

15 forming a second insulating layer on the first main side;

etching a contact opening through the insulating layer and the second dopants and by filling a resulting contact opening with metal.

18. A method for manufacturing a power semiconductor, the method comprising:

providing a lowly doped wafer of a first conductivity type having an emitter side and

20 a collector side, forming a drift layer;

applying a mask and etching a trench recess on the first main side of the substrate of a first conductivity type;

forming a first oxide layer on a first main side of a substrate of a first conductivity type;

25 producing a structured gate electrode layer with at least one opening on the first main side on top of the first oxide layer;

using the structured gate electrode layer on the first main side as a mask for implanting a first dopant of a second conductivity type, which is different than the first conductivity type, into the substrate on the first main side for forming a well;

30 diffusing the first dopants into the substrate;

applying a mask and using this mask together with the structured gate electrode layer on the first main side as a mask for implanting second dopants of a first conductivity type into the substrate on the first main side;

diffusing the second dopants to a lower depth than the first dopants for forming a
5 source contact;

applying a mask and using this mask together with the structured gate electrode layer for implanting third dopants of a second conductivity type into the substrate on the first main side to a depth higher than the second dopants;

diffusing the third dopants into the substrate, characterized in that, the third dopants
10 are diffused to a lower depth than the first dopants;

forming a second insulating layer on the first main side;

etching a contact opening through the insulating layer and by filling a resulting contact opening with metal.

19. The method for manufacturing an insulated gated bipolar transistor, according to
15 claim 17 and claim 18, wherein the first dopants are preferably implanted with an energy of 20-100 keV and / and a dose of 5×10^{13} / cm^2 to 2×10^{14} / cm^2.

20. The method for manufacturing an insulated gated bipolar transistor, according to claims 17 thru 19, wherein the second dopants are preferably implanted with an energy of 100 -160 keV and / and a dose of 1×10^{15} / cm^2 to 1×10^{16} / cm^2.

20 21. The method for manufacturing an insulated gated bipolar transistor, according to claims 17 thru 20, wherein the third dopants are preferably implanted to a higher depth than the second region with an energy of 100 -160 keV and a dose of 1×10^{15} / cm^2 to 1×10^{16} / cm^2.

22. The method for manufacturing an insulated gated bipolar transistor, according to
25 claims 17 thru 21, wherein the fourth dopants are preferably implanted with an energy of 20-100 keV and a dose of 5×10^{12} / cm^2 to 5×10^{13} / cm^2.

23. Semiconductor module package comprising a single or multiple device according to claims 1 to 22.

24. Converter with a plurality of devices according to any of the claims 1 to 23.

Intellectual Property Office

Application No:	GB1911357.0	**Examiner:**	Mr Steve Morgan
Claims searched:	1-16	**Date of search:**	20 February 2020

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
X	1-16, 23 & 24	WO2018/034818 A1 (ZENG) See figures 2-6 & 8b in particular
X	1, 3-16, 23 & 24	US2017/0110562 A (CHEN) See figures

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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Field of Search:

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H01L

The following online and other databases have been used in the preparation of this search report

WPI, EPODOC

International Classification:

Subclass	Subgroup	Valid From
H01L	0029/10	01/01/2006
H01L	0029/423	01/01/2006
H01L	0029/739	01/01/2006