OPIC
Office de la propriété intellectuelle du Canada

CIPO
Canadian Intellectual Property Office

(12) (19) (CA) **Brevet-Patent**

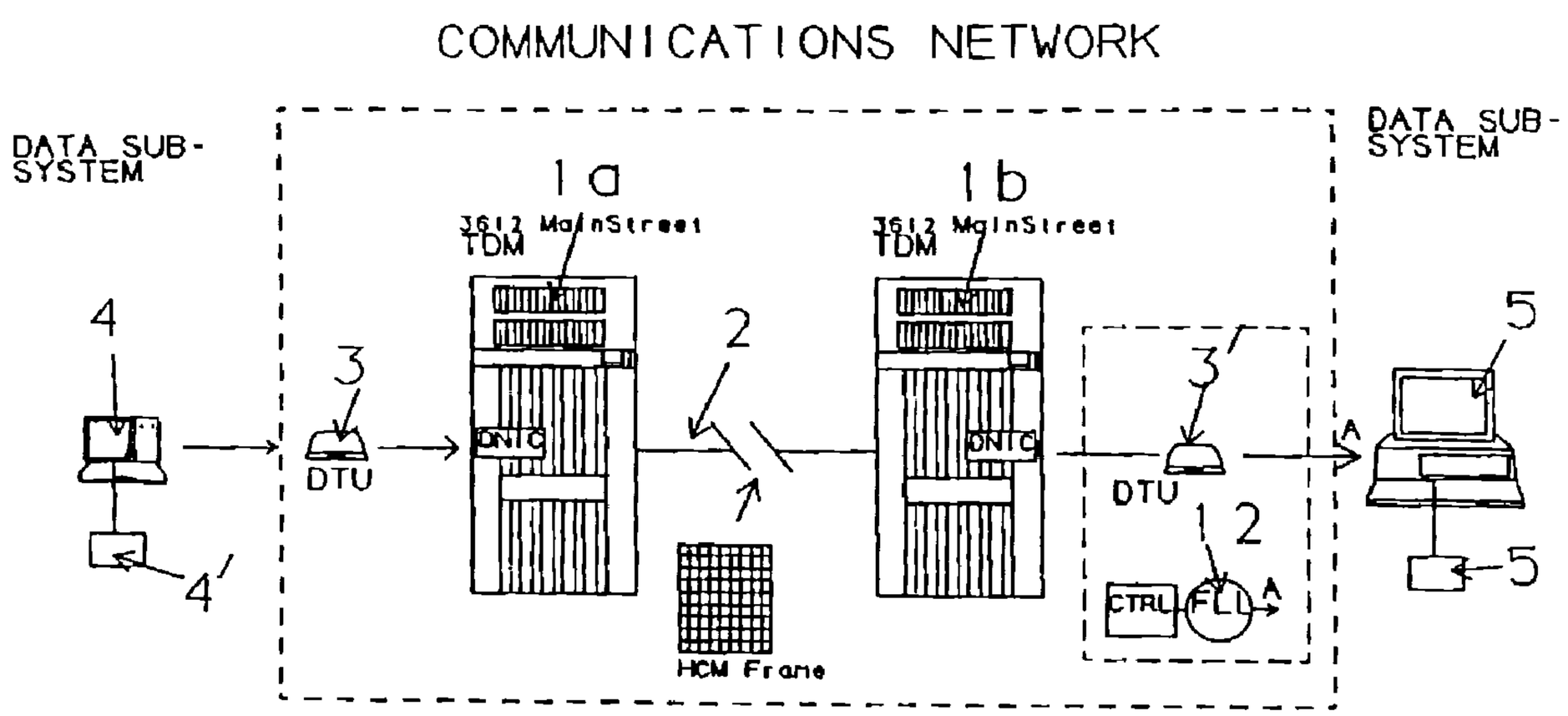
(11) (21) (C) **2,019,649**
(22) 1990/06/22
(43) 1991/12/22
(45) 2000/05/02

(72) Gallant, Denis, CA
(73) Newbridge Networks Corporation, CA

(51) Int.Cl.[5] H04J 3/06

(54) **SYSTEME DE TRANSMISSION DE DONNEES NUMERIQUES**

(54) **DIGITAL DATA TRANSMISSION SYSTEM**



(57) A digital data transmission system comprises at least two data sub-systems connected to respective data termination units interconnected via a time-division multiplexed communications network having an internal system clock. The DTUs are part of the communications network and have their internal timing slaved to the network. The data sub-systems have independent timing from the communications network and therefore data sub-systems clocks will be liable to drift relative to the DTU clocks. The incomin data stream is applied to a FIFO memory, whose state is used to identify overate or underate conditions in the the transmitting sub-system. Clock adjustment data is transmitted with communications data in a superframe consisting of n frames of m bits each (where n, m are integers), and the received data steam is adjusted in accordance with said clock adjustment data to compensate the received bit stream for overate or underrate conditions.

ABSTRACT OF THE DISCLOSURE

A digital data transmission system comprises at least two data sub-systems connected to respective data termination units interconnected via a time-division multiplexed communications network having an internal system clock. The DTUs are part of the communications network and have their internal timing slaved to the network. The data sub-systems have independent timing from the communications network and therefore data sub-systems clocks will be liable to drift relative to the DTU clocks. The incomin data stream is applied to a FIFO memory, whose state is used to identify overate or underate conditions in the the transmitting sub-system. Clock adjustment data is transmitted with communications data in a superframe consisting of n frames of m bits each (where n, m are integers), and the received data stream is adjusted in accordance with said clock adjustment data to compensate the received bit stream for overate or underrate conditions.

This invention relates to a digital data transmission system, and more particularly to a system applicable to a communications network connected to data sub-systems.

In a data transmission system comprising local devices communicating through a communications network via respective DTUs (data termination units), each local device has its own clock, which may deviate from the communications network system clock. If the local clocks drift too far from the network clock, loss of data will result as data bits are dropped from the transmission or missed by the receiving DTU.

In order to transmit clock data from a over a network, it is known to compare the phase of the network clock with that of the transmitting network to derive coded phase information which is transmitted over the data channel along with the data. This requires that the data channel have a bandwith higher than the bandwith of the data. For example, in one scheme a 16kb/s channel is used for a 9.6 kb/s data rate. In another scheme the data is transmitted over a primary data channel, with the phase information being sent over a secondary channel. In both cases, the phase information is used to drive a voltage-controlled-oscillator so that the received data is output to the receiving data network at the clock rate of the transmitting network.

A disadvantage with the above schemes is that they are expensive to implement and ill-suited to communications networks, where data loss may occur in the network, resulting in mismatch at the receiving end. Such schemes mainly have applicability to computer - PBX (Private Branch Exchange) on-premise environments.

An object of the present invention is to alleviate the aforementioned disadvantages by reducing the risk of data errors when the local clocks drift from the network clock by as much as 50 bits per second and by providing an effective

solution of reduced complexity applicable to communications networks.

According to the present invention there is provided a digital data transmission system comprising: respective data transmitting and receiving data sub-systems connected to respective transmitting and receiving data termination units (DTUs) forming part of a time-division multiplexed communications network having an internal system clock, said communications network establishing a data channel between said DTUs; said transmitting sub-system having an associated sub-system clock liable to drift; each DTU having a FIFO (First-in First-out) memory, the data to be transmitted being applied to the FIFO of the transmitting DTU, and the received data appearing at the output of the FIFO of the receiving DTU, said FIFOs operating at the clock rate of the communications network; means for monitoring the amount of data in the transmitting FIFO; means for speeding up or slowing down the rate of transmission of data through the network according to whether said amount of data in the transmitting FIFO is above or below predetermined threshold values; means for monitoring the amount of data in the receiving FIFO; variable rate output clock means determining the rate at which data is output from said receiving FIFO, the rate of said output clock means being controlled to maintain the amount of data in said receiving FIFO to be within predetermined threshold values; and the clock rate of the receiving data subs-system being slaved to said output clock means.

Preferably, a secondary channel is employed, such that when overrate conditions occur extra data can be transmitted through the secondary channel, and when underate conditions occur dummy bits can be inserted in the nmain channel with an appropriate instruction to remove the dummy bits at the receiving end being transmitted over the secondary channel.

Clock adjustment data is transmitted with communications data in a superframe consisting of n frames of m bits each (where n, m are integers), and the received data stream is adjusted in accordance with said clock adjustment data to compensate the received bit stream for overate or underrate conditions in the transmitting sub-system.

Preferably, the superframe is an HCM (high capacity multiplexing) frame consisting of sixteen TDM frames, each containing one signalling bit. Two bits (KO, K1) of the superframe carry clock adjustment data according to the following scheme:

K1	KO	Operation
1	1	No adjustment required
1	0	Transmit clock is underspeed. Delete data bit following the KO signal bit. The deleted data bit was used as a filler bit.
0	1	Transmit clock is overspeed. Insert data bit "1" in front of the data bit normally following the KO signalling bit.
0	0	Transmit clock is overspeed. Insert a data bit "0" in front of the data bit normally following the KO signalling bit.

In accordance with this scheme, data that would otherwise be lost is inserted into the transmitted bit stream to be recovered at the receiving end, or a filler bit is added in order to prevent the incoming bit stream becoming out of sync. Loss of data can thus be prevented even when the local clocks drift apart by up to 50 bits per second, and there is no requirement that they be locked in sync.

The invention will now be described in more detail, by way of example only, with reference to the accompanying drawings, in which:-

Figure 1 is a diagram illustrating a digital data transmission system in accordance with one embodiment of the present invention;

Figure 2 is a block diagram showing in more detail the clock drift compensation scheme employed in the system shown in Figure 1; and

Figure 3 is a more detailed diagram of the encoding circuits shown in Figure 2.

The data transmission scheme shown in Figure 1 comprises a pair of 3612 MainStreet network controllers 1a, 1b connected via a T1 or CEPT (Conférence Européan des Postes et Télécommunications) time division multiplex data communications link 2. The MainStreet controllers 1a, 1b are connected to respective DTUs (data termination units) 3, 3' which in turn are connected respectively to a transmitting local terminal 4 and a receiving local terminal 5. The entire communications network, including the DTUs 3, 3', operates at the network clock rate B, which may be different from the clock rates of the local terminals 4, 5.

The local terminal 4 has local clock 4' which is liable to drift from the network clock B by as much as +/- 0.01%. The transmitting terminal 4 transmits a 2.4 kbps sub-rate data stream to the transmitting MainStreet controller 1a. The local terminal 5 needs to derive its timing 5' from local terminal 4' in order for error free data transmission to occur between the two data sub-systems.

In the absence of any special measures, a drift in the clock rates of the local devices 4 and 5 will cause data loss. If the clock of the transmitting device 4 is underspeed, gaps will occur in the data stream, and similarly if it is overspeed bits will be lost in the outgoing bit stream.

The clock 5′ in the receiving device 5 is therefore slaved to the clock 12 in the receiving DTU 3′. Data is output from the receiving DTU 3′ at this clock rate, i.e. the clock rate of the local terminal 5. The receiving clock 12 consists of a digital FLL (frequency lock loop) whose clock rate is controlled by adjustment data carried by the incoming bit stream in a manner that will be described in more detail below. Alternatively, the receiving clock 12 could be a voltage-controlled oscillator or other suitable device.

Figure 2 shows in more detail the scheme for transmitting clock information through the communications network.

The transmitted bit stream at data rate A determined by clock A is input to a FIFO (first-in first-out) transmit memory 10 in the clock A time domain. The data is then output from the FIFO 10 in the clock B domain at data rate B, clock B being the internal system clock for the communications network controlled by network controllers 1a, 1b. Data is transmitted over the communications link in the clock B domain, along with rate adjustment data, through data encoders 14 to the FIFO (first-in first-out) receive memory 11 connected to frequency-locked loop (FLL) 12 to which clock 5′ of the receiving device is slaved. The incoming bit stream is output from the FIFO memory 11 at data rate A, which is adjusted to the data rate A of the transmitting device clock by the data adjustment data transmitted in the signalling bits of the superframe sent over the communications link 2, consisting of a main data channel 2a and a 50 bps side channel 2b.

When the clock rate A of the incoming bit stream exactly matches the rate B, the amount of data in the FIFO 10 remains stable and no adjustment is required. If rate A exceeds rate B, the amount of data in 10 will increase until the high threshold (HT) is reached, at which point encoder circuit 14 causes data to be transmitted over side channel 2b indicating

that extra data bits are to be inserted at the receiving end. When the contents of FIFO 10 fall below HT, encoder circuit indicates that no further bits are to be added. When the contents of FIFO 10 fall below the low threshold (LT), dummy bits are added in the data channel 2a and signals sent over the side channel 2b indicating that these dummy bits are to be removed at the receiving end.

The clock adjustment data is transmitted in a signalling superframe of an HCM (high capacity multiplexing) scheme. The HCM frame consists of ten frames, 0 to 9, each consisting of eight bits. The HCM framing pattern is transmitted in a sequence covering four HCM frames, where the first three HCM frames commence with a framing bit and the fourth HCM frame commences with an alarm indication bit for reporting lost of superframe sync to the receiver. Frame 0 is transmitted first, followed by frames 2 to 9.

The framing pattern is illustrated in more detail in Table 1 below:

Table 1: HCM Frame Structure

HCM#	Frame #'s	I	b0	b1	b2	b3	b4	b5	b6	b7
	0	F1	X	X	X	X	X	X	X	
	1	X	X	X	X	X	X	X	X	
1	2	X	X	X	X	X	X	X	X	
	3	X	X	X	X	X	X	X	X	
	9	X	X	X	X	X	X	X	X	
	0	F2	X	X	X	X	X	X	X	X
	1	X	X	X	X	X	X	X	X	
2	2	X	X	X	X	X	X	X	X	

		9	X	X	X	X	X	X	X	X	
		0	F3	X	X	X	X	X	X	X	
		1	X	X	X	X	X	X	X	X	
5	3	2	X	X	X	X	X	X	X	X	
		9	X	X	X	X	X	X	X	X	
		0	L	X	X	X	X	X	X	X	X
		1	X	X	X	X	X	X	X	X	
10	4	2	X	X	X	X	X	X	X	X	
		9	X	X	X	X	X	X	X	X	
		0	F1	X	X	X	X	X	X	X	
	5	1	X	X	X	X	X	X	X	X	
15		2	X	X	X	X	X	X	X	X	

In the above table, HCM# represents an HCM frame, Fx, framing bits, L loss of sync bit, and X data bits. Frame 0 is transmitted first, in each HCM frame, followed by frames 2 to 9. In each frame 0 is transmitted first, followed by bits 1 to 7.

HCM also serves as a highly efficient sub-rate multiplexing protocol. The total data and signalling bandwidth, X bits, is 63.2 kbps, which is 98.75% of DSO (Digital Signal - ϕ) (base 64 k digital channel). The total framing and LOS (Loss of Synchronization) alarm bandwidth is 800 bps (i.e. 1.25% of DSO) is 600 bps for framing and 200 bps for LOS alarm.

Each HCM superframe does not require the full DSO bandwidth. It can operate anywhere from 1 (8 kbps) 8 (64 kbps) bits wide. The first bit transmitted in each superframe should also be the F1 framing bit.

As shown from the frame structure in Table 1 above, the HCM framing signal is a 3-bit pattern (F1, F2, and F3) with a don't care (L bit) every fourth HCM frame. The framing bits are located in the first bit of each HCM (bits 0).

The framing bits (F1, F2, F3) add-up to a Framing bandwidth of 600 bps for HCM which is 0.9375% of the total channel (DSO).

The L bit is an alarm indication bit in HCM for indicating a Loss of Framing condition to the far end transmitter. The L bit is transmitted once every fourth HCM frame by taking a bit from the framing signal. The bandwidth allocated to the L bit is 200 bps (0.3125% of DSO). If the L bit is de-bounced once, then it will have a reaction time of 10 ms (1/200 Hz X 2).

There are a total of 79 bits per HCM frame which can be used for "user data" transfer and end-to-end signalling. This bandwidth is totally flexible and any combination of data ports from Table 1 that will fit into these 78 bits is allowed. HCM is a synchronous scheme for Sync data; but will handle Async data if the Async data stream is processed by an Async-to-Sync converter first. If the data stream is not synchronized to the system timing (DSO clock), the HCM scheme will use the extra bandwidth in the associated signalling channel to accommodate the overspeed or underspeed data port.

Some examples of "user data traffic" that can be accommodated (without and with signalling) by one HCM formatted DSO channel are the following:

		Without Signalling	With Signalling
1)	1 x 56	70	71

	2)	1 x 48	60	61
		1 x 9.6	12	13
		Total	72 bits	74 bits
	3)	1 x 38.4	48	49
		1 x 19.2	24	25
		Total	72 bits	74 bits
	4)	3 x 19.2	72 bits	75 bits
	5)	6 x 9.6	72 bits	78 bits
	6)	1 x 19.2	24	25
		2 x 9.6	24	26
		3 x 4.8	18	21
		1 x 2.4	3	4
		Total	69 bits	76 bits

Signalling in

HCM is optional and carries the following information when present:

- o Data Interface Control Leads
- o add/delete slip bits for independent clock transport
- o End-Point (EP) type
- o EP Synchronization status

When present, signalling in HCM for a data channel is always an 800 bps channel (1 bit/SF) (Superframe) with the associated Data channel. The 1-bit signalling channel is always located in the bit position just preceding the Data channel as shown in Table 4 below.

Table 2: Signalling Channel Examples

HCM# Frame #'s	I	b0	b1	b2	b3	b4	b5	b6	b7
0	Fx	S1	D1	D1	D1	X	X	X	
1	X	X	X	X	X	X	X	X	
2	S2	D2	D2	D2	D2	D2	D2	D2	
3	D2	D2	D2	D2	D2	X	X	X	
9	X	X	D3	D3	D3	D3	D3	D3	

Fx - Framing bit
Sx - Signalling bits
Dx - Data bits

S1, D1 - A 2.4 kbps channel with signalling.
S2, D2 - A 9.6 kbps channel with signalling.
D3 - A 4.8 kbps channel without signalling.

The HCM signalling superframe channel is defined as a sequence of bits which are transmitted serially one per HCM frame with a repetition period of 16 SF (Signalling SF). The Signalling SF (SSF) (Signalling Superframe) bit assignment is shown in the following table:

Table 3: SSF Bit Definition

HCM#	Name	Description	Definition
1	F1	Framing bit 1	See below
2	F2	Framing bit 2	See below
3	KO	Slip bit information	
4	K1	Slip bit information	
5	EPG	End-Point Gender	1=DCE; 0=DTE
6	DTR/DSR		1=OFF; 0=ON
7	RTS/DCD		1=OFF; 0=ON

	8	LOS	Loss of Sync status	1=OUT; 0=IN SYNC
	9	ALB/CTS		1=OFF; 0=ON
	10	RDL/RI		1=OFF; 0=ON
	11	DSR/DTR		1=OFF; 0=ON
5	12	DCD/RTS		1=OFF; 0=ON
	13	CTS/ALB		1=OFF; 0=ON
	14	RI/RDL		1=OFF; 0=ON
	15	RTS/DCD		1=OFF; 0=ON
	16	LOS	Loss of Sync status	1=OUT; 0=IN SYNC
10				
	17	F3	Framing bit 3	See below
	18	F4	Framing bit 4	See below
	19	KO	Slip bit information	
	20	K1	Slip bit information	
15	21	EPG	End-Point Gender	1=DCE; 0=DTE
	22	DTR/DSR		1=OFF; 0=ON

F1, F2, F3, and F4:
The F bits provides the framing for establishing Sync with the SSF. The framing pattern for the SSF is as follows:

20 F1 - 0
F2 - 1
F3 - 1
F4 - 0

The End-Point Gender (EPG) bit is for distinguishing the type
25 of device immediately attached to the EP termination unit. The EPG bit will indicate the simulation mode of the EP unit. For an attached DTE (Data Terminal Equipment) device, the EP simulates a DCE (EPG=1) and for an attached DCE (Data Communications Equipment) device; the EP is configured as a
30 DTE (EPG=0).

The RS-232 signal names in the above table refer to the interface control leads to/from an attached DTE (symbol on left of slash) or DCE (symbol on right of slash) device.

When attached to a DTE device, the transmitted DTR/DSR bit will be equivalent to the state of the DTR signal from the DTE. When attached to a DCE device, the transmitted DTR/DSR bit will be equivalent to the state of the DSR signal from the attached DCE device.

The RTS/DCD (Ready-to-Send/Data Carrier Detect) bit is repeated two times in the SSF in order to get shorter propagation delays for RTS/DCD signals. The propagation delay for RTS/DCD is 10 ms when repeated every two bit position in the SSF. The propagation delay for the other bits is 20 ms.

When attached to a DTE device, the transmitted RTS/DCD bit will be equivalent to the state of the RTS signal from the DTE. When attached to a DCE device, the transmitted RTS/DCD bit will be equivalent to the state of the DCD signal from the attached DCE device.

When attached to a DTE device, the transmitted ALB/CTS bit will be equivalent to the state of the ALB signal from the DTE. When attached to a DCE device, the transmitted ALB/CTS bit will be equivalent to the state of the CTS signal from the attached DCE device.

When attached to a DTE device, the transmitted RDL/RI bit will be equivalent to the state of the RDL signal from the DTE. When attached to a DCe device, the transmitted RDL/RI bit will be equivalent to the state of the RI signal from the attached DC device.

When attached to a DTE device, the transmitted DSR/DTR bit will be equivalent to the state of the DSr signal to the DTE. When attached to a DCe device, the transmitted DSR/DTR bit will be equivalent to the state of the DTR signal to the attached DCE device.

When attached to a DTE device, the transmitted DCD/RTS bit will be equivalent to the state of the DCD signal to the DTE. When attached to a DCE device, the transmitted DCD/RTS bit will be equivalent to the state of the RTS signal to the attached DCE device.

When attached to a DTE device, the transmitted CTS/ALB bit will be equivalent to the state of the CTS signal to the DTE. When attached to a DCE device, the transmitted CTS/ALB bit will be equivalent to the state of the ALB signal to the attached DCE device.

When attached to a DTE device, the transmitted RI/RDL bit will be equivalent to the state of the RI signal to the DTE. When attached to a DCE device, the transmitted RI/RDL bit will be equivalent to the state of the RDL signal to the attached DCe device.

These are the bits used for handling the independent clocks. They are coded as follows:

K1	K0	Operation	Example (K0,D1,D2,...
1	1	No Adjustment required	D1 D2 D3...
1	0	Delete next data bit after KO	D2 D3....
0	1	Insert a "1" bit just preceding the next data bit after KO	1 D1 D2 D3..
0	0	Insert a "0" bit just preceding the next data bit after KO	0 D1 D2 D3...

The Loss of Sync (LOS) bit will be used to report the local EP SSf synchronization status to the remote EP. An EP will transmit LOS Low, when SSF is in SYNC and will transmit a High when SSF is out of SYNC. This bit is also transmitted twice in the SSF in order to reduce the propagation delay to 10 ms.

Figure 3 shows in more detail the encoding circuit 12. FIFO 10 is connected to a 4- bit shift register 30 having a data output connected to a superframe-forming circuit 31 and HCM Mux 32, and a control output connected to the superframe-forming circuit 31. The superframe-forming circuit 31 has 16 outputs, including K0, K1, connected to Mux 33 over an 800bps side channel, the outpur of which is connected to the HCM Mux 32.

To insert a dummy bit, in the event of an underate condition, the shift register is not shifted, which causes the previous bit to be resent.

The superframe-forming circuit 31 generates the K0,K1 bits according to the three states (below LT, between LT and HT, and above HT) of the FIFO 10. Bits K0,K1 are applied to MUx 33 from where there are input with date from shift register 30 to HCM Mux 32.

In addition to the ability to permit independent clocking of communicating devices, HCM (high capacity multiplexing) provides an efficient scheme for sub-rate multiplexing. In many schemes, the lowest speed data (for example 2.4, 9.6 kbps) is over sampled in order to make the data compatible with the high speed data rate. As a result the same data occupies the same bandwidth. The HCM sub-rate superframe multiplexing technique allows performance of up to 98% efficiency to be achieved. HCM also allows transparent data to co-exist with non-transparent data. Transparent data is data that is locked to a multiple of the 8kb/s building block rate. The data is considered "transparent" since it does not require rate adaption by the system.

The following table is a comparison of HCM and DDS (Digital Data Service) and 1.460 schemes:

Number of Channels Supported on 64 Kb/s service	Channel Rate 2.4 kb/s	4.8 Kb/s	9.6 kb/s	19.2 kb/s
HCM	24	12	6	3
DDS	20	10	5	2
1.460	8	8	4	2

Table 2-3: Comparison of Rate Adaption Schemes

The HCM frame can be viewed as a 10-row bandwidth allocation table, where each entry represents 800 b/s of aggregate bandwidth. The width of the table depends upon the bandwidth of the aggregate, with each column representing 8 kb/s of bandwidth.

The table mirrors an identical size data buffer containing the current session of data to be sent. This data is sent row-by-row until a complete HCM frame is transmitted. The process is repeated each frame with new data.

The HCM technique utilizes a 10-row table which yields a resolution of 800 b/s, since a particular bit in any single row is sent only once in every ten rows (8 k/10 = 800). Any data source that is a multiple of 800 b/s can be handled simply by being allocated the proper number of bit positions in the table. For example a 2.4 kb/s data source requires 3 bit positions (2400/3 = 800).

Transparent data (multiples of 8 kb/s) occupies a full 10-bit column in the table for each factor of 8 kb/s in its rate. For example, a 32 kb/s data rate requires four columns (32000/8000 = 4).

Unused bit positions in the table can be assigned to other date sources, both transparent or non-transparent to yield up to 98% efficiency. Transparent data, since it requires multiples of 8 kb/s, occupies full columns in the table,

where each column represents 10 * 800 b/s = 8 Kb/s. Note, the only overhead is a framing bit. Four consecutive framing bits, in four consecutive HCM frames, form a 4-bit code that makes possible frame alignment.

Signalling information such as control lines and data clock can be assigned to the HCM frame allowing handshaking and clock reference to pass through the system. The signalling bit "S" coding is spread over 16 HCM frames and information is encoded on a per port basis.

HCM Frame #	Signal	Description
1	F1	Framing Bit 1
2	F2	Framing Bit 2
3	K1	Transparent Clocking Bit 1
4	K0	Transparent Clocking Bit 0
5	EPG	End-Point Gender
6	DTR	Data Terminal Ready
7	RTS	Ready to Send
8	LOS	Loss of Sync status
9	ALB	Analog Loopback
10	RDL	Remote Digital Loopback
11	DSR	Data Set Ready
12	DCD	Data Carrier Detect
13	CTS	Clear to Send
14	RI	Ring Indicator
15	RTS	Ready to Send
16	LOS	Loss of Sync status

Table 2-4: Coding of Signalling Bits in HCM Frames

HCM used for all non-transparent data transfers

The operator defines the table locally via the Node Manager, or remotely from a Network Manager. HCM framing is impressed on all non-transparent data transfers between endpoints. Each DTU/DNIC (Digit Network Interface Card), Aggregate module, etc., is capable of

assembling and disassembling the HCM frame. As well, all internal non-transparent data transfers over the serial busses are in HCM format.

An HCM example

A 3612 MainStreet™ based system has the following interfaces:

* 64 kb/s, V.35 aggregate with HCM encoding;
* two 2.4 kb/s data channels with signalling;
* one 4.8 kb/s data channel without signalling;
* four 8 kb/s compressed voice circuits;
* one 16 kb/s compressed voice circuit.

Under many conditions HCM is more efficient than other schemes. Table 3 below shows a comparison of HCM against AT&T DDS schemes and CCITT 1.460 schemes.

The DCMs each create an HCM frame which has exactly the same general structure as the aggregate frame with a framing bit in the top left hand corner. However, the only data present in this frame is data pertaining to the DCM, itself. Also, the data occupies the same relative position as in the aggregate HCM frame.

The HCV module receives PCM data from the LGS modules and after compression, forwards this data to the aggregate module as transparent data.

The aggregate module mixes the two internal HCM frames in what is essentially an "anding" function, then adds in the transparent data from the HCV module. A framing bit is added and the compiled HCM frame is sent out by row. After ten rows, a new HCM frame begins.

The HCM framing structure is maintained (and respected) from endpoint to endpoint. In a three node, narrow-band network,

the two links can operate with different HCM framing, but the framing at the opposite ends of each link must match.

HCM2 Encoding: A super-rate enhancement
In systems that have aggregate bandwidths greater than 64 kb/s, additional frames or circuits are defined. The resulting structure is referred to as HCM2 and can contain a combination of HCM frames and transparent (unframed) data.

One circuit is defined as the "supervisory circuit" and is required to have HCM framing (and hence a framing bit). The other circuits can contain purely transparent data without any framing information or they can be HCM framed.

It will be seen therefore that the HCM scheme not only provides a convenient vehicle for permitting independent clocking of the communicating devices, but also provides a highly efficient sub-rate multiplexing scheme.

THE EMBODIMENTS OF THE INVENTION IN WHICH AN EXCLUSIVE PROPERTY OR PRIVILEGE IS CLAIMED ARE DEFINED AS FOLLOWS:

1. A digital data transmission system comprising: respective data transmitting and receiving data sub-systems connected to respective transmitting and receiving data termination units (DTUs) forming part of a time-division multiplexed communications network having an internal system clock, said communications network establishing a data channel between said DTUs; said transmitting sub-system having an associated sub-system clock liable to drift; each DTU having a FIFO (First-in First-out) memory, the data to be transmitted being applied to the FIFO of the transmitting DTU, and the received data appearing at the output of the FIFO of the receiving DTU, said FIFOs operating at the clock rate of the communications network; means for monitoring the amount of data in the transmitting FIFO; means for speeding up or slowing down the rate of transmission of data through the network according to whether said amount of data in the transmitting FIFO is above or below predetermined threshold values; means for monitoring the amount of data in the receiving FIFO; variable rate output clock means determining the rate at which data is output from said receiving FIFO, the rate of said output clock means being controlled to maintain the amount of data in said receiving FIFO to be within predetermined threshold values; and the clock rate of the receiving data subs-system being slaved to said output clock means.

2. A digital data transmission system as claimed in claim 1, wherein said network provides a side channel to said data channel, and when the amount of data in said transmitting FIFO is above said predetermined value, signals are sent over said side channel to cause extra data bits to be added at the receiving end, and when the amount of data in said transmitting FIFO falls below said predetermined value, dummy bits are sent in the data channel, and signals are sent over

said side channel to cause said dummy bits to be removed at the receiving end.

3. A digital data transmission system as claimed in claim 2, the clock adjustment data is transmitted with communications data in a superframe consisting of n frames of m bits each (where n, m are integers), and the received data stream is adjusted in accordance with said clock adjustment data to compensate the received bit stream for overate or underrate conditions in the transmitting sub-system.

4. A digital data transmission system as claimed in claim 1 or claim 2, wherein bits are added or deleted to the received bit stream in accordance with said clock adjustment data.

5. A digital data transmission system as claimed in claim 3 or claim 2, wherein said superframe contains signalling bits (K0,K1) carrying said clock adjustment data according to the following scheme:

K1	KO	Operation
1	1	No adjustment required
1	0	Transmit clock is underspeed. Delete data bit following the KO signal bit. The deleted data bit was used as a filler bit.
0	1	Transmit clock is overspeed. Insert data bit "1" in front of the data bit normally following the KO signalling bit.
0	0	Transmit clock is overspeed. Insert a data bit "0" in front of the data bit normally following the KO signalling bit.

6. A digital data transmission system as claimed in claim 1, wherein said variable rate clock means is a frequency-controlled loop.

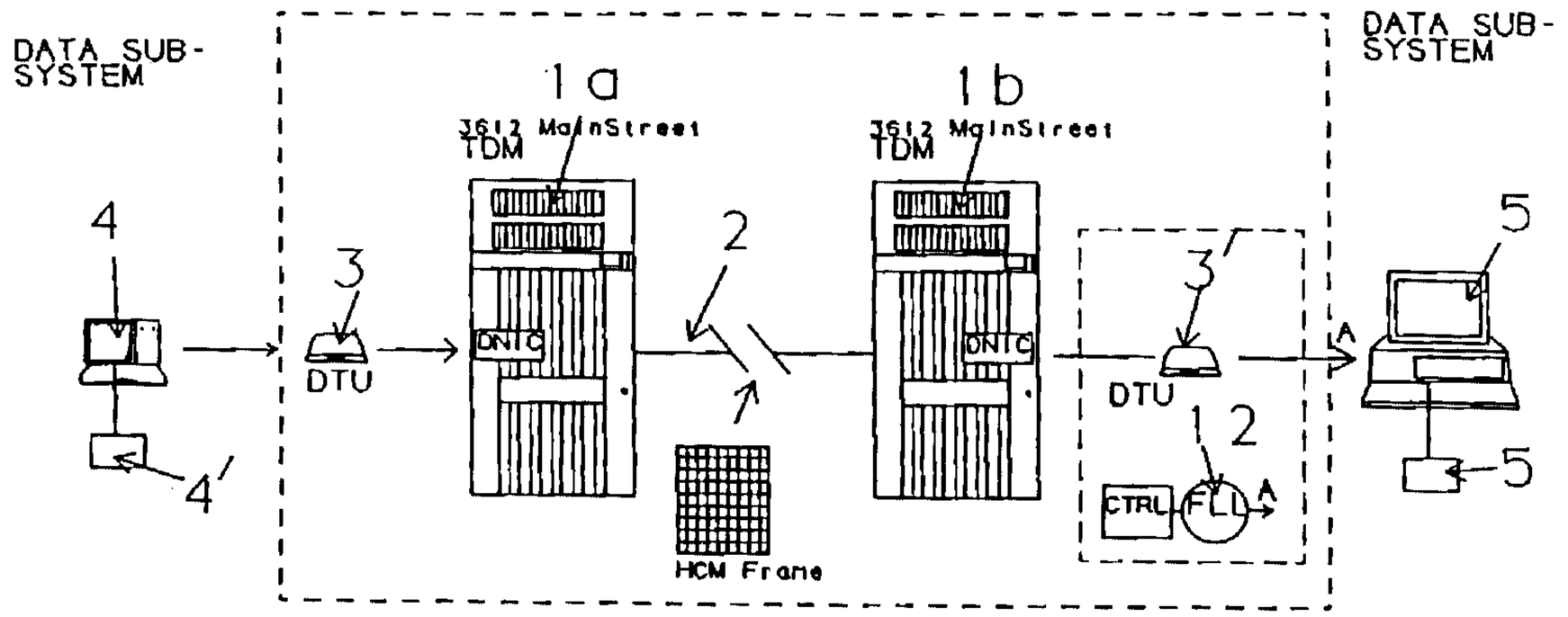

COMMUNICATIONS NETWORK
DATA SUB-SYSTEM
1a
1b
3612 MainStreet
TDM
DNTC
HCM Frame
DTU
CTRL
FLL
4
4'
3
3'
2
12
5
A

Fig 1

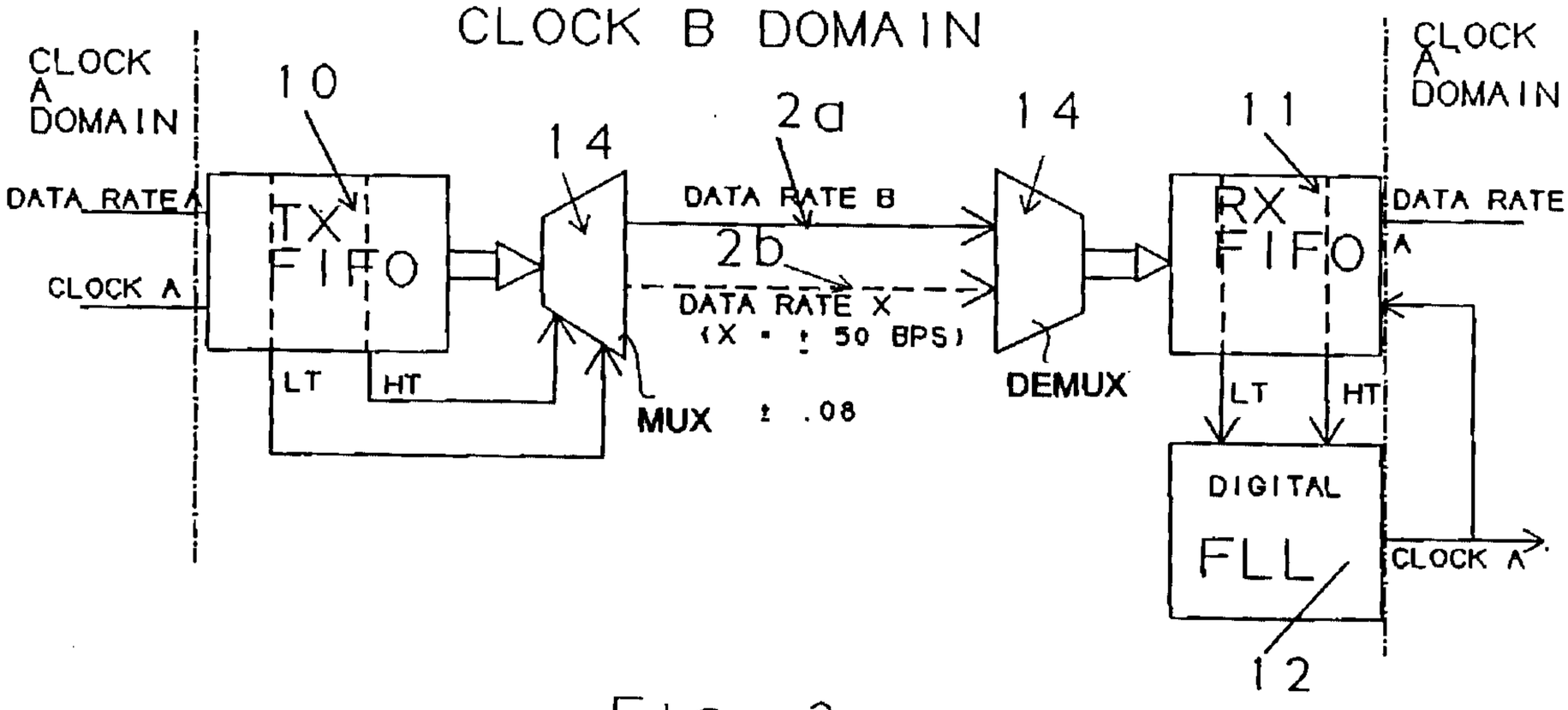

CLOCK B DOMAIN
CLOCK A DOMAIN
DATA RATE A
CLOCK A
TX FIFO
LT
HT
10
14
MUX ± .08
2a
DATA RATE B
2b
DATA RATE X
(X = ± 50 BPS)
DEMUX
11
RX FIFO
DATA RATE A
DIGITAL FLL
CLOCK A
12

Fig. 2

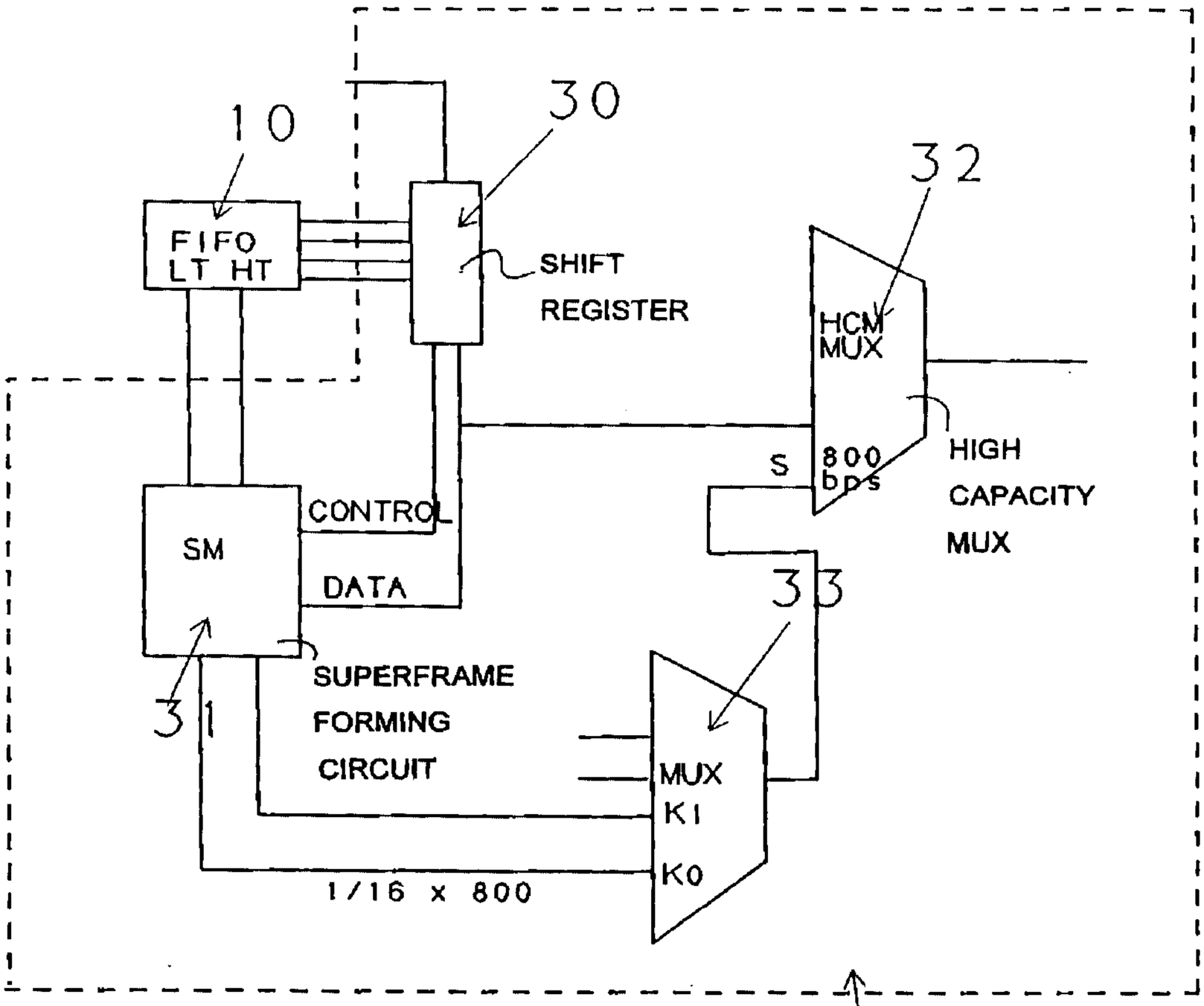

10
30
32
FIFO
LT HT
SHIFT
REGISTER
HCM
MUX
S
800
bps
HIGH
CAPACITY
MUX
CONTROL
SM
DATA
33
SUPERFRAME
FORMING
CIRCUIT
31
MUX
K1
K0
1/16 x 800
12

Fig. 3