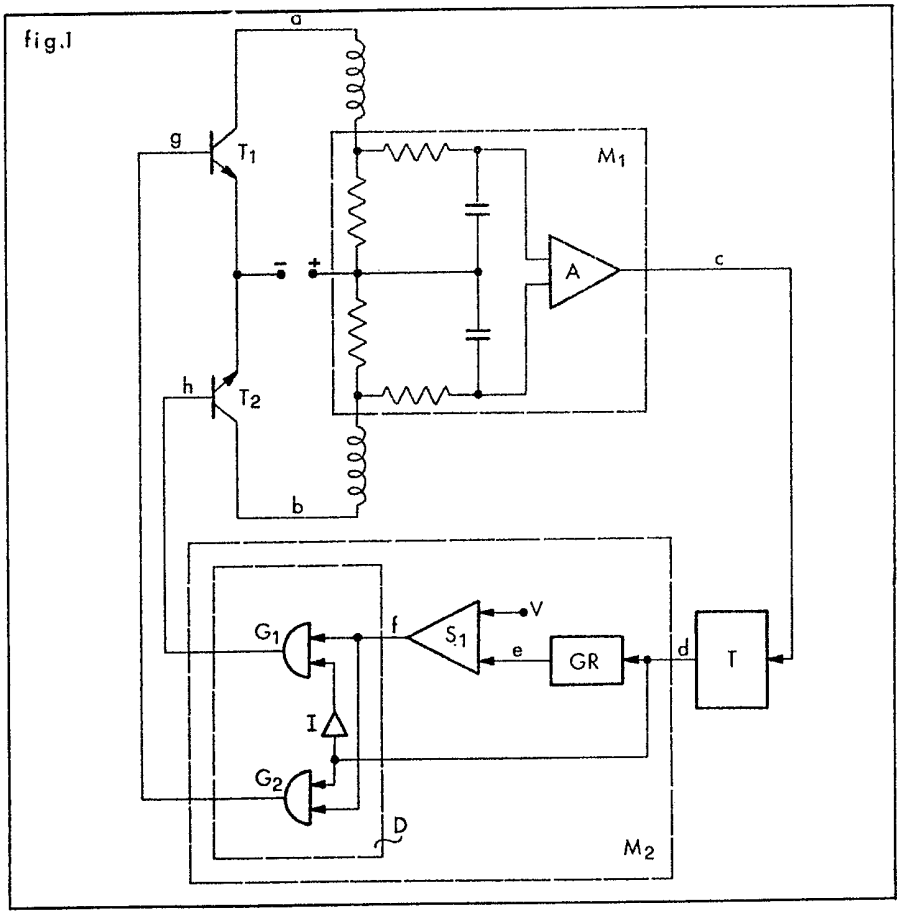
(12) UK Patent Application (19) GB (11) 2 072 964 A

(21) Application No 8109851
(22) Date of filing 30 Mar 1981
(30) Priority data
(31) 20996
(32) 28 Mar 1980
(33) Italy (IT)
(43) Application published
7 Oct 1981
(51) INT CL³
H02M 1/18 1/08
(52) Domestic classification
H2F 9GX 9K12 9K1 9N2A 9R39C 9T2 9T5 P
(56) Documents cited
GB 2012501A
GB 2004137A
GB 1569773
GB 1556342
GB 1554214
GB 1537754
GB 1525544
GB 1508423
GB 1473592
GB 1469035
GB 1421797
GB 1345062
(58) Field of search
H2F
(71) Applicants
Italtel Societe Italiana Telecomunicazioni S.p.A., Piazzale Zavattari, 12, 20149 Milano, Italy
(72) Inventors
Andrea Leti,
Enrico Valacca
(74) Agents
Marks & Clerk, 57—60 Lincoln's Inn Fields, London WC2A 3LS

(54) Circuits for making symmetrical the hysteresis loops in push-pull power supplies

(57) A circuit for making symmetrical the hysteresis loop of a push pull power supply unit comprising power transistors T_1, T_2 connected to the parts of a transformer primary winding includes means M_1 which measures the difference in the energy supplied to the transformer by the two power transistor and controls the duty cycle of a square wave generator T which controls means M_2 which supplies control signals to the power transistors to equalize the energy supplied to the parts of the primary winding. Thus, the asymmetries caused by two power transistors having different base storage times can be avoided and the efficiency of the transformer improved. M_1 includes RC circuits integrating with respect to time primary current or voltage (Fig. 4). M_2 includes a ramp generator GR reset at each transition from the generator T. The output of the ramp generator is compared with a voltage level V derived from the output voltage of the power supply unit for use in the regulation circuit. Then gates G1, G2 are alternately enabled to control the power transistors.

fig.1



GB 2 072 964 A

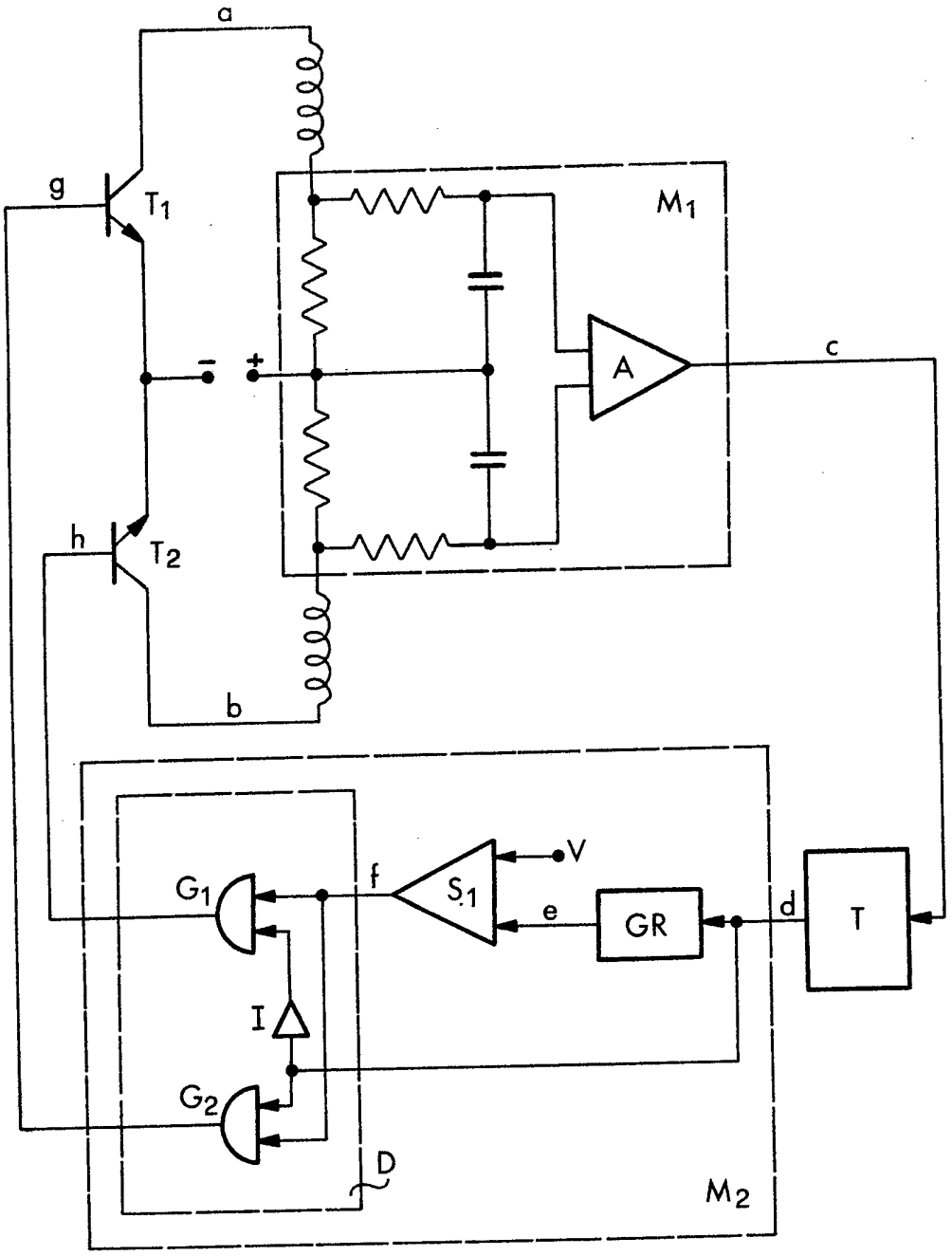


fig.1

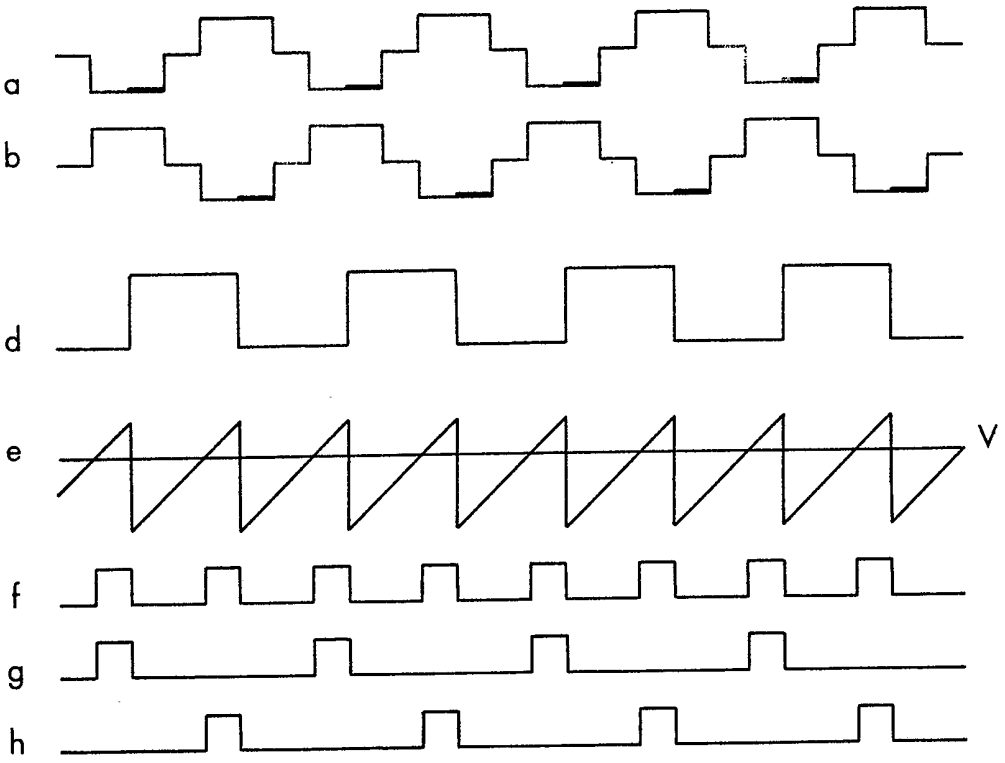


fig.2

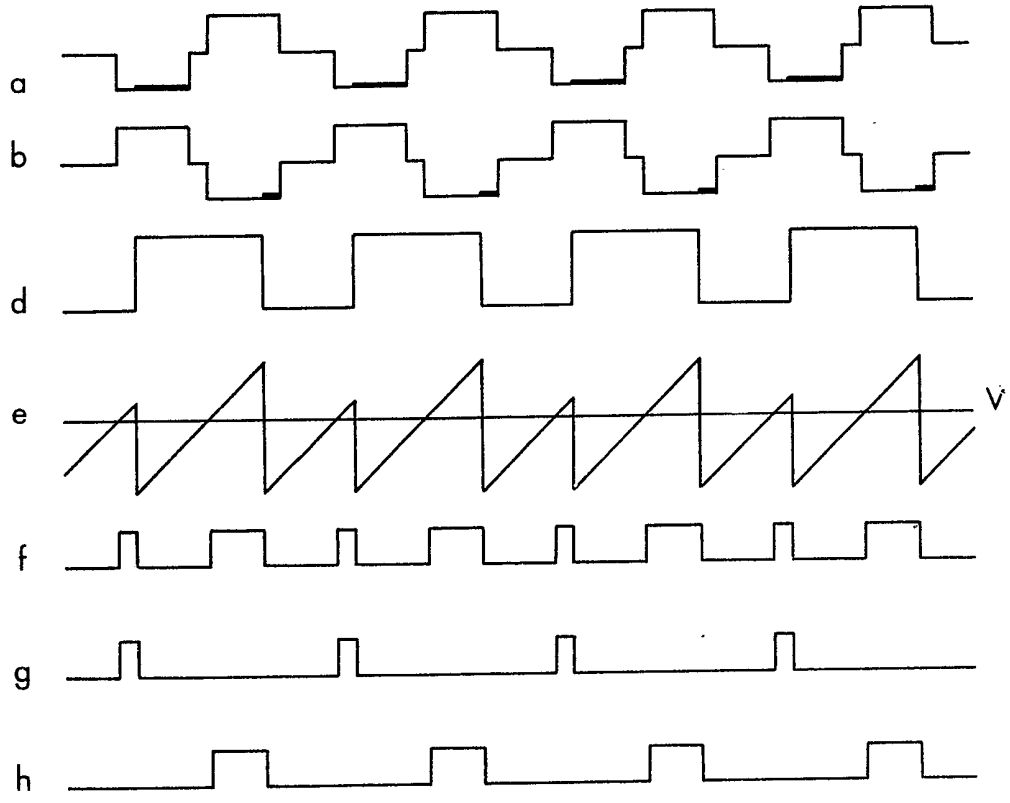


fig.3

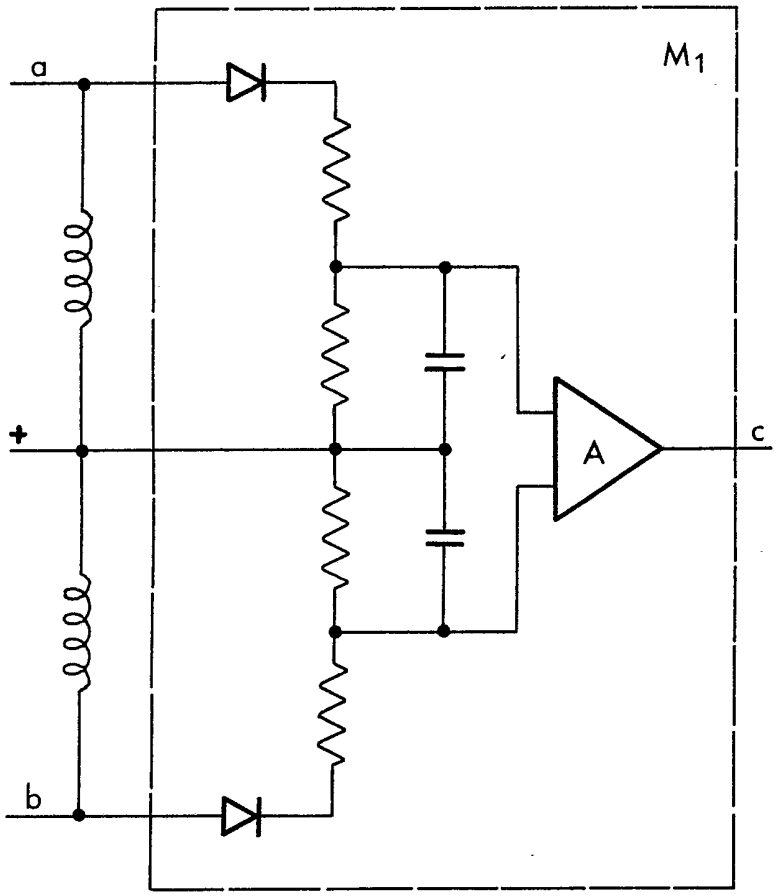


fig.4

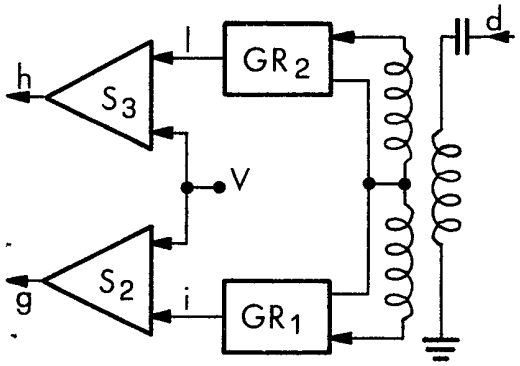


fig.5

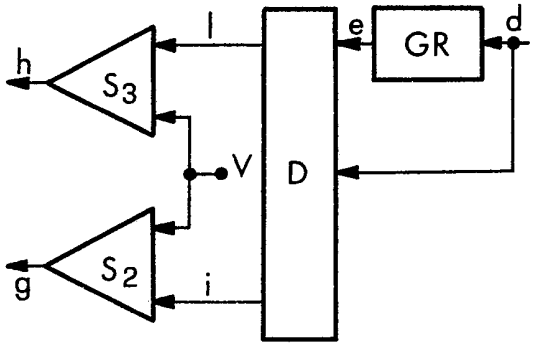


fig.8

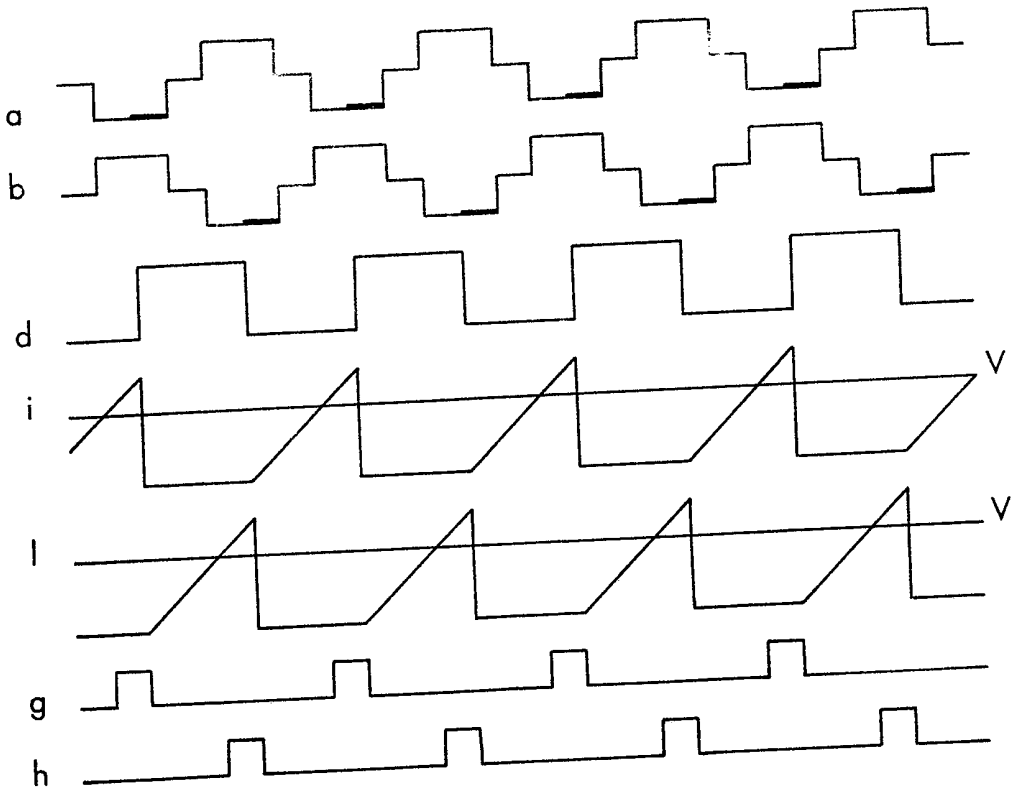


fig.6

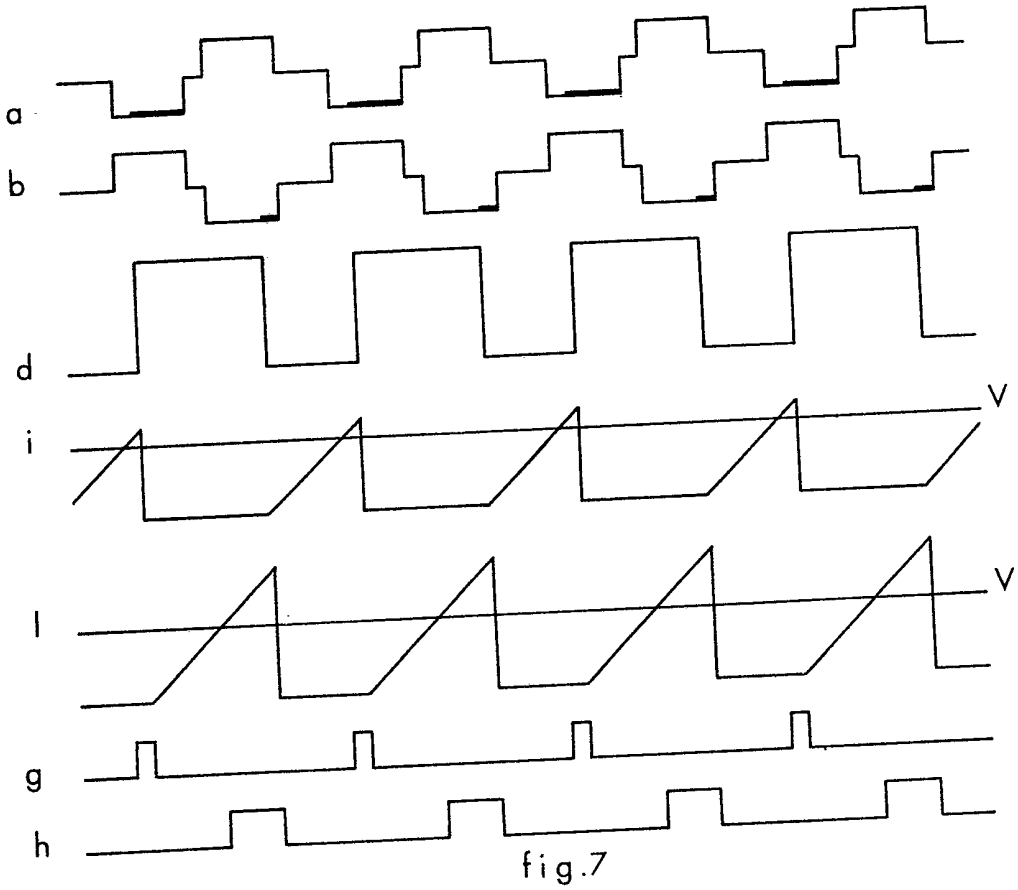


fig.7

SPECIFICATION

Improvements in or relating to circuit arrangements for making symmetrical the hysteresis loops in power supplies of push-pull type

The invention relates to a circuit arrangement for providing control pulses for power transistors of a push-pull power supply unit in order to make symmetrical the operation thereof.

A known power supply unit comprises two power transistors controlled by their bases and having one terminal (generally the emitter) connected to a pole of a direct power supply source, while the other terminal is connected to one end of a coupling transformer primary winding having the centre tip connected to the other pole of the power supply. The voltage induced across the secondary winding is filtered in order to supply a direct output voltage. The power transistors are caused to conduct alternately by constant frequency pulse signals. The output voltage is stabilized by a pulse width modulation technique i.e. regulating circuits are provided which, in response to the difference between the output voltage (or a voltage proportional to it) and a reference voltage, change the duration of the control pulses for the transistors.

By this means it is tried to make constant the energy transferred to the secondary winding (viz., the product of the voltage applied to the ends of each half primary winding with the time of application). The hysteresis loop of the flux within the transformer core is required to be symmetrical because the core is dimensioned so as not to reach saturation and to obtain maximum efficiency. This is true if the circuits connected to the primary and secondary windings of transformer are perfectly balanced. However, usually such a condition is not met and the hysteresis loop does not have the required characteristics of symmetry. This results in increased losses which become particularly noticeable if the core reaches saturation during one half cycle.

One of the main causes of dissymmetry is due to the so-called "storage time" i.e. the time elapsing between the instant when a cut-off control signal is supplied to the transistor and the instant when the transistor is actually cut-off. The storage time depends on the type of transistor, but can vary from specimen to specimen and according to the operating conditions of the transistor itself. If the control pulses supplied to the bases of the two transistors have the same duration, the periods of effective conduction of the two transistors can be different and consequently the hysteresis loop can be asymmetrical. Known control circuits for push-pull power supply units where the control pulses have a different duration so as to take into account the difference between the storage times and make equal the periods of effective conduction of the two transistors and to be somewhat complicated.

According to the invention, there is provided a circuit arrangement for making substantially symmetrical the hysteresis loop of a push-pull power supply unit comprising two power transistors connected to respective parts of a primary winding of a transformer, the circuit arrangement comprising first means connected to the primary winding parts and arranged to provide an output signal representative of the difference in energies supplied by the power transistors of the primary winding parts, a constant frequency squarewave generator whose duty cycle is arranged to be controlled by the output signal of the first means, and second means for generating control signals for controlling conduction of the power transistors in accordance with the output of the squarewave generator so as to make substantially symmetrical the hysteresis loop of the power supply unit.

The invention will be further described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 shows a circuit arrangement constituting a preferred embodiment of the invention;

Figures 2 and 3 show waveforms produced by the circuit arrangement of Figure 1;

Figure 4 shows another arrangement of first means M_1;

Figure 5 shows an alternative arrangement of second means M_2;

Figures 6 and 7 show waveforms produced by the circuit arrangement of Figure 5; and

Figure 8 shows another alternative arrangement of the second means M_2.

Figure 1 shows only the elements of a push-pull power supply unit necessary for illustrating a circuit arrangement constituting a preferred embodiment of the invention.

Power transistors T_1 and T_2 have collectors connected respective half primary windings of a coupling transformer whose secondary winding and associated circuits are not shown. Also the circuits for obtaining from the output voltage of the power supply unit a voltage level V for use in the regulation circuit are not shown as they may be of known type. The collector voltages *a*m *b* of the two transistors T_1, T_2 alternately drive currents through the two halves of the primary winding. These currents produce across two equal-value resistors connected in series between the two half primary windings two differences of potentials which are integrated with respect to time by two identical RC circuits which form part of a first means M_1. The signals at the outputs of the RC circuits are proportional to the energy transferred by the respective transistors to the corresponding half primary windings. A differential amplifier A supplies a signal *c* proportional to the difference between these energies.

Alternatively, the energy transferred by each transistor may be formed by integrating with respect to time voltage instead of current, with the first means M_1 for instance being as shown in Figure 4. The difference signal *c* controls a square-wave generator T to alter the duty-cycle of its

output *d*, which in turn controls a ramp generator GR by resetting it at each transition (either positive or negative). The signal *e* at the output of the ramp generator GR is compared with the voltage level V in a threshold circuit S_1 generating a sequence *f* of pulses which are sent alternately by a distributing circuit D to the two power transistors T_1 and T_2 (signals *g* and *h* respectively).

In the drawings, the distributor D is shown having a well-known arrangement comprising two gates G_1 and G_2 alternately enables by the signal *d* by means of an inverter 1. However, any other scheme suitable for the purpose may be used.

Figures 2 and 3 show waveforms produced by the circuit of Figure 1. Figure 2 illustrates the case of transistors having equal storage times (represented in the waveforms *a* and *b* with a thicker line) and Figure 3 illustrates the case of different storage times, where the pulses *g*, *h* are of different duration and are such that the times of effective conduction (controlled conduction + storage time) of the two transistors are made equal, the value of the reference voltage V remaining unchanged.

Figure 5 shows another possible arrangement for the second means M_2 of Figure 1. By means of an inductive coupling the square-wave signal *d* operates alternately the two ramp generators GR_1 and FR_2. Signals *i*, *l* thus obtained are compared with the voltage level V by two threshold circuits S_2, S_3 in order to generate the control pulses *g*, *h* for the transistors T_1, T_2.

Figures 6 and 7 show the waveforms produced by the arrangement of Figure 5 for storage times which are equal and different respectively.

Figure 8 shows another possible arrangement for the second means M_2 of Figure 1. A distributing circuit D (e.g. identical to that shown in Figure 1) send the ramps generated by the generator GR alternately to the two threshold circuits S_2 and S_3. The signals which are present in this arrangement have not been shown explicitly since they are similar to those indicated by the same symbols in Figures 2, 6 and 3, 7, respectively.

The variation in storage times is usually the main cause of dissymmetry of the hysteresis loop in the transformer core. Circuit arrangements constituting preferred embodiments of the invention measure the difference between the energies delivered to the two half primary windings, and consequently to the core, during each period, and can compensate the effect of all dissymmetries existing in the circuits connected to both primary and secondary windings of the transformer.

CLAIMS

1. A circuit arrangement for making substantially symmetrical the hysteresis loop of a push-pull power supply unit comprising two power transistors connected to respective parts of a primary winding of a transformer, the circuit arrangement comprising first means connected to the primary winding parts and arranged to provide an output signal representative of the difference in energies supplied by the power transistors to the primary winding parts, a constant frequency squarewave generator whose duty cycle is arranged to be controlled by the output signal of the first means, and second means for generating control signals for controlling conduction of the power transistors in accordance with the output of the squarewave generator so as to make substantially symmetrical the hysteresis loop of the power supply unit.

2. A circuit arrangement as claimed in claim 1, in which the second means comprises at least one ramp generator arranged to be controlled by the variation duty-cycle square wave signal and at least one threshold circuit arranged to compare the output of the ramp generator with a voltage corresponding to the output voltage of the power supply unit.

3. A circuit arrangement as claimed in claim 1 and 2, in which the first means comprises first and second resistors connected in series with respective primary winding parts, first and second integrating circuits arranged to integrate the voltages across the first and second resistors, respectively, and a differential amplifier whose inputs are connected to the outputs of the integrating circuits.

4. A circuit arrangement as claimed in claim 1 or 2, in which the first means comprises first and second integrating circuits arranged to integrate the voltages across the respective primary winding parts and a differential amplifier whose inputs are connected to the outputs of the integrating circuits.

5. A circuit arrangement as claimed in any one of the preceding claims, in which the second means comprises one ramp generator arranged to be reset by each transition of the variable duty cycle square wave signal, one threshold circuit arranged to compare the output of the ramp generator with a voltage corresponding to the output voltage of the power supply unit to produce a series of control pulses to the power transistors.

6. A circuit arrangement as claimed in any one of claims 1 to 4, in which the second means comprises two ramp generators arranged to be started and stopped by respective opposite polarity transitions of the variable duty cycle square wave signal, and two threshold circuits arranged to compare the outputs of the ramp generators with a voltage corresponding to the output voltage of the power supply unit to produce control pulses for the respective transistors.

7. A circuit arrangement as claimed in any one of claims 1 to 4, in which the second means comprises one ramp generator arranged to be reset by reach transition of the variatable duty cycle square wave signal, and means for distributing the ramps from the ramp generator alternately to two threshold circuits arranged to compare the ramps with a voltage corresponding to the output voltage of the power supply unit so

as to produce control pulses for the respective power transistors.

8. A circuit arrangement substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1981. Published by the Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.