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(54) **Title**: EMBEDDED MEMS SENSORS AND RELATED METHODS

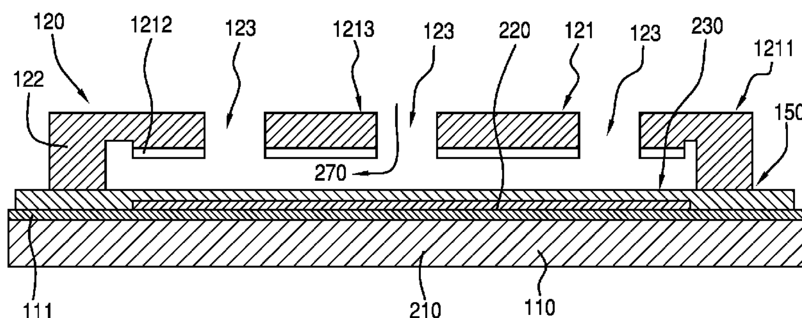

FIG. 2

(57) **Abstract**: Embodiments of embedded MEMS sensors and related methods are described herein. Other embodiments and related methods are also disclosed herein.

EMBEDDED MEMS SENSORS AND RELATED METHODS

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10 CROSS REFERENCE TO RELATED APPLICATIONS

This application claims priority to:

U.S. Patent Application 61/147,683, titled "MEMS Shock Sensor Fabricated on Flexible Substrate," and filed on January 27, 2009;

U.S. Patent Application No. 61/174,438, titled "Embedded MEMS Sensors And Related
15 Methods," and filed on April 30, 2009; and

U.S. Patent Application 61/222,451, titled "Displays With Embedded MEMS Sensors And Related Methods," and filed on July 1, 2009.

GOVERNMENT FUNDING

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TECHNICAL FIELD

25 The disclosure herein relates generally to semiconductor devices and methods of providing semiconductor devices, and relates, more particularly, to semiconductor devices for displays with embedded MEMS (Micro Electro Mechanical System) sensors and related methods.

BACKGROUND

30 In the electronics industry, flexible substrates are quickly becoming popular as a base for electronic circuits. Flexible substrates can include a wide variety of materials including, for example, any of a myriad of plastics. Once a desired electronic component, circuit, or circuits are formed over a surface of the flexible substrate, the flexible substrate can be attached to a final product or incorporated into a further structure. As an example, recent developments have fabricated display
35 matrices on flexible substrates.

MEMS (microelectromechanical system) devices have also gained in popularity in the electronics industry. Many types of MEMS devices have been developed for a myriad of applications, including MEMS sensors configured to measure pressure variations. Due to manufacturing constraints, however, the fabrication of MEMS devices has been relegated thus far to standard substrates such as silicon substrates. Integration of MEMS devices with displays and/or other devices fabricated on flexible substrates has thus been constrained.

Therefore, a need exists in the art to develop MEMS devices compatible with flexible substrates and methods to integrate the fabrication of such MEMS devices along with other devices on flexible substrates.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be better understood from a reading of the following detailed description of examples of embodiments, taken in conjunction with the accompanying figures in the drawings in which:

FIG. 1 illustrates a perspective view of a semiconductor device comprising a MEMS device according to a first embodiment.

FIG. 2 illustrates a cross-sectional view along a line 1-1 of the semiconductor device of FIG. 1.

FIG. 3 illustrates a perspective view of a semiconductor device comprising a MEMS array having the MEMS device of FIGs. 1-2.

FIG. 4 illustrates a flowchart for a method for providing a semiconductor device.

FIG. 5 illustrates a cross-sectional view of a portion of a MEMS device comprising a flexible substrate and a first plate in accordance with the method of FIG. 4.

FIG. 6 illustrates a cross-sectional view of a portion of the MEMS device of FIG. 5 further comprising a first dielectric.

FIG. 7 illustrates a cross-sectional view of a portion of the MEMS device of FIG. 6 after a first part of the formation of a sacrificial structure.

FIG. 8 illustrates a cross-sectional view of a portion of the MEMS device of FIG. 7 after a second part of the formation of the sacrificial structure.

FIG. 9 illustrates a cross-sectional view of a portion of the MEMS device of FIG. 8 after a first part of the formation of a sensor membrane.

FIG. 10 illustrates a cross-sectional view of a portion of the MEMS device of FIG. 9 after a second part of the formation of the sensor membrane.

FIG. 11 illustrates a cross-sectional view of a portion of the MEMS device of FIG. 10 after removal of the sacrificial layer.

FIG. 12 illustrates a cross-sectional view of a semiconductor device comprising both the MEMS device of FIG. 11 and an electronic device 12500 fabricated over the same flexible substrate.

5 For simplicity and clarity of illustration, the drawing figures illustrate the general manner of construction, and descriptions and details of well-known features and techniques may be omitted to avoid unnecessarily obscuring the invention. Additionally, elements in the drawing figures are not necessarily drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help improve understanding of embodiments of the
10 present invention. The same reference numerals in different figures denote the same elements.

The terms "first," "second," "third," "fourth," and the like in the description and in the claims, if any, are used for distinguishing between similar elements and not necessarily for describing a particular sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments described herein are,
15 for example, capable of operation in sequences other than those illustrated or otherwise described herein. Furthermore, the terms "include," and "have," and any variations thereof, are intended to cover a non-exclusive inclusion, such that a process, method, system, article, device, or apparatus that comprises a list of elements is not necessarily limited to those elements, but may include other elements not expressly listed or inherent to such process, method, system, article, device, or
20 apparatus.

The terms "left," "right," "front," "back," "top," "bottom," "over," "under," and the like in the description and in the claims, if any, are used for descriptive purposes and not necessarily for describing permanent relative positions. It is to be understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments of the invention
25 described herein are, for example, capable of operation in other orientations than those illustrated or otherwise described herein.

The terms "couple," "coupled," "couples," "coupling," and the like should be broadly understood and refer to connecting two or more elements or signals, electrically, mechanically or otherwise. Two or more electrical elements may be electrically coupled, but not mechanically or
30 otherwise coupled; two or more mechanical elements may be mechanically coupled, but not electrically or otherwise coupled; two or more electrical elements may be mechanically coupled, but not electrically or otherwise coupled. Coupling (whether mechanical, electrical, or otherwise) may be for any length of time, e.g., permanent or semi-permanent or only for an instant.

"Electrical coupling" and the like should be broadly understood and include coupling involving
35 any electrical signal, whether a power signal, a data signal, and/or other types or combinations of

electrical signals. "Mechanical coupling" and the like should be broadly understood and include mechanical coupling of all types. The absence of the word "removably," "removable," and the like near the word "coupled," and the like does not mean that the coupling, etc. in question is or is not removable.

5

DETAILED DESCRIPTION

In one embodiment, a semiconductor device comprises a flexible substrate and a MEMS device fabricated over the flexible substrate. In the same or a different embodiment, the semiconductor
10 device can comprise an electronic device fabricated over the substrate and electrically coupled to the MEMS device. In the same and other embodiments, the MEMS device can comprise an electrically conductive material located over the flexible substrate, a sensor membrane movably suspended over the electrically conductive material, and a first dielectric located over the electrically conductive material and under the sensor membrane.

15 In another embodiment, a method for providing a semiconductor device can comprise providing a flexible substrate and forming a MEMS device over the substrate. Forming the MEMS device can comprise providing an electrically conductive layer over the substrate, providing a first dielectric over the electrically conductive layer, providing a sacrificial structure over the first dielectric, and providing a sensor membrane over the sacrificial structure. Other embodiments are
20 described and claimed herein.

Turning to the drawings, FIG. 1 illustrates a perspective view of a semiconductor device comprising MEMS device 120 in accordance with an embodiment of the present disclosure. FIG. 2 illustrates a cross-sectional view along a line 1-1 of MEMS device 120 of FIG. 1. MEMS device 120 is merely exemplary and is not limited to the embodiments presented herein.

25 In the example of FIGs. 1-2, semiconductor device 100 comprises MEMS device 120 integrally fabricated over flexible semiconductor substrate 110. In the same and other examples, substrate 110 (or substrate body 210) can be a plastic substrate, and/or can comprise at least one of a flexible polyethylene naphthalate (PEN) material, such as that available from Teijin DuPont Films of Tokyo, Japan, under the tradename planarized "Teonex® Q65," a polyethylene terephthalate (PET)
30 material, a polyethersulfone (PES) material, a polyimide, a polycarbonate, a cyclic olefin copolymer, and/or a liquid crystal polymer. In other examples, substrate 110 can comprise other materials such as a stainless steel material, a silicon material, an iron nickel (FeNi) alloy material (e.g., FeNi, FeNi36, or Inver™; where Inver™ comprises an alloy of iron (64 percent (%)) and nickel (36%) (by weight) with some carbon and chromium), an iron nickel cobalt (FeNiCo) alloy material (e.g., Kovar™,
35 where Kovar™ typically comprises 29% nickel, 17% cobalt, 0.2% silicon, 0.3% manganese, and

53.5% iron (by weight)), a titanium material, a tantalum material, a molybdenum material, an aluchrome material, and/or an aluminum material.

As seen in FIG. 2, semiconductor substrate 110 comprises planarization layer 111 between substrate body 210 of substrate 110 and MEMS device 120 in the present example. In some
5 examples, planarization layer 111 can comprise a dielectric passivation material over substrate body 210, such as silicon nitride.

As illustrated in FIGs. 1-2, MEMS device 120 can be fabricated directly on substrate 110, and can comprise electrically conductive material 220 located over substrate 110, dielectric 230 located over electrically conductive material 220, and sensor membrane 121 suspended over dielectric 230.
10 Electrically conductive material 220 comprises a metallic layer in the present example, and can comprise a metallic material such as molybdenum, tantalum, aluminum, tungsten, and/or gold in at least some embodiments. There can be some embodiments where electrically conductive material 220 can be referred to as a plate. Dielectric 230 comprises a dielectric layer in the present example, and can comprise materials such as silicon nitride, silicon dioxide (SiO_2), and/or polyimide, in at
15 least some embodiments.

In the present embodiment, membrane perimeter 1211 of sensor membrane 121 is supported by wall structure 122 over dielectric 230. Wall structure 122 comprises one or more dielectric layers deposited over dielectric 230 along sensor perimeter 150 of MEMS device 120 in the present example, and can comprise a silicon nitride material in at least some embodiments. As seen in FIG.
20 1, sensor perimeter 150 comprises a circular shape, and membrane perimeter 1211 of sensor membrane 121 is also correspondingly circular. In the same or a different embodiment, sensor perimeter 150 and/or membrane perimeter 1211 can comprise a radius of between approximately 50 micrometers to approximately 250 micrometers. In the example of FIGs. 1-2, sensor membrane 121 comprises a radius of approximately 70 micrometers. Another example can comprise a sensor
25 membrane with a radius of approximately 200 micrometers. There can also be other embodiments where at least one of sensor perimeter 150 and/or membrane perimeter 1211 can comprise non-circular shapes, such as oval or square shapes. With a circular shape, however, MEMS device 120 can be more stable without needing a central support, as shown in FIG. 2. Wall structure 122 also defines sacrificial compartment 270 between sensor membrane 121 and dielectric 230. In the
30 present example, sacrificial compartment 270 comprises an air gap.

As shown in FIGs. 1-2, sensor membrane 121 comprises one or more openings 123 leading to sacrificial compartment 270. In the present embodiment, MEMS device 120 comprises 7 openings 123 in sensor membrane 121, although other embodiments can comprise a different number of openings. For example, some implementations can comprise between approximately 5 to 20
35 openings leading to the sacrificial compartment. In the present example, one or more of openings

123 of sensor membrane 121 can measure approximately 12 micrometers by approximately 12 micrometers. In other examples where the sensor membrane comprises approximately between 10 to 150 openings, one or more of such openings can measure approximately 10-20 micrometers by approximately 10-20 micrometers. There can be further examples with openings comprising non-
5 square perimeters, but otherwise can be similar to openings 123. In the present and other embodiments, openings 123 can be employed during the formation of sacrificial compartment 270. The formation of sacrificial compartment 270 will be further described below.

Sensor membrane 121 also comprises electrically conductive material 1212 facing dielectric 230 in the present example, where electrically conductive material 1212 can comprise a metallic material
10 such as molybdenum, aluminum, tantalum, tungsten, and/or gold. In the same or other examples, a layer of doped amorphous silicon can also comprise part of electrically conductive material 1212 or be located adjacent thereto.

As seen in FIG. 2, electrically conductive material 1212 couples to support layer 1213 of sensor membrane 121, where support layer 1213 can be deposited above electrically conductive material
15 1212 during fabrication. In the present embodiment, perimeter 1211 of sensor membrane 121 comprises a perimeter of support layer 1213, and the perimeter of support layer 1213 anchors sensor membrane 121 to wall structure 122 past a perimeter of electrically conductive material 1212. In some examples, support layer 1213 can comprise a silicon nitride material, a silicon oxynitride (SiO_xN_y) material, a silicon dioxide (SiO_2) material, a passivation material, a siloxane-based material,
20 an organosiloxane material, an organic siloxane-based material, and/or another dielectric material. In the same or other examples, support layer 1213 can comprise a PTS material such as that available from Honeywell International, Inc. of Morristown, New Jersey, under the name PTS-R.

In the same or a different example, support layer 1213 can comprise a thickness of between approximately 2 micrometers to approximately 2.5 micrometers. In the same or a different example,
25 MEMS device 120 can comprise a height of between approximately 2.5 micrometers to approximately 3.5 micrometers over substrate 110.

In the present embodiment MEMS device 120 comprises a shock or pressure sensor, and is configured to sense variations in pressure by detecting changes in capacitance between sensor membrane 121 and electrically conductive material 220. In the same and other embodiments,
30 electrically conductive material 220 and electrically conductive material 1212 of sensor membrane 121 can be considered as the plates of a capacitor, where the capacitance between the plates changes as sensor membrane 121 moves or deforms, at least temporarily, relative to electrically conductive material 220 as a result of the variations in pressure. In the same or other embodiments, when subject to shock waves and/or pressure changes, sensor membrane 121 can move or deform
35 enough to move toward and/or make contact with dielectric 230 over electrically conductive

material 220. In some embodiments, when in a steady state not subject to pressure variations, MEMS device 120 can comprise a capacitance of between approximately 1.5 picofarads and approximately 8.0 picofarads. In the same or different embodiments, MEMS device 120 can comprise a capacitance of between approximately 1.89 picofarads and approximately 7.8 picofarads. There can be embodiments where MEMS device 120 can sense pressure changes or shocks of between approximately 15 kilopascals (kPa) and 60kPa. For example, where sensor membranes 121 comprises a radius of 70 micrometers, MEMs device 120 may be configured to sense pressure changes of approximately 50kPa. In other examples with sensor membranes comprising a radius of 200 micrometers, pressure changes of approximately 20kPa may be sensed.

FIG. 3 illustrates a perspective view of semiconductor device 300 comprising MEMS array 320. In the embodiment of FIG. 3, MEMS array 320 comprises one or more MEMS sensors coupled together, including MEMS device 120 of FIGs. 1-2 as fabricated over substrate 110. Although the MEMS sensors of array 320 comprise the same diameter in the present examples, there can be examples where the MEMS array can comprise one or more MEMS sensors with a first diameter and one or more MEMS sensors with a different diameter and/or a different shape. In the present and other embodiments, semiconductor device 100 can comprise one or more electronic devices fabricated over substrate 110 different than MEMS device 120. For example, as shown in FIG. 3, one or more electronic devices 310, such as electronic device 311, can also be fabricated over substrate 110 and electrically coupled to MEMS device 120.

In the same or a different embodiment, MEMS device 120 and the other MEMS sensors of MEMS array 320 can be fabricated simultaneously over substrate 110 with electronic devices 310 using the same semiconductor process flow, or a modification of the semiconductor process flow, used for electronic devices 310, or vice versa. For example, electronic device 311 can comprise at least one transistor (not shown), and electrically conductive material 220 of MEMS device 120 (FIG. 2) can comprise a gate material used for a gate electrode of the at least one transistor of electronic device 311. In the same or a different example, dielectric 230 of MEMS device 120 (FIG. 2) can comprise a gate dielectric material used for a gate dielectric of the at least one transistor of electronic device 311.

Semiconductor device 300 can be implemented as a shock sensor and/or to detect pressure variations, and in the present and other examples, two or more of the MEMS sensors of MEMS array 320 can be coupled together in parallel to enhance the sensitivity of semiconductor device 300. The parallel coupling of the MEMS sensors of MEMS array 320 can increase the total capacitance of semiconductor device 300 and can help to minimize false readings by adding a level of redundancy to semiconductor device 300. In the same or other examples, such an arrangement can help to overcome false positives caused by random and/or faulty MEMs sensors.

In the present example, electronic device 311 represents a capacitance measurement circuit configured to measure and/or process the shock or pressure variations detected by MEMS array 310. In the same or a different example, semiconductor device 300 can comprise other electronic devices 310 such as display circuits (not shown) integrally fabricated over substrate 110. In such
5 embodiments, the display circuits can comprise display elements such as pixels (picture elements) of a display, and can be electrically coupled to MEMS array 320 and/or to the capacitance measurement circuit of electronic device 311.

In the present and other implementations, semiconductor device 300 can integrate MEMS array 320 and other electronic devices 310 onto a single flexible substrate suitable for sensing and/or
10 measuring shock or pressure variations, processing information out of the measurements, and displaying the information on the single flexible substrate. In the same or different embodiments, semiconductor device 300 can be configured to process blast dosimetry information measured at least partially via MEMS device 120 and/or to keep record of, for example, a number and/or magnitude of nearby explosions or shockwaves that a soldier has been exposed to during a period of
15 time. In such examples, semiconductor device 300 can be attached to the soldier's gear and/or to the body of the soldier at predetermined locations, including locations expected to be exposed to peak shockwaves. As an example, semiconductor device 300 can be attached to a helmet and/or near the top back of the skull of the soldier. In the same or other examples, semiconductor device 300 can be attached with or as an adhesive bandage.

20 Moving along, FIG. 4 illustrates a flowchart for a method 400 that can be used for providing a semiconductor device. In the same or different embodiments, method 400 can be considered a method of manufacturing a MEMS device, such as MEMS device 120 (FIGs. 1-3), over a flexible substrate. Method 400 is merely exemplary and is not limited to the embodiments presented herein. Method 400 can be employed in many different embodiments or examples not specifically depicted
25 or described herein.

Method 400 includes a procedure 410 of providing a substrate. FIG. 5 illustrates a cross-sectional view of a portion of MEMS device 500 comprising substrate 510, where substrate 510 can be similar to the substrate of procedure 410 and/or to substrate 110 (FIGs. 1-2) in some embodiments. In the same or different embodiments, procedure 410 of method 400 can include
30 providing a flexible substrate. In many examples, the flexible substrate can be a plastic substrate. For example, in the embodiment of FIG. 5, body 512 of substrate 510 can be similar to substrate body 210 in FIG. 2, and can comprise a flexible polyethylene naphthalate (PEN) material, such as that available from Teijin DuPont Films of Tokyo, Japan, sold under the tradename planarized "Teonex® Q65." In other embodiments, the substrate of procedure 410 can comprise a flexible
35 substrate comprising polyethylene terephthalate (PET), polyethersulfone (PES), polyimide,

polycarbonate, cyclic olefin copolymer, and/or liquid crystal polymer. The thickness of the substrate of method 400 can be in the range of approximately 25 micrometers to approximately 300 micrometers in some embodiments. In the same or different embodiments, the thickness of the substrate can be in the range of approximately 100 micrometers to approximately 200 micrometers.

5 In some examples, procedure 410 can further comprise providing a planarized surface over the substrate. In the example of FIG. 5, the planarized surface of procedure 410 can be formed by planarization layer 511, where layer 511 can comprise a passivation layer at the top of substrate 510. In some embodiments, planarization layer 511 can comprise a dielectric material such as silicon nitride, and can have a thickness of approximately 3000 Angstroms. Layer 511 can be similar to 10 planarization layer 111 in FIG. 2.

In a different example, procedure 410 can include providing a stainless steel flexible substrate. In still further examples, the substrate of procedure 410 can include silicon, iron nickel (FeNi) alloys (e.g., FeNi, FeNi36, or Inver™; where Inver™ comprises an alloy of iron (64%) and nickel (36%) (by weight) with some carbon and chromium), iron nickel cobalt (FeNiCo) alloys (e.g., Kovar™, 15 where Kovar™ typically comprises 29% nickel, 17% cobalt, 0.2% silicon, 0.3% manganese, and 53.5% iron (by weight)), titanium, tantalum, molybdenum, aluchrome, and/or aluminum.

In the same or different embodiments, the substrate of procedure 410 can be coupled to a carrier (not shown) to provide rigidity and/or to support the substrate. In various embodiments, the carrier includes at least one of the following: alumina (Al_2O_3), silicon, glass, steel, sapphire, 20 barium borosilicate, soda lime silicate, alkalai silicates, or other materials. The carrier can be coupled to the substrate using an adhesive or by other means. For example, the carrier could comprise sapphire with a thickness between approximately 0.7 millimeters (mm) and approximately 1.1 mm. The carrier could also comprise 96% alumina with a thickness between approximately 0.7 mm and approximately 1.1 mm. In a different embodiment, the thickness of the 96% alumina can be 25 approximately 2.0 mm. In another example, the carrier could comprise single crystal silicon with a thickness of at least approximately 0.65 mm. In some examples, the carrier is slightly larger than the substrate.

The substrate of procedure 410 can be cleaned in some examples to remove any particles on the substrate. In some embodiments, the substrate can be cleaned to remove any adhesives on the 30 substrate. For example, if the substrate is stainless steel, the substrate can be washed with hexanes for approximately twenty seconds while spinning at approximately 1,000 rpm (revolutions per minute). In some examples, the edge of the substrate can be sprayed with hexanes for the last ten seconds. Afterwards, the substrate can be spun at approximately 3,000 rpm for approximately twenty seconds to dry the substrate. In some examples, the substrate can be baked for 35 approximately sixty seconds at approximately 105 degrees Celsius (°C) to further dry the substrate.

To remove large particles from the substrate, the substrate of procedure 410 can be scrubbed. For example, if the substrate is stainless steel, the substrate can be scrubbed with soap and water (e.g., 40 milliliters (mL) of Alconox Detergent 8 mixed with one liter of water) using a sponge. Alconox Detergent 8 is manufactured by Alconox, Inc. of White Plains, New York. Organics can
5 also be removed from the substrate by ashing in some examples. For example, if the substrate is stainless steel, the substrate can be ashed for approximately ninety minutes in an oxygen (O_2) environment at a pressure of approximately 1,200 milliTorr.

Continuing with method 400, procedure 420 comprises forming a first MEMS device over the substrate of procedure 410. In some embodiments, the first MEMS device of procedure 420 can be
10 similar to MEMS device 120 from FIGs. 1-3). In the same or different embodiments, procedure 420 can comprise several subparts such as such as procedures 421-425.

In the present example of FIG. 4, procedure 421 comprises providing an electrically conductive layer over the substrate of procedure 410. In some embodiments, the electrically conductive layer can be referred to as a gate layer or as a first plate. In the same or other embodiments, the
15 electrically conductive layer of procedure 421 can be similar to plate 520 of MEMS device 500 in FIG. 5. In turn, plate 520 can be similar to electrically conductive material 220 of semiconductor device 100 (FIG. 2). In the same or a different embodiments, plate 520 can be deposited over substrate 510 and then patterned to a desired form.

Procedure 422 of method 400 comprises providing a first dielectric over the electrically
20 conductive layer of procedure 421. FIG. 6 illustrates a cross-sectional view of a portion of MEMS device 500 comprising dielectric 630, where dielectric 630 can be similar to the first dielectric of procedure 420 and/or to dielectric 230 (FIG. 2) in some embodiments. Dielectric 630 is deposited over planarization layer 511 of substrate 510 in the present example to a thickness of approximately 3000 Angstroms.

25 Procedure 423 of method 400 comprises providing a sacrificial structure over the first dielectric of procedure 422. In some examples, the sacrificial structure can be used to form sacrificial compartment 270 (FIG. 2) described for MEMS device 120 above. In the same or a different example, the sacrificial structure can be similar to sacrificial structure 770 as described in FIGs. 7-8. FIG. 7 illustrates a cross-sectional view of a portion of MEMS device 500 after a first part of the
30 formation of sacrificial structure 770. FIG. 8 illustrates a cross-sectional view of a portion of MEMS device 500 after a second part of the formation of sacrificial structure 770.

In the present example of method 400, part of procedure 423 comprises providing a sacrificial layer over the first dielectric of procedure 422. In the example of FIG. 7, sacrificial layer 771 deposited over dielectric 630 can be similar to the sacrificial layer of procedure 423 of method 400.
35 In some examples, sacrificial layer 771 can comprise an amorphous silicon channel material. In the

same or other examples, the sacrificial layer can be deposited over dielectric 630 to a thickness of approximately 0.08 micrometers. In the present example, sacrificial structure 770 also comprises dielectric layer 772 deposited over sacrificial layer 771, where dielectric layer 772 can comprise a patterned silicon nitride intermetal dielectric (IMD) layer having a thickness of approximately 0.10 micrometers in some examples. In other embodiments, sacrificial structure 700 can comprise a single layer.

In the present example, part of procedure 423 of method 400 can also comprise providing a compartment wall at a perimeter of the sacrificial layer and over the first dielectric, where the compartment wall for procedure 423 can be similar to wall structure 122 of semiconductor device 100 (FIGs. 1-2). In the same or different examples, now referring to FIG. 8, compartment wall 822 can correspond to the compartment wall for procedure 423 as formed by dielectric layer 873. In the present example, dielectric layer 873 comprises a patterned approximately 0.10 micrometer thick silicon nitride layer. In the same or other examples, dielectric layer 873 can comprise a passivation material. There can also be other examples where dielectric layer 873 can comprise other dielectric materials and/or IMD layer.

As seen in FIG. 8, compartment wall 822 can be formed by providing one or more dielectric layers, such as dielectric layers 772 and 873, over sacrificial layer 771. In other examples, dielectric layer 772 can be omitted from compartment wall 822 such that compartment wall 822 would only comprise a single dielectric layer comprising the space occupied by dielectric layers 772 and 873 in FIG 8. A perimeter of dielectric layer 873 contacts dielectric 630 in the present example past a perimeter of sacrificial layer 771 and dielectric layer 772. As a result, compartment wall 822 bounds the perimeter of sacrificial layer 771 and dielectric layer 772 in the present example.

Once placed over sacrificial layer 771, the one or more dielectric layers described above can be patterned to remove portions thereof over sacrificial layer 771 and thereby further define compartment wall 822. For example, FIG. 8 presents dielectric layers 873 and 772 after being etched to expose at least part of sacrificial layer 771.

Continuing with method 400, procedure 424 comprises providing a sensor membrane over the sacrificial structure of procedure 423. In some examples, the sensor membrane of procedure 424 can be similar to sensor membrane 121 of MEMS device 120 (FIGs. 1-2). In the same or different examples, the sensor membrane of procedure 424 and/or sensor membrane 121 can be similar to sensor membrane 921 as illustrated in FIGs. 9-11, and/or can comprise a substantially circular perimeter.

In the present example, part of procedure 424 comprises providing a second electrically conductive layer over the sacrificial structure of procedure 423. FIG. 9 illustrates a cross-sectional view of a portion of MEMS device 500 after a first part of the formation of sensor membrane 921.

In the embodiment of FIG. 9, the second electrically conductive layer described for procedure 424 can be similar to plate 9212 of sensor membrane 921 over sacrificial structure 770. In the same or a different embodiment, the second electrically conductive layer of procedure 424 and/or plate 9212 can be similar to electrically conductive material 1212 described above for MEMS device 120 (FIG. 2). In some examples, plate 9212 can have a thickness of approximately 0.20 micrometers. In the same or different examples, plate 9212 can comprise at least one of an aluminum material, a molybdenum material, a tungsten material, a gold material and/or a tantalum material. There may be embodiments where plate 9212 can comprise a stack of more than one material.

As seen in FIG. 9, one or more openings 923 can be etched through plate 9212 to expose one or more portions of sacrificial structure 770 and/or of sacrificial layer 771 in at least some embodiments. Openings 923 can be similar, for example, to openings 123 through membrane 121 of MEMS device 120 as described above for FIGs. 1-2. In the same or different examples, plate 9212 can be etched in one in-situ etching procedure with dielectric layer 873 and/or sacrificial layer 771 acting as etch stop layers. In some examples, plate 9212 can be etched using an AMAT 8330, manufactured by Applied Material, Inc. of Santa Clara, California. A perimeter of plate 9212 can extend beyond a perimeter of plate 520, as illustrated in FIG. 9.

Another part of procedure 424 of method 400 can comprise providing a structural layer over the second electrically conductive layer. As an example, FIG. 10 illustrates a cross-sectional view of a portion of MEMS device 500 after a second part of the formation of sensor membrane 921. In the embodiment of FIG. 10, the structural layer described for procedure 424 can be similar to structural layer 10211 of sensor membrane 921 over plate 9212. In the same or a different embodiment, the structural layer of procedure 424 and/or structural layer 10211 can be similar to support layer 1213 described above for MEMS device 120 (FIG. 2), and can comprise similar materials. There may be embodiments where structural layer 10211 can comprise a stack of more than one material. In the present example of FIG. 10, a perimeter of structural layer 10211 is shown coupled with a perimeter of sacrificial structure 770 past a perimeter of plate 9212. As a result, the perimeter of structural layer 10211 contacts with dielectric layer 873 at the perimeter of compartment wall 822 and bounds the perimeter of plate 9212 in the present example. As seen in FIG. 10, one or more openings 1023 can be etched through structural layer 10211 to expose one or more portions of sacrificial structure 770 and/or of sacrificial layer 771 in at least some embodiments. Openings 1023 can be similar to, and substantially aligned with, openings 923 as etched through plate 9212, and can also be similar to openings 123 through membrane 121 of MEMS device 120 as described above for FIGs. 1-2. In some examples, openings 1023 can be plasma etched. In the same of different embodiments, openings 1023 can be etched with a fluorine-based etchant. In some examples, the etchant can be trifluoromethane (CHF_3), sulfur hexafluoride (SF_6), or other fluorine-based etchants. In some

embodiments, openings 1023 can be formed before openings 923, and after forming openings 1023, the remainder of structural layer 10211 can be used as a self-aligned etch mask for openings 923.

There can be examples, including those where the substrate of procedure 410 comprises a plastic substrate, where the different procedures of method 400 to form the first MEMS device are carried out at temperatures not exceeding approximately 190 degrees Celsius. In such examples, the low temperature at which the MEMS device of procedure 420 is fabricated can assist in preventing heat-related damage to the susbstrate of procedure 410 and/or to elements of the MEMS device of procedure 420.

Continuing with method 400, procedure 425 comprises removing the sacrificial layer described above for procedure 423 via one or more openings of the sensor membrane of procedure 424. In some examples, a sacrificial compartment similar to sacrificial compartment 270 of MEMS device 120 (FIG. 2) remains between the sensor membrane of procedure 424 and the first dielectric of procedure 422 after the sacrificial layer is removed in procedure 425. FIG. 11 illustrates a cross-sectional view of a portion of MEMS device 500 after removal of sacrificial layer 771 from sacrificial compartment 1170 between sensor membrane 921 and dielectric 630 in accordance with an implementation of procedure 425 of method 400. In the example of FIG. 11, sacrificial layer 771 has been removed via etching through openings 1023 of sensor membrane 921 to release sensor membrane 921. In some examples, the etching through openings 1023 can be performed using a dry etch process. In the same or a different example, the etching through openings 1023 can comprise the use of a xenon difluoride (XeF_2) reactant or another gaseous reactant. The use of a dry etchant eliminates the problem of stiction when a wet etchant is used. In the same or a different example, the reactant used for etching sacrificial layer 771 comprises enough selectivity to etch only at sacrificial layer 771 without etching or at least without substantially etching sacrificial structure 770 or any other element bounding sacrificial compartment 1170, including plate 9212, dielectric 630, compartment wall 822, dielectric layer 873, structural layer 10211, or dielectric layer 772. In the same or a different example, no separate masking is needed prior to carrying out the etch of sacrificial layer 771.

In some examples, method 400 can comprise procedure 440, comprising forming over the substrate a second MEMS device electrically coupled in parallel with the first MEMS device of procedure 420. In some examples, the second MEMS device can be similar to the first MEMS device and/or can be manufactured using the same semiconductor process flow. In the same or a different example, the first and second MEMS devices of method 400 can be coupled together as described above with respect to FIG. 3 for the MEMS sensors of MEMS array 320. In the same or a different example, the second MEMS device of procedure 440 can comprise a sensor membrane

with a diameter and/or a perimeter different than a diameter and/or a perimeter of the sensor membrane provided in procedure 424 for the first MEMS device of procedure 420.

There can be some examples where method 400 also can comprise procedure 450, comprising forming over the substrate an electronic device electrically coupled to the MEMS device of
5 procedure 420. In the same or a different example, the electronic device can be similar to one of electronic devices 310 described above for FIG. 3, and/or could comprise at least part of a display element and/or a capacitance measurement circuit.

In some embodiments, method 400 can be implemented such that the MEMS device of procedure 420 is fabricated pursuant to a semiconductor process flow for the electronic device of
10 procedure 450 over the flexible substrate of procedure 410, or a modification of such semiconductor process flow. As an example, FIG. 12 illustrates a cross-sectional view of semiconductor device 12000 comprising both MEMS device 500 and electronic device 12500 fabricated over flexible substrate 510. In some examples, electronic device 12500 can correspond to at least part of the electronic device of procedure 450. In the same or a different examples, the part
15 of the electronic device comprises a transistor, and in particular, a thin film transistor.

As can be seen in FIG. 12, MEMS device 500 shares substrate 510, including body 512 and planarization layer 511, with electronic device 12500. Other elements of MEMS device 500 can be fabricated with layers used to fabricate corresponding elements of electronic device 12500. For example, plate 520 of MEMS device 500 can be fabricated out of the same layer or electrically
20 conductive material used to fabricate gate electrode 12520 of electronic device 12500. As a result, the electrical conductive material of plate 520 and the gate electrode of electronic device 12500 can be provided simultaneously during the fabrication of semiconductor device 12000.

In similar fashion, dielectric 630 of MEMS device 500 can be fabricated out of the same layer of material used to fabricate gate dielectric 12630 of electronic device 12500. As a result, dielectric 630
25 and gate dielectric 12630 can be provided simultaneously during fabrication of semiconductor device 12000.

Plate 9212 of sensor membrane 921 if MEMS device 500 can be fabricated out of the same layer or layers of electrically conductive material as source/drain conductive layer 129212 of electronic device 12500. As a result, plate 9212 and source/drain conductive layer 129212 can be provided
30 simultaneously during fabrication of semiconductor device 12000.

Structural layer 10211 of sensor membrane 921 of MEMS device 500 can be fabricated out of the same layer or layers of material used to fabricate planarization layer 1210211 of electronic device 12500. As a result, structural layer 10211 and planarization layer 1210211 can be provided simultaneously during fabrication of semiconductor device 12000.

Other elements of MEMS device 500 can be similarly fabricated based on layers used to fabricate elements of electronic device 12500. For example, although sacrificial layer 771 is already removed from MEMS device 500 in FIG. 12, in accordance with procedure 425 of method 400, sacrificial layer 771 of MEMS device 500 can be fabricated out of the same layer of channel material used to fabricate channel 12771 of electronic device 12500. Similarly, dielectric layer 772 of MEMS device 500 can be fabricated out of the same layer of material used to fabricate IMD layer 12772 of electronic device 12500. Dielectric layer 873 of MEMS device 500 can be fabricated out of the same layer of material used to fabricate passivation layer 12873 of electronic device 12500.

In the example of FIG. 12, layer 12020 is located over planarization layer 1210211 of electronic device 12500, and layer 12010 is located over layer 12020 of electronic device 12500. In some examples, layer 12020 can comprise an indium-tin-oxide material, and/or layer 12010 can comprise silicon nitride or other dielectric material configured to create an overglass protection layer. Although layers 12010 and 12020 are not needed in the present example for MEMS device 500, MEMS device 500 is still compatible with the semiconductor process for electronic device 12500. For example, layers 12010 and 12020 can be formed and patterned over structural layer 10211 before the removal of sacrificial layer 771.

In some examples, one or more of the different procedures of method 400 can be combined into a single step or performed simultaneously, and/or the sequence of such procedures can be changed. For example, procedure 450 could be performed before procedure 440 in some examples. In other examples, the first MEMS device of procedure 420, the second MEMS device of procedure 440, and the electronic device of procedure 450 can be fabricated simultaneously and/or combined into a single step. There can also be examples where method 400 can comprise further or different procedures. As an example, a procedure could be added after procedure 450 to form a second electronic device over the substrate of procedure 410. In such an example, the electronic device of procedure 450 could form part of a capacitance measurement circuit, and the electronic device of procedure 460 could form part of a display circuit for the semiconductor device of method 400. Other variations can be implemented for method 400 without departing from the scope of the present disclosure.

Although the embedded MEMS sensors and related methods herein have been described with reference to specific embodiments, various changes may be made without departing from the spirit or scope of the present disclosure. For example, even though openings 123 of MEMS device 120 have been presented as square-shaped, there can be embodiments with similar openings comprising other geometrical perimeters. Additional examples of such changes have been given in the foregoing description. Accordingly, the disclosure of embodiments herein is intended to be illustrative of the scope of the invention and is not intended to be limiting. It is intended that the

scope of this application shall be limited only to the extent required by the appended claims. The embedded MEMS sensors and related methods discussed herein may be implemented in a variety of embodiments, and the foregoing discussion of certain of these embodiments does not necessarily represent a complete description of all possible embodiments. Rather, the detailed description of the drawings, and the drawings themselves, disclose at least one preferred embodiment, and may disclose alternative embodiments.

All elements claimed in any particular claim are essential to the embodiment claimed in that particular claim. Consequently, replacement of one or more claimed elements constitutes reconstruction and not repair. Additionally, benefits, other advantages, and solutions to problems have been described with regard to specific embodiments. The benefits, advantages, solutions to problems, and any element or elements that may cause any benefit, advantage, or solution to occur or become more pronounced, however, are not to be construed as critical, required, or essential features or elements of any or all of the claims.

Moreover, embodiments and limitations disclosed herein are not dedicated to the public under the doctrine of dedication if the embodiments and/or limitations: (1) are not expressly claimed in the claims; and (2) are or are potentially equivalents of express elements and/or limitations in the claims under the doctrine of equivalents.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:
5 a flexible substrate; and
a MEMS device fabricated over the flexible surface.

2. The semiconductor device of any of claims 1-2, further comprising:
a planarization layer between the flexible substrate and the MEMS device.

10

3. The semiconductor device of claim 1, further comprising:
an electronic device fabricated over the flexible substrate and electrically coupled to the MEMS device.

15 4. The semiconductor device of claim 3, wherein:
the electronic device comprises at least one of:
a display element; or
a capacitance measurement circuit.

20 5. The semiconductor device of any of claims 3-4, wherein:
the electronic device is configured to process blast dosimetry information measured via the MEMS device.

6. The semiconductor device of any of claims 1-5, wherein:
25 the flexible substrate comprises at least one of:
a PEN material, a PET material, a PES material, a polyimide, a polycarbonate, a cyclic olefin copolymer, or a liquid crystal polymer.

7. The semiconductor device of any of claims 1-5, wherein:
30 the flexible substrate comprises at least one of:
a stainless steel material, a FeNi alloy material, a FeNiCo alloy material, a titanium material, a tantalum material, a molybdenum material, an aluchrome material, or an aluminum material.

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8. The semiconductor device of any of claims 1-7, wherein:
the MEMS device comprises:
an electrically conductive material located over the flexible substrate;
a sensor membrane movably suspended over the electrically conductive material; and
5 a first dielectric located over the electrically conductive material and under the sensor membrane.

9. The semiconductor device of claim 8, wherein:
the electrically conductive material comprises at least one of molybdenum, tantalum,
10 aluminum, tungsten, or gold.

10. The semiconductor device of any of claims 8-9, wherein:
the sensor membrane is configured to move toward the first dielectric when deformed by at least one of a shock wave or a pressure change.

15

11. The semiconductor device of any of claims 8-10, wherein:
the MEMS device further comprises:
a compartment between the electrically conductive material and the sensor membrane.

20

12. The semiconductor device of claim 11, wherein:
the sensor membrane comprises between approximately 5 openings to approximately 20 openings into the compartment.

25 13. The semiconductor device of any of claims 11-12, wherein:
the compartment defines an air gap between the electrically conductive material and the sensor membrane.

14. The semiconductor device of any of claims 8-13, wherein:
30 the sensor membrane comprises:
a second electrically conductive material facing the first dielectric; and
a support layer located over the second electrically conductive material and anchored at a perimeter of the sensor membrane.

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15. The semiconductor device of claim 14, wherein:
    the second electrically conductive material comprises at least one of aluminum, tantalum, molybdenum, tungsten, or gold;
    and
5   the support layer comprises at least one of a silicon nitride material, a silicon oxynitride material, a silicon dioxide material, a passivation material, a siloxane-based material, an organosiloxane material, an organic siloxane-based material, or a PTS material.

16. The semiconductor device of any of claims 14-15, wherein:
10 the support layer comprises a thickness of between approximately 2 micrometers to approximately 2.5 micrometers.

17. The semiconductor device of any of claims 8-16, wherein:
    the sensor membrane is substantially circular.

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18. The semiconductor device of any of claims 8-17, further comprising:
    a wall structure coupled to the first dielectric;
    wherein the sensor membrane is suspended by the wall structure over the electrically conductive material.

20

19. The semiconductor device of claim 18, wherein:
    the wall structure comprises one or more dielectric layers located over the first dielectric along a sensor perimeter of the MEMS device.

25 20. The semiconductor device of any of claims 8-19, further comprising:
    an electronic device fabricated over the flexible substrate and electrically coupled to the MEMS device;
    wherein:
        the electronic device comprises at least one transistor; and
30   the electrically conductive material comprises a gate material used for a gate electrode of the at least one transistor of the electronic device.

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21. The semiconductor device of any of claims 8-19, further comprising:
    an electronic device fabricated over the flexible substrate and electrically coupled to the MEMS device;
    wherein:
5   the electronic device comprises at least one transistor; and
        the first dielectric comprises a gate dielectric material used for a gate dielectric of the at least one transistor of the electronic device.

22. The semiconductor device of any of claims 1-21, wherein:
10 the MEMS device comprises a circular perimeter with a radius of between approximately 50 micrometers to approximately 250 micrometers.

23. The semiconductor device of any of claims 1-22, wherein:
    the MEMS device comprises a height of between approximately 2.5 micrometers to
15 approximately 3.5 micrometers.

24. The semiconductor device of any of claims 1-23, wherein:
    the MEMS device comprises a steady state capacitance of between approximately 1.5 picofarads to approximately 8.0 picofarads.
20

25. The semiconductor device of any of claims 1-24, further comprising:
    two or more MEMS sensors electrically coupled in parallel with each other;
    wherein one of the two or more MEMS sensors comprises the MEMS device.

25 26. The semiconductor device of claim 25, wherein:
    a first MEMS sensor of the two or more MEMS sensors comprises a diameter different than a diameter of a second MEMS sensor of the two or more MEMS sensors.

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27. A method comprising:
    providing a flexible substrate; and
    forming a first MEMS device over the substrate;
    wherein forming the first MEMS device comprises:
        providing an electrically conductive layer over the substrate;
        providing a sacrificial structure over the electrically conductive layer; and
        providing a sensor membrane over the sacrificial structure.

28. The method of claim 27, wherein:
    providing the flexible substrate comprises:
        providing the flexible substrate to comprise at least one of a PEN material, a PET material, a PES material, a polyimide, a polycarbonate, a cyclic olefin copolymer, or a liquid crystal polymer.

29. The method of any of claims 27-28, wherein:
    the sacrificial structure comprises an amorphous silicon material.

30. The method of any of claims 27-29, wherein:
    providing the sacrificial structure comprises:
        providing a sacrificial layer over the electrically conductive layer.

31. The method of claim 30, wherein:
    providing the sacrificial structure comprises:
        providing a compartment wall at a perimeter of the sacrificial layer and over the electrically conductive layer, the compartment wall comprising one or more dielectric layers.

32. The method of claim 31, wherein:
    providing the compartment wall comprises:
        providing a perimeter of at least one of the one or more dielectric layers of the compartment wall to couple with the first MEMS device past a perimeter of the sacrificial layer.

33. The method of any of claims 31-32, wherein:
    the one or more dielectric layers over the sacrificial layer comprise at least one of:
        an intermetal dielectric material;
        a passivation material; or
5   a silicon nitride material.

34. The method of any of claims 30-33, further comprising:
    etching one or more openings through the sensor membrane to expose one or more portions of the sacrificial layer; and
10 removing the sacrificial layer via the one or more openings of the sensor membrane.

35. The method of claim 34, wherein:
    removing the sacrificial layer comprises:
        dry etching the sacrificial layer through the one or more openings of the sensor
15   membrane.

36. The method of claim 35, wherein:
    dry etching the sacrificial layer comprises using at least one of:
        a dry etch reactant;
20   a gaseous reactant; or
        an XeF_2 reactant.

37. The method of any of claims 27-36, wherein:
    providing the sensor membrane comprises:
25   providing the sensor membrane to comprise a substantially circular perimeter.

38. The method of any of claims 27-37, wherein:
    providing the sensor membrane comprises:
        providing a second electrically conductive layer over the sacrificial structure; and
30   providing a structural layer over the second electrically conductive layer.

39. The method of claim 38, wherein:
    providing the structural layer comprises:
        providing a perimeter of the structural layer to couple with a perimeter of the
35   sacrificial structure past a perimeter of the second electrically conductive layer.

40. The method of any of claims 38-39, wherein:

providing the sensor membrane further comprises:

etching one or more openings through the second electrically conductive layer to expose one or more portions of the sacrificial structure prior to providing the structural layer.

41. The method of any of claims 38-40, wherein:

the second electrically conductive layer comprises at least one of:

an aluminum material, a tantalum material, a molybdenum material, a tungsten material, or a gold material;

and

the structural layer comprises at least one of:

a silicon nitride material, a silicon oxynitride material, a silicon dioxide material, a passivation material, a siloxane-based material, an organosiloxane material, an organic siloxane-based material, or a PTS material.

42. The method of any of claims 38-41, wherein:

providing the sensor membrane further comprises:

etching one or more openings through the structural layer to expose at least a portion of the sacrificial structure.

43. The method of any of claims 27-42, further comprising:

forming over the substrate a second MEMS device electrically coupled in parallel with the first MEMS device.

44. The method of any of claims 27-43, further comprising:

forming over the flexible substrate an electronic device electrically coupled to the first MEMS device;

wherein the electronic device comprises at least one of:

a display element; or

a capacitance measurement circuit.

45. The method of claim 44, wherein:
    the first MEMS device is fabricated pursuant to at least one of:
        a semiconductor process flow for the electronic device; or
        a modification of the semiconductor process flow for the electronic device.

5

46. The method of any of claims 44-45, wherein:
    providing the electrically conductive layer comprises:
        simultaneously providing the electrically conductive layer and a gate electrode for a transistor of the electronic device.

10

47. The method of any of claims 44-46, wherein:
    providing the sensor membrane comprises:
        providing at least a portion of the sensor membrane simultaneously with a channel material of a transistor of the electronic device.

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48. The method of any of claims 44-47, wherein:
    forming the electronic device comprises:
        providing a gate dielectric of a transistor of the electronic device simultaneously with a dielectric of the first MEMS device.

20

49. The method of any of claims 27-48, wherein:
    forming the first MEMS device comprises:
        forming the first MEMS device at temperatures not exceeding approximately 190 degrees Celsius.

25

50. The method of any of claims 27-49, wherein:
    forming the first MEMS device further comprises:
        providing a first dielectric between the electrically conductive layer and the sacrificial structure.

30

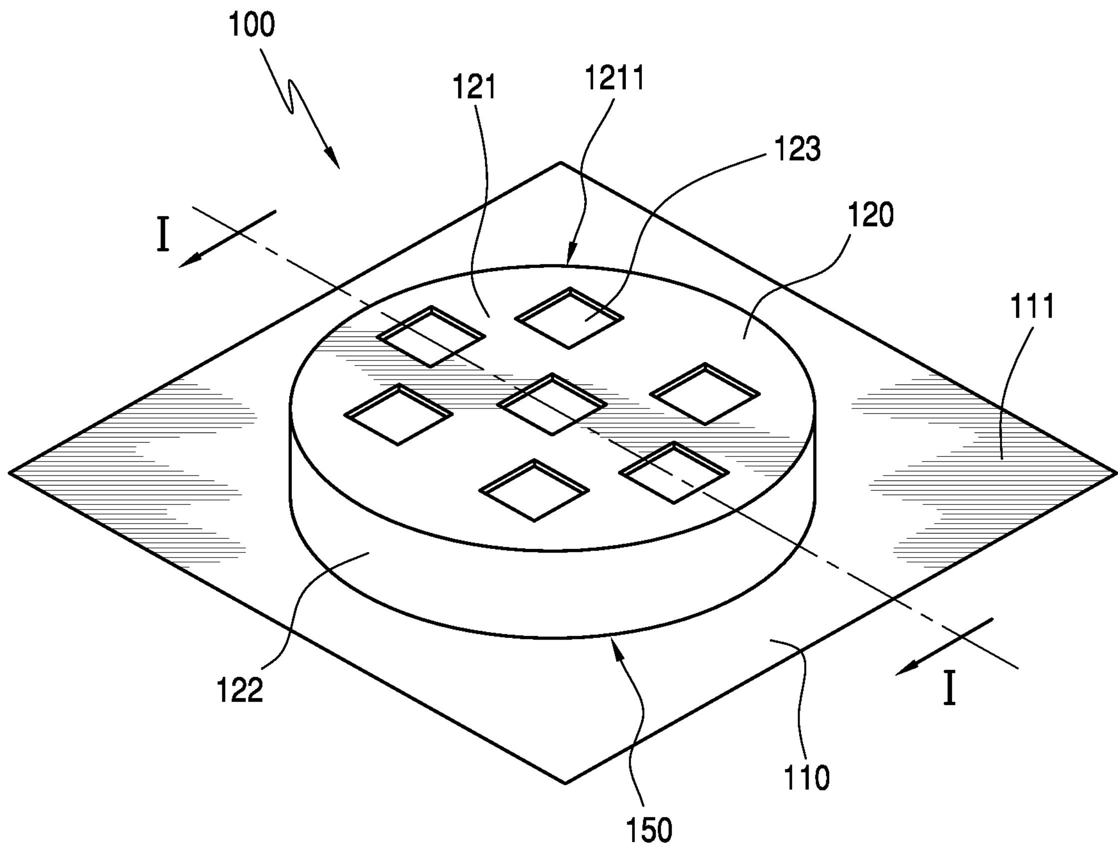

FIG. 1

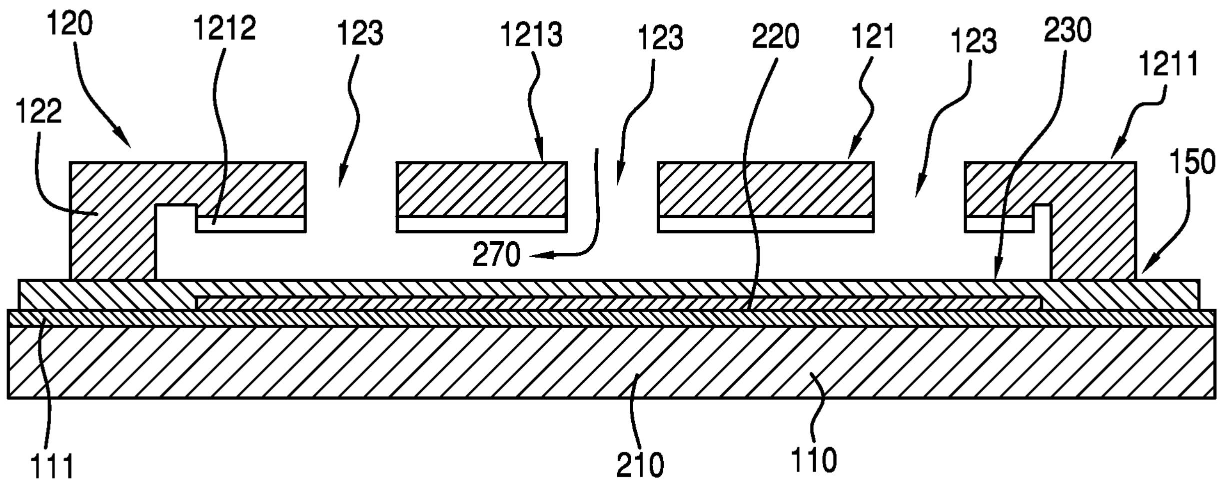

FIG. 2

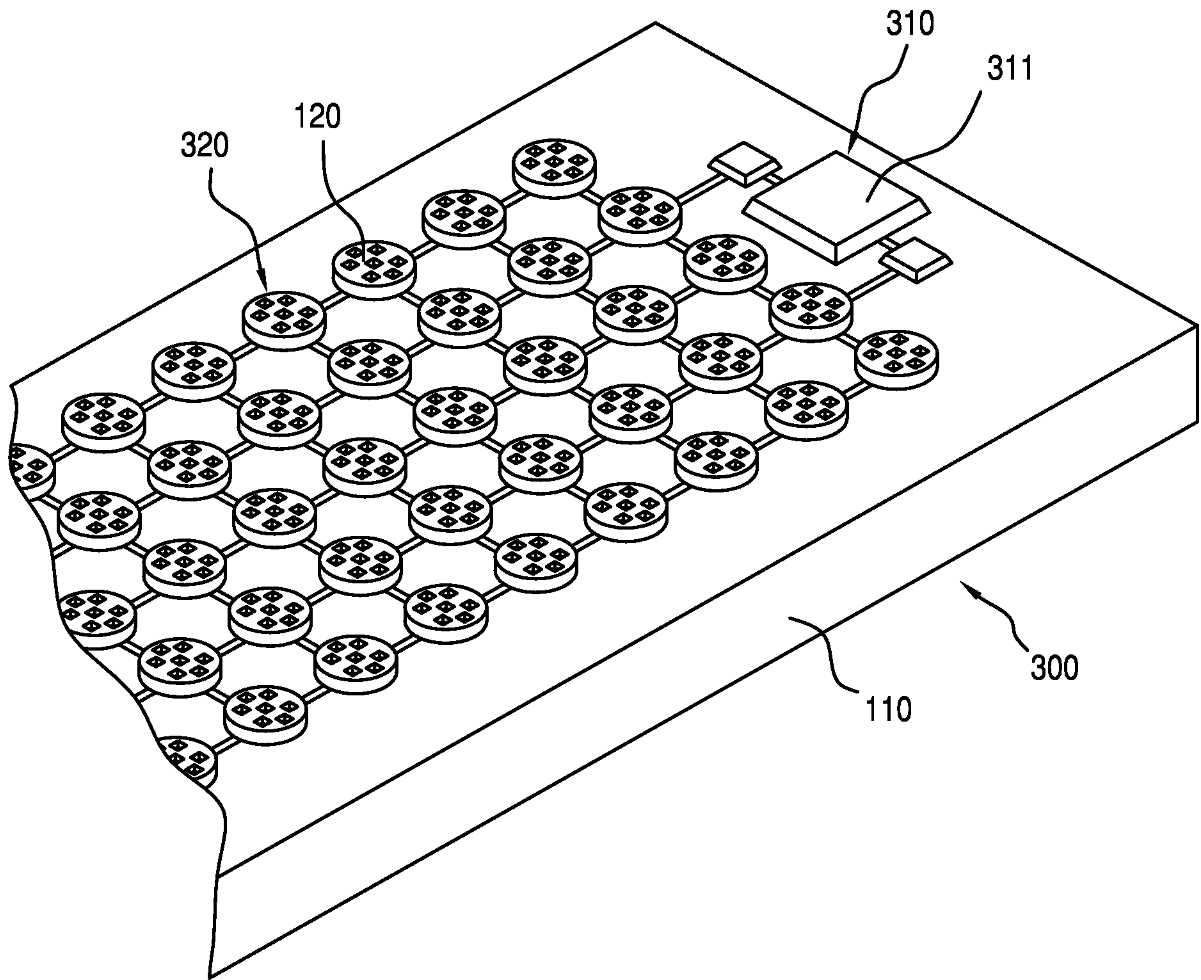

FIG. 3

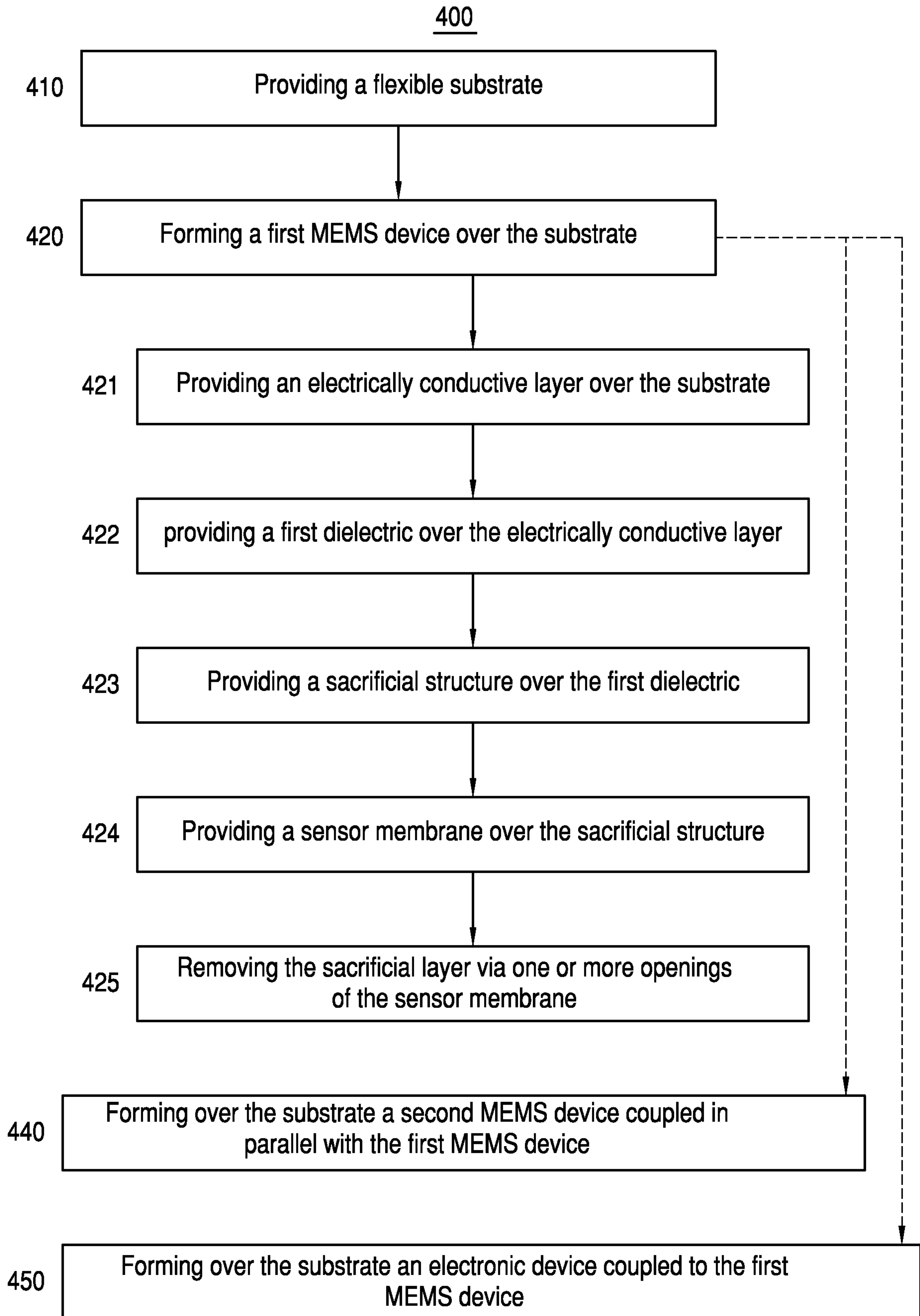

FIG. 4

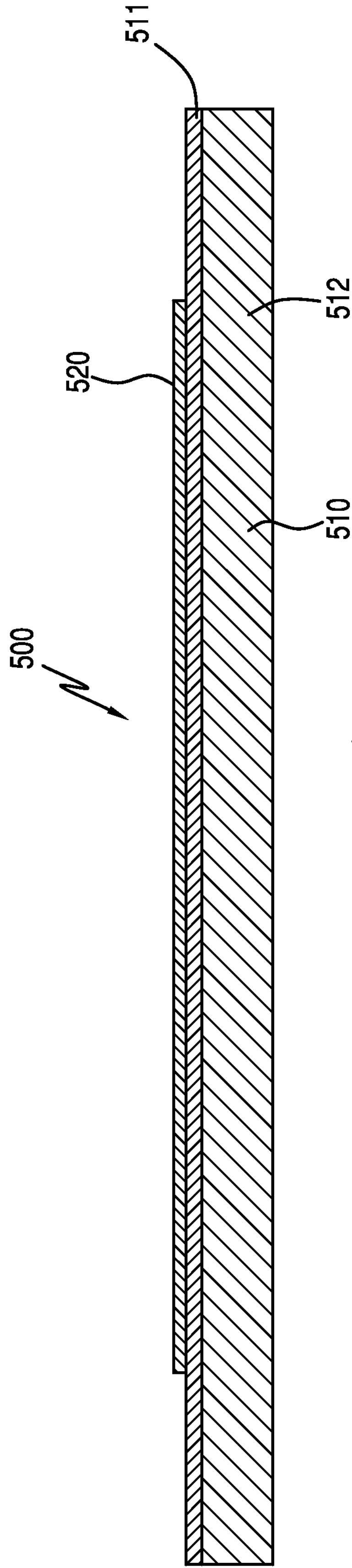

FIG. 5

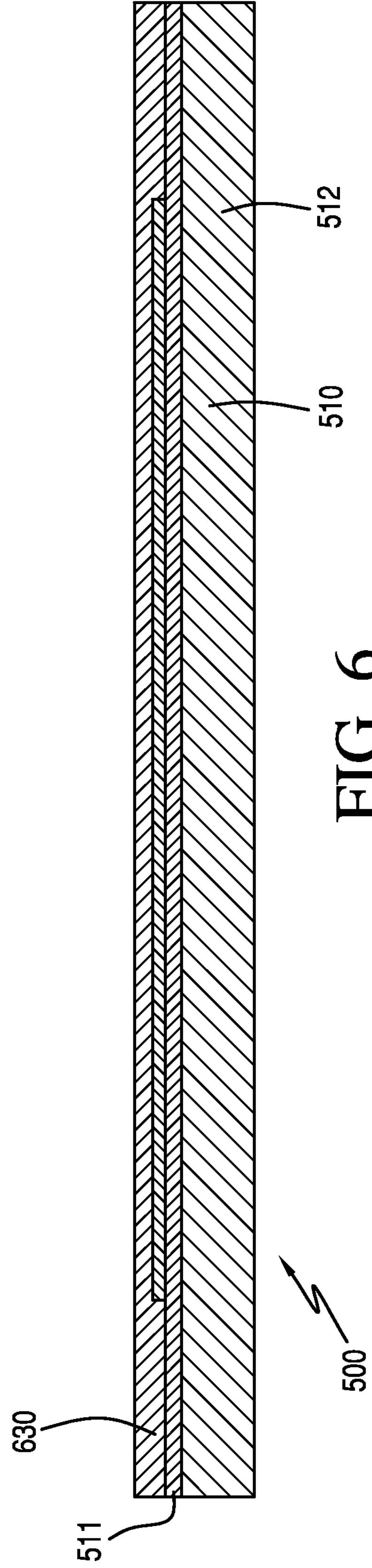

FIG. 6

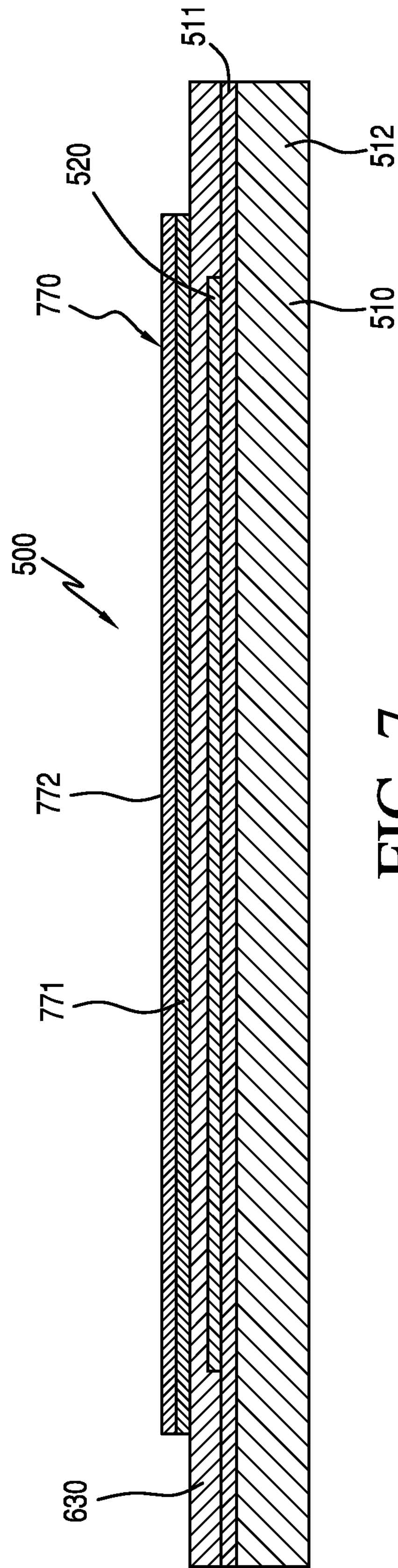

FIG. 7

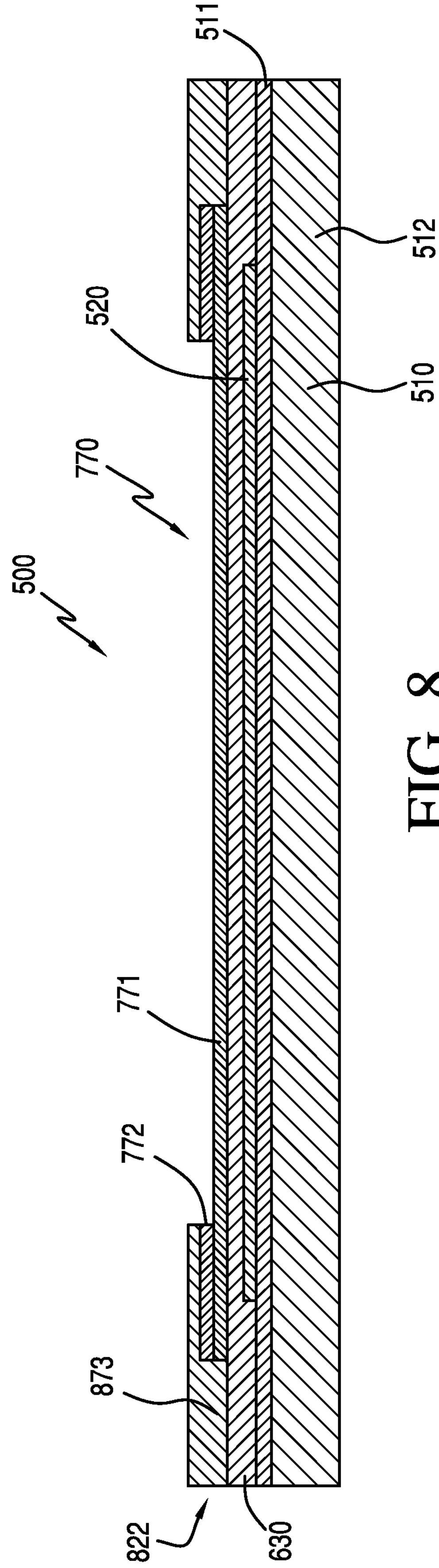

FIG. 8

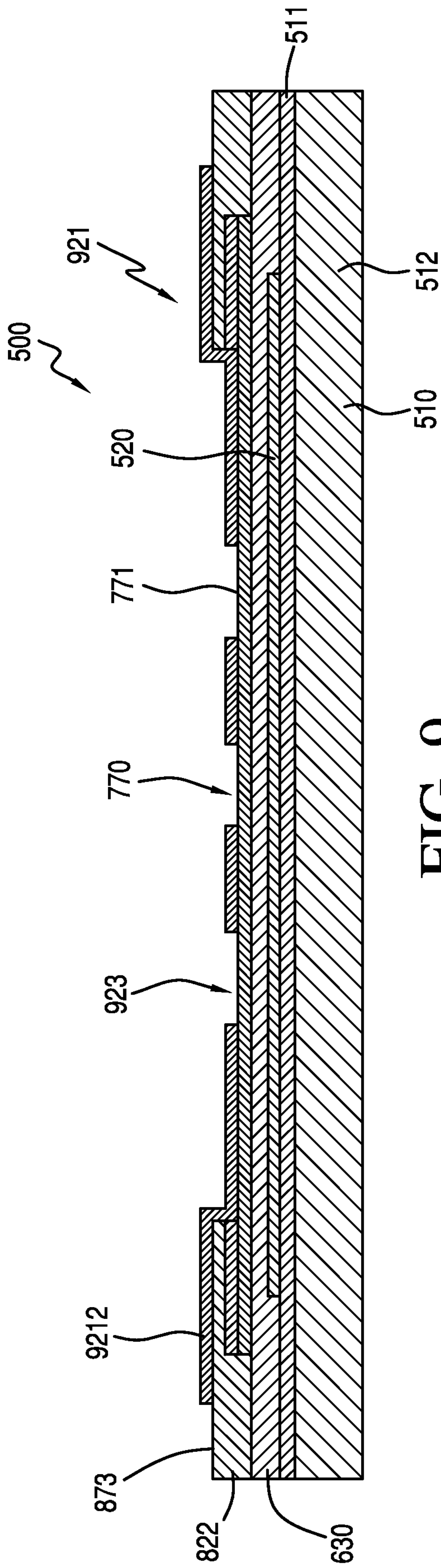

FIG. 9

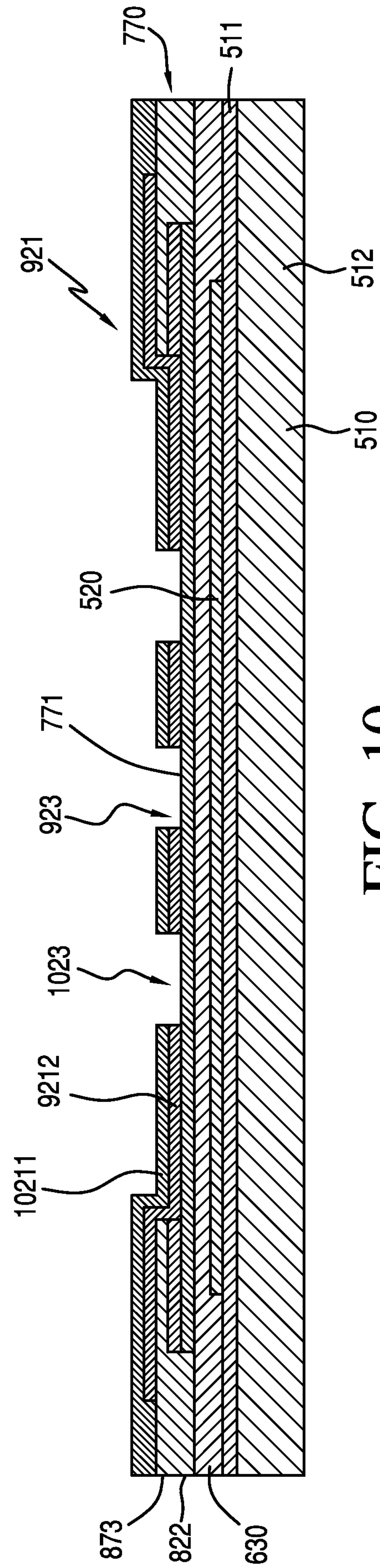

FIG. 10

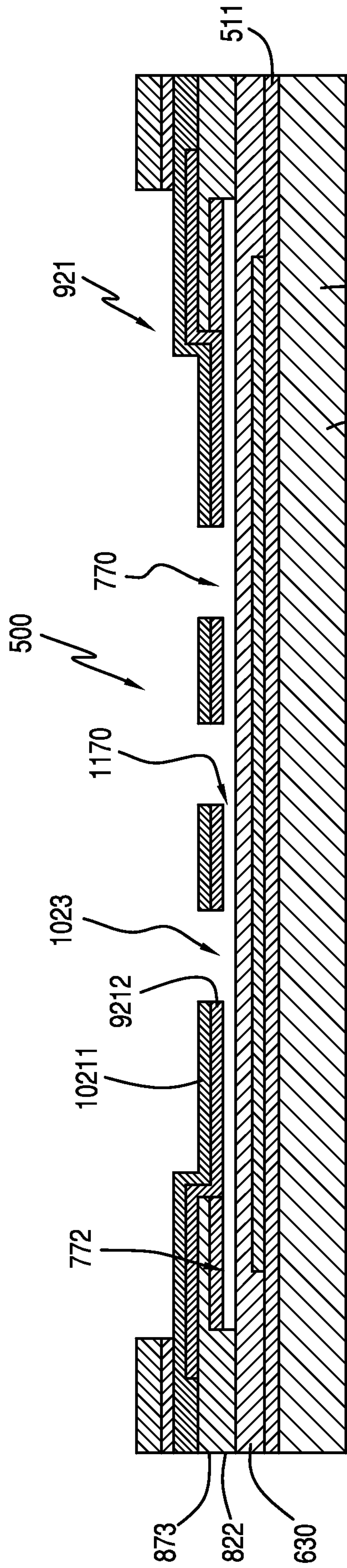

FIG. 11

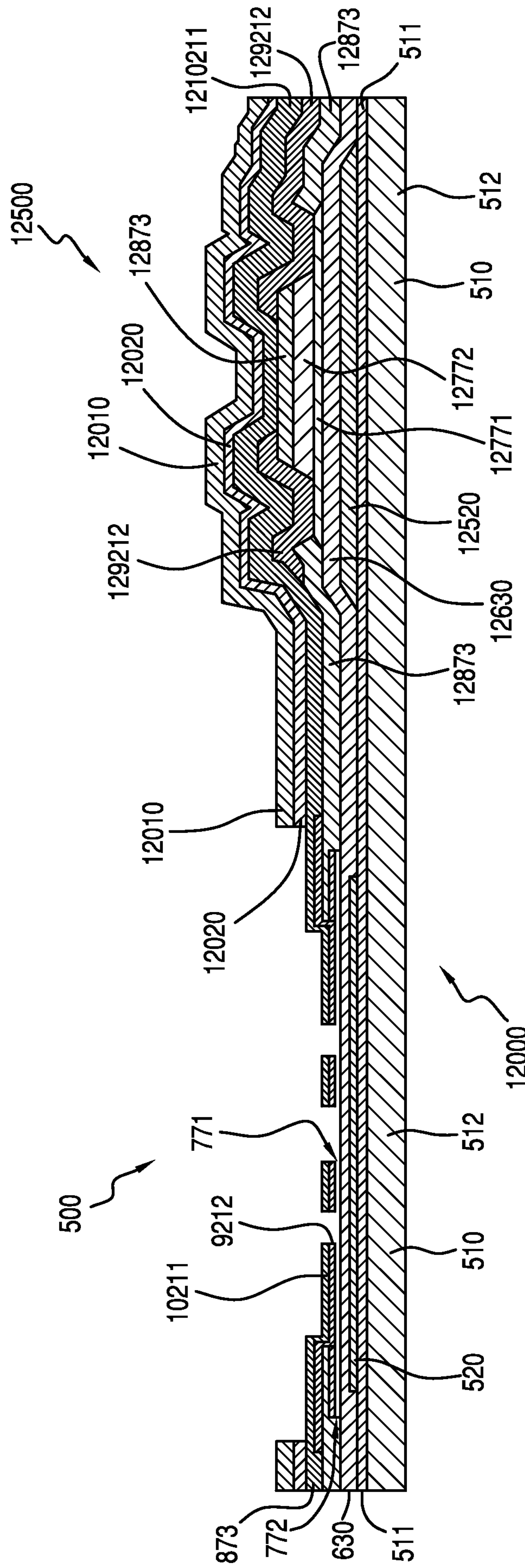

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 09/68528

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G01M 7/00 (2010.01)
USPC - 73/12.01; 340/665; 73/514.01
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC 73/12.01; 340/665; 73/514.01

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC 73/12.01; 340/665; 73/514.01 (text search--see below)

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
PubWest (PGPB,USPT,EPAB,JPAB); Google Scholar (Patents,Articles)
Search terms: MEMS, flexible, substrate, silicon, amorphous, sacrificial, polyimide, PET, PES, PEN, olefin, sensor, circuit, capacitance, blast, dosimeter

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X --- Y	US 2006/0067651 A1 (CHUI) 30 March 2006 (30.03.2006), FIG. 5; para [0086],[0087], [0095], [0105], [0106], [0174]	1, 2 ------------- 3-5, 27-29
Y	US 2005/0121734 A1 (DEGERTEKIN et al.) 09 June 2005 (09.06.2005), FIG 2, 4; para [0033], [0034], [0038]-[0043], [0008]	3-5, 27-29
Y	ALLEE et al., "Threshold Voltage Instability in a-Si:H TFTs and the Implications for Flexible Displays and Circuits." In: Proccedings of the Army Science Conference (26th). Orlando, Florida. 1-4 December 2008, (04.12.2008), p. 6, col. 1, para (2)-col. 2, para (4) Retrieved from the Internet: <URL: http://74.125.155.132/scholar-q=cache:o_oW8m7fmksJ:scholar.google.com/> [Retrieved on 14 August 2010 (14.08.2010)]	5
A	US 2007/0023851 A1 (HARTZELL et al.) 01 February 2007 (01.02.2007), para [0046]-[0050], [0074]-[0096]	1-5, 27-29

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
15 August 2010 (15.08.2010)	01 SEP 2010

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 09/68528

Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☒ Claims Nos.: 6-26, 30-50
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.

☐ The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.

☐ No protest accompanied the payment of additional search fees.