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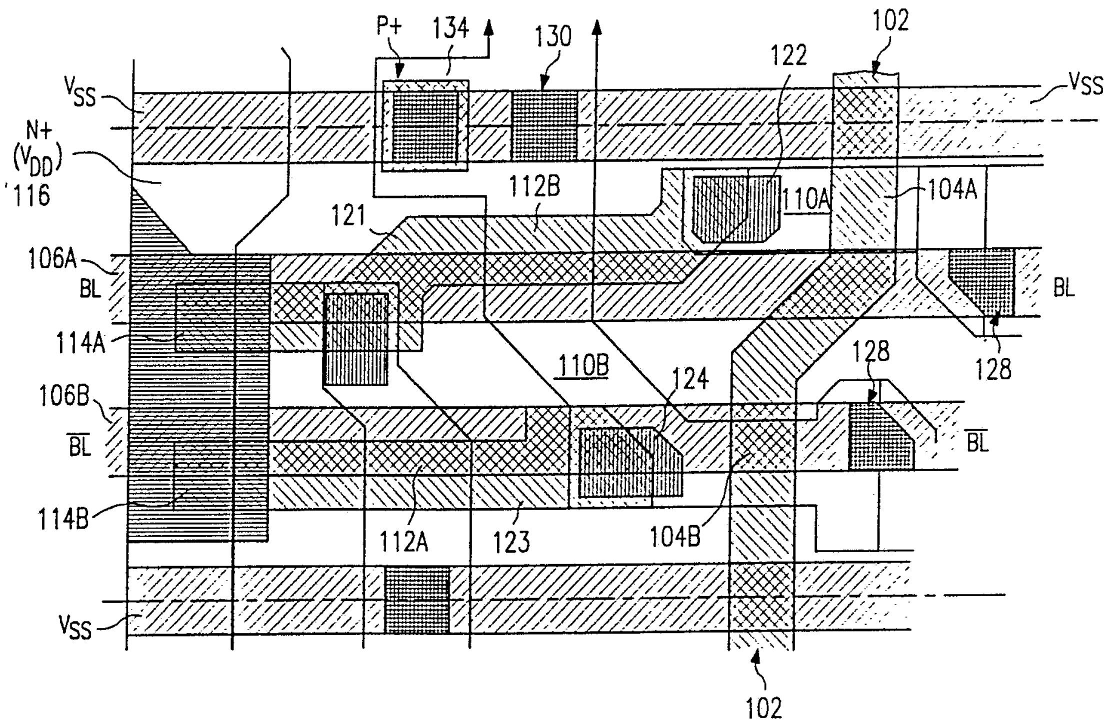

(57) Abstract

An integrated circuit memory (400-430) which uses vertical current flow through arsenic-implanted oxide films (320') to provide low-current loads (114). These load elements (114), together with driver transistors (112) and pass transistors (104), provide the four-transistor cells for a static random-access memory array (400) which has very simple fabrication and very low power consumption.

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INTEGRATED CIRCUIT WITH COMPACT LOAD ELEMENTS

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BACKGROUND AND SUMMARY OF THE INVENTION

The present invention relates to integrated circuits, and to the provision of the load elements in integrated circuits. More particularly, the present invention relates to low-power integrated circuits, and to low-power static RAM access memories (SRAMs).

5 In integrated circuits generally, it is necessary to be able to change the voltages of nodes in two directions. For example, in conventional CMOS logic, p-channel insulated gate field effect transistors (PMOS devices) are used to pull up the voltage of a node, and NMOS devices are used to pull down the voltage of a node. In conventional NMOS logic, NMOS devices

10 are used to pull down nodes, and resistor loads are used to pull up the nodes.

A specific example of this is in SRAMs (static random access memories). In a conventional CMOS SRAM, six transistors are used in each cell. The cell has two data nodes, which have opposite logic states.

15 Each node is connected to ground through an NMOS driver transistor. The driver transistor which connects each node to ground has its gate connected to the opposite data node so that, when one data node goes high, it will pull the opposite data load low by turning on its driver transistor. Similarly, each node is connected, through a PMOS pull-up

20 transistor, to the high supply voltage V_{DD} (which is typically 5 volts). Again, the data nodes are connected to control the pull-up transistors of the opposite data node, so that, when one of the data nodes goes low, it will turn on the pull up transistor of the opposite node, so that the opposite node is held high. In addition, two pass transistors (normally

NMOS transistors) selectively connect the two data nodes to a pair of bit lines. (The gates of the pass transistors are connected to a word line, so that the cell nodes will be connected to the bit line pair only if the word line goes high.) Such a 6-transistor cell will hold its logic state indefinitely (as long as the supply voltages are maintained and no transient upset occurs). Moreover, while such a cell is simply holding data, it has almost zero power consumption, since each of the nodes will be disconnected from one of the two power supply voltages.

The low power consumption of CMOS is extremely advantageous in a wide variety of environments, and is one of the reasons why CMOS logic has become very widely used for a wide variety of digital circuits. Low power consumption is not only advantageous where the total drain on system power supply must be conserved (as, for example, in applications where the power is being supplied from a battery), but also implies that the on-chip power dissipation will be less. This can be important in a wide variety of applications where a very high density is required.

However, while conventional CMOS logic has some major advantages, it also has significant disadvantages. The use of both PMOS and NMOS devices means that additional masking and doping steps must be used to provide both n-type device areas (for the PMOS devices) and p-type device areas (for the NMOS active devices). Moreover, for a given device area, the use of both PMOS and NMOS active devices means that some new spacing constraints must be observed. An important spacing constraint is imposed by the need to avoid latchup.

Latchup is a failure mode to which conventional bulk CMOS devices are inherently susceptible. A parasitic thyristor exists wherever an N+ source/drain region in the p- well of an NMOS device is close to a P+ source/drain region in the n- well of a PMOS device. The N+ source/drain, the P-well, the N-well, and the P+ source/drain of the PMOS device define a PNPN parasitic thyristor structure. In many locations, an n+ region will be connected to the positive power supply V_{DD} and the nearest p+ will be connected to ground. Thus, if the parasitic thyristor fires, it can conduct a large amount of current. This can provide a stuck logic state, or even destroy the device.

An immense amount of effort has been devoted to reducing the propensity of CMOS devices to latchup, and some CMOS processes produce devices with reduced susceptibility to latchup. However, for any conventional bulk CMOS process, a certain minimum P+ to N+ separation must be observed, to prevent the possibility of latchup.

Thus, an inherent limitation of conventional CMOS technology is that some space is lost at the interface between PMOS and NMOS active device regions. This constraint is particularly inconvenient in memory design. In the conventional 6-transistor CMOS SRAM cell described above, the transistor types require that a P-well/N-well boundary must run through every single memory cell in the array.

NMOS static random access memory cells tend to be more compact than CMOS static random access memory cells, because they do not require a P-well/N-well boundary within the cell. However, the static power consumption of NMOS memory cells is much larger than for CMOS memory cells. This is because current will flow through at least one of the load resistors all the time.

During normal operating conditions, the current provided by the load resistors only needs to be large enough to compensate for junction leakage. With normal high-quality processing techniques, this junction leakage will be substantially less than a picoAmpere per cell, and may range down to values in the neighborhood of one femtoAmpere (10^{-15} Ampere) per cell. The highest-resistivity material conventionally available in integrated circuit processing is intrinsic polysilicon. While this material has very high bulk resistivity, it is difficult to fabricate it with a sheet resistance higher than a few hundred gigohms per square. This means that the largest resistor value which can be conveniently placed within a memory cell layout (without expanding the cell) will be about one teraohm. A one-teraohm resistor will pass a current, at 5 Volts, of 5 picoamps. Therefore, this resistor value is still several times smaller than would be desirable for low-power applications.

For comparison, the leakage specification on Hitachi's 256K slow static SRAMs (which represent a typical mass-market CMOS SRAM as of 1989) require a leakage current of less than 800 nA (3 pA per cell),

and some individual parts have leakage as low as about 200 nA. Thus, it may be seen that the power conservation of conventional CMOS technology leaves considerable room for improvement.

Other attempts to make compact high-value resistors have used oxygen implantation into polysilicon. However, such process approaches require the use of quite unusual process steps, and would therefore be more expensive.

The innovative teachings set forth herein include a novel load element for integrated circuits. This load element is a very high-impedance compact vertical resistance. This resistance readily provides a very compact load element, which can provide a sub-picoAmpere current.

A further advantageous teaching of the present application is a novel SRAM cell, wherein very-high-impedance doped-oxide load elements are used to provide a 4-transistor SRAM cell with very low standby current (less than a picoAmpere). Thus, this cell provides extremely high power efficiency, while also providing compact layout.

A particular advantage of this doped-oxide resistance element is that its temperature dependence provides a reasonably close match to the temperature dependence of the junction leakage in the integrated circuit. Thus, areas can be selected so that the current passed by the load elements is greater than the leakage current at every operating temperature, but the current passed by the load elements is small enough that battery energy is well conserved. (Minimization of load current is driven by the demands of battery lifetime. As long as the specification for battery lifetime can be met, increased pull-up current will help the electrical operation of the cell.) The static power consumption of a full-CMOS device (six-transistor cell) will be defined by the leakage current in any case, so it may be seen that the SRAM embodiments enabled by the present invention can actually achieve power dissipation levels which are reasonably close to those of a full-CMOS SRAM using 6-transistor cells.

The innovative load used in the SRAM of the present invention will not be slower than an analogous six-transistor cell. In fact, if desired, some of the area savings provided by the compact load element can be

used to enlarge the driver and pass transistors, so that an SRAM according to the present invention can be made faster than a full-CMOS SRAM of comparable dimensions and technology.

A further advantage of the SRAM of the present invention is that it can be compactly laid out in a single-polysilicon, single-metal configuration. This means that fabrication costs can be drastically reduced over the double-polysilicon and double-metal technologies commonly used. This in turn means that yield can be increased. While this configuration is somewhat slower than embodiments using double-level metal, its advantages may make it preferable for some applications.

Note also that the fabrication process is much simpler than that of conventional DRAM processing. DRAM processing normally requires the use of charge pumps and (at the 1M (one megabit) level and above) of trench processing. Thus, DRAM process development has increasingly diverged from the processing used for general-purpose digital circuits. This process divergence has contributed to the high cost of entry into the DRAM manufacturing business. By contrast, the SRAM provided by the innovative teachings herein is not only compatible with standard logic processing (requiring only one additional masking and implantation step), but can actually be made simpler than standard logic processing (since functional and compact SRAMs can be made with a single-poly single-metal process). This means that, by using the innovative teachings set forth herein, companies wishing to manufacture low-cost memory can easily begin to manufacture SRAMs.

The lowest-cost (mass-market) SRAMs have typically had access times which are less than those of the fastest mass-market DRAMs by about 30-50%. The increasing speeds of advanced commercial microprocessors have made this access time more relevant, since (for example) a 20 MHz microprocessor can typically access a 40 nsec SRAM in one cycle of the processor's internal clock, but an 85 nsec DRAM will require at least two clock cycles. Moreover, SRAMs are much more convenient for system designers, because they do not require refreshing. However, even the lowest-cost SRAM chips have normally had a substantially higher cost per bit than DRAMs.

A recent trend in the design of small computers (such as those built around an 80386 microprocessor) has been to use SRAM rather than DRAM chips for main memory. Notwithstanding the high cost of SRAMs, their advantages have led to such use in high-end personal computers. Thus, the SRAM described herein may also be particularly advantageous for applications where SRAMs are competing with DRAMs for system design. The present invention provides a cost-per-bit which is much lower than that of the traditional SRAM process, and much closer to that of a DRAM.

Of course, memory cells do not have to be used only in memory parts. Microprocessors (and other complex logic parts) commonly contain substantial quantities of memory. The present invention provides a very low-power compact memory array, and blocks of memory of this kind can readily be inserted into the design of a complex logic part. A particular advantage of the disclosed single-poly, single-metal layout is that the space over this memory cell can readily be used, in complex logic parts, for routing lines in second-level metal. Similarly, in triple-poly processes, it may be possible to route lines in third poly right over the memory array.

The innovative load element described herein can also be used in non-memory circuits in a wide variety of other integrated circuit devices, including analog integrated circuits and various random-logic digital circuits.

Preferably this improved high-impedance load device is used in combination with a full CMOS process. This means that the compact load can be used in locations where high pull-up current is not necessary, and PMOS active devices can be used in other locations. For example, in the SRAM provided by the presently preferred embodiment, the peripheral logic is full-CMOS, i.e. uses PMOS active devices for pull-up (e.g. for bit line precharge and in buffers).

The present invention also discloses a novel method for fabricating doped-oxide loads of this type. In this novel method, a polysilicon capping level is deposited over the oxide before it is implanted. This capping level of polysilicon means that the implant energy can be selected so that the peak of the implant falls in the middle of the oxide, and yet the peak of

the implant distribution is a fairly broad peak. (That is, the straggle of the implant is caused to be reasonably high.) Thus, sharp gradients in conductivity do not occur within the small thickness of the oxide.

Another novel teaching of the present application is that a gate oxide is preferably used for the doped oxide conductor. This gate oxide is formed, using methods well known to those in the MOS art (such as the growth of a sacrificial gate oxide layer), to have a very high purity and high quality microstructure. This means that the qualities of this oxide can be very closely controlled. In alternative embodiments, an oxide over polysilicon can be used to provide a poly-to-poly resistor, but this is less preferable.

The use of gate oxide and a polysilicon capping layer has the further advantage that the tail of the implant which dopes the oxide will also dope the substrate. This assures a low contact resistance between the resistor and the substrate.

An SRAM cell which has such a high-impedance load may be more susceptible to single event upset than a 6-transistor CMOS SRAM cell. However, the SRAM provided by the present invention will be no worse in this respect than a conventional DRAM cell.

Single-event upset is normally caused when a particle of ionizing radiation (for example, an alpha particle) is absorbed by the integrated circuit. As the particle passes through the substrate, it will generate a flood of electron-hole pairs. These carriers will diffuse to all parts of the integrated circuit, so that logic states which are stored as charged packets in the substrate will be lost.

The SRAM cell provided by the present invention has dimensions which are more than 40% smaller than a 6-transistor full-CMOS SRAM cell, for comparable device dimensions. The precise area savings will, of course, depend on the particular process and layout optimization being used, but a substantial area savings is available in any process.

A further advantage of the disclosed SRAM cell, and of the disclosed load element, is that the scaling is extremely favorable. As is well known to those in the integrated circuit art, the minimum dimensions of devices in mass production have been continually reduced, over a period of years,

to achieve lower cost and greater functionality. To adapt existing device designs to reduced manufacturing dimensions, direct linear shrinkage is typically used. This process is known as "scaling." For example, once a process has been shown to be reliable, manufacturers may attempt to
5 implement an "80% shrink," where all lateral dimensions in the device layout are simply multiplied by 0.8.

Although linear scaling is the ideal case, adjustments must be made in practice. For example, scaling of the vertical dimensions must often be adjusted. As lateral dimensions shrink, vertical dimensions (such as the
10 depth of the source/drain junctions, the thickness of the gate oxide and thick field-isolation oxides, and the thicknesses of deposited layers) are normally also reduced, but this reduction is often not proportional to the lateral shrinkage. For example, the minimum thickness of the gate oxide will be limited by leakage and breakdown characteristics. Many device
15 characteristics do not scale favorably to smaller dimensions. For example, metal lines tend to become slower: the resistance (per unit length) of a metal line scales approximately as the square of the scaling parameter, but its capacitance (per unit length) scales with an exponent which is slightly less than one (due to fringing field effects). Thus, an important
20 criteria in selecting process features is scaling, since it is desirable not to design in a process feature which will soon have to be designed out again.

The present invention is particularly advantageous in its scaling behavior. The specific resistance of the vertical resistors provided is so high that one minimum-area ($lambda^2$) contact provides a current equal
25 to the leakage current generated by active devices over an area of about one hundred to one thousand $lambda^2$. As the minimum dimension lambda is scaled, the area of the resistor will naturally scale in approximate proportion to the area of the circuit, and therefore the load current will track the leakage current over a wide scaling range.
30 Of course, if a higher or lower area-specific resistance (ohm-cm^2) is desired, the implantation dose may be changed. At higher doses the innovative load element exhibits a more linear relation of I to V. (At the doses used in the presently preferred embodiment, the disclosed load

element has electrical characteristics which are rather nonlinear, as discussed below.)

A further advantage of the disclosed innovative process is that it does not introduce critical process steps, but merely takes advantage of an existing critical process step. Gate oxide growth is very critical in MOS processing, and a tremendous amount of engineering has been invested to achieve reliable processes for manufacturing thin gate oxide layers with very high quality and very low defects. The disclosed innovative load takes advantage of this engineering, and of the presence of these steps in a normal MOS process flow, to provide a new functionality without requiring additional process controls or any significant yield degradation.

A further novel and advantageous teaching is that high-impedance resistors, according to the present invention, can be combined with V_{DD} power supply routing through a substrate diffusion. By routing power supply through a substrate diffusion, the high-impedance oxide resistors can be provided at the surface of this diffusion, where polysilicon lines make connection from the power supply voltage to the cell nodes. The load elements provided by the present invention are essentially no larger than the area which would be required for this contact any way, so that it may be seen that the area of the SRAM cell provided by the present invention is almost as small as that which would be required for a 4-transistor SRAM cell with no load element whatsoever (if such a thing were possible).

A further novel teaching provided by the present invention is an integrated circuit wherein a chain of high-impedance load elements as disclosed is used as a resistive divider network, to provide a high-impedance fully static reference voltage at a desired fraction of the supply voltage V_{DD}. Such a reference voltage is highly advantageous in many applications, since higher-power negative-feedback circuits can be turned on, when needed, to provide a low-impedance output which tracks this high-impedance reference voltage.

In the presently preferred embodiment, the peripheral logic (which includes such conventional elements as address decoders, word line drivers, sense amplifiers, output buffers, write buffers, etc.) is full CMOS. Thus,

PMOS devices are used to pull up the bit lines for pre-charge, although only passive load elements are used for pull-up in the cells.

A similar technique of combining high-impedance and low-impedance pull-ups can be used in random logic. Where it is simply necessary to maintain a node in a high state, or to assure that a node is not in an unknown state after having been inactive for some time, high-impedance load elements can advantageously be used. Where rapid low-to-high transitions are needed, PMOS pull-up devices would be used. For example, such a high-impedance load element could be used with a one-shot circuit which pulled up a node when a low-to-high transition was needed. For another example, such a high-impedance load can be used in open drain circuits, e.g. for wired-OR logic.

Another sample use of the high-impedance load to the present application is as a latching feedback element in logic circuits. For example, where two inverters are in series, the output of the second inverter could be fed back through a high-impedance load to the input of the first inverter. Since the load is so high-impedance, this load would not significantly retard the time required to switch the input to the first impedance. However, this feedback could provide enough current to maintain the first inverter in a known and stable state, until some other upstream active logic element applied a current to switch the first inverter.

Yet a further alternative embodiment includes high-impedance oxide loads in a in a bipolar or biCMOS integrated circuit. As is well known to those skilled in the art of integrated circuit fabrication, biCMOS integrated circuits typically include NPN bipolar devices, in addition to the NMOS and PMOS devices used for conventional CMOS. See, for example, T. Yuzuriha et al., "Submicron Bipolar-CMOS Technology using 16 GHz f_T Double poly-Si Bipolar Devices," 1988 IEDM Proceedings 748; Chiu et al., "Non-overlapping Super Self-Aligned BiCMOS with 87ps Low Power ECL," 1988 IEDM Proceedings 752; Chapman et al., "Submicron BiCMOS Well Design for Optimum Circuit Performance," 1988 IEDM Proceedings 756; Kobayashi et al., "High Performance LSI Process Technology: SST CBi-CMOS, 1988 IEDM Proceedings 760; all of which are hereby

incorporated by reference. In biCMOS circuits, the high-impedance load described above can be substituted for a PMOS pull-up transistor, just as in CMOS circuits.

In a further alternative class of embodiments, a dielectric over polysilicon is doped to provide a high-resistivity resistor.

Such resistors have now been experimentally demonstrated, and turn out to have properties which are surprisingly different from the doped-grown-oxide resistors of the primary embodiment. Such resistors tend to exhibit a more linear relation between voltage and current, which can be advantageous in some circuits, and also tend to have a different relation between doping level, impedance, and peak field strength.

A further class of embodiments of the invention provides a very different device structure, which provides substantial advantages and which can be used for many of the same purposes, from a circuit designer's point of view, as the class of embodiments discussed above.

In this alternative class of embodiments, an oxide resistor is formed over polysilicon. As is well known to the skilled in the art of integrated circuit fabrication and/or device structures, the surface of the polysilicon is not microscopically smooth to the same degree that the surface of a clean monocrystalline silicon wafer is. Thus, the integrity of oxides grown on polysilicon is typically very much less than that of oxides grown over a silicon substrate. Even if an oxide or other dielectric is deposited on polysilicon, the integrity of a dielectric will typically not be as good as that of the same dielectric layer on a monocrystalline silicon substrate.

In this alternative class of embodiments, a thin layer of silicon dioxide (or other dielectric) is deposited over polysilicon, and is doped to provide a high-impedance load.

Surprisingly, it has been discovered that such thin leaky dielectric layers over polycrystalline material have very different electrical characteristics from a comparable a leaky dielectric over monocrystalline silicon. For example, it has been found that the conduction mechanism, in the doped gate oxide, is Frenkel-Poole conduction. In such conduction, the current (and therefore the resistance) varies exponentially with the applied voltage. By contrast, in leaky dielectrics over polysilicon according

to this class of embodiments, it has been experimentally discovered that a very linear V(I) curve can be obtained. That is, such devices act more nearly as if they were ideal resistors, where current is directly proportional to applied voltage over a certain range.

5 It should also be noted that the oxide resistor over polysilicon tends to break down at a much lower dopant concentration.

This resistor has actually been demonstrated using a polysilicon top contact layer. However, it should also be noted that this resistor can also be used with other top contact layers. For example, a metal top capping 10 layer, such as aluminum alloy could be used instead. (Depending on the metal system used, it may be necessary to interpose a layer of a diffusion barrier material, such as titanium nitride, between the leaky oxide and the top contact layer).

A further innovative teaching set forth herein is an SRAM cell, 15 including two driver transistors, two pass transistors, and two load resistors, wherein the load resistors for the two nodes of the cell have different sizes (and therefore different impedances). The ratio of the resistors' impedances has been chosen in accordance with the leakage characteristics of the two nodes of the cell, as actually laid out. That is, leakage is 20 determined by the combination of junction area and perimeter length in the SRAM cell layout actually used. In the SRAM cell of the presently preferred embodiment (as in many SRAM cell layouts), the diffusions in the two nodes of the cell do not have equal parameter lengths. Thus, in the presently preferred embodiment, unequal load impedances are used 25 to compensate for the resulting unequal leakage.

The presently preferred embodiment also provides a novel SRAM cell layout, and features of this novel layout can optionally be applied to SRAM cells in other technologies too. According to this innovative teaching, the SRAM cell is fabricated in a process which allows two layers 30 of polysilicon, and the second level of polysilicon is used solely for the V_{SS} (ground) lines.

The ground line is routed as an extremely broad stripe, whose pitch (line width plus spacing width) is approximately equal to two row pitches of the memory array. These layers are preferably aligned so that the

edges of the second-polysilicon line, within the array, all fall on top of the first polysilicon level. Thus, metal step coverage problems are avoided. In addition, these POLY-2 lines act as a ground plane, to provide increased protection from electrical noise signals.

BRIEF DESCRIPTION OF THE DRAWING

The present invention will be described with reference to the accompanying drawings, which show important sample embodiments of the invention and which are incorporated in the specification hereof by
5 reference, wherein:

Figure 1A schematically shows the layout of the SRAM cell of the presently preferred embodiment, and Figure 1B shows a circuit diagram of the layout of Figure 1.

Figure 2 shows the temperature dependence of the resistor of the
10 presently preferred embodiment, as compared to the temperature dependence of substrate leakage current.

Figure 3 shows a section of an integrated circuit device with load elements, according to the present invention, during the process of fabrication.

15 Figure 4 shows an example of the architecture of an SRAM enabled by the present invention.

Figures 5A-5H are overlays, showing the outlines of mask levels which can be used, in a sample embodiment, to implement an innovative SRAM cell which demonstrates a further class of important inventive teachings.

20 Figure 6A-6D are a set of graphics showing the experimentally measured I(V) curves for vertical-current-flow resistors, according to a further embodiment of the invention, which include a thin doped oxide layer over polysilicon.

Figures 7A-7G are overlays, showing the outlines of mask levels which
25 can be used, in a sample embodiment, to implement an innovative SRAM cell which demonstrates a further class of important inventive teachings.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The numerous innovative teachings of the present application will be described with particular reference to the presently preferred embodiment, wherein these innovative teachings are advantageously applied to the particular problems of low-power CMOS technology, and particularly to a low-power SRAM. However, it should be understood that this embodiment is only one example of the many advantageous uses of the innovative teachings herein. For example, the innovative load structures described herein can optionally be used in logic or analog circuits, as well as in SRAMs. In general, statements made in the specification of the present application do not necessarily delimit any of the various claimed inventions. Moreover, some statements may apply to some inventive features but not to others.

It will be recognized by those skilled in the art that the innovative concepts disclosed in the present application can be applied in a wide variety of contexts. Moreover, the preferred implementation can be modified in a tremendous variety of ways. Accordingly, it should be understood that the modifications and variations suggested below and above are merely illustrative. These examples may help to show some of the scope of the inventive concepts, but these examples do not nearly exhaust the full scope of variations in the disclosed novel concepts.

Figure 1B shows the circuit connections of the novel SRAM memory cell which is enabled by some of the innovative teachings of the present application. Electrically this cell resembles a conventional four-transistor SRAM cell, **except** that the load resistors 114 have a much higher impedance than has been normal in an NMOS SRAM. In the presently preferred embodiment, with a total cell area of about 125 square microns, the impedance of resistors 114 is in the neighborhood of 5 Teraohms ($5x10^{12}$ ohms). For smaller cell dimensions, even higher effective resistance values can be used. When the wordline (not shown) is pulled high, to turn on NMOS pass transistors 104A and 104B, one of the two driver transistors 112A or 112B (whichever one is on, depending on the data stored in the cell) will sink current, through pass transistor 104A or 104B, from one of the bitline pair BL or BL-bar. As a result, the voltage

on one of the bitlines begins to change. A sense amplifier senses the resulting voltage differential on the bitline pair, and provides a digital data signal accordingly. In the write mode, the desired data signal is driven onto the bitlines, and the pass transistors 104 are turned on to reset the
5 state of the driver transistors 112.

The speed of an SRAM will be determined by many factors other than cell size, such as the speed and drive capability of drivers in the decoders, the word line drivers, and the sense amplifiers. These factors are all dependent on the relative dimensions given to various devices, as
10 well as on the general process and minimum dimension used. The innovative teachings herein can be applied to a wide variety of NMOS and CMOS SRAM designs, including both high-speed and low-speed parts, to produce area savings without any degradation of speed. The cell parameters which affect the speed of the read operation are primarily the
15 widths of the driver and pass transistors, and those widths can even be increased if desired. The write operation may be made slightly faster, since the high-impedance loads will source approximately no current to the low bitline during the write operation.

Figure 4 shows the overall organization of one example of an SRAM
20 integrated circuit provided by the present invention. The arrays 400 contain memory cells such as those shown in Figures 1A and 1B. Row address bits X_0-X_7 encode the row address of the cell to be accessed, and column address bits Y_0-Y_7 encode the column address of the cell to be accessed. When an address transition is detected by circuit 402,
25 equilibrator circuits 404 precharge the bitline pairs. As soon as the new address has been decoded, one of the row decoders 410 drives the wordline of the selected row of cells.

Meanwhile, the column decoder 420, driven by data from the buffer 418, will multiplex the bitline pair of the selected column to sense
30 amplifier 430. This then provides digital data signals to the data out buffer 440.

Of course, as will be readily recognized by those skilled in the art of memory design, a tremendous variety of architectural options exist. For example, multiple subarrays can be used, the array sizes can be varied,

multiphase power-down control logic can be used, and other such modifications are well known.

Figure 1A shows the layout of a sample embodiment of an SRAM enabled by the present invention. This drawing schematically shows the different as-patterned shapes of the thin films which would be overlaid, by a series of mask operations (which will be detailed below), to produce a functional integrated circuit.

A polysilicon word line 102 runs across the rows of the memory cell array. This word line 102 gates pass transistors 104A and 104B. These two pass transistors connect to the pair of bit lines 106A and 106B (which are also referred to as BL and BL-bar) to the two nodes 110A and 110B. These nodes are cross-coupled. Driver transistor 112B has its gate line 121 connected (through buried contact 124) to node 110A. Similarly, the other driver transistor 112A has its gate line 123 connected, through buried contact 122, to node 110B. Thus, the cross-coupled transistor pair 112A and 112B provide a latch. However, note that the polysilicon lines 121 and 123, which are connected to the nodes 110A and 110B, respectively, are also connected, through a vertical-current-flow resistor area 114, to a heavily doped active device diffusion 116. The diffusion 116 is connected to the positive power supply V_{DD}. Thus, for example, in the state where driver transistor 112B is turned off, node 110B will be steadily pulled high, by the small current through resistor 114B, so that transistor 112A is held on and node 110A is held low (despite the very small current through resistor 114A). The cell can stay in this condition indefinitely. When a read operation is desired, the polysilicon word line 102 will be driven high, to turn on pass transistors 104A and 104B. This will connect the nodes 110A and 110B, respectively, to bit line 106A (BL) and bit line 106B (BL-bar). The metal bit lines make contact at ohmic contact locations 128. An additional contact 130 makes ohmic contact to the active device region which is accessed by driver transistor 112B. Note that the V_{SS} supply line 132 is also connected, through an additional ohmic contact 134, to provide a contact to the p-type well, to prevent the potential of the well from floating.

The complete array of memory cells is defined by replicating a cell as shown (through mirror reflection on the top side and point reflection on the right side, in the orientation shown) to produce a block of four cells, which can then be replicated.

5 A sample process flow for fabricating this SRAM is as follows. This process flow is included to provide extremely clear disclosure of the best mode as presently practiced. However, it should be recognized that, as of the filing date of the present application, the following is not an established production process. As is well known to those skilled in the 10 art of semiconductor manufacturing, processes may be extensively modified in the transfer to production. A tremendous variety of modifications could be made in this process flow, as will readily be recognized by those skilled in the art.

This sample process flow is as follows:

15 1. The starting wafer is a (100) oriented wafer, doped n-type to a resistivity of about 20 to 40 ohm-centimeters. After clean-up, an initial oxide is grown to about 950 Ångstroms, and about 1,500 Ångstroms of silicon nitride is then deposited over the oxide. Photoresist is then deposited, and patterned according to the N-well pattern. Exposed 20 portions of the nitride are then etched away by plasma etching, and phosphorus is implanted to dope the N-well. In this sample embodiment, phosphorous is implanted at 175 keV at a dosage of $8.5 \times 10^{12} cm^{-2}$. A first field oxide is then grown to about 5,500 Ångstroms. (Note that this field oxide will grow generally in places which were exposed by the N-well 25 mask, where phosphorous was implanted.) The remaining silicon nitride is then cleared, and boron is implanted to dope the P-well areas. (The first field oxide, which is thick over the N-well areas, will keep this implant out of the N-well areas.) In this sample embodiment, the P-well boron dose is 5.0×10^{12} at 100 keV. A long high-temperature drive step will then 30 be performed to drive in the N-well and P-well dopings (for example about 250 minutes at about 1150 degrees C). The first field oxide is then stripped. This completes the formation of the N-well and P-well regions, in which the PMOS and NMOS active devices (respectively) will be formed.

2. The active device areas will now be fabricated. First, a pad oxide is grown, to about 600 Ångstroms, and nitride is deposited, to about 1,500 Ångstroms. Photoresist is deposited and patterned, so that the areas where active devices will be desired are covered, and remaining areas are
5 exposed. A plasma etch is now used to strip the nitride from these areas. The photoresist is now stripped, and another layer of photoresist is deposited and patterned to expose only the regions where channel stops for the NMOS devices are desired. Boron is now implanted, e.g. at 30 keV at a dosage of $0.8x10^{14}$ per centimeter squared, and the photoresist
10 is then stripped. A high temperature oxidation is now performed, to grow oxide to a thickness of about 5,900 Ångstroms. (This is the field isolation oxide 310, seen in Figure 3.) A plasma etch now removes the remaining silicon nitride portions.

3. The next steps form the active devices and the high-
15 impedance resistors.

A sacrificial gate oxide is now grown to a thickness of about 350 Ångstroms. A blanket implant is now performed to adjust the threshold voltages of the active devices. In the presently preferred embodiment, this V_T-adjust implant is 20 keV Boron at a dosage of
20 $3.0x10^{12}$ per centimeter squared. The sacrificial oxide is now stripped.

The slice is again cleaned up, and the final gate oxide 320 (seen in Figure 3) is grown. In the presently preferred embodiment, this oxide is grown to 225 ± 25 Ångstroms, at a temperature of 950 degrees C in a dry atmosphere which includes argon, oxygen, and a
25 chlorinating agent such as TCA. Of course, alternatively, a wide variety of other gate dielectric thicknesses could be used. Results in the literature commonly show gate oxide thicknesses near 150 Ångstroms or less, and such thicknesses can also be used (although somewhat less preferably) with the innovative resistor structure and process disclosed herein.

30 A thin polysilicon capping layer 330 (seen in Figure 3) is now deposited over the gate oxide. In the presently preferred embodiment, this polysilicon is deposited to 500 ± 25 Ångstroms. After this thin polysilicon layer 330 is deposited, a brief phosphorus diffusion is preferably performed. In the presently preferred embodiment, this is

performed using $POCl_3$. This achieves a final sheet resistance in the polysilicon capping layer of about 25 ohms per square.

Another photoresist layer (shown as photoresist layer 340 in Figure 3) is deposited, and is patterned to expose areas where the
5 oxide resistor is desired. Arsenic is now implanted to form the doped oxide film 320' in desired locations. Where the thickness parameters are as given above, arsenic is implanted with an energy of 100 keV. The dosage is preferably in the range of from about $5x10^{15}cm^{-3}$ to about $1.5x10^{16}$ per square centimeter. (In a recent example, successful results
10 have been demonstrated at a dose of $1.4x10^{16}$ per square centimeter. Results using a dose of $1.6x10^{16}$ per square centimeter were less successful.) (Optionally, the implant dose can be adjusted at this stage, to compensate for any deviation in the actual measured thickness of the gate oxide actually grown.) (In a further alternative embodiment, an
15 additional light phosphorus implant (e.g. $3x10^{13}$ per centimeter squared at 100 keV) can be added as a backing implant. This assures that the junction 352 in the substrate, which results from the tail from the arsenic implant which is used to dope the oxide, will not be too abrupt.) The resist is then ashed and stripped. (The first polysilicon layer 330 will
20 remain in place, to protect the resistor oxide 320' from contaminants and harsh atmospheres in subsequent processing steps (e.g. in the asher.))

Another layer of photoresist is now applied and patterned, to expose areas where buried contacts are desired to be formed. (Buried contacts are contacts which are formed directly between
25 a polysilicon layer and the substrate in an active device area.) A brief polysilicon etch, and a very brief oxide etch, are now performed to expose the substrate in buried contact areas. An arsenic implant is now performed to dope the buried contact areas, e.g. at 50 keV with a dose of $5.0x10^{14}$ per square centimeter. The resist is now ashed and stripped.

30 A second polysilicon deposition, which contains the bulk of the polysilicon layer thickness, is now performed. The thickness of this second deposition is preferably about 4,000 Ångstroms. This second

deposition will make contact to the first thin polysilicon layer, and will also make contact directly to the substrate at the buried contact locations.

The polysilicon layer will now be phosphorus doped (e.g. by $POCl_3$ deposition), to a net sheet resistance of about 10 ohms per square. After clean-up, photoresist is deposited and patterned to expose the areas where the polysilicon layer is desired to be removed. A short oxide etch is applied, to clear native oxide from the exposed areas of polysilicon, and a silicon etch is then performed to clear the polysilicon from the undesired areas. The photoresist is then removed. A short oxidation is now performed, to passivate the exposed surfaces of the polysilicon layer. The remainder of the active device fabrication steps are entirely conventional, e.g. formation of N- LDD (lightly doped drain) regions and N+ and P+ source/drain regions by masked implantation steps.

4. The foregoing steps essentially complete the formation of the active devices. The remaining steps are primarily directed to interconnect and hermeticity.

An interlevel oxide is now formed, e.g. by low-temperature oxidation to deposit 500 Ångstroms of undoped silicate glass, followed by 5500 Ångstroms of phosphorus-doped silicate glass. (Alternatively, this can be done using "spin-on glass" (a widely used sol-gel composition which, when baked, provides a silicate glass). This interlevel oxide is then densified and reflowed, to provide a cleaner surface for subsequent steps.

Another level of photoresist is now deposited and patterned, to expose locations where contacts are desired to be formed. A long oxide etch is now performed, to etch down to the substrate at contact locations. The photoresist is then stripped.

The metal layer will now be formed. In the presently preferred embodiment, 8,000 Ångstroms of aluminum alloy is deposited, patterned, and etched, to provide metal connecting lines in a desired pattern.

Protective overcoat deposition and bond pad etch can then be performed according to conventional technology, to complete fabrication of the device.

Of course, the foregoing process flow is merely illustrative, and can be widely modified and varied. For example, if it is desired not to use buried contacts, TiN local interconnects could be used instead, or both buried contacts and local interconnects could be omitted. The use of the
5 preliminary polysilicon capping layer facilitates the use of buried contacts with the present invention, since this layer contributes to the successful fabrication of buried contacts as well as to the fabrication of high-impedance loads according to the present invention, but this is certainly not a necessary feature of the invention.

10 When the first sample embodiment was implemented, using a minimum feature size (lambda) of 1.2 microns, the resulting cell size was found to be 8.4 microns by 14.9 microns (total cell area 87 $lambda^2$). In this first embodiment, the driver transistors preferably have a width of 2.2 microns and a length of 1.1 microns, and the pass transistors preferably
15 have a width of 1.2 microns and a length of 1.4 microns.

An alternative embodiment was also tested, wherein the driver transistors had a width of 2 microns and a length of 1.2 microns, and the pass transistors had a width of 1.5 microns and a length of 1.2 microns, but this alternative embodiment was found not to give fully adequate AC
20 performance. Thus, comparison of this alternative embodiment with the first embodiment indicates a further subpoint, regarding the electrical ratio of the cell. In general, the electrical (effective) channel width of a transistor can be estimated (at least at scales near 1.2 micron) by subtracting 0.5 micron from the drawn gate width. Thus, a parameter to
25 consider is the ratio WLR_D/WLR_P, where WLR_D is the ratio of each driver transistor's effective (electrical) channel width to its channel length, and where WLR_P is the ratio of each pass transistor's effective (electrical) channel width to its channel length. For the alternative embodiment just discussed, this ratio is 1.5. By contrast, in the first embodiment as
30 described, the ratio WLR_D/WLR_P is equal to about 3.1. Therefore, it is most preferable (although not strictly necessary) that the ratio WLR_D/WLR_P be equal to or greater than 2.

Test devices have been fabricated to demonstrate the oxide resistor. Following is a table of measured values of current for resistors of this kind. These sample devices were fabricated using an arsenic implanted dose of $1.4x10^{16}cm^{-2}$.

TABLE 1

Site	Voltage	Temperature	Background Leakage	Load Current Per Cell
1	3	25C	.25pA	5.48fA
	5	25C	.30pA	51.80fA
	3	80C	.50pA	986.00fA
	5	80C	.90pA	3.99pA
2	3	25C	.55pA	7.68fA
	5	25C	.25pA	203.10fA
	3	80C	.85pA	1.57pA
	5	80C	.30pA	6.50pA
3	3	25C	0pA	85.90fA
	5	25C	.40pA	2.83pA
	3	80C	.15pA	5.662pA
	5	80C	.35pA	11.18pA
	3	40C	.50pA	244.30fA
	5	40C	.55pA	4.882pA
4	3	25C	.20pA	12.70fA
	5	25C	.20pA	371.00fA
	3	80C	.50pA	586.40fA
	5	80C	.65pA	2.00pA
5	3	25C	.35pA	330.00fA
	5	25C	.90pA	6.00pA
	3	80C	.15pA	8.21pA
	5	80C	.15pA	12.41pA
	3	40C	.60pA	755.30fA
	5	40C	.60pA	8.175pA

5 These measurements were made with the positive supply voltage V_{DD} connected to the substrate. If it is desired to avoid any asymmetric (rectifying) characteristics, a further alternative teaching of the present

application is that load elements can be connected back to back by connecting them into a diffusion in a common active device area.

Note that the measured resistances are highly nonlinear with temperature. If this dependence is modelled using the relation $I = I_0\exp(C_t(T - T_0))$, then C_t, for measurements of current at 3 V at 25 C, 40 C, and 80 C, ranges from 0.055 up to 0.097.

At doses above $2\text{x}10^{16}\text{cm}^{-2}$, the behavior begins to change significantly. For a dose of $5\text{x}10^{16}\text{cm}^{-2}$, the area-specific resistance was found to be about 120 kilohm-micron^2. Moreover, the resistance of these heavily implanted devices also exhibits much more linear temperature dependence and I-V characteristics. If the dose is increased to $1\text{x}10^{17}\text{cm}^{-2}$, the area-specific resistance was found to have decreased only to about 100 kilohm-micron^2. At doses of $2\text{x}10^{16}\text{cm}^{-2}$, the behavior of the resistors appeared to be very widely scattered: some exhibited linear dependence on temperature, and some exhibited exponential dependence. For the SRAM cell described above, doses in the neighborhood of about $5\text{x}10^{15}\text{cm}^{-2}$ have been found to be partially effective.

A dose of about $5\text{x}10^{15}\text{cm}^{-2}$ produces an as-implanted concentration, in the oxide, of slightly more than $1\text{x}10^{21}\text{cm}^{-3}$. After process steps which include high-temperature steps equivalent to about an hour at 975 C, the peak concentration of dopant in the oxide is estimated to be about $1\text{x}10^{21}\text{cm}^{-3}$, with some fall-off of concentration at the upper and lower interfaces.

The measured current through the test samples may be translated into familiar resistance parameters. (In view of the nonlinearities referred to above, it should be noted that the "resistance" is calculated from the current measured when 3 V is applied at 25 C. Different values would be calculated at other voltages or temperatures.) For square resistors of 1.2 microns on a side, the measured current (at 3 V and 25 C) corresponds to a resistance of about 30 to 35 Teraohms. This corresponds to an area-specific resistance of about 50 Teraohm-micron^2. (Other samples tested had values, for this parameter, of as high as 788 Teraohm-micron^2 and as low as 13 Teraohm-micron^2.) For the 225 Ångstrom film tested, the equivalent bulk resistivity was about 220

Gigaohm-cm. (Other samples tested had values, for this parameter, of as high as 3500 Gigaohm-cm and as low as 58 Gigaohm-cm.)

The following table provides additional measured data, taken from further device structures which make use of some of the inventive concepts disclosed herein. Thus, while this data is not strictly necessary for practicing the invention, this data may be helpful in showing the advantages of the various points of invention set forth herein.

TABLE 2

64K SRAM with Oxide Resistor Load Elements:
Active and Power Down Currents over Voltage and Temperature

	I_{CC} @ 25 C Active/ /CMOS	I_{CC} @ 40 C Active/ /CMOS	I_{CC} @ 85 C Active/ /CMOS	I_{CC} - 100 C Active/ /CMOS
2V	304.2uA/ /2.9nA	303.6uA/ /3.35nA	316.5uA/ /92.8nA	326uA/ /398nA
3V	2.307mA/ /12.9nA	2.323mA/ /14.40nA	2.355mA/ /123.1nA	2.354mA/ /442nA
3.5V	5.068mA/ /27.2nA	5.003mA/ /29.57nA	4.75mA/ /147.1nA	4.634mA/ /509nA
5V	19.28mA/ /190nA	18.58mA/ /205nA	16.51mA/ /379.3nA	15.67mA/ /779nA
5.5V	25.42mA/ /331.1nA	24.33mA/ /355nA	21.57mA/ /563.9nA	0.38mA/ /989nA

In this Table, the Active Current is measured with the Device powered up (CE* low). The CMOS (Power Down) Current is measured with the device powered down. Thus, the only current component is the junction leakage in the memory cells. (If this current component were not compensated, the cells would eventually lose their data.) At 40 degrees C and 3.5 V supply, the CMOS current is approximately 30 nA (for a 64K SRAM). For the alternative 256K embodiment of an SRAM as described herein, the CMOS current is approximately equal to 120 nA at 40 C and 3.5 V.

This data shows that an SRAM fabricated according to the innovative teachings set forth here have very good leakage characteristics. This structure provides a memory which can easily be battery backed up.

Following is additional data, showing how the current per resistor
5 varies with voltage and with temperature.

TABLE 3

Measured Resistor Currents per resistor
(1.2 x 1.2 um^2 Oxide Resistor)
over Voltage and Temperature

10

	25 C	40 C	85 C	100 C
2 V	21fA	22.9fA	94.4fA	330fA
3 V	125fA	139fA	261fA	532fA
3.5 V	280fA	310fA	489fA	787fA
5 V	2.06pA	2.23pA	2.88pA	3.39pA
5.5 V	3.57pA	3.84pA	4.84pA	5.48pA

15

As will be obvious to those skilled in the art, this data shows that current increases very sharply (approximately exponentially) with voltage and also with temperature.

Figure 2 is a graph showing the temperature dependence of current
20 through a sample load element according to the present invention (data points shown as circles), and also showing the temperature dependence of leakage current (data points shown as squares). Note that the temperature dependence of the two curves is almost identical. (Note that this is a logarithmic plot, showing the exponential behavior of the current.)
25 As noted above, this correspondence is very advantageous. The specific values shown are for a resistor of 1.44 square microns.

Following is additional data, showing actual test results for a number of oxide resistors fabricated using the methods disclosed in the present application. For each of the test structures, the measured resistance is
30 shown for applied voltages of 2.0, 2.5, and 5.0 volts, at temperatures of 25, 55, and 85 C:

TABLE 4

Measured Resistances in Teraohms:

Lot	25. C			55. C			85. C		
91897A	2.0V	2.5V	5.0V	2.0V	2.5V	5.0V	2.0V	2.5V	5.0V
Wafer#:									
01	129	56.6	3.23	88.0	41.2	2.70	68.8	33.1	2.30
03	337	180	13.9	275	148	11.9	226	124	10.2
05	252	130	8.73	215	112	7.65	182	95.4	6.69
13	281	92.4	3.02	163	60.0	2.46	118	45.7	2.07
16	43.7	18.2	0.861	31.5	13.8	0.723	25.0	11.3	0.618
17	20.4	9.05	0.458	13.9	6.47	0.356	BROKE		
19	103	47.8	3.00	74.3	36.2	2.52	58.8	29.4	2.15
21	88.7	44.0	2.95	69.2	35.4	2.52	56.2	29.2	2.16
23	7.21	1.18	0.101	BROKE					
07	3.84	0.666	0.424	BROKE					
09	10.8	0.945	0.231	BROKE					
11	11.1	2.79	0.0302	BROKE					
Lot 91896A:									
01	41.3	18.3	0.975	30.2	14.1	0.819	23.9	11.4	0.696
03	37.0	16.6	0.917	27.3	12.9	0.771	22.2	10.6	0.658
05	59.7	28.1	1.58	45.9	22.4	1.34	36.7	18.2	1.14
07	61.1	28.3	1.49	46.7	22.2	1.25	37.0	18.1	1.06
09	45.1	20.3	1.06	33.8	15.8	0.894	26.5	12.7	0.759
11	37.4	16.9	0.862	28.7	13.4	0.732	22.6	10.9	0.622
13	123	52.4	2.87	82.4	37.8	2.40	63.6	30.1	2.03

The various implantation parameters which were used to produce these test wafers are listed below. Also listed are derived parameters, including the peak concentration of dopant in the oxide, the minimum concentration of dopant in the oxide, the area-specific dosage which stops in the oxide, and the area-specific dosage which stops in the silicon.

TABLE 5

Lot 91897A	Min cm^{-3} in SiO_2	Max cm^{-3} in SiO_2	Total cm^{-2} in SiO_2	Total cm^{-2} in Si
1-2: 1.4E16@100KeV	2.41E21	2.87E21	6.09E15	3.18E15
3-4: 1.4E16@75KeV	1.46E21	3.61E21	6.04E15	1.62E15
5-6: 1.6E16@75KeV	1.67E21	4.13E21	6.90E15	1.85E15
7-8: 1.8E16@75KeV	1.88E21	4.64E21	7.76E15	2.08E15
9-10: 2.0E16@75KeV	2.08E21	5.16E21	8.62E15	2.32E15
11-12: 2.2E16@75KeV	2.29E21	5.67E21	9.48E15	2.55E15
13-14: 1.4E16@130KeV	1.22E21	2.30E21	4.24E15	8.40E15
15-16: 2.0E16@130KeV	1.75E21	3.29E21	6.05E15	1.20E16
17-18: 2.4E16@130KeV	2.10E21	3.95E21	7.27E15	1.44E16
19-20: 3.0E15@75KeV+1.2E16@100KeV	[illegible]	3.08E21	6.51E15	4.35E15
21-22: 7.0E15@75KeV+1.0E16@100KeV	[illegible]	3.66E21	7.36E15	4.15E15
23-25: 1.0E16@75KeV+8.0E15@100KeV	[illegible]	3.99E21	7.79E15	3.83E15
Lot 91896A				
1-2: 1.0E16@100KeV+9.0E15@130KeV	[illegible]	3.36E21	7.07E15	8.73E15
3-4: 8.0E15@100KeV+1.2E16@130KeV	[illegible]	3.43E21	7.11E15	9.87E15
5-6: 1.0E16@75KeV+1.0E16@150KeV	[illegible]	3.14E21	6.46E15	8.46E15
7-8: 8.0E15@75KeV+1.2E16@150KeV	[illegible]	2.80E21	6.03E15	9.69E15
9-10: 7.0E15@75KeV+1.4E16@150KeV	[illegible]	2.74E21	6.03E15	1.10E16
11-12: 6.0E15@75KeV+1.6E16@150KeV	[illegible]	2.77E21	6.02E15	1.24E16
13: 1.4E16@100KeV				

Figures 5A-5H are overlays, showing the outlines of mask levels which can be used, in a sample embodiment, to implement an innovative SRAM cell which demonstrates a further class of important inventive teachings. These Figures should be regarded as overlays, to more clearly show the complex multilevel structure of this sample embodiment. Of course, layouts, such as those of Figure 5 or Figure 1A, can readily be varied, by a skilled designer,

in a tremendous variety of ways, and it must be understood that the variations described are purely illustrative, and do not limit the claimed innovations.

Note that the embodiment of Figure 5 includes several features which are significantly different from the embodiment of Figure 1A. The design of Figure 5, unlike that of Figure 1A, uses two layers of polysilicon (or polycide, or other equivalent material). (To distinguish these two layers, they are commonly referred to as "POLY-1" and "POLY-2".) In conventional SRAM technology, when a two-poly process is used to build a polysilicon-resistor SRAM, the POLY-1 layer is usually used for transistor gates and for routing ground voltage through the array, and the POLY-2 layer is typically used for providing resistors and for routing the positive supply voltage (V_{DD}) through the array.

However, one innovative feature of this second embodiment is a different use of the two polysilicon levels. The POLY-2 layer is used, inside the array, only for routing ground. The V_{DD} lines are routed in the substrate. This is particularly convenient in connection with the oxide resistor, since the oxide resistor fits into the device structure very much as if it were a buried contact structure.

Driver transistors are indicated as 112A and 112B, and pass transistors are indicated as 104A and 104B (referring to the circuit diagram of Figure 1B).

Figures 5A-5H show the layout of a sample SRAM cell enabled by the present invention. These Figures are overlays: all are drawn to approximately the same scale, and each Figure includes a central reference mark which corresponds to the locations of the reference marks of the other Figures.

To better show the repetitive layout of the preferred embodiment, these Figures actually show four complete memory cells. Devices and nodes have been labelled in the top right cell only, for clarity. The block of cells shown can be replicated, in horizontal and vertical directions, to provide a full array of memory cells.

Figure 5A shows the Active area 502, where the thick field oxide is absent. A transistor will occur wherever the polysilicon layer crosses these active areas (except at buried contact locations, where ohmic contact will be made between the active area and the overlying polysilicon.

Figure 5B shows the Buried-Contact pattern 504, where ohmic contact will be made between the substrate and the overlying polysilicon.

Figure 5C shows the POLY-1 layer 508, which forms the gates of MOS transistors. Note that the two word lines WL_n and WL_{n+1} are continuous with
5 the same lines in neighboring cells, as shown by arrows on these lines, and thus extend across the array.

Figure 5D shows the pattern of POLY/POLY contacts 510 (which define locations where contact is made from the POLY-2 layer to the underlying POLY-1 or active area).

10 Figure 5E shows the Oxide-Resistor pattern 506.

Figure 5F shows the POLY-2 layer 512.

Figure 5G shows the pattern of Contacts 514 (which define locations where contact is made from the METAL layer to the underlying POLY-1 or active area).

15 Figure 5H shows the pattern of the METAL layer 516. The area shown includes two pairs of bit lines (for two columns of cells) namely BL_k and BL^*_k, and BL_{k+1} and BL^*_{k+1}. These four lines are each continuous with the corresponding lines in neighboring cells, as shown by arrows on these lines, and thus extend across the array.

20 The N-well, VT-ADJUST, N+, P+, and PASSIVATION masks are not shown, since they are not particularly relevant to the cell structure used in the array.

Obviously these specific masks could be modified and varied in a very wide variety of ways, and this specific layout does not delimit the claimed
25 invention in any way. This great amount of detail is provided merely to facilitate a full understanding of one sample implementation of the invention, and to comply with the requirements of U.S. patent law regarding disclosure of the contemplated best mode.

In the second SRAM embodiment (described above), note that the load
30 resistors R1 and R2 for the two nodes of the cell are of different sizes, even though the two pass transistors are of identical nominal dimensions, and the two driver transistors also have equal nominal dimensions. On one side of the cell, the load resistor R2 has dimensions of 2.6 microns by 1.2 microns (for a total area of 3.12 microns^2). On the other side of the cell, the load resistor

R1 has one portion whose dimensions are 2.6 microns by 1.2 microns, and also has another portion whose area is 0.85 microns by 0.9 micron, for a total area of 3.88 microns^2. Thus, the areas of the two resistors (and therefore their impedances) differ by more than 20%. (Thus, the cell sizing, in this embodiment is asymmetrical only in the resistors R1 and R2, but symmetrical in the driver transistors D1 and D2, and also symmetrical in the pass transistors P1 and P2.)

The asymmetrical sizing of the load resistors, in the presently preferred embodiment, has been chosen in accordance with the leakage characteristics of the two nodes of the cell, as actually laid out. That is, leakage is determined by the combination of junction area and perimeter length in the SRAM cell layout actually used. In the SRAM cell of the presently preferred embodiment (as in many SRAM cell layouts), the diffusions in the two nodes of the cell do not have equal parameter lengths. Thus, in the presently preferred embodiment, unequal load impedances are used to compensate for the resulting unequal leakage.

This second (and presently preferred) embodiment also provides a novel layout for the SRAM. This novel layout can optionally be applied to other SRAM cells as well. According to this innovative teaching, the SRAM cell is fabricated in a process which provides two layers of polysilicon (or equivalent), and the second level of polysilicon is used solely for the V_{SS} (ground) lines.

The ground line is routed as an extremely broad stripe, whose pitch (line width plus spacing width) is approximately equal to two row pitches of the memory array. The POLY-2 layer is preferably silicided, but of course other conductive materials could be used instead.

This architecture is particularly advantageous in connection with the thin film resistor of the presently preferred embodiment. However, it has other advantages as well. For example, according to this innovative teaching the edges of the second-polysilicon line, within the array, all fall on top of the first polysilicon level. Thus, metal step coverage problems are avoided.

This second embodiment (using 1.2 micron dimensions) provides a cell size, in a layout as shown in Figures 5A-5H, of 6.7 micron by 14.9 micron (total cell area 69 lambda^2).

Figures 7A-7G are overlays, showing the mask level outlines of a single-poly version of an innovative SRAM cell. This layout provides slightly different device sizings than the layout of Figure 1A, which have been found to be more advantageous. As in Figure 5, these Figures should be regarded as overlays, to more clearly show the complex multilevel structure of this sample embodiment. Of course, layouts, such as those of Figures 7, 5, or 1, can readily be varied, by a skilled designer, in a tremendous variety of ways, and it must be understood that the variations described are purely illustrative, and do not limit the claimed innovations.

Note that the embodiment of Figure 7 includes several features which are significantly different from the embodiment of Figure 5. This memory cell is slightly larger than that of Figure 5, but requires the use of only one layer of polysilicon (or equivalent material).

Figure 7A shows the Active area 702.

Figure 7B shows the Buried-Contact pattern 704.

Figure 7C shows the POLY layer 708.

Figure 7D shows the Oxide-Resistor pattern 706.

Figure 7E shows the masking used (at two separate steps) for the P+ and N+ implantation. Areas 707 are protected from the N+ implant (which forms N+ source/drain regions for NMOS devices, in the portions of the active areas which are not covered by this mask or by polysilicon. Such masking is conventionally used in a CMOS process to provide N+ source/drains for the NMOS devices, and P+ source/drains for the PMOS devices. By exposing part of the NMOS area to the P+ implant, well ties (ohmic contacts to the P-type well) can be formed, as in areas 707.

Figure 7F shows the pattern of Contacts 714 (which define locations where contact is made from the METAL layer to the underlying POLY-1 or active area).

Figure 7G shows the pattern of the METAL layer 716.

The N-well, VT-ADJUST, and PASSIVATION masks are not shown, since they do not show significant details within the cell structure of the array.

Yet another class of embodiments has been identified, and may be even more advantageous. In this embodiment, the oxide resistor is used between the first and second polysilicon (or equivalent) layers. In an SRAM according

to this embodiment, the POLY-2 layer can be used to carry both power and ground (V_{DD} and V_{SS}), in alternating stripes. Thus, in this further embodiment the cell area can be even less than in the first and second embodiments described.

5 Such poly-to-poly resistors have now been demonstrated, and have been found to have surprisingly advantageous characteristics. It has been discovered that such thin leaky dielectric layers over polycrystalline material have very different electrical characteristics from a comparable a leaky dielectric over monocrystalline silicon. For example, it has been found that the conduction 10 mechanism, in the doped gate oxide, is Frenkel-Poole conduction. In such conduction, the current varies exponentially with the applied voltage. By contrast, in leaky dielectrics over polysilicon according to this class of embodiments, it has been experimentally discovered that a very linear V(I) curve can be obtained. That is, such devices act more nearly as if they were 15 ideal resistors, where current is directly proportional to applied voltage over a certain range.

Figure 6A-6D are a set of graphs showing the experimentally measured I(V) curves for vertical-current-flow resistors, according to a further embodiment of the invention, which include a thin doped oxide layer over 20 polysilicon.

These Figures show the measured electrical characteristics of several samples of

vertical-current-flow doped-oxide resistors over polysilicon. In each sample, the oxide was approximately 500 Ångstroms thick, and was implanted with 25 arsenic. Each of these Figures includes a curve (labelled I) which shows measured current (with reference to the scale on the left side of the graph), and a curve (labelled R) showing the calculated resistance in ohms (with reference to the scale on the right side of the chart). The current measurement is taken from 7424 resistors in parallel, each of which had an 30 area of approximately 1.44 square microns.

Figure 6A shows data from an oxide sample which was implanted with a dose of 2E15 cm^{-2} of Arsenic ions at 130 keV. At 2 Volts applied, the measured current was 17.35 pA, and the calculated resistance is therefore 8.55E14 ohms (855 Teraohm). At 5 Volts applied, the measured current was

37.00 pA, and the calculated resistance is therefore 1E15 ohms (1000 Teraohms).

Figure 6B shows data from an oxide sample which was implanted with a dose of 6E15 cm^{-2} of Arsenic ions at 130 keV. At 2 Volts applied, the measured current was 24.85 pA, and the calculated resistance is therefore 5.97E14 ohms (597 Teraohms). Note that this graph also includes a third curve, showing the noise floor (which was measured at 1.550 picoAmperes at 2.0 Volts). This helps to show the accuracy of the measurements.

Figure 6C shows data from an oxide sample which was implanted with a dose of 1E16 cm^{-2} of Arsenic ions at 130 keV. At 2 Volts applied, the measured current was 15.75 pA, and the calculated resistance is therefore 9.42E14 ohms (942 Teraohms). At 5 Volts applied, the measured current was 33.00 pA, and the calculated resistance is therefore 1.12E15 ohms (1120 Teraohms).

Figure 6D shows data from an oxide sample which was implanted with a dose of 1.4E16 cm^{-2} of Arsenic ions at 130 keV. At 2 Volts applied, the measured current was 468.0 pA, and the calculated resistance is therefore 3.17E13 ohms (31.7 Teraohms). Note that the behavior of this resistor is exponential in voltage, as shown by curve I_1. This behavior is quite different from that of the examples of Figures 6A-6C, and more nearly resembles that of the resistors discussed earlier, which were fabricated in gate oxide. At 4.8 Volts applied, the resistor broke down, and began to act as a low-impedance linear resistor (as shown by curves I_2 and R_2). The average field strength in the oxide, at breakdown, was in the neighborhood of 1 MV per cm.

Note that oxide-over-poly resistors show even higher resistances than oxide-over-monocrystalline resistors, at comparable doses. Note also that the resistance value of oxide-over-poly resistors is insensitive to arsenic dose, over a range of arsenic doses which spans nearly a decade (from about 2E15 to about 1E16 cm^{-2}, in these specific examples). In addition, the oxide-over-poly resistors act as more nearly linear resistors, which can be highly advantageous in many embodiments. In fact, it may even be advantageous, in some processes, to provide both oxide-over-poly and oxide-over-monocrystalline resistors, so that users can use either of the two types, or

series or parallel combinations of them, at different points in a circuit, to achieve the desired temperature dependence.

This resistor has actually been demonstrated using a top contact layer which is N-type doped polysilicon. However, it should also be noted that this resistor can also be used with other top contact layers. For example, a metal top capping layer, such as aluminum alloy could be used instead. (Depending on the metal system used, it may be necessary to interpose a layer of a diffusion barrier material, such as titanium nitride, between the leaky oxide and the top contact layer).

In fabricating oxide resistors, it is of course preferable to do a preliminary oxidation and deglaze, to reduce the asperities on the polysilicon and improve the integrity of the deposited oxide layer.

In one sample alternative embodiment such resistors could be formed by doping an oxide/nitride/oxide layer, where the oxide/nitride/oxide layer is formed by the process described in U.S. Patent 4,613,956, which is hereby incorporated by reference. Other doped dielectrics may alternatively (and less preferably) be used.

For one example, other dopant species could be substituted for arsenic. Arsenic has the advantages of short stopping distance and relatively low diffusivity. Moreover, since arsenic is such a heavy ion, it provides large momentum-transfer effects in the oxide, since the incoming arsenic atoms will disturb many of the silicon and oxygen atoms in place.

One possible substitution is antimony, which also has the advantages of high mass and low diffusivity. However, alternatively (and less preferably) other species could be used, such as gallium, phosphorus, or silicon.

Another alternative is the use of implanted oxynitrides. Many processes use oxynitrides (SiO_2/Si_3N_4 mixtures) for gate dielectrics, and processes with such oxynitrides can also (less preferably) be adapted for use with the present invention. Silicon nitride generally tends to be a somewhat "tougher" dielectric, with a shorter stopping distance for implants than silicon dioxide.

A further advantage of the disclosed load element is that the lateral spacing of such load elements is not at all critical, and is determined entirely by the spacing of top conductor.

As will be recognized by those skilled in the art, the innovative concepts described in the present application can be modified and varied over a tremendous range of applications, and accordingly their scope is not limited except by the allowed claims.

CLAIMS

What is claimed is:

1. A static random-access memory (SRAM), comprising:
address decoding logic;
a plurality of word line drivers;
one or more sense amplifiers;
5 at least one data output amplifier;
and an array of memory cells, connected so that said word line drivers can select respective rows of cells which then provide data signals to said sense amplifiers;
wherein said cells of said array each comprise:
10 a first pass transistor, interposed between a first circuit node and a first bitline of a bitline pair, and a second pass transistor, interposed between a second circuit node and a second bitline of said bitline pair;
a first driver transistor, connected to pull said first node
15 toward a first power supply voltage, and a second driver transistor, connected to pull said second node toward said first power supply voltage;
a first high-impedance passive load element, connected to pull said first node toward a second power supply voltage, and a second high-impedance passive load element, connected to pull said second node toward
20 said second power supply voltage;
wherein said respective load elements each comprise a thin semi-insulating film which is less than one micron thick, and has an area-specific resistance (as determined for electric fields of about 150 Volts per micron, and for temperatures in the neighborhood of 25 C) in the range of 10
25 to 1000 Teraohm-micron^2, and is connected so that, when said respective node is at a potential which is not equal to said second supply voltage, current flows through said semi-insulating film substantially normal to the plane thereof.

2. The SRAM of Claim 1, wherein said thin semi-insulating film comprises a silicon oxynitride.

3. A static random-access memory (SRAM) cell, comprising:

a first pass transistor, interposed between a first circuit node and a first bitline of a bitline pair, and a second pass transistor, interposed between a second circuit node and a second bitline of said bitline pair;

a first driver transistor, connected to pull said first node toward
5 a first power supply voltage, and a second driver transistor, connected to pull said second node toward said first power supply voltage;

a first high-impedance passive load element, connected to pull said first node toward a second power supply voltage, and a second high-impedance passive load element, connected to pull said second node toward
10 said second power supply voltage;

wherein said respective load elements each comprise a thin semi-insulating film

which is less than one micron thick,

and predominantly comprises silicon dioxide,

15 and is doped with a concentration in the range of about $10^{18}cm^{-3}$ to $10^{23}cm^{-3}$ inclusive

and is connected so that, when said respective node is at a potential which is not equal to said second supply voltage, current flows through said semi-insulating film substantially normal to the plane thereof.

4. The SRAM cell of Claim 3, wherein said thin semi-insulating film comprises a silicon oxynitride.

5. An integrated circuit, comprising:

first and second power supply voltages;

a plurality of circuit nodes, of which at least one node is connected, through a respective active device, to said first power supply voltage, and also

5 connected, through a high-impedance passive load element, to said second power supply voltage;

wherein said high-impedance passive load element comprises a thin semi-insulating film

which is less than one micron thick,

10 and predominantly comprises silicon dioxide,

and is doped with a concentration in the range of about $10^{18}cm^{-3}$ to $10^{23}cm^{-3}$ inclusive

and is connected so that, when said respective node is at a potential which is not equal to said second supply voltage, current flows

15 through said semi-insulating film substantially normal to the plane thereof.

6. The integrated circuit of Claim 5, wherein some groups of said circuit nodes are electrically configured to provide an array of memory cells, and others are configured to implement random logic.

7. The integrated circuit of Claim 5, wherein some groups of said circuit nodes are electrically configured to implement random logic.

8. An integrated circuit load element, comprising:

a thin semi-insulating film which is less than one micron thick, and predominantly comprises silicon dioxide, doped with a concentration in the range of about $10^{18}cm^{-3}$ to $10^{23}cm^{-3}$ inclusive;

a top contact which makes electrical contact to an upper surface

5 of said film, and a bottom contact which makes electrical contact to a lower surface of said film;

said top and bottom contacts being positioned so that, when a voltage is applied therebetween, current flows through said semi-insulating film substantially normal to the plane thereof.

9. The load element of Claim 8, wherein said bottom contact is formed by a diffusion in a body of doped monocrystalline silicon, and wherein said thin semi-insulating film is formed directly on said body.

10. The load element of Claim 8, wherein said thin semi-insulating film comprises a silicon oxynitride.

11. The load element of Claim 8, wherein said thin semi-insulating film comprises a multilayered dielectric.

12. The load element of Claim 8, wherein said thin semi-insulating film comprises a multilayered dielectric, and at least one layer of said semi-insulating film consists essentially of silicon dioxide.

13. The load element of Claim 8, wherein said thin semi-insulating film has a composition which is within 1% of stoichiometry.

14. The load element of Claim 8, wherein the maximum concentration of dopant species in said thin semi-insulating film is less than about $6\times10^{21}cm^{-3}$.

15. The load element of Claim 8, wherein the average concentration of dopant species in said thin semi-insulating film is in the range of about $10^{19}cm^{-3}$ to $10^{22}cm^{-3}$ inclusive.

16. The load element of Claim 8, wherein the average concentration of dopant species in said thin semi-insulating film is greater than about $5\times10^{20}cm^{-3}$.

17. The load element of Claim 8, wherein said thin semi-insulating film comprises a silicon oxynitride, and has an oxygen:nitrogen atomic ratio of at least 4:1.

18. The load element of Claim 8, wherein said thin semi-insulating film has a bulk resistivity (as determined for electric fields of about 150 Volts per micron, and for temperatures in the neighborhood of 25 C) in the range of 30-10,000 Gigaohm-cm.

19. The load element of Claim 8, wherein said thin semi-insulating film has a bulk resistivity (as determined for electric fields of about 150 Volts per micron, and for temperatures in the neighborhood of 25 C) which is less than 10 Teraohm-cm.

20. The load element of Claim 8, wherein said top and bottom contacts make ohmic contact to said thin semi-insulating film.

21. The load element of Claim 8, wherein said thin semi-insulating film has an area-specific resistance (as determined for electric fields of about 150 Volts per micron, and for temperatures in the neighborhood of 25 C) in the range of 10 to 1000 Teraohm-micron^2.

22. The load element of Claim 8, wherein said thin semi-insulating film has a effective resistance, for applied voltages near 3 Volts, which is greater than 3 Teraohms and less than 300 Teraohms.

23. A process for making an integrated circuit, comprising the steps of:

providing a substrate including monocrystalline semiconductor portions therein;

growing a high-quality thin dielectric film on said monocrystalline
5 semiconductor portions;

covering said thin dielectric film with a thin capping layer;

implanting impurities into a predetermined area portion of said thin dielectric film, to induce a significantly increased leakage current therein;

and providing a gate layer over said capping layer, said gate
10 layer being a thin film conductive layer being patterned to form the gate electrode of multiple operable insulated-gate field-effect transistors in predetermined locations, other portions of said high-quality thin dielectric film providing the gate dielectric of said transistors, and said monocrystalline semiconductor portions providing the channel of at least some of said
15 transistors;

and interconnecting ones of said transistors in circuit paths to implement a desired electrical function, wherein some of said circuit paths include current flowing vertically through said increased-leakage-current portions of said high-quality thin film to provide electrical load elements.

24. A static random access memory (SRAM) cell, comprising:

a **first** pass transistor, interposed between a first circuit node and a first bitline of a bitline pair, and a **second pass transistor**, interposed between a second circuit node and a second bitline of said bitline pair, said
5 first pass transistor having nominal width and length dimensions which are substantially equal to those of said second pass transistor;

a **first** driver transistor, connected to pull said first node toward a first power supply voltage, and a **second driver transistor**, connected to pull said second node toward said first power supply voltage, said first pass
10 transistor having nominal width and length dimensions which are substantially equal to those of said second pass transistor;

a **first** passive load element, connected to pull said first node toward a second power supply voltage, and a **second passive load element**, connected to pull said second node toward said second power supply voltage;
15 wherein said first and second passive load elements are respective portions of a common thin film layer,

and wherein said first passive load element is sized to have a significantly greater impedance than said second passive load element,

and wherein the geometry of said transistors is such that said
20 transistors will draw a greater leakage current from said second passive load element than from said first passive load element.

25. The memory cell of Claim 24, wherein all portions of said second thin film layer within said array are connected directly to ground voltage.

26. The memory cell of Claim 24, wherein the pitch of said second thin film layer within said array is equal to twice the row pitch of said array.

27. The memory cell of Claim 24, wherein said first thin film layer consists essentially of doped polycrystalline silicon.

28. The memory cell of Claim 24, wherein said first thin film layer consists of a composite of polycrystalline silicon and a silicide compound.

29. The memory cell of Claim 24, wherein said second thin film layer consists of a composite of polycrystalline silicon and a silicide compound.

30. The memory cell of Claim 24, wherein said second thin film layer consists essentially of doped polycrystalline silicon.

31. The memory cell of Claim 24, wherein said power supply voltage is routed through a junction-isolated diffusion in said substrate.

32. The memory cell of Claim 24, wherein the ratio of the effective channel width to the channel length of each of said driver transistors is more than twice as much as the ratio of the effective channel width to the channel length of said respective pass transistors.

33. A static random access (SRAM) memory, comprising:

address decoding logic;

a plurality of **word line drivers;**

one or more **sense amplifiers;**

at least one **data output amplifier;**

5 and an **array of memory cells,** connected so that said word line drivers can select respective rows of cells which then provide data signals to said sense amplifiers;

wherein said cells of said array each comprise:

a **first** pass transistor, interposed between a first circuit 10 node and a first bitline of a bitline pair, and a **second pass transistor,** interposed between a second circuit node and a second bitline of said bitline pair;

a **first** driver transistor, connected to pull said first node toward ground voltage, and a **second driver transistor,** connected to pull said 15 second node toward ground voltage;

a **first** load element, connected to pull said first node toward a positive power supply voltage, and a **second load element,** connected to pull said second node toward said power supply voltage;

said driver and pass transistors each being field-effect 20 transistors having channel regions in a substrate of monocrystalline semiconductor material, and having gates formed in a **first conductive thin film layer,** said first layer being polycrystalline and comprising a substantial fraction of silicon;

said power supply voltage being routed to said load elements of 25 said cells through a doped portion of said substrate;

ground voltage being routed to said driver elements of said cells through a **second conductive thin film layer,** said second layer being polycrystalline and comprising a substantial fraction of silicon;

wherein all edges of said second layer, within said array, overlie 30 a portion of said first layer;

and wherein said bitline pairs are routed, to ones of said cells of said array, through a third thin film layer which consists essentially of a metallic substance.

34. The memory of Claim 33, wherein all portions of said second thin film layer within said array are connected directly to ground voltage.

35. The memory of Claim 33, wherein the pitch of said second thin film layer within said array is equal to twice the row pitch of said array.

36. The memory of Claim 33, wherein said first thin film layer consists essentially of doped polycrystalline silicon.

37. The memory of Claim 33, wherein said first thin film layer consists of a composite of polycrystalline silicon and a silicide compound.

38. The memory of Claim 33, wherein said second thin film layer consists of a composite of polycrystalline silicon and a silicide compound.

39. The memory of Claim 33, wherein said second thin film layer consists essentially of doped polycrystalline silicon.

40. The memory of Claim 33, wherein said power supply voltage is routed through a junction-isolated diffusion in said substrate.

41. The memory of Claim 33, wherein the ratio of the effective channel width to the channel length of each of said driver transistors is more than twice as much as the ratio of the effective channel width to the channel length of said respective pass transistors.

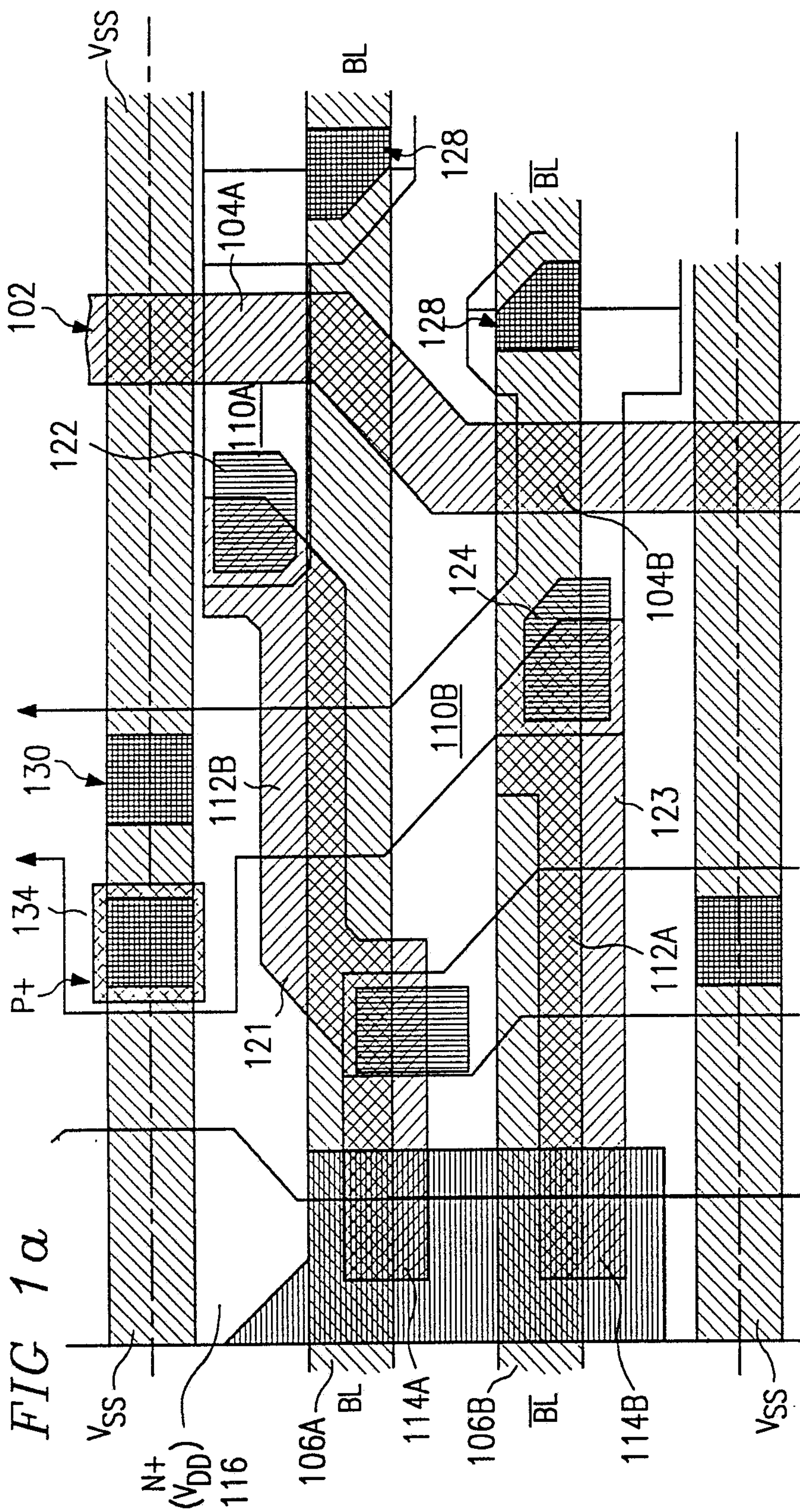


FIG 1a

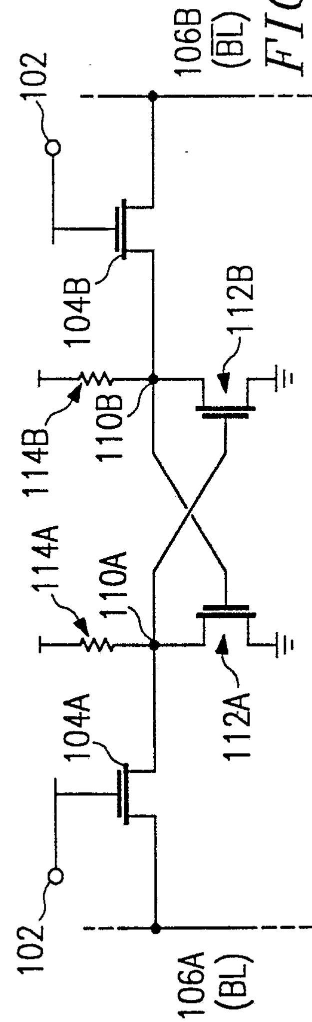


FIG. 1b

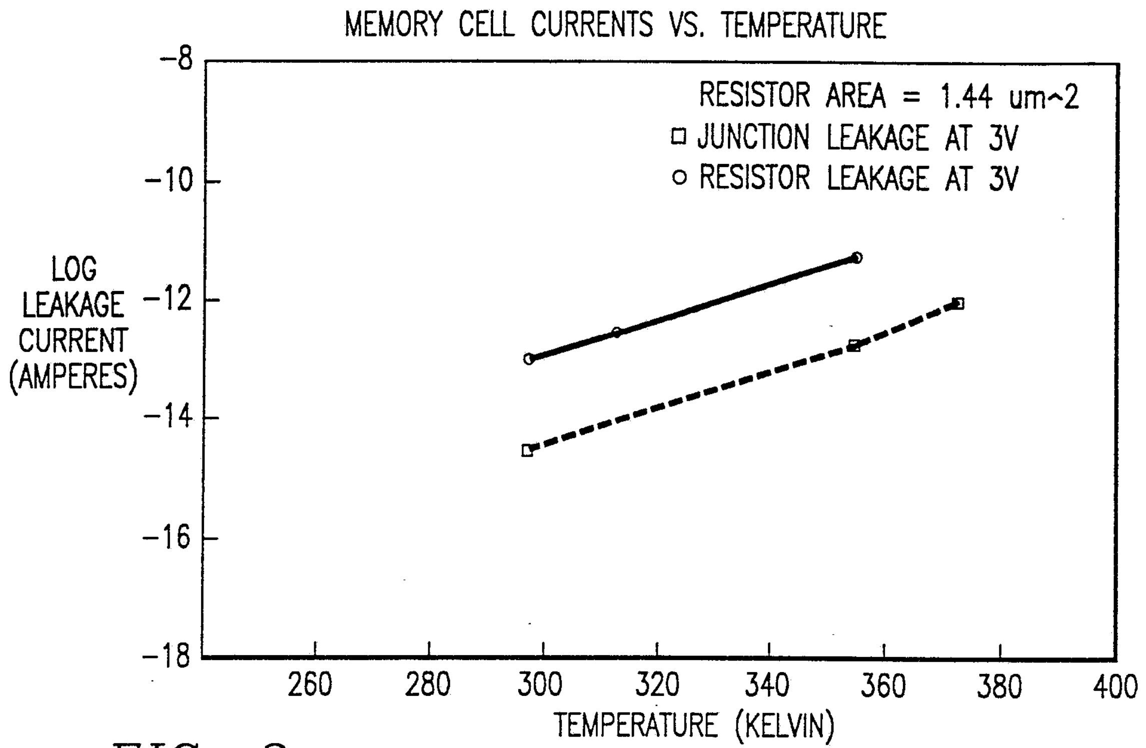


FIG. 2

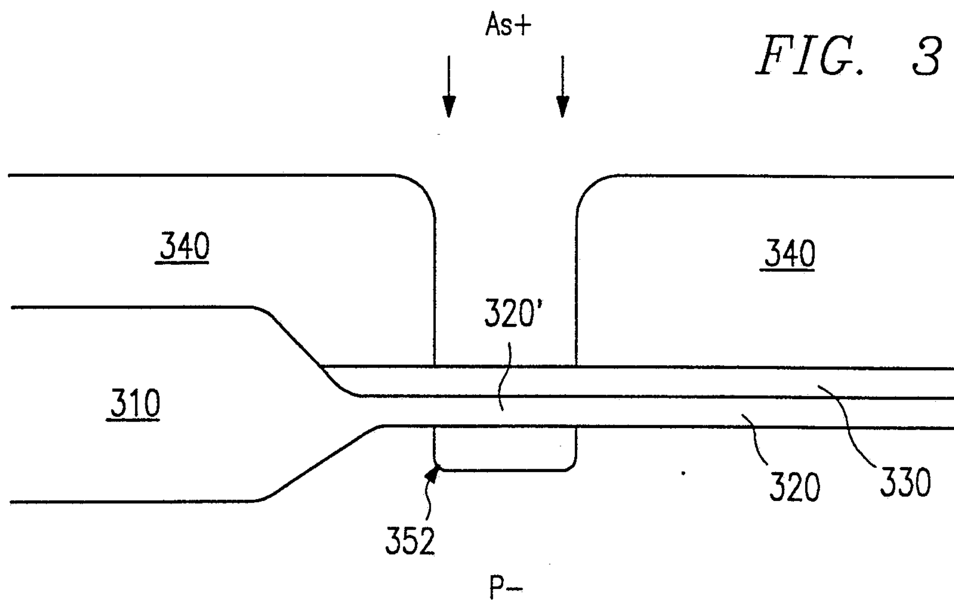


FIG. 3

Y_7 $X_0 \sim X_7$

ROW ADDRESS BUFFER

402

TRANSITION DETECTOR

ROW PRE DECODER

EQUILIBRATOR

EQUILIBRATOR

404

$\overline{Y_7}$ Y_7

CELLS

400

2 SPARE COLUMNS

ROW MAIN DECODER

410

2 SPARE COLUMNS

CELLS

400

420

COLUMN DECODER

COLUMN DECODER

CHIP CONTROL

D_{IN} BUFFER

430

COLUMN SPARE

SENSE AMPLIFIER

COLUMN ADDRESS BUFFER

D_{OUT} BUFFER

418

440

CE R/W $Y_0 \sim Y_6$ D_{IN} D_{OUT}

FIG. 4

SUBSTITUTE SHEET

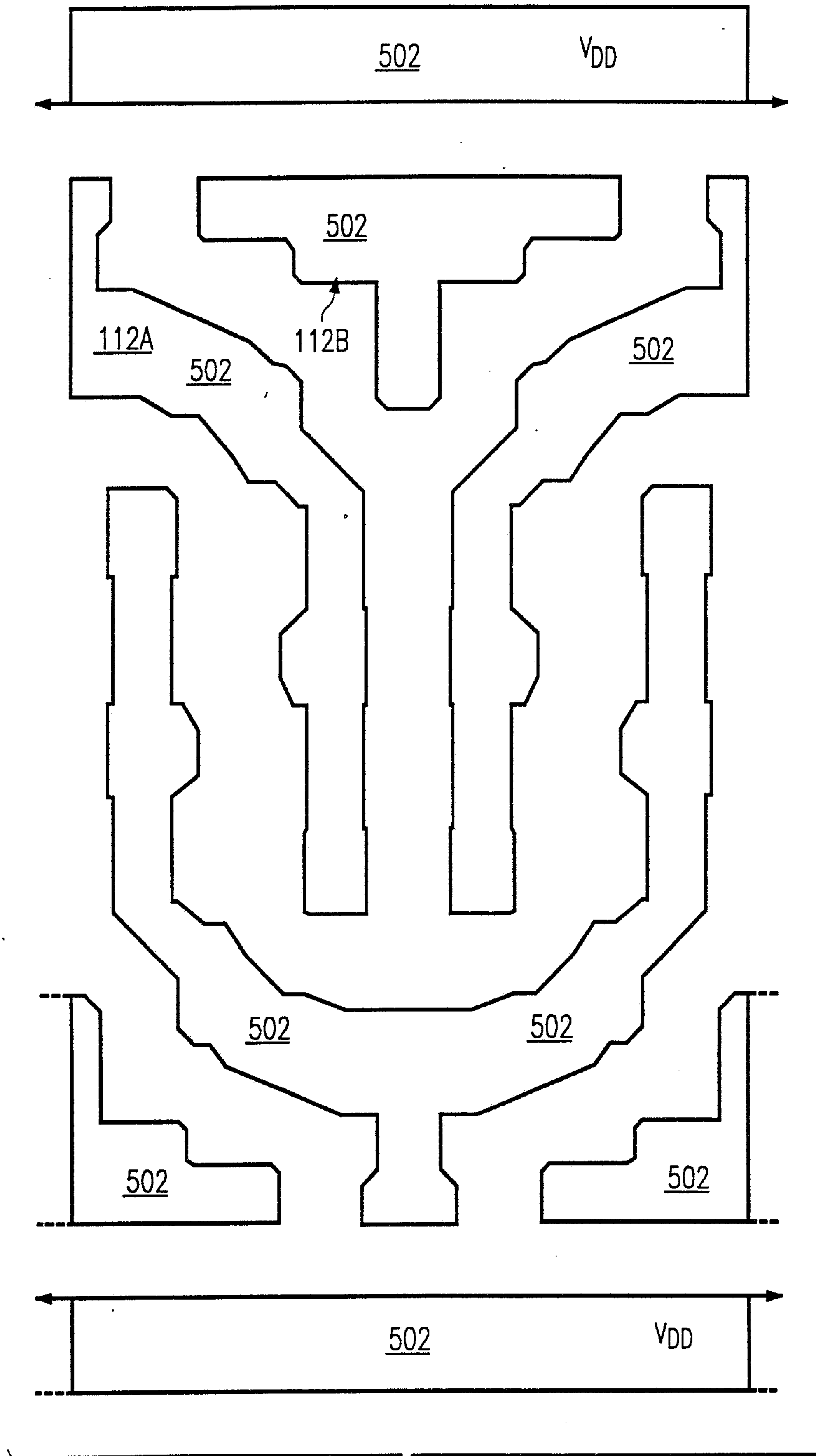


FIG. 5A *ACTIVE*

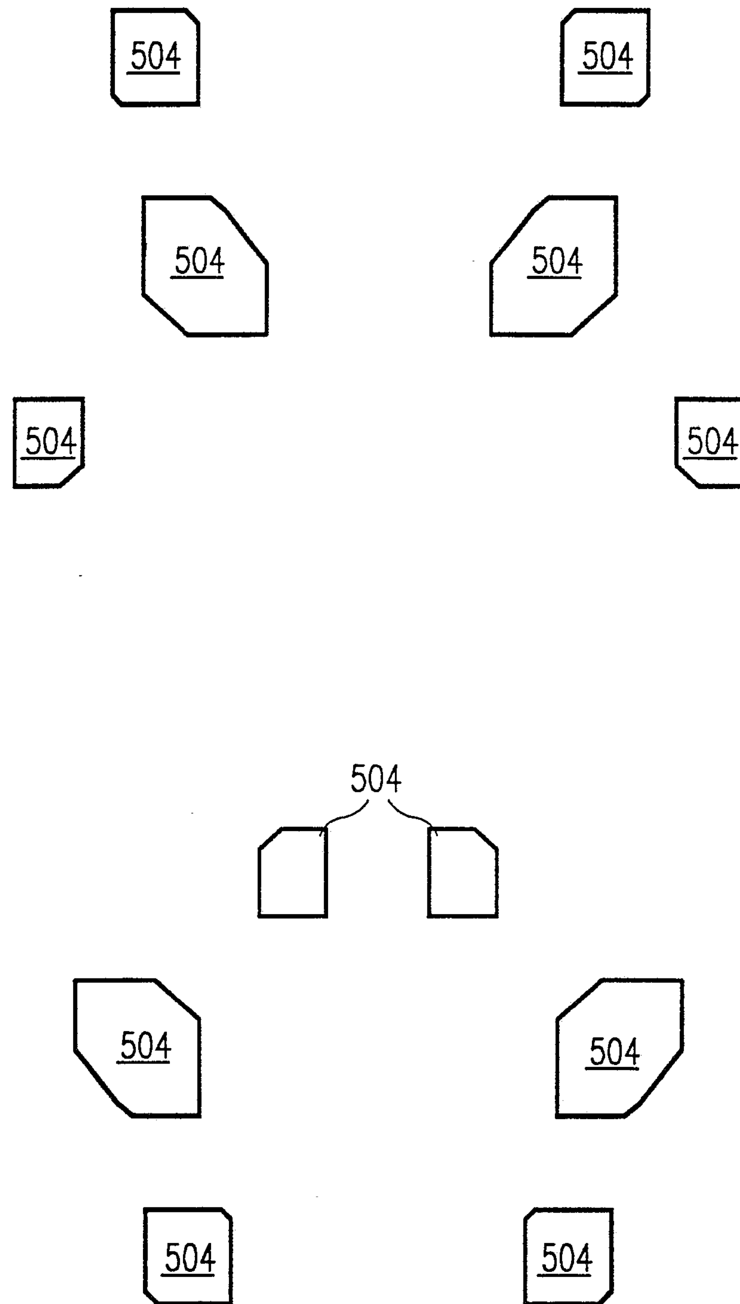


FIG. 5B BURIED CONTACT

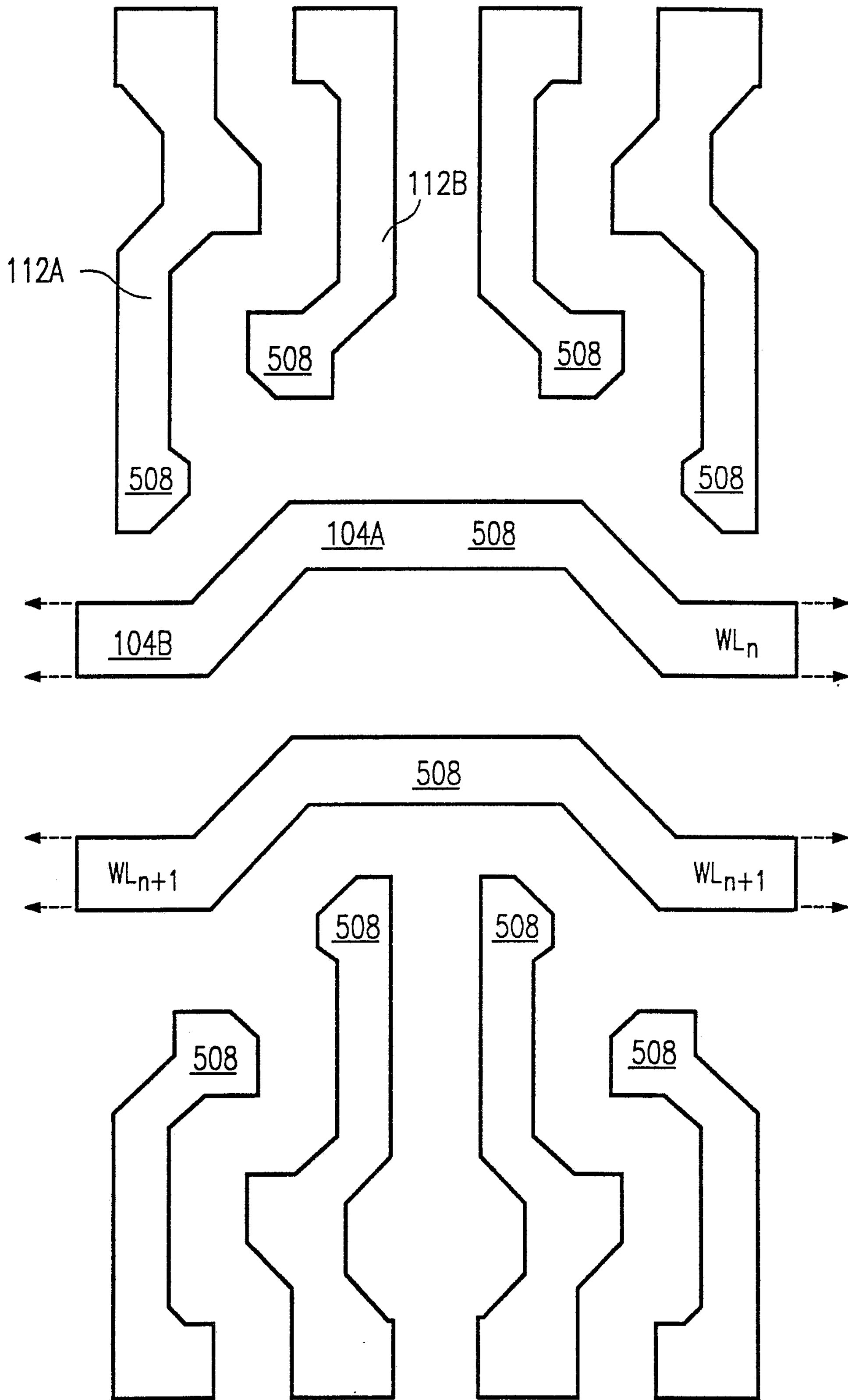
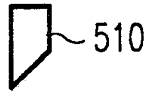
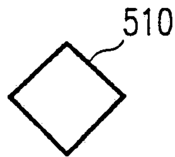
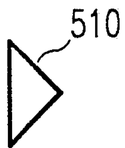


FIG. 5C POLY







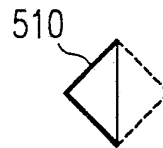


FIG. 5D P1/P2 CONTACTS

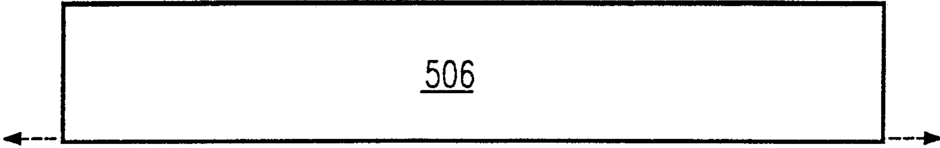


FIG. 5E OXIDE-R

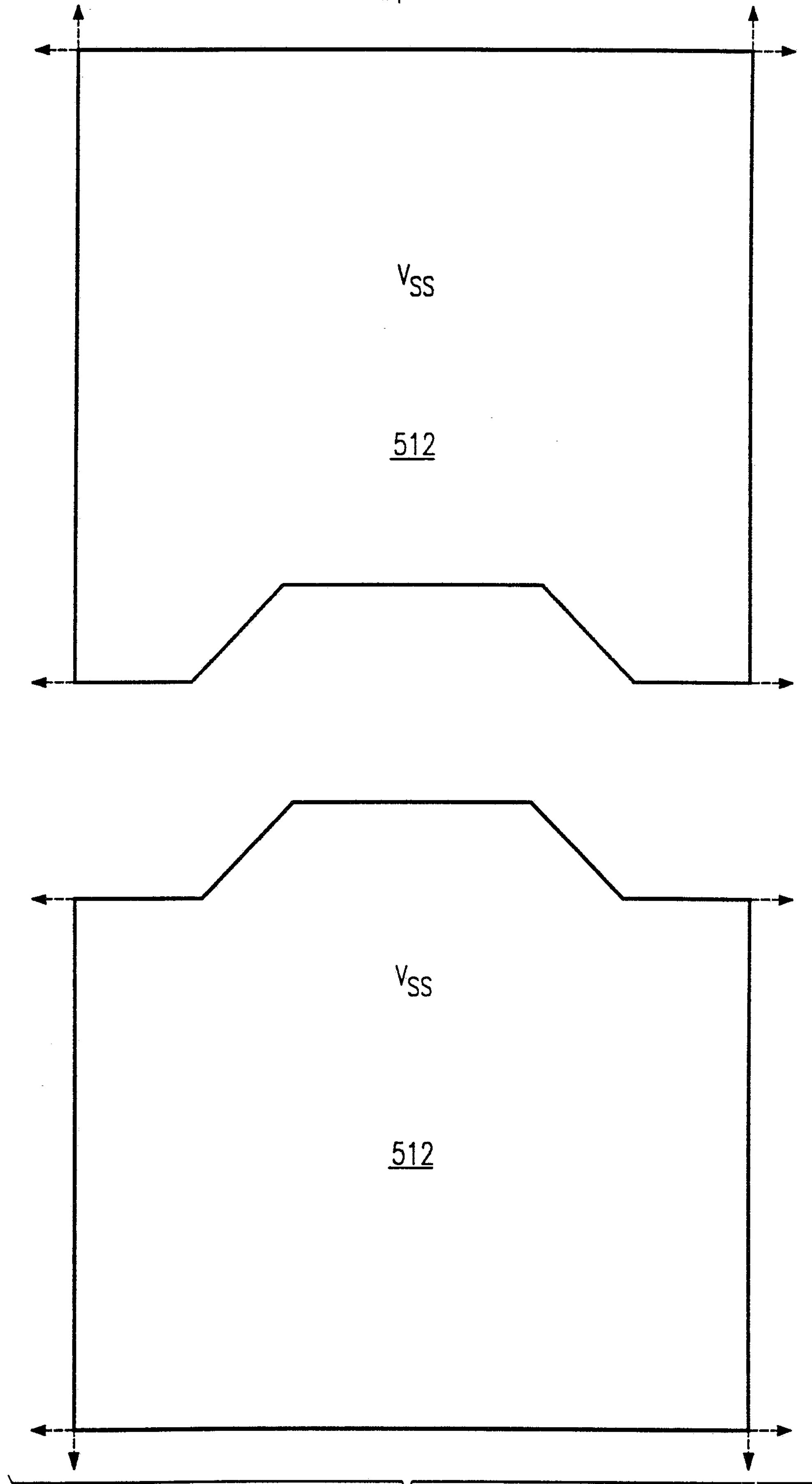


FIG. 5F

SUBSTITUTE SHEET

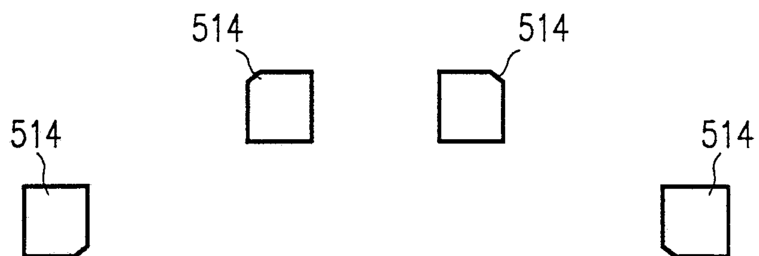


FIG. 5G CONTACTS

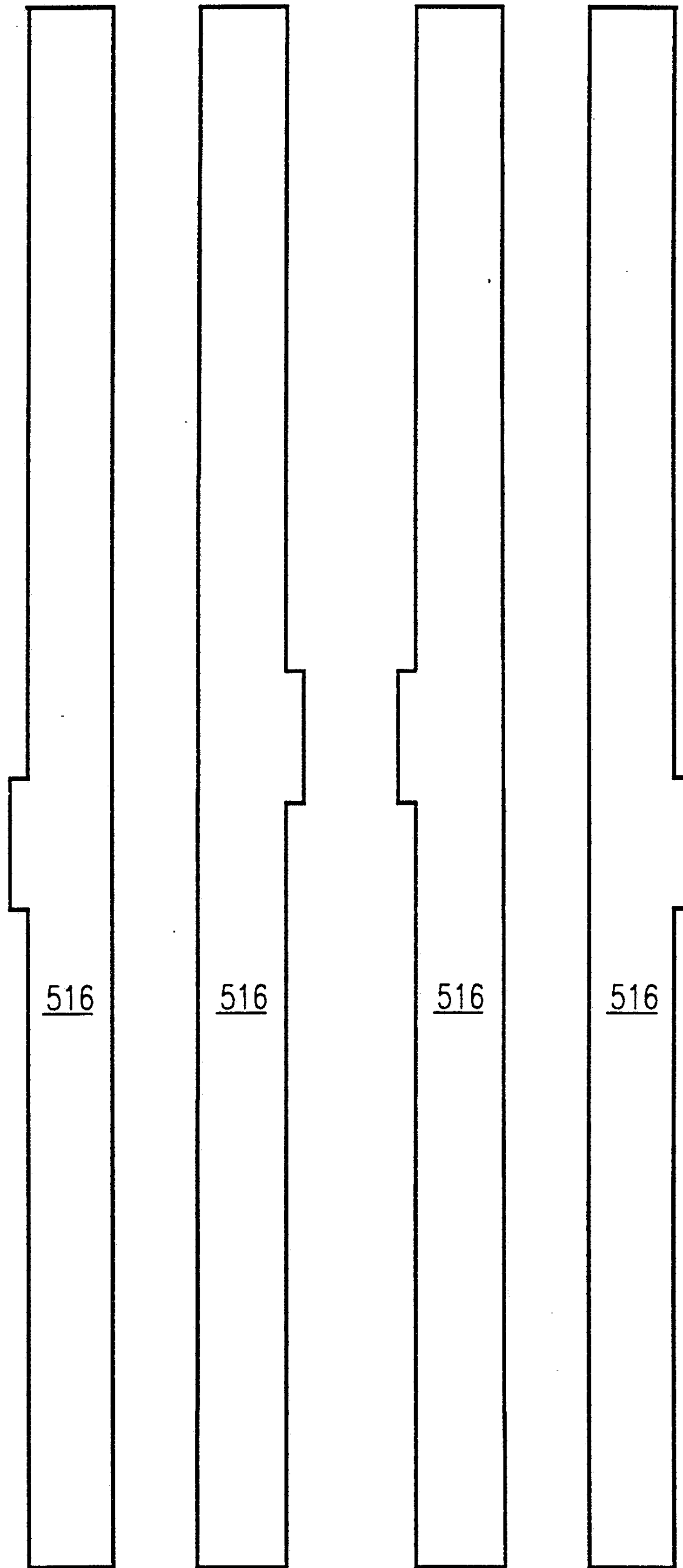


FIG. 5H METAL

SUBSTITUTE SHEET

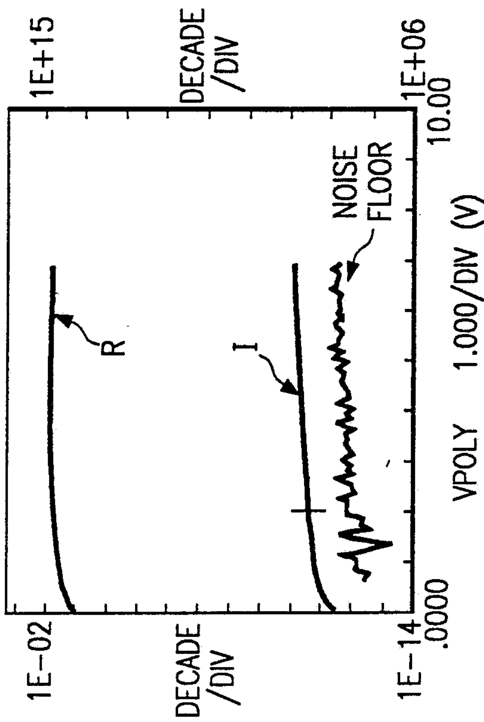


FIG. 6b

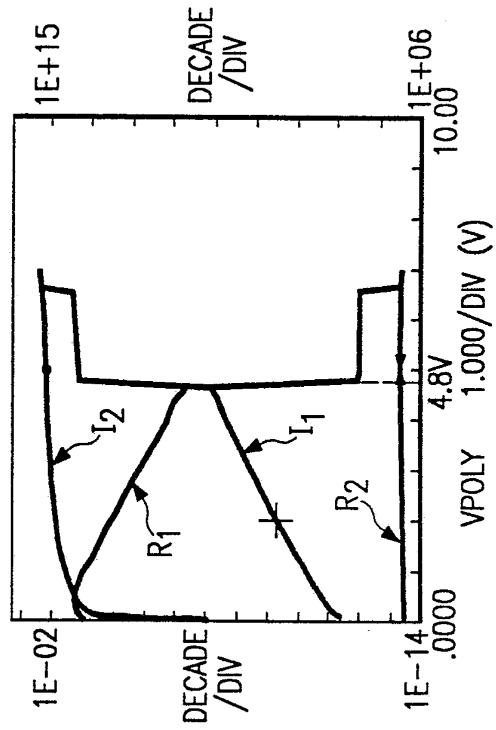


FIG. 6d

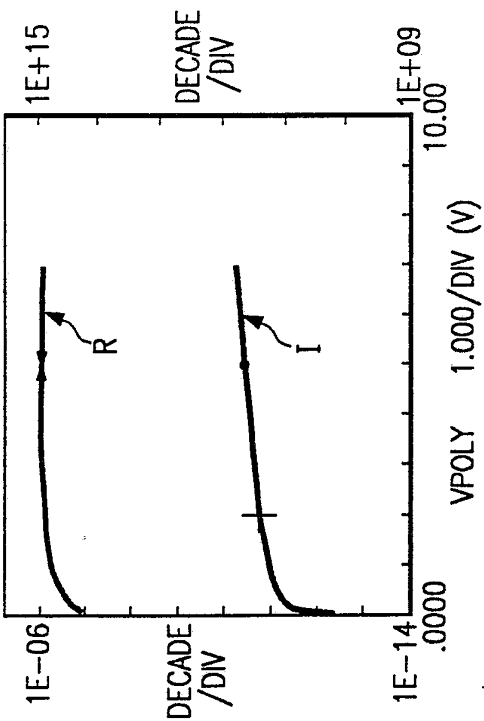


FIG. 6a

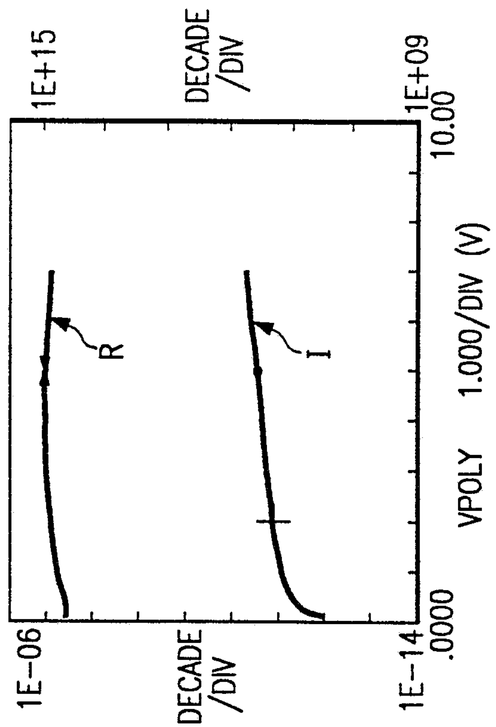


FIG. 6c

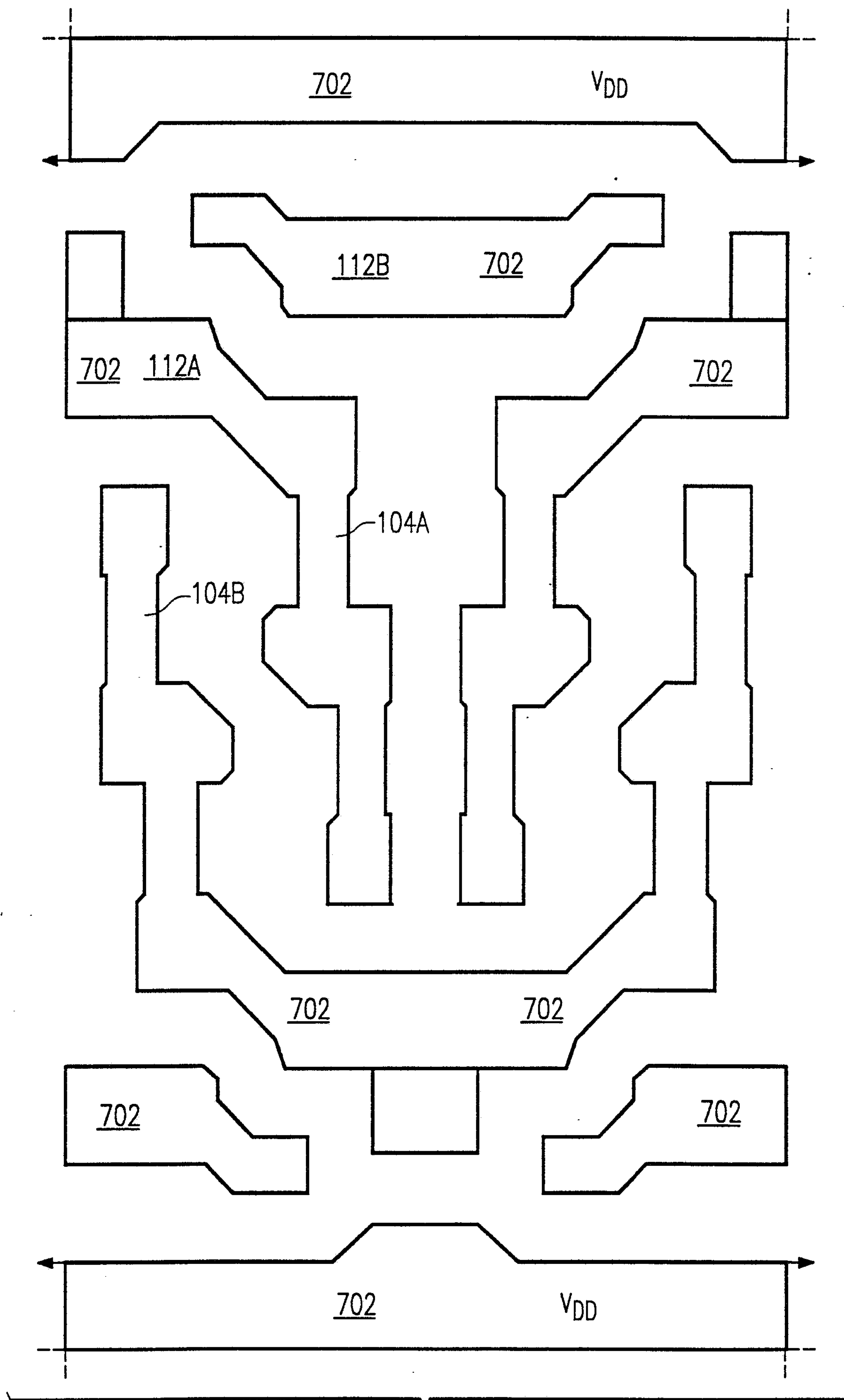


FIG. 7A

SUBSTITUTE SHEET

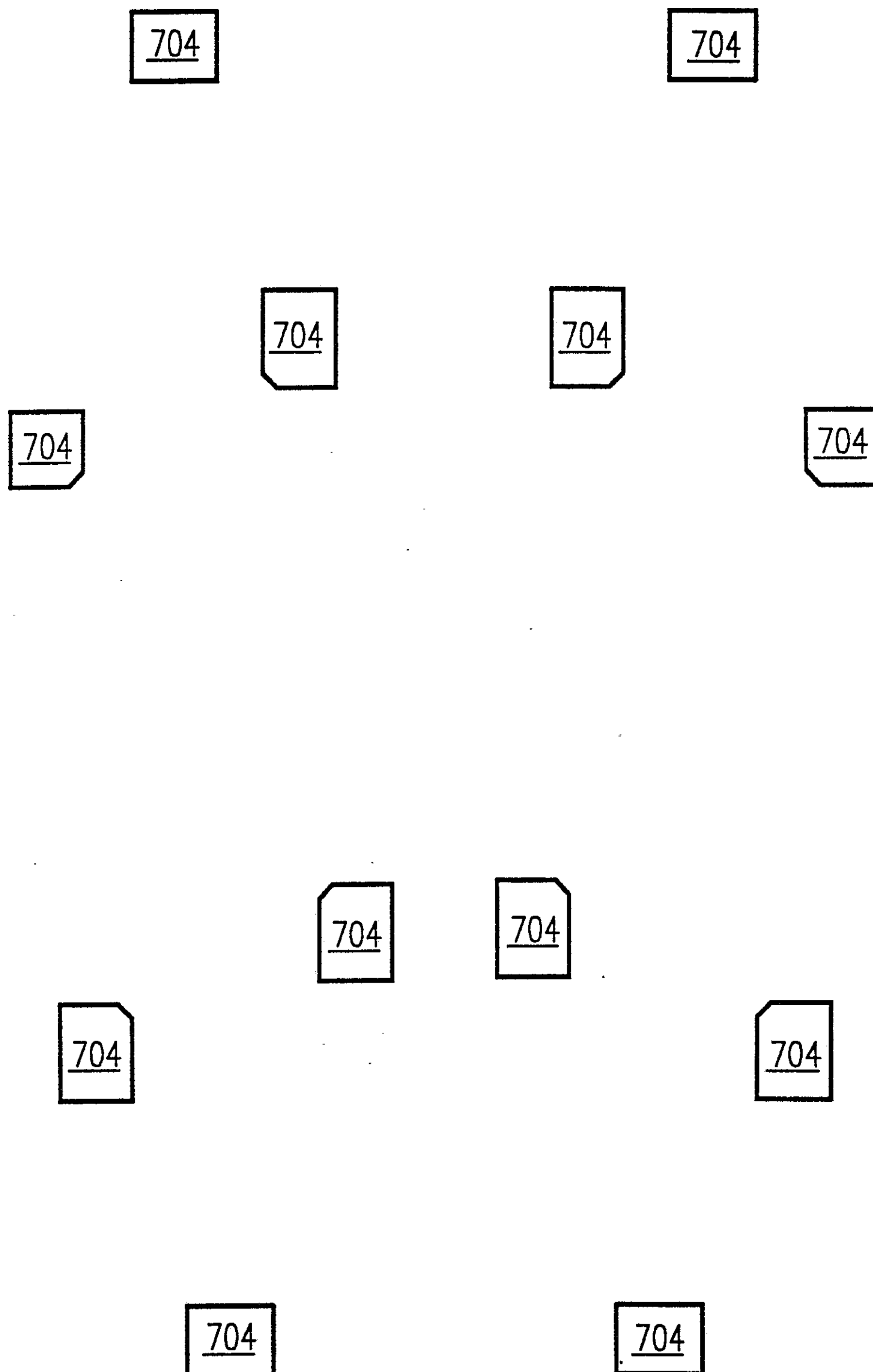


FIG. 7B BURIED CONTACT

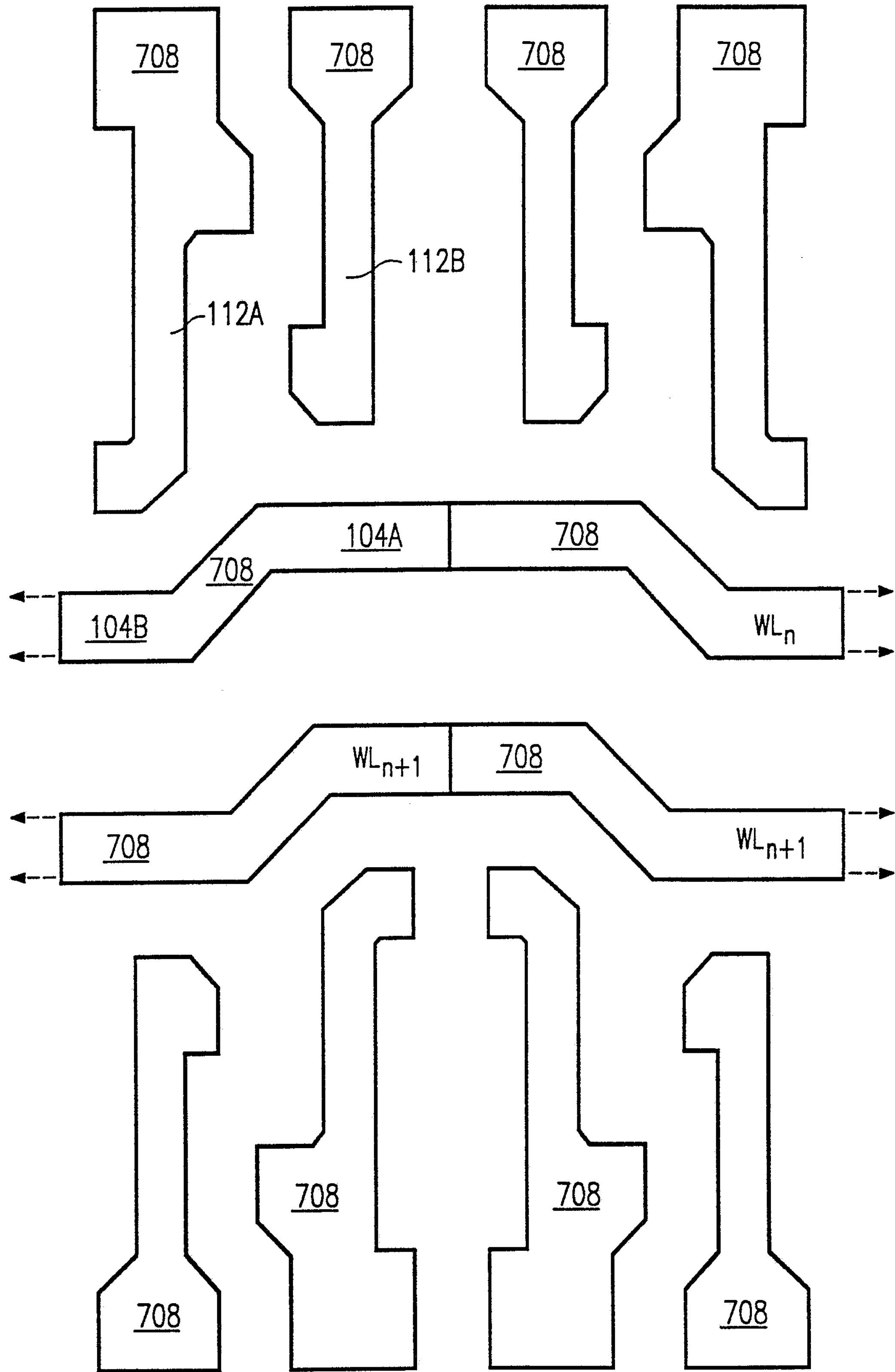
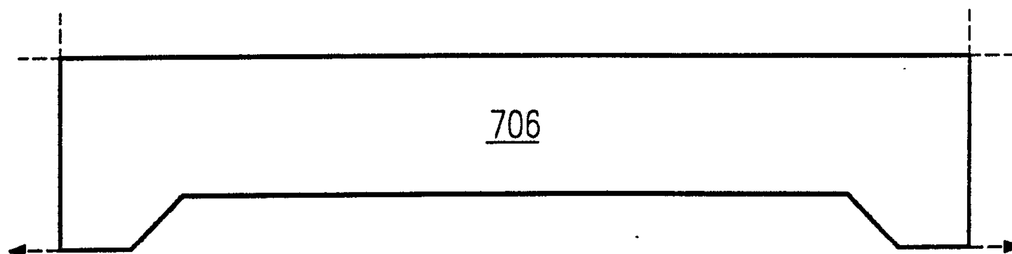


FIG. 7C POLY

SUBSTITUTE SHEET



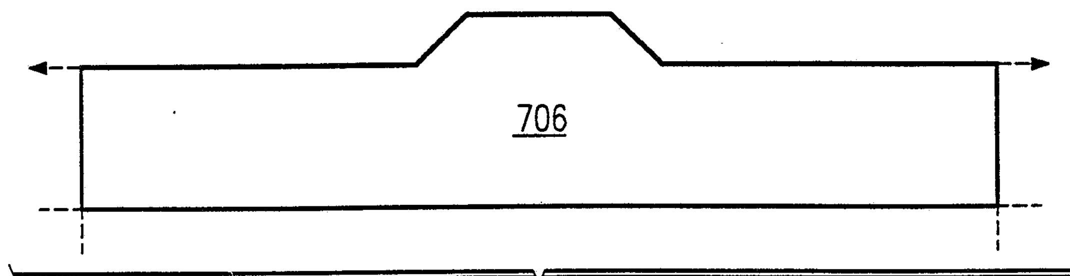
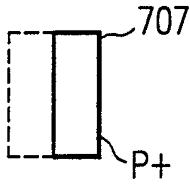
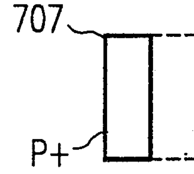


FIG. 7D OXIDE-R





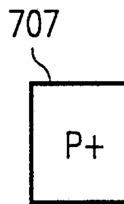


FIG. 7E *P+ AND $\overline{N+}$*

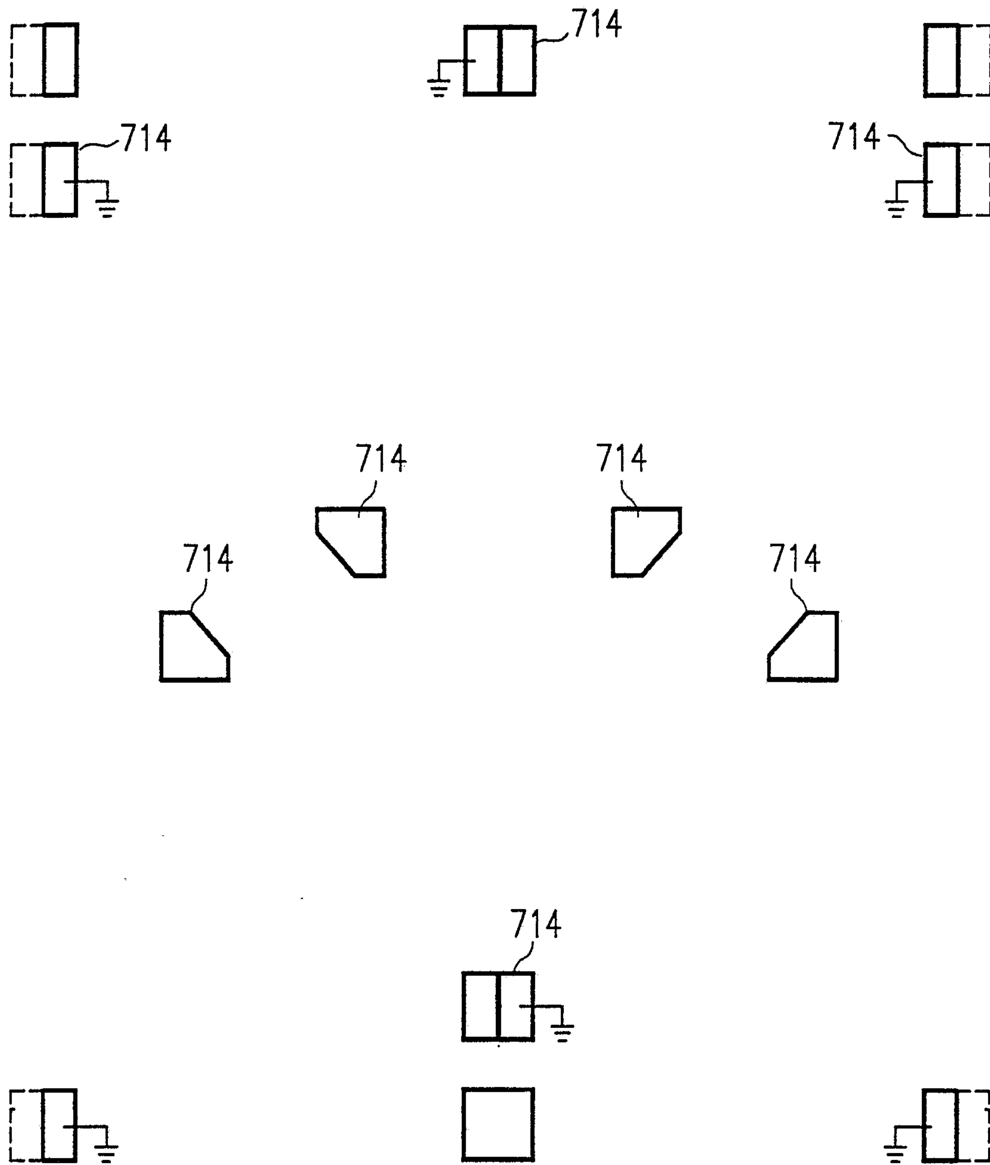


FIG. 7F CONTACTS

SUBSTITUTE SHEET

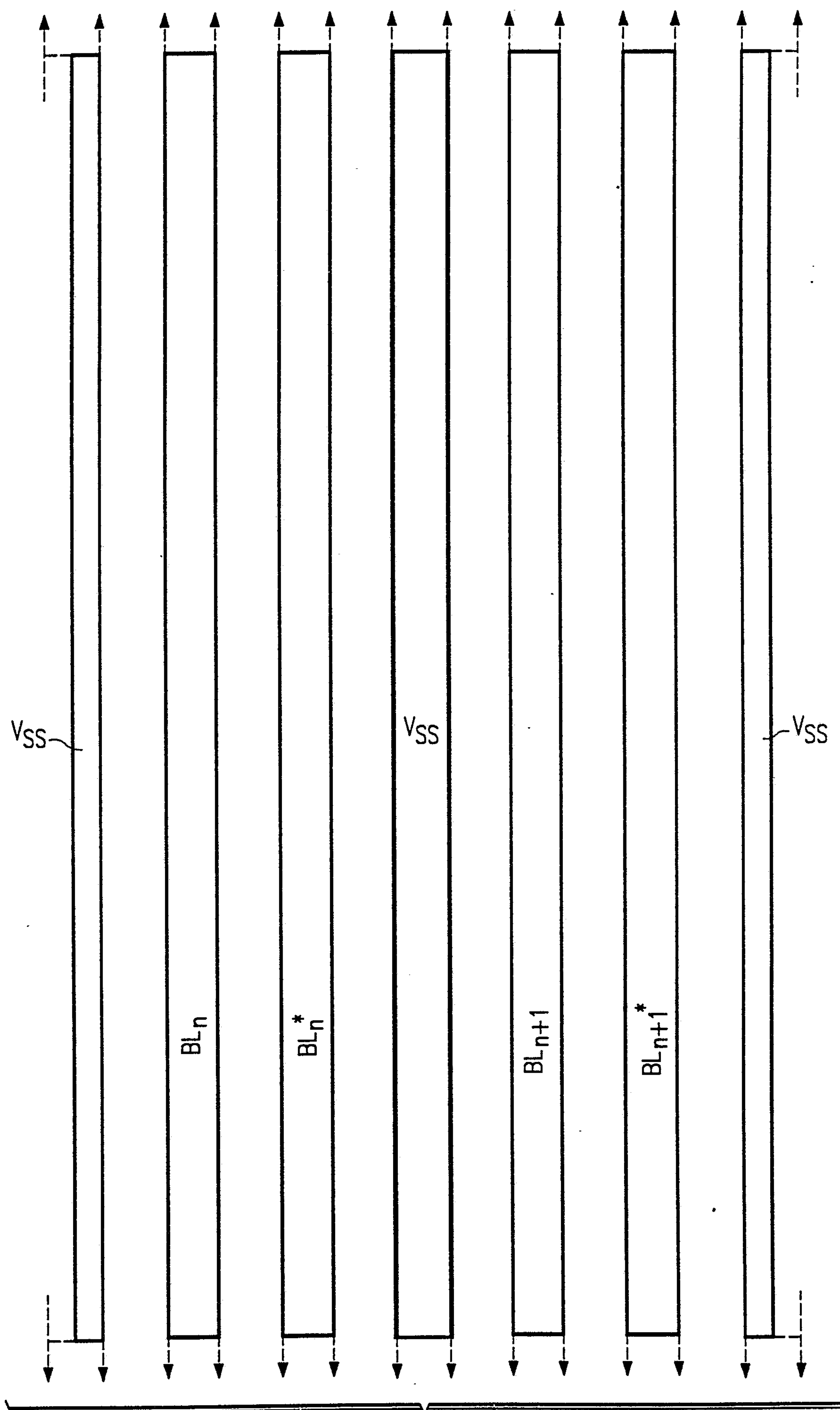
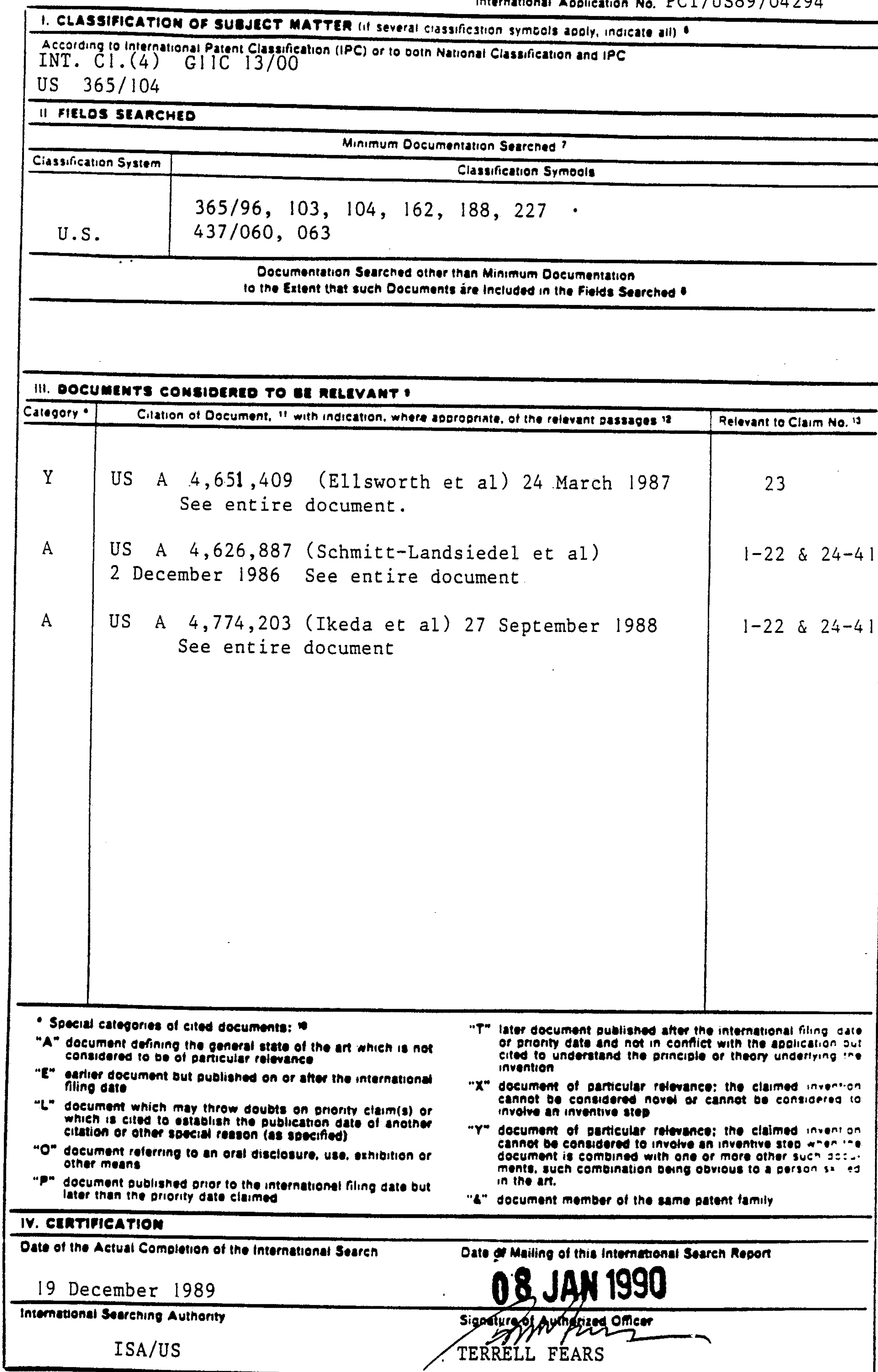


FIG. 7G METAL



INTERNATIONAL SEARCH REPORT

International Application No. PCT/US89/04294

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

INT. Cl.(4) G11C 13/00

US 365/104

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
U.S.	365/96, 103, 104, 162, 188, 227 · 437/060, 063

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	US A 4,651,409 (Ellsworth et al) 24 March 1987 See entire document.	23
A	US A 4,626,887 (Schmitt-Landsiedel et al) 2 December 1986 See entire document	1-22 & 24-41
A	US A 4,774,203 (Ikeda et al) 27 September 1988 See entire document	1-22 & 24-41

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
19 December 1989	08 JAN 1990
International Searching Authority	**Signature of Authorized Officer**
ISA/US	TERRELL FEARS

International Application No. PCT/US89/04294

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [1]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers . because they relate to subject matter [12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers . . . . because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

3. ☐ Claim numbers____________, because they are dependent claims not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☒ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [2]

This International Searching Authority found multiple inventions in this international application as follows:

I Claims 1-4 and 24-32, a memory device of class 364/189.01.
II Claims 5-22, an integrated circuit device of class 357/23.1.
III claims 23, a method of making an electronic device of Class 29/571.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.