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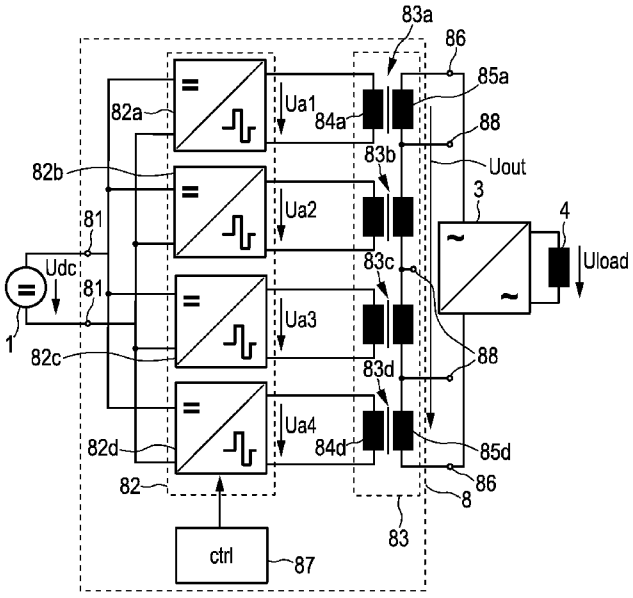

FIG. 8

(57) Abstract: The present invention relates to a multi-level inverter apparatus and a multi- level inversion method for converting a DC input voltage into an AC output voltage. The apparatus comprises one or more pairs of DC input terminals (61; 81; 61a', 61b') for receiving one or more DC input voltages (Udc; Udc1', Udc2'), a plurality of inverter circuits (67a-67d; 82a-82d; 11a-11d; 11a', 11b'), coupled to one of said DC input terminals, each receiving a DC input voltage (Udc; Udc1', Udc2') or a supply voltage (Udc1-Udc4) derived therefrom and generating an AC intermediate voltage (Ua1-Ua4), connection means (83) coupled to said plurality of inverter circuits (67a-67d; 82a-82d) for connecting the AC intermediate voltages in series, a pair of AC output terminals (68; 86) coupled to the end terminals of the series connection of AC intermediate voltages (Ua1-Ua4), and a control means (69; 87; 10, 20) for controlling said inverter circuits (67a-67d; 82a-82d; 11a-11d; 11a', 1b') to convert the one or more DC input voltages (Udc; Udc1', Udc2') into predetermined AC intermediate voltages (Ua1-Ua4).

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Multi-level inverter apparatus and inversion method

FIELD OF THE INVENTION

The present invention relates to a multi-level inverter apparatus and a corresponding method for converting a DC input voltage into an AC output voltage.

The present invention relates further to a power supply circuit for supplying an AC load voltage to a load, in particular to a Magnetic Particle Imaging (MPI) device for influencing and/or detecting magnetic particles in a field of view, wherein the field of view comprises an object of interest containing magnetic particles.

BACKGROUND OF THE INVENTION

Magnetic Particle Imaging (MPI) is an emerging medical imaging modality. The first versions of MPI were two-dimensional in that they produced two-dimensional images. Future versions will be three-dimensional (3D). A time-dependent, or 4D, image of a non-static object can be created by combining a temporal sequence of 3D images to a movie, provided the object does not significantly change during the data acquisition for a single 3D image.

MPI is a reconstructive imaging method, like Computed Tomography (CT) or Magnetic Resonance Imaging (MRI). Accordingly, an MP image of an object's volume of interest is generated in two steps. The first step, referred to as data acquisition, is performed using an MPI scanner. The MPI scanner has means to generate a static magnetic gradient field, called "selection field", which has a single field free point (FFP) at the isocenter of the scanner. In addition, the scanner has means to generate a time-dependent, spatially nearly homogeneous magnetic field. Actually, this field is obtained by superposing a rapidly changing field with small amplitude, called "drive field", and a slowly varying field with large amplitude, called "focus field". By adding the time-dependent drive and focus fields to the static selection field, the FFP may be moved along a predetermined FFP trajectory throughout a volume of scanning surrounding the isocenter. The scanner also has an arrangement of one or more, e.g. three, receive coils and can record any voltages induced in these coils. For the data acquisition, the object to be imaged is placed in the scanner such that

the object's volume of interest is enclosed by the scanner's field of view, which is a subset of the volume of scanning.

The object must contain magnetic nanoparticles; if the object is an animal or a human, a contrast agent containing such particles is administered to the animal or human prior to the scan. During the data acquisition, the MPI scanner steers the FFP along a deliberately chosen trajectory that traces out the volume of scanning, or at least the field of view. The magnetic nanoparticles within the object experience a changing magnetic field and respond by changing their magnetization. Only those, which are in the field free point, exhibit a change. All other particles do not respond, because of being saturated by the selection field. The changing magnetization of the nanoparticles induces a time dependent voltage in each of the receive coils. This voltage is sampled in a receiver associated with the receive coil. The samples output by the receivers are recorded and constitute the acquired data. The parameters that control the details of the data acquisition make up the scan protocol.

In the second step of the image generation, referred to as image reconstruction, the image is computed, or reconstructed, from the data acquired in the first step. The image is a discrete 3D array of data that represents a sampled approximation to the position-dependent concentration of the magnetic nanoparticles in the field of view. The reconstruction is generally performed by a computer, which executes a suitable computer program. Computer and computer program realize a reconstruction algorithm. The reconstruction algorithm is based on a mathematical model of the data acquisition. As with all reconstructive imaging methods, this model is an integral operator that acts on the acquired data; the reconstruction algorithm tries to undo, to the extent possible, the action of the model.

Such an MPI apparatus and method have the advantage that they can be used to examine arbitrary examination objects – e. g. human bodies – in a non-destructive manner and without causing any damage and with a high spatial resolution, both close to the surface and deep in the body of the examination object. Such an arrangement and method are generally known and are first described in DE 101 51 778 A1 and in Gleich, B. and Weizenecker, J. (2005), "Tomographic imaging using the nonlinear response of magnetic particles" in nature, vol. 435, pp. 1214-1217. The arrangement and method for magnetic particle imaging (MPI) described in that publication take advantage of the non-linear magnetization curve of small magnetic particles.

For medical equipment signal generators are required, which have at the same time very high requirements of reactive power and signal to noise ratio. In particular

applications like the above described MPI application, levels of reactive power in the range of some MVA are needed, while the signal to noise ratio has to achieve extreme quality levels in respect to the suppression of the harmonics of the fundamental signal. At the same time also the in-band inter-modulation products from non-linear distortion have to be kept very low. The combination of high reactive power with low distortion is not feasible with current linear or switched mode power amplifier technology. Linear amplifier technology suffers from severe losses (minimum $4/\pi$ times the required reactive power). Switched mode converters suffer from switching noise and non-linear distortion, which makes the achievement of the required signal quality impossible.

For MPI, a high quality sinusoidal input current is required to supply the drive field coil inside a scanner for MPI. Since the spatial resolution depends on the quality of the drive field coil current, a high quality signal is required. The drive field coil can be treated electrically as an inductance with low parasitic resistance. The coil will cause very high reactive power, when supplied with a desired AC-current. The reactive power flow can be reduced by means of paralleling capacitances either in a tapped or non-tapped outline to the coil. Additionally, a filter can be placed between the supply unit and the drive field coil.

Conventionally, the supply unit is realized by means of analogue amplifiers. Due to the high demand of reactive power, an analogue amplifier solution is not a favorable solution. The losses of this solution equals at least the amount of apparent power times $4/\pi$. On a clinical scale, the power requirements are huge and lead to enormous energy consumption and cost.

The selection of a switched amplifier will provide a higher efficiency and will be able to cope with the high reactive power demand. However, known switched amplifiers would cause higher harmonic contents at the inverter output, when operating with a Pulse Width Modulation (PWM) control. It would require a very high switching frequency and an enormous resolution in time to fulfill the typical precision requirements of the application. Standard multi-level converters (sometimes also called multistep converters) tend to become extremely complex if a sufficient fine stepping of voltage levels has to be achieved. Furthermore, nonlinear signal distortion is prevalent in switched amplifiers because of imperfections of the implemented semiconductor switches that have current dependent voltage drop and even more relevant current dependent delay effects. This can be mitigated by either increasing the number of stages and so levels in multi-level converter to very high numbers, or use a switching frequency at the PWM converters that is substantially higher

than the frequency range, which is relevant for the application. The second is known from PWM audio amplifiers for high-fidelity applications.

Both methods are not possible for the desired use in medical applications, because the frequency band of interest covers already a range from some 10 kHz to more than 1 MHz. A switching frequency substantially higher than 1 MHz is not feasible in high power applications.

US 5,757,633 discloses a multi-level inverter using multiple inverter H-bridges connected in series to piecewise approximate a sine wave. The inverter H-bridges are bypassed or switched into service as required for sine wave synthesis. After a step is switched in, it creates its portion of the sine wave. Each step is further smoothed using pulse width modulation which leads to a smoother sine wave with the consequent advantages of lower distortion, smaller and lighter filtering circuits, and lower conversion losses during transistor switching.

One particular problem of all previous solutions is that they require a rather high power of the active filter, if the signal quality in the baseband is included and not only higher frequency harmonics. Another problem is that the stability of the active filter control loop strongly depends on the impedance behavior both of the primary amplifier and the load. A third problem is that a feed-forward scheme for compensation of unwanted signal components require an enormous precision of the compensation signal if a relevant suppression of the noise shall be achieved.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a multi-level inverter apparatus and a corresponding method for converting a DC input voltage into an AC output voltage, which solves both the high power requirements of linear amplifiers and the harmonics problem of conventional switched amplifiers. Further, a desired high quality output voltage shall be achievable, compared to a PWM-controlled standard audio amplifier, and a fine stepping of the output voltage levels shall be possible.

It is a further object of the present invention to provide a power supply circuit for supplying an AC load voltage to a load, in particular by which the high power demanding field coils for MPI applications can be driven.

It is a still further object of the present invention to provide an MPI device for influencing and/or detecting magnetic particles in a field of view using an appropriate power supply.

In a first aspect of the present invention a multi-level inverter apparatus is presented that comprises

- one or more pairs of DC input terminals for receiving one or more DC input voltages,
- a plurality of inverter circuits, coupled to one of said DC input terminals, each receiving a DC input voltage or a supply voltage derived therefrom and generating an AC intermediate voltage,
- connection means coupled to said plurality of inverter circuits for connecting the AC intermediate voltages in series,
- a pair of AC output terminals coupled to the end terminals of the series connection of AC intermediate voltages,
- a control means for controlling said inverter circuits to convert the one or more DC input voltages into predetermined AC intermediate voltages.

In a further aspect of the present invention a corresponding multi-level inversion method is presented comprising the steps of:

- receiving one or more DC input voltages or a supply voltage derived therefrom,
- converting the one or more DC input voltages or said supply voltage into a plurality of AC intermediate voltages,
- generating an AC output voltage from said AC intermediate voltages by a series coupling of said AC intermediate voltages,
- controlling the conversion of the one or more DC input voltage or said supply voltage into predetermined AC intermediate voltages.

The invention is based on the idea to use a stacked configuration of several digital amplifiers, which produce voltage levels in the manner of a numbering system, for instance based on the radix 5, and to achieve an optimal trade-off between quantization and required maximum switching frequency. In particular, a large number of different voltage levels with a rather limited number of individual inverters are obtained by an optimized scaling of the voltage levels of the individual stages. This results into easy to fulfill requirements of precision and power dimensioning of the individual stages, within the technical constraints of the components, e.g. with regard to the required switching frequency.

The invention thus provides a solution both for the high power requirements of linear amplifiers and the harmonics problem of conventional switched amplifier solutions. The switched amplifier and control method according to the present invention enable the

supply of high power demanding field coils for magnetic particle imaging applications, and also a fine stepping of the output voltage levels is achieved leading to low signal distortion and noise, with a relatively simple configuration.

Another advantage is that the system control is not obliged anymore to take care of a proper balancing of the loading of the different inverter stages. As these are coupled over a common DC supply, they will all have the same voltage, and differences in the individual load are balanced automatically.

According to a preferred embodiment at least two, in particular all, inverter circuits are adapted for converting the one or more DC input voltages into AC intermediate voltages having different voltage levels.

According to a preferred embodiment of the multi-level inverter apparatus said pair of output terminals is coupled to the end terminals of said aid series connection of AC intermediate voltages. Further, according to another embodiment one or more additional AC output terminals coupled to interconnections between said series connection of AC intermediate voltages, i.e. not only the total voltage from the end terminals of said series connection of AC intermediate voltages.

According to the present invention at least two of said AC intermediate voltages produce different sets of voltage levels, wherein the different sets of voltage level preferably follow a rule of $1:n:n^2:n^3$ etc.. Further, the different AC intermediate voltages are obtained by different DC supply voltages of the inverters.

There exist various embodiments of the connection means. In a first, very effective embodiment the connection means comprises a transformer circuit having a plurality of transformers, each comprising a primary winding coupled to the output of an associated inverter circuit for receiving an AC intermediate voltage, and a secondary winding, wherein said secondary windings are coupled in series and wherein said transformer circuit generates an AC output voltage from said AC intermediate voltages.

In this embodiment it is preferred that at least two, in particular all, transformers have a different turn ratio. The output voltages of the various transformers, in particular at the various secondary windings of the transformers, are thus different. This enables to selectively "compose" the desired voltage level of the AC output voltage, in particular by appropriate control of the individual inverter circuits (in the apparatus according to the first aspect) or of the individual secondary inverter circuits (in the apparatus according to the second aspect), e.g. by switching the switching elements comprised in the individual (secondary) inverter circuits on or off as desired.

The transformer having the highest turn ratio provides the smallest voltage level and, thus, is used for enabling the smallest changes in the AC output voltage. When decomposing the output voltage into the components with different step size, the smallest changes in the AC output voltage, which is preferably a sinusoidal function, show the highest frequency, caused by a plurality of small voltage portions during short switching intervals of the respective inverter).

In another, quite simple embodiment the connection means comprises a series connection of said inverter circuits, and the DC supply voltages or DC input voltages of the individual inverter circuits are galvanically isolated. This generally requires less hardware.

Particularly with the latter embodiment of the connection means, the multi-level inverter apparatus further comprises

- a primary inverter circuit coupled to said DC input terminals for converting said DC voltage into an AC primary transformer input voltage,
- a primary transformer circuit having a plurality of primary transformers each comprising a primary winding and a secondary winding, wherein said primary windings are connected in parallel to the output of said primary inverter circuit for providing said AC primary transformer input voltage to said parallel connection, said transformer circuit generating AC primary transformer output voltages from said AC primary transformer input voltage,
- a plurality of rectifier circuits coupled to said secondary windings for converting said AC primary transformer output voltages into said DC supply voltages.

Similarly as mentioned above for the transformers, in this embodiment the at least two, in particular all, primary transformers preferably have a different turn ratio leading to the same advantages as mentioned above for the transformers. .

In the multi-level inverter apparatus using the above mentioned embodiments of the connection means the corresponding inverter has the lowest current in switching elements of the respective control means. This is advantageous for the operation of these inverters, which can be operated at a higher frequency with reduced current or voltage, which in turn reduces the losses in the switching elements of the control means.

Another degree of freedom can be achieved in a further embodiment of the multi-level inverter apparatus according to which at least two, in particular all, rectifier circuits are adapted for converting said AC transformer output voltages into DC intermediate voltages having different voltage levels.

Each inverter preferably comprises two pairs of switching elements forming a H-bridge. The switching elements of a first pair are connected in series, forming three independent terminals. A first terminal is connected to the positive input voltage terminal of the respective inverter, a second terminal is connected to the negative input voltage terminal of the inverter, and the third terminal is forming an alternating output voltage terminal. The second pair is connected the same way, thereby forming a second output voltage terminal of the inverter. Each switching element can preferably be switched on and off individually such that two serially coupled switching elements are never in a switched on state at the same and that the voltage difference at the output voltage terminals of the inverter is zero, equal to the input voltage of the inverter, or equal to the input voltage multiplied by minus 1.

A balance of the losses in the switches of the inverter circuits, particularly if the power supply is to deliver output voltages with small amplitude or with zero output voltage level, can be achieved according to a further embodiment according to which said control means is adapted for controlling said inverter circuits such that an equal current distribution is obtained in the switching elements over a predetermined time period by changing the switching configuration depending on whether a reference signal changes sign.

This embodiment is preferably further developed such that said control means is adapted for changing the freewheeling path of an inverter circuit synchronized with a zero crossing of the output current of said inverter circuit or synchronized to a predetermined, in particular first, switching state of the sign of the output current of said inverter circuit.

Hence, according to these embodiments the switching configuration is changed depending on whether a reference signal changes sign. The reference signal is preferably an input signal to the modulator. The modulator maps the desired output voltage to the appropriate switching configuration of the inverter circuits. This embodiment thus ensures that the change of a switching configuration no longer depends on the previous state of the switching configuration. This way the stress on the switches may be balanced even if output voltages with small amplitudes are required.

According to these embodiments the switching frequency is several times higher than the fundamental operating frequency, and the conduction loss distribution is averaged over half cycles or cycles, in particular one or two cycles, of the fundamental operating frequency.

The multi-level inverter apparatus is preferably applied in a power supply circuit. Hence, in an aspect of the present invention a power supply circuit for supplying a load with an AC voltage signal is presented, comprising:

- a multi-level inverter apparatus according to the present invention for converting a DC input voltage provided by a DC voltage source into an AC output voltage, and
- a filter circuit coupled to the output of said multi-level inverter apparatus for filtering said AC output voltage signal into said AC voltage signal.

To further improve the required signal quality, it is proposed according to an embodiment that said (active or passive) filter circuit comprises a control loop including:

- a loop control circuit for receiving the difference between said AC voltage signal and a reference signal and for generating a loop control signal and
- a loop amplifier circuit for generating a correction signal based on said loop control signal for correcting said AC voltage signal.

With this embodiment all above explained problems are solved at a comparatively low design power and a stable control loop of the (active) filter, while minimizing the in-band distortion and also the harmonics of the amplifier system. In addition, precision of the system has to fulfill only normal requirements.

The multi-level inverter apparatus and the inversion method as well as the power supply circuit can be used in various applications. A preferred use is in the field of medical application in devices for medical imaging, such as Magnetic Resonance Imaging (MRI) devices or, preferably, Magnetic Particle Imaging (MPI) devices as described above.

Hence, in an aspect of the present invention an imaging device is provided for imaging an object, in particular a patient, comprising imaging means and one or more power supply circuits as described above for supplying power to said imaging means. Preferably, said imaging means comprises an X-ray unit or a magnetic resonance unit, wherein said power supply unit is, for instance, adapted to supply power to the cathode of an X-ray generator, to provide the voltage between the cathode and the anode, or to provide the supply power to the control grid of a grid-controlled X-ray generator. In an MRI device the multi-level inverter apparatus may, for instance, be used in the power supply units for supplying power or control voltages to the gradient coils.

In another aspect of the present invention an MPI device is presented comprising:

- selection means comprising a selection field signal generator unit and selection field elements for generating a magnetic selection field having a pattern in space of its magnetic field strength such that a first sub-zone having a low magnetic field strength where the magnetization of the magnetic particles is not saturated and a second sub-zone

having a higher magnetic field strength where the magnetization of the magnetic particles is saturated are formed in the field of view,

- drive means comprising drive field signal generator units and drive field coils for changing the position in space of the two sub-zones in the field of view by means of a magnetic drive field so that the magnetization of the magnetic material changes locally, wherein said drive field signal generator units comprises one or more power supply circuit according to the present invention.

Dependent on the kind of application of said MPI device, e.g. whether it is desired to be used for imaging (a small or large area), heating a certain area in the object and/or moving an object, it might comprise further means, such as focus coils, receive coils, image processing means, control means etc., which are generally all known in the art of MPI devices.

In a particular exemplary embodiment the multi-level inverter apparatus comprises

- a pair of DC input terminals for receiving a DC input voltage,
- a plurality of inverter circuits coupled in parallel to said DC input terminals for converting the DC input voltage into a plurality of AC intermediate voltages,
- a transformer circuit having a plurality of transformers each comprising a primary winding, to which an AC intermediate voltage is applied, and a secondary winding, wherein said secondary windings are coupled in series and wherein said transformer circuit generates an AC output voltage from said AC intermediate voltages,
- a pair of AC output terminals coupled to said transformer circuit for providing said AC output voltage, and
- a control means for controlling said inverter circuits to convert the DC input voltage into predetermined AC intermediate voltages.

In another particular exemplary embodiment the multi-level inverter apparatus comprises

- a pair of DC input terminals for receiving a DC input voltage,
- a primary inverter circuit coupled to said DC input terminals for converting the DC input voltage into an AC transformer input voltage,
- a transformer circuit having a plurality of transformers each comprising a primary winding and a secondary winding, wherein said primary windings are connected in parallel, which parallel connection being coupled to the output of said primary inverter circuit for providing said AC transformer input voltage to said parallel connection, said transformer

circuit generating AC transformer output voltages from said AC transformer input voltage,

- a plurality of rectifier circuits coupled to said secondary windings for converting said AC transformer output voltages into DC intermediate voltages,
- a plurality of secondary inverter circuits coupled to the output of said rectifier circuits for converting said DC intermediate voltages into a plurality of AC intermediate voltages,
- a pair of AC output terminals coupled to said secondary inverter circuits for providing said AC output voltage from said AC intermediate voltages,

wherein at least two, in particular all, secondary inverter circuits are adapted for converting the DC input voltage into AC intermediate voltages having different voltage levels.

It shall be understood that the claimed methods, the claimed power supply circuit and the claimed MPI device have similar and/or identical preferred embodiments as the claimed devices and as defined in the dependent claims.

BRIEF DESCRIPTION OF THE DRAWING

These and other aspects of the invention will be apparent from and elucidated with reference to the embodiment(s) described hereinafter. In the following drawings

Fig. 1 shows a block diagram of the general layout of a system, in which the present invention can be used,

Fig. 2 shows a diagram illustrating a PWM modulated output voltage,

Fig. 3 shows a diagram illustrating a piecewise approximated inverter output voltage,

Fig. 4 shows a block diagram of a first embodiment of a multi-level inverter apparatus according to the present invention,

Fig. 5 shows a diagram illustrating the number of addressable output voltages vs. the number of inverter stages using identical inverter supply voltages,

Fig. 6 shows a diagram illustrating the number of addressable output voltages vs. the number of inverter stages using inverter supply voltages that are halved at each additional inverter,

Fig. 7 shows a diagram illustrating the number of addressable output voltages vs. the number of inverter stages having two pairs of inverters with a stepping of 1:5 between the pairs,

Fig. 8 shows a block diagram of a second embodiment of a multi-level inverter apparatus according to the present invention,

Fig. 9 shows a block diagram of an embodiment of a power supply circuit according to the present invention,

Fig. 10 shows a block diagram of the power supply circuit shown in Fig. 9 in more detail,

Fig. 11 shows a first embodiment of an MPI device in which the power supply circuit according to the present invention can be used,

Fig. 12 shows an example of the selection field pattern produced by a device as shown in Fig. 11,

Fig. 13 shows a block diagram of an MPI device according to the present invention,

Fig. 14 shows a block diagram of a control unit according to a further embodiment of the present invention,

Fig. 15 shows diagrams illustrating a first embodiment of the control method applied by the control unit shown in Fig. 14,

Fig. 16 shows diagrams illustrating a second embodiment of the control method applied by the control unit shown in Fig. 14, and

Fig. 17 shows a block diagram of a third embodiment of a multi-level inverter apparatus according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

Fig. 1 shows a block diagram of the general layout of a system in which the present invention can be used. A DC power source 1 with an output voltage Udc is used to supply the amplifier 2. The amplifier 2 can either be of linear mode of operation or digital switching. The output Ua of the amplifier 2 is connected to a filter 3 which interfaces the output of the amplifier 2 to a load 4, e.g. a field coil of a MPI device, as AC load voltage Uload. The amplifier 2 and the filter 3 thus form a power supply circuit 5 for supplying the load with the AC load voltage Uload. A digital operating amplifier offers the option of reduced losses, especially with respect to the high amount of reactive power flow.

The output amplitude of the switched amplifier 2 can be set by means of a pulse width modulation. Fig. 2 shows an example for a sinusoidally modulated output voltage. Therein, Um denotes the modulated output voltage and Us denotes the fundamental voltage component. As it can be seen from Fig. 2 the difference between both the traces

denotes the amount of filtering which is required. In applications which need a high quality output voltage and/or current a large filter is required. However, a highly effective filter set-up implies a large amount of reactive power at the inverter.

The first embodiment of the present invention described herein applies a piecewise approximated output voltage Ua. The piecewise steps are arranged in a way which provides the lowest possible harmonic content of the output voltage Ua. Thus, the amount of filtering can be reduced. In Fig. 3 an example of the piecewise approximated inverter output voltage Ua described above is shown. Higher numbers of different output voltage steps will lower the output voltage harmonic content.

The mentioned discrete output voltage steps can be realized by means of series connected H-bridge inverters as used in a first embodiment of a multi-level inverter apparatus 6 according to the present invention as shown in Fig. 4.

The multi-level inverter apparatus 6 shown in Fig. 4 comprises a pair of DC input terminals 61 for receiving a DC input voltage Udc from the DC voltage source 1. A primary inverter circuit 62 is coupled to said DC input terminals 61 for converting the DC input voltage Udc into an AC transformer input voltage Ut1, which is provided to a transformer circuit 63 having a plurality of transformers 63a-63d (here four transformers) comprising a plurality of primary windings (e.g. primary winding 64a for transformer 63a) connected in parallel, which parallel connection being coupled to the output of said primary inverter circuit 62 for providing said AC transformer input voltage Ut1 to said parallel connection. Said transformer circuit 63a further comprises a plurality of secondary windings (e.g. secondary winding 65a for transformer 63a). The transformers 63a-63d thus generate a plurality of AC transformer output voltages Ut2a-Ut2d from said AC transformer input voltage Ut1.

The multi-level inverter apparatus 6 further comprises a plurality 66 of rectifier circuits 66a-66d coupled to said secondary windings of the transformers 63a-63d for converting said AC transformer output voltages Ut2a-Ut2d into DC intermediate voltages Udc1-Udc4. Coupled to the output of said rectifier circuits 66a-66d is a plurality 67 of secondary inverter circuits 67a-67d for converting said DC intermediate voltages Udc1-Udc4 into a plurality of AC intermediate voltages Ua1-Ua4. In this embodiment the secondary inverter circuits 67a-67d are coupled in series.

A pair of AC output terminals 68 is coupled to said secondary inverter circuits, in this embodiment the first output terminal of the first secondary inverter circuit 67a and the last output terminal of the last secondary inverter circuit 67d, so that a maximum AC output

voltage Uout is provided as the sum of the AC intermediate voltagesUa1-Ua4 at said AC output terminals 68.

Finally, a control means 69 is coupled to the plurality 67 of secondary inverter circuits 67a-67d, in particular comprising a control line to each secondary inverter circuits 67a-67d, for controlling said secondary inverter circuits 67a-67d to convert the DC input voltagesUdc1-Udc4 into predetermined AC intermediate (galvanically insulated) voltages Ua1-Ua4, wherein at least two, in particular all, secondary inverter circuits 67a-67d are adapted for converting the respective DC input voltage Udc1-Udc4 into AC intermediate voltages Ua1-Ua4 having different voltage levels.

The AC output voltage Uout is provided to a (passive or active) filter circuit 3, at the output of which the load 4 is coupled, which is provided with the load voltage Uload.

The multi-level inverter circuit can be used to provide several levels of output voltages. The number of secondary inverter circuits 67 denotes the number of output voltage levels, which can be addressed. The output voltages addressable are depicted in the diagram shown in Fig. 5, which particularly shows the number Nv of addressable output voltages versus the number Ni of secondary inverter circuits. For this case identical DC input voltage Udc1-Udc4 at each secondary inverter circuit 67a-67d has been assumed, i.e. Udc1 = Udc2 = Udc3 = Udc4. As it can be seen from Fig. 5 the diagram the number Nv of addressable output voltage levels is twice the number Ni of secondary inverter circuits plus the voltage level zero, i.e. $Nv = 2 * Ni + 1$.

With respect to the embodiment of the multi-level inverter apparatus as shown in Fig. 4, it is proposed that the contributions of the secondary inverter circuits 67a-67d are non-equal, i.e. that the AC intermediate voltages Ua1-Ua4 are non-equal. This can be achieved by having different secondary inverter circuits 67a-67d and/or by providing different DC input voltages Udc1-Udc4 to the (equal or non-equal secondary inverter circuits 67a-67d), the latter being achievable by using transformers 63a-63c having primary and/or secondary windings 64a-64d or 65a-65d having different numbers of windings.

In this way a higher number of different output voltage levels can be achieved in form of a numbering system with a given radix. Assuming binary distributed inverter voltages (i.e. DC input voltages Udc1-Udc4 being reduced by half for each additional inverter), a wider range of output voltage levels of the total output voltage Uout can be addressed. The possible addressable voltage levels versus the number Ni of secondary inverter circuits are depicted in Fig. 6.

As can be seen using binary distributed binary inverter supply voltages two times 15 discrete output voltages can be addressed plus voltage level zero when exemplarily four secondary inverter circuits are implemented as shown in Fig. 4. However, when providing a sinusoidal output voltage (summarized voltage) each of the secondary inverter circuits 67a-67d will operate at different switching frequencies. Typically, the switching frequency doubles along the tree at each stage, i.e. the fourth inverter has a switching frequency of 2^4=16 times that of the first. It is also visible, that there are overlapping states, resulting from the fact that the stepping of the converters is binary, while the output levels are are actually ternary, i.e. plus, minus, and zero.

Another embodiment of the present invention has a semi-linear distribution for the DC input voltages Udc1-Udc4. When choosing DC input voltage levels with exemplarily a rating of 5:2 an optimum of output levels and switching frequency range can be achieved.

A further embodiment of the present invention described herein has pairs of inverters exemplarily having identical level of DC input voltages Udc1-Udc4 and a stepping of the DC input voltage between the pairs by 5:1For such an embodiment the number Nv of addressable output voltages versus the number Ni of secondary inverter circuits is depicted in Fig. 7. Each pair effectively forms a five-level inverter as could be read from the diagram shown in Fig. 5. The stepping of 5:1 between the two pairs avoids the overlapping of states in the finest quantization level and thus achieves almost the same number of levels as in Fig. 6. Yet, switching frequency of the high resolution steps is only 5 times higher than the fundamental.

A further embodiment of the invention described herein provides the operation of inverter circuits from one identical intermediate DC input voltage. A block diagram of a multi-level inverter apparatus 8 according to such an embodiment is shown in Fig. 8. The apparatus 8 shown in Fig. 8 comprises a pair of DC input terminals 81 for receiving a DC input voltage Udc provided by the DC voltage supply 1. A plurality 82 of inverter circuits 82a-82d is coupled in parallel to said DC input terminals 81 for converting the DC input voltage Udc into a plurality of AC intermediate voltages Ua1-Ua4. A transformer circuit 83 having a plurality of transformers 83a-83d comprising a plurality of primary windings 84a-84d, to which said AC intermediate voltages Ua1-Ua4 are applied, and a plurality of secondary windings 85a-85d coupled in series. The transformer circuit 83 thus generates the AC output voltage Uout from said AC intermediate voltages Ua1-Ua4, provided at a pair of AC output terminals 86 coupled to said transformer circuit 83, in particular the first contact of the first secondary winding 85a and the last contact of the last secondary winding 85d. A

control unit 87 is finally provided for controlling said inverter circuits 82a-82d to convert the DC input voltage Udc into predetermined AC intermediate voltages Ua1-Ua4.

According to the embodiment depicted in Fig. 4 isolated DC voltages Udc1-Udc4 are provided for each secondary inverter circuit 67a-67d. Thus, each branch needs an isolated DCDC converter, which is implemented by the primary inverter and the arrangement of primary transformers. In contrast, the embodiment described in Fig. 8 uses a common DC rail for all the inverter circuits 67a-67d. The isolation is realized with the four transformers 83a-83d, which may have different turn ratios to address different output voltage steps. Thus, the non-identical voltage steps can be realized. The advantage here is that the system control is not obliged anymore taking care for a proper balancing of the loading of the different inverter stages. As these are coupled over a common DC supply, they will all have the same voltage, and differences in the individual load are balanced automatically.

In both embodiments shown in Fig. 4 and Fig. 8 one or more additional AC output terminals 88, as shown in Fig. 8, coupled to interconnections between said series connection of AC intermediate voltages are provided. This enables, if needed, a further refinement of the output voltage Uout, if the output voltage is taken from one or more of the end terminals 86 or additional output terminals 88. Preferably, another control means is provided for controlling from which terminals the output voltage Uout is taken.

Fig. 9 shows a block diagram of an embodiment of a power supply circuit according to the present invention. It comprises a multi-level inverter apparatus 9 according to the present invention, e.g. as shown in Fig. 4 or 8, and an active filter circuit 3 coupled in series to the multi-level inverter apparatus 9. Further, a modulator 10 is coupled to the input of the multi-level inverter apparatus 9. A control loop is provided that receives the difference between the final output voltage Utot and the desired output voltage Uref and feeds the active filter 3, comprising a control element 31 and a linear amplifier 32, with a control signal, which leads to minimized difference between the two.

More details of the power supply circuit shown in Fig. 9 are depicted in Fig. 10. The multi-level inverter apparatus 9, which is similar to the multi-level inverter apparatus 8 shown in Fig. 8 comprises several inverter circuits 9a, 9b, 9c, 9d, each comprising, for example, a full bridge circuit (H-bride circuit) 11a, 11b, 11c, 11d with a transformer 12. In this embodiment a number of four inverter circuits 9a, 9b, 9c, 9d are shown, which are grouped in two pairs, i.e. the pair of inverter circuits 9a, 9b and the pair of inverter circuits 9c, 9d. In each pair the inverter circuits produce the same output voltage. The first pair 9a, 9b produces a voltage quantity “5”, which leads to five different output voltages for this pair,

namely -10,-5, 0, 5, and 10, depending on the switching state of the individual inverter circuits 9a, 9b. Similarly, in the second pair 9c, 9d the inverter circuits produce a voltage quantity of only "1", leading to output voltages of -2, -1, 0, 1, and 2.

This represent two digits of a numbering system of the radix 5 which means, that altogether 25 different voltage levels of the output voltage Uout can be generated from -12, -11, -10, ... -1, 0, 1, ..., 10, 11, 12. Thus, the amplifier 32 is able to generate a voltage which approximates the input in a range from -12.5 to + 12.5 with a quantization error of +/- 0.5, or +/- 4%. The modulator 10 maps the input voltage Uref to the appropriate switching states of the inverter apparatus 9, for example in the manner of a nearest sample method. The desired input voltage (reference voltage) Uref ist a predetermined (analog or digital) voltage prescribing the desired form of the effective output voltage Utot.

As shown, the inverter circuits preferably each comprise two pairs of switching elements 13, 14, 15, 16 forming a H-bridge. The switching elements 13, 14 and 15, 16 of each pair are coupled in series, and the pairs are coupled in parallel. The switching elements 13-16 can preferably be switched on and off individually such that two serially coupled switching elements 13, 14 and 15, 16 are never in a switched on state at the same time and that at the output of the inverter circuit 11 a voltage Ua1 is zero, equal to the input voltage of the inverter, or equal to the input voltage multiplied by minus 1.

The active filter 3 is shown in the lower part of Fig. 9. It is effectively connected in series with the multi-level inverter apparatus 9. As such multi-level inverters 10 are typically voltage sources, the output impedance of the multi-level inverter 9 has little or even no influence on the effect of the active filter 3. It is therefore relatively easy to design a stable control function G(s) with a high gain to eliminate any differences in the effective output signal Utot.

At the same time the maximum voltage that has to be produced by the active filter 3 is exactly the quantization error of +/-4%, in the given exemplary configuration. This is widely not affected by the waveform of the output current and corresponds also to the power dimensioning and the potential losses of the presumably linear amplifier 32 in the active filter 3. It is now much easier to design a linear amplifier 32 for only 4% of the power level rather than 100%.

The power dimensioning of the active filter 3 may be even further reduced by increasing the number of different levels of the multi-level inverter apparatus 9, either by adding further digit level (e.g. 0.2, which multiplies the number of levels by 5) or by

changing to a higher order numbering system, e.g. by adding one more full-bridge circuit per level and ending up with a radix of 7, producing 49 steps.

It is self-explaining that the number of various elements, in particular inverters, transformers, rectifiers, switching element, etc. in the various embodiments is not limited to the numbers of elements shown in the above described figures, can be deviate there from in both directions, i.e. can be lower or higher without departing from the present invention.

The present invention is usable to provide an output voltage with low harmonic content. It is particularly useful to supply a field coil in a magnetic particle imaging apparatus, e.g. for use as a drive coil amplifier in a magnetic particle imaging apparatus where extremely high quality power signals are required in combination with a high flexibility in respect to the waveform within a defined frequency window.

In the following the basics of MPI and an embodiment of such an MPI apparatus shall be briefly explained by reference to Figs. 11 to 13.

The embodiment 200 of the MPI scanner shown in Fig. 11 has three prominent pairs 212, 214, 216 of coaxial parallel circular coils, each pair being arranged as illustrated in Fig. 11. These coil pairs 212, 214, 216 serve to generate the drive and, optionally, the focus fields. The axes 218, 220, 222 of the three coil pairs 212, 214, 216 are mutually orthogonal and meet in a single point, designated the isocenter 224 of the MPI scanner 200.

The scanner 200 can be set to direct a predetermined, time dependent electric current through each of these coils 212, 214, 216, and in either direction (polarity). If the current flows clockwise around a coil when seen along this coil's axis, it will be taken as positive, otherwise as negative. To generate the static selection field, a constant positive current I^S is made to flow through the z^+-coil, and the current $-I^S$ is made to flow through the z^--coil. The z-coil pair 216 then acts as an anti-parallel circular coil pair.

The magnetic selection field which is generally a gradient magnetic field is represented in Fig. 12 by the field lines 250. It has a substantially constant gradient in the direction of the (e.g. horizontal) z-axis 222 of the z-coil pair 216 generating the selection field and reaches the value zero in the isocenter 224 on this axis 222. Starting from this field-free point (not individually shown in Fig. 12), the field strength of the magnetic selection field 250 increases in all three spatial directions as the distance increases from the field-free point. In a first sub-zone or region 252 which is denoted by a dashed line around the isocenter 224 the field strength is so small that the magnetization of particles present in that first sub-zone 252 is not saturated, whereas the magnetization of particles present in a second sub-

zone 254 (outside the region 252) is in a state of saturation. The field-free point or first sub-zone 252 of the scanner's field of view 228 is preferably a spatially coherent area; it may also be a punctiform area, a line or a flat area. In the second sub-zone 254 (i.e. in the residual part of the scanner's field of view 228 outside of the first sub-zone 252) the magnetic field strength of the selection field is sufficiently strong to keep the magnetic particles in a state of saturation.

By changing the position of the two sub-zones 252, 254 within the field of view 228, the (overall) magnetization in the field of view 228 changes. By measuring the magnetization in the field of view 228 or physical parameters influenced by the magnetization, information about the spatial distribution of the magnetic particles in the field of view 228 can be obtained. In order to change the relative spatial position of the two sub-zones 252, 254 in the field of view 228, further magnetic fields, i.e. the magnetic drive field, and, if applicable, the magnetic focus field, are superposed to the selection field 250 in the field of view 228 or at least in a part of the field of view 228.

To generate the drive field, a time dependent current I^D_1 is made to flow through both x-coils 212, a time dependent current I^D_2 through both y-coils 214, and a time dependent current I^D_3 through both z-coils 216. Thus, each of the three coil pairs acts as a parallel circular coil pair. Similarly, to generate the focus field, a time dependent current I^F_1 is made to flow through both x-coils 212, a current I^F_2 through both y-coils 14, and a current I^F_3 through both z-coils 216.

The embodiment 200 of the MPI scanner has at least one further pair, preferably three further pairs, of parallel circular coils, again oriented along the x-, y-, and z-axes. These coil pairs, which are not shown in Fig. 11, serve as receive coils. As with the coil pairs 212, 214, 216 for the drive and focus fields, the magnetic field generated by a constant current flowing through one of these receive coil pairs is spatially nearly homogeneous within the field of view and parallel to the axis of the respective coil pair. The receive coils are supposed to be well decoupled. The time dependent voltage induced in a receive coil is amplified and sampled by a receiver attached to this coil. More precisely, to cope with the enormous dynamic range of this signal, the receiver samples the difference between the received signal and a reference signal. The transfer function of the receiver is non-zero from DC up to the point where the expected signal level drops below the noise level.

The embodiment 200 of the MPI scanner shown in Fig. 11 has a cylindrical bore 226 along the z-axis 222, i.e. along the axis of the selection field. All coils are placed outside this bore 226. For the data acquisition, the patient (or object) to be imaged (or treated)

is placed in the bore 226 such that the patient's volume of interest – that volume of the patient (or object) that shall be imaged (or treated) – is enclosed by the scanner's field of view 228 – that volume of the scanner whose contents the scanner can image. The patient (or object) is, for instance, placed on a patient table. The field of view 228 is a geometrically simple, isocentric volume in the interior of the bore 226, such as a cube, a ball, or a cylinder. A cubical field of view 228 is illustrated in Fig. 11.

The patient's volume of interest is supposed to contain magnetic nanoparticles. Especially prior to a therapeutic and/or diagnostic treatment of, for example, a tumor, the magnetic particles are positioned in the volume of interest, e.g. by means of a liquid comprising the magnetic particles which is injected into the body of the patient (object) or otherwise administered, e.g. orally, to the patient.

An embodiment of magnetic particles comprises, for example, a spherical substrate, for example, of glass which is provided with a soft-magnetic layer which has a thickness of, for example, 5 nm and consists, for example, of an iron-nickel alloy (for example, Permalloy). This layer may be covered, for example, by means of a coating layer which protects the particle against chemically and/or physically aggressive environments, e.g. acids. The magnetic field strength of the magnetic selection field 250 required for the saturation of the magnetization of such particles is dependent on various parameters, e.g. the diameter of the particles, the used magnetic material for the magnetic layer and other parameters.

In the case of e.g. a diameter of 10 μm, a magnetic field of approximately 800 A/m (corresponding approximately to a flux density of 1 mT) is then required, whereas in the case of a diameter of 100 μm a magnetic field of 80 A/m suffices. Even smaller values are obtained when a coating of a material having a lower saturation magnetization is chosen or when the thickness of the layer is reduced. Magnetic particles that can generally be used are available on the market under the trade name Resovist.

For further details of the generally usable magnetic particles and particle compositions, the corresponding parts of EP 1304542, WO 2004/091386, WO 2004/091390, WO 2004/091394, WO 2004/091395, WO 2004/091396, WO 2004/091397, WO 2004/091398, WO 2004/091408 are herewith referred to, which are herein incorporated by reference. In these documents more details of the MPI apparatus and method in general can be found as well.

The data acquisition starts at time t_s and ends at time t_e. During the data acquisition, the x-, y-, and z-coil pairs 212, 214, 216 generate a position- and time dependent

magnetic field, the applied field. This is achieved by directing suitable currents through the coils. In effect, the drive and focus fields push the selection field around such that the FFP moves along a preselected FFP trajectory that traces out the volume of scanning – a superset of the field of view. The applied field orientates the magnetic nanoparticles in the patient. As the applied field changes, the resulting magnetization changes too, though it responds nonlinearly to the applied field. The sum of the changing applied field and the changing magnetization induces a time dependent voltage V_k across the terminals of receive coil pair along the x_k-axis. The associated receiver converts this voltage to a signal $S_k(t)$, which it samples and outputs.

It is advantageous to receive or to detect signals from the magnetic particles located in the first sub-zone 252 in another frequency band (shifted to higher frequencies) than the frequency band of the magnetic drive field variations. This is possible because frequency components of higher harmonics of the magnetic drive field frequency occur due to a change in magnetization of the magnetic particles in the scanner's field of view 228 as a result of the non-linearity of the magnetization characteristics.

The embodiment shown in Fig. 11 is, of course, only an example of such an MPI apparatus. Further embodiments are known and can be envisaged. As shown in the above embodiment the various magnetic fields can be generated by coils of the same coils pairs and by providing these coils with appropriately generated currents. However, and especially for the purpose of a signal interpretation with a higher signal to noise ratio, it may be advantageous when the temporally constant (or quasi constant) selection field and the temporally variable drive field and focus field are generated by separate coil pairs. Generally, coil pairs of the Helmholtz type can be used for these coils, which are generally known, e.g. from the field of magnetic resonance apparatus with open magnets (open MRI) in which a radio frequency (RF) coil pair is situated above and below the region of interest, said RF coil pair being capable of generating a temporally variable magnetic field. Therefore, the construction of such coils need not be further elaborated herein.

In an alternative embodiment for the generation of the selection field, permanent magnets (not shown) can be used. In the space between two poles of such (opposing) permanent magnets (not shown) there is formed a magnetic field which is similar to that shown in Fig. 12, that is, when the opposing poles have the same polarity. In another alternative embodiment, the selection field can be generated by a mixture of at least one permanent magnet and at least one coil.

Fig. 13 shows a general block diagram of an MPI apparatus 100 according to the present invention. The general principles of magnetic particle imaging and of magnetic resonance imaging explained above are valid and applicable to this embodiment as well, unless otherwise specified.

The embodiment of the apparatus 100 shown in Fig. 13 comprises a set of various coils for generating the desired magnetic fields. First, the coils and their functions in a MPI mode shall be explained.

For generating the magnetic (gradient) selection field explained above, selection means are provided comprising a set of selection field (SF) coils 116, preferably comprising at least one pair of coil elements. The selection means further comprises a selection field signal generator unit 110. Preferably, a separate generator subunit is provided for each coil element (or each pair of coil elements) of the set 116 of selection field coils. Said selection field signal generator unit 110 comprises a controllable selection field current source 112 (generally including an amplifier) and a filter unit 114 which provide the respective section field coil element with the selection field current to individually set the gradient strength of the selection field in the desired direction. Preferably, a DC current is provided. If the selection field coil elements are arranged as opposed coils, e.g. on opposite sides of the field of view, the selection field currents of opposed coils are preferably oppositely oriented.

The selection field signal generator unit 110 is controlled by a control unit 150, which preferably controls the selection field current generation 110 such that the sum of the field strength and the sum of the gradient strength of all spatial fractions of the selection field is maintained at a predefined level.

For generation of a magnetic focus field the apparatus 100 further comprises focus means comprising a set of focus field (FF) coils, preferably comprising three pairs 126a, 126b, 126c of oppositely arranged focus field coil elements. Said magnetic focus field is generally used for changing the position in space of the region of action. The focus field coils are controlled by a focus field signal generator unit 120, preferably comprising a separate focus field signal generation subunit for each coil element (or at least each pair of coil elements) of said set of focus field coils. Said focus field signal generator unit 120 comprises a focus field current source 122 (preferably comprising a current amplifier) and a filter unit 124 for providing a focus field current to the respective coil of said subset of coils 126a, 126b, 126c which shall be used for generating the magnetic focus field. The focus field current unit 120 is also controlled by the control unit 150.

For generation of the magnetic drive field the apparatus 100 further comprises drive means comprising a subset of drive field (DF) coils, preferably comprising three pairs 136a, 136b, 136c of oppositely arranged drive field coil elements. The drive field coils are controlled by a drive field signal generator unit 130, preferably comprising a separate drive field signal generation subunit for each coil element (or at least each pair of coil elements) of said set of drive field coils. Said drive field signal generator unit 130 comprises a drive field current source 132 (preferably including a current amplifier) and a filter unit 134 for providing a drive field current to the respective drive field coil. The drive field current source 132 is adapted for generating an AC current and is also controlled by the control unit 150.

For signal detection receiving means 148, in particular a receiving coil, and a signal receiving unit 140, which receives signals detected by said receiving means 148, are provided. Said signal receiving unit 140 comprises a filter unit 142 for filtering the received detection signals. The aim of this filtering is to separate measured values, which are caused by the magnetization in the examination area which is influenced by the change in position of the two part-regions (252, 254), from other, interfering signals. To this end, the filter unit 142 may be designed for example such that signals which have temporal frequencies that are smaller than the temporal frequencies with which the receiving coil 148 is operated, or smaller than twice these temporal frequencies, do not pass the filter unit 142. The signals are then transmitted via an amplifier unit 144 to an analog/digital converter 146 (ADC). The digitalized signals produced by the analog/digital converter 146 are fed to an image processing unit (also called reconstruction means) 152, which reconstructs the spatial distribution of the magnetic particles from these signals and the respective position which the first part-region 252 of the first magnetic field in the examination area assumed during receipt of the respective signal and which the image processing unit 152 obtains from the control unit 150. The reconstructed spatial distribution of the magnetic particles is finally transmitted via the control means 150 to a computer 154, which displays it on a monitor 156. Thus, an image can be displayed showing the distribution of magnetic particles in the field of view of the examination area.

Further, an input unit 158 is provided, for example a keyboard. A user is therefore able to set the desired direction of the highest resolution and in turn receives the respective image of the region of action on the monitor 156. If the critical direction, in which the highest resolution is needed, deviates from the direction set first by the user, the user can still vary the direction manually in order to produce a further image with an improved imaging resolution. This resolution improvement process can also be operated automatically

by the control unit 150 and the computer 154. The control unit 150 in this embodiment sets the gradient field in a first direction which is automatically estimated or set as start value by the user. The direction of the gradient field is then varied stepwise until the resolution of the thereby received images, which are compared by the computer 154, is maximal, respectively not improved anymore. The most critical direction can therefore be found respectively adapted automatically in order to receive the highest possible resolution.

According to the present invention, the above described power supply circuits, e.g. comprising a multi-level inverter apparatus as, for instance, shown in Figs. 4 or 8, can be used in such an MPI apparatus 100 as said drive field signal generator unit 130.

The above described embodiments of the multi-level inverter apparatus thus achieve two goals at the same time, namely to deliver reactive power and to maintain low total harmonic distortion (THD). Each single inverter circuit, e.g. each single H-bridge module, is able to generate output voltages of level: -1, 0, +1. Zero output voltage of each individual inverter or zero state may be realized by either turning on both low-side or both high-side switches of a single inverter circuit.

During normal operation all inverter circuits are active to synthesize a desired output voltage. The switching configuration of each inverter circuit changes repeatedly to produce one of the desired levels: -1, 0, +1. A simple method guarantees that if the current zero state has been realized by both low-side switches, the subsequent zero state will be realized by both high-side switches. This way the stress on the switches resulting from the conduction losses is distributed equally between the low-side and high-side switches.

The simple method to balance the losses, however, is not very effective or even fails if the power supply is to deliver output voltages with small amplitude. In this case, few inverter circuits may be required. The switching configuration of the other inverter circuits no longer changes. They remain in the zero state by either having both low-side or both high-side switches closed.

In the following further embodiments of a multi-level inverter apparatus will be explained. The following scenario with respect to the embodiment shown in Fig. 10 shall be considered: If the power supply is to generate a low output voltage Uout the amplitude of the (sinusoidal) reference signal Uref will be small. Then the H-bridge circuits 11a, 11b may contribute zero volts to the output voltage Uout. As already mentioned this zero state may be realized by closing either both high-side switches 13, 15, i.e. the switches connected to the high potential terminal of the DC input voltage Udc, or the low-side switches 14, 16, i.e. the switches connected to the low potential terminal of the DC input voltage Udc, respectively.

Supposing the reference signal Uref is initially in its positive halfwave, then the zero state of H-bridge circuits 11a and 11b may be accomplished by turning on both high-side switches 13, 15. If the reference signal Uref becomes negative the zero state of H-bridge circuits 11a and 11b may now be accomplished by turning on both low-side switches 14, 16.

The embodiment shown in Fig. 10 shows four inverter circuits 9a, 9b, 9c, 9d each including a H-bridge (full bridge) circuit 11a, 11b, 11c, 11d connected in series by means of an isolating output transformer 12. To explain the following embodiments by which equal current load distribution in the four switches 13-16 in each inverter circuit 9a-9d only one inverter with a sinusoidal output current shall be looked at in the following. The switching pattern assumed in the explanation may differ from practically implemented switching patterns dependent on the application, but the embodiments are applicable to various types of switching patterns for voltage source inverters, and those applications where they are connected in series.

A first embodiment for achieving equally distributed conducting losses in all the switches 13-16 employed in a full bridge circuit 11a changes the path of freewheeling, i.e. when the output of the inverter is zero, synchronic to each period of the applied pulse pattern. Fig. 14 shows a schematic diagram of a control circuit 20 for generate control signals for the switches 13-16 of a full bridge circuit 11a. Here, "equally distributed conducting losses" means that the current distribution in the switches 13, 15, which are connected to +Udc, is equal to the current coverage in the switches 14, 16, which are connected to –Udc. In an embodiment the control circuit 20 may be a separate element coupled between the modulator 10 and the inverters 9, but it may also be implemented within the modulator 10, e.g. in the form of software or dedicated hardware (e.g. EPLD).

Exemplarily two input control signals C1, C2 are provided, e.g. by means of a microprocessor (not shown), in particular by means of the modulator 10. The first input control signal C1 sets the output voltage Uout either to the positive or negative supply rail voltage. The second input control signal C2 enables the output voltage Uout to be set. The switching pattern for the switching control signals T13-T16 for controlling the switching of the switches 13-16 is generated with respect to the desired output voltage level and shape. The control circuit 20, e.g. a programmable logic device (PLD), extracts the switching control signals T13-T16 to turn on and off each the power switches 13-16 of the full bridge circuit 11a.

Additionally, a freewheel control signal FWD is provided as input to the control circuit 20, e.g. by means of the above mentioned microprocessor (not shown), in

particular by means of the modulator 10, which preferably generates said signal from the control signals C1, C2. Said freewheel control signal FWD indicates whether the freewheeling is realized at the positive rail of the supply voltage Udc (embracing the switches 13, 15) or at the negative rail (embracing the switches 14, 16).

Alternatively, said signals C1, C2, FWD (generally, all being simple binary control signals) are determined in another superior unit (not shown), wherein said sequences are calculated in advance. In this case, the modulator 10 (or the above mentioned microprocessor) is not required.

Fig. 15 shows signal diagram of the inverter output voltage Uinv and the inverter output current Iinv. In the case shown, both the output voltage Uinv and current Iinv are in phase. The currents I13, I14, I15, I16 in the switches 13-16 are shown in the lower part of Fig. 15. As it can be seen from the traces, the current distribution (over the first or second four half periods) is not equal in all the switches 13-16. leading to the disadvantage that the switches 13-16 are subjected to different stress.

Fig. 15 particularly shows the switching of the freewheeling path together with the resulting current distributions in the switches 13-16. As is shown, an identical current distribution is achieved in all switches 13-16. The switching of the freewheeling path is made in the zero crossing of the current Iinv.

Hence, according to this embodiment of the present invention the switching pattern will be varied in the control circuit 20 in such a manner that the currents in the switches 13-16 are identical over two periods. In Fig. 16 the inverter output voltage Uinv and the inverter output current Iinv are depicted with respect to the described switching scheme. The average over two full periods of the current I in each individual switch13-16 shows equal current coverage. The switching manner shown enables a current load averaging over two half cycles.

In Fig. 16, the switching of the freewheeling path is thus depicted together with the resulting current distributions in the switches 13-16. As is shown, an identical current distribution is achieved in all switches 13-16. The switching of the freewheeling path is made in the the first switching process of a half phase of the basic oscillation.

In a further improvement the averaging timer can be set over one, three or more half cycles by varying the FWD signal which controls the freewheeling.

Another embodiment of a a multi-level inverter apparatus, in which equal distributed conducting losses are achieved in all the switches 13-16 focuses on the synchronization of the freewheeling signal FWD. In the embodiment mentioned above with

respect Figs. 15 and 16 the current and the first harmonic content of the output voltage Uinv is in phase with each other. Thus, the commutation of the freewheeling states is done at zero current levels at $\omega t = \pi, 2\pi, 3\pi$. Due to parasitic effects, the switching at zero current, as shown in the signals depicted in Fig. 15, may cause additional noise on the output voltage Uinv caused by capacitance components.

To overcome this problem, the change of the freewheeling path can be done according to a further improvement by changing the freewheeling path at the first switching instance after the current changes its sign. This is illustrated in the corresponding signals shown in Fig. 16. Here, the freewheeling signal FWD switches from high level to low level at an earlier moment in time with respect to the reference signal Uref.

It is important that the zero vector, i.e. output voltage zero, is once provided over the positive branch of the full bridge and in the subsequent sequence over the negative branch of the full bridge. The switching (positive and negative path) can selectively be made in the zero crossing of the current (as shown in Fig. 15) or at another moment. It is, however, important that the duration of the single freewheeling paths always n times π. A special embodiment is shown in Fig. 16, since the switching of the freewheeling path is made with the first switching operation after the zero crossing.

Still another embodiment focuses on the condition, if not all full bridge inverters are operating. If a lower output voltage is required, exemplarily only one or two full bridge inverters of a set of a plurality of inverters are operated. The remaining inverters are turned into a zero state and the output of those inverters is zero. This is realized by turning on the switches T13 and T15. Other combinations are possible also to set the output voltage actively to zero and thus to short-circuit the output. The switches, which short-circuit the output voltage, are changed to achieve the current load averaging over all switches in the inverters.

With respect to this last embodiment, the freewheeling path will be changed in a full bridge inverter according to the above described embodiment. Thus, the change of the freewheeling path will change synchronously with the zero crossing of the load current (as shown in Fig. 15) or synchronously with the first switching state after the change of the load current sign. (as shown in Fig. 16).

The control method explained above with reference to Figs. 14 to 16 is does not require that a common DC input voltage is used and that the outputs of the inverter are coupled in series or in parallel via transformers. Further, it is also not required, that

individual, isolated DC voltages are used and that the outputs of the inverters are coupled in series.

For instance, this control method may also be used in an embodiment of a multi-level inverter apparatus according to the present invention shown in Fig. 17, where two (or more) inverters 11a', 11b' are arranged as a cascaded H-bridge inverter circuit. In this embodiment, each inverter 11a', 11b' is provided at its own input terminals 61a', 61b' with its own DC input voltage Udc1', Udc2'. These DC input voltage Udc1', Udc2' can be equal or different and may be provided from a common voltage source or separate voltage sources, e.g. may be derived from a DC voltage supplied from a single voltage source. The switching control signals for the various switches of the inverters 11a', 11b' are provided from the control unit 20 which derives them from the control signals C1, C2 and FWD as explained above.

It is the aim of this control method that the current distribution in all switching elements is equal, wherein the average of the current in the switches of the inverters over one, two or more half periods of a periodic current signal is identical to achieve an equal load of the switches. Particularly, if an inverter within a cascaded embodiment does not make a change of the output voltage, i.e. if the output voltage has the value zero over a longer period of time, said method provides that at predetermined moments in time a change of the switching states in the respective inverter is performed. Said change is done such that the desired value of the output voltage is maintained, but the load on the switches is equally distributed. Tis can also be achieved with a cascaded embodiment of inverters, and the output voltage can also have the value zero over multiple periods.

Further, this control method can be applied in various applications. One application is in an MPI apparatus as explained above, but this control method can also be applied in an MRI apparatus or an X-ray apparatus. In particular, the power supplied to the gradient coils of an MRI apparatus, or the power supplied to the cathode and/or a control grid of an X-ray apparatus can be generated as proposed according to the present invention.

Without loss of generality, the number of inverter circuits in the above described embodiments has been selected to be four. In principle, however, any number of modules may be chosen. Further, the transformers turns ratio can be freely selected as needed, i.e. they may or may not be equal.

While the invention has been illustrated and described in detail in the drawings and foregoing description, such illustration and description are to be considered illustrative or exemplary and not restrictive; the invention is not limited to the disclosed embodiments.

Other variations to the disclosed embodiments can be understood and effected by those skilled in the art in practicing the claimed invention, from a study of the drawings, the disclosure, and the appended claims.

In the claims, the word "comprising" does not exclude other elements or steps, and the indefinite article "a" or "an" does not exclude a plurality. A single element or other unit may fulfill the functions of several items recited in the claims. The mere fact that certain measures are recited in mutually different dependent claims does not indicate that a combination of these measured cannot be used to advantage.

Any reference signs in the claims should not be construed as limiting the scope.

CLAIMS:

1. Multi-level inverter apparatus for converting a DC input voltage into an AC output voltage comprising:

- one or more pairs of DC input terminals (61; 81; 61a', 61b') for receiving one or more DC input voltages (Udc; Udc1', Udc2'),
- a plurality of inverter circuits (67a-67d; 82a-82d; 11a-11d; 11a', 11b'), coupled to one of said DC input terminals, each receiving a DC input voltage (Udc; Udc1', Udc2') or a supply voltage (Udc1-Udc4) derived therefrom and generating an AC intermediate voltage (Ua1-Ua4),
- connection means (83) coupled to said plurality of inverter circuits (67a-67d; 82a-82d) for connecting the AC intermediate voltages in series,
- a pair of AC output terminals (68; 86) coupled to the end terminals of the series connection of AC intermediate voltages (Ua1-Ua4),
- a control means (69; 87; 10, 20) for controlling said inverter circuits (67a-67d; 82a-82d; 11a-11d; 11a', 11b') to convert the one or more DC input voltages (Udc; Udc1', Udc2') into predetermined AC intermediate voltages (Ua1-Ua4).

2. Multi-level inverter apparatus as claimed in claim 1,

wherein at least two, in particular all, inverter circuits (67a-67d; 82a-82d) are adapted for converting the one or more DC input voltages into AC intermediate voltages having different voltage levels.

3. Multi-level inverter apparatus as claimed in claim 1,

comprising one or more additional AC output terminals (88) coupled to interconnections between said series connection of AC intermediate voltages.

4. Multi-level inverter apparatus as claimed in claim 1,

wherein said connection means comprises a transformer circuit (83) having a plurality of transformers (83a-83d), each comprising a primary winding (84a-84d) coupled to the output of an associated inverter circuit (82a-82d) for receiving an AC intermediate

voltage (Ua1-Ua4), and a secondary winding (85a-85d), wherein said secondary windings are coupled in series and wherein said transformer circuit (83) generates an AC output voltage (Uout) from said AC intermediate voltages (Ua1-Ua4).

5. Multi-level inverter apparatus as claimed in claim 4, wherein at least two, in particular all, transformers (83a-83d) have a different turn ratio.

6. Multi-level inverter apparatus as claimed in claim 1, wherein said connection means comprises a series connection (67) of said inverter circuits (67a-67d), and wherein the DC supply voltages (Udc1-Udc4) or DC input voltages (Udc1', Udc2') of the individual inverter circuits are galvanically isolated.

7. Multi-level inverter apparatus as claimed in claim 1 or 6, further comprising:

- a primary inverter circuit (62) coupled to said DC input terminals (61) for converting said DC voltage (Udc) into an AC primary transformer input voltage (Ut1),
- a primary transformer circuit (63) having a plurality of primary transformers (63a-63d) each comprising a primary winding (64a-64d) and a secondary winding (65a-65d), wherein said primary windings (64a-64d) are connected in parallel to the output of said primary inverter circuit (62) for providing said AC primary transformer input voltage (Ut1) to said parallel connection, said primary transformer circuit (63) generating AC primary transformer output voltages (Ut2a-Ut2d) from said AC primary transformer input voltage (Ut1),
- a plurality of rectifier circuits (66a-66d) coupled to said secondary windings (65a-65d) for converting said AC primary transformer output voltages (Ut2a-Ut2d) into said DC supply voltages (Udc1-Udc4).

8. Multi-level inverter apparatus as claimed in claim 7, wherein at least two, in particular all, primary transformers (63a-63d) have a different turn ratio.

9. Multi-level inverter apparatus as claimed in claim 1, wherein each inverter comprises two pairs of switching elements (13, 14, 15, 16) forming a H-bridge, wherein the switching elements of a first pair (13, 14) and the second

pair (15, 16) are respectively connected in series, forming three independent terminals, a first terminal being connected to the positive input voltage terminal of the respective inverter, a second terminal being connected to the negative input voltage terminal of the inverter, and the third terminal forming an alternating output voltage terminal.

10. Multi-level inverter apparatus as claimed in claim 9,

wherein said control means (10; 20) is adapted for controlling said inverter circuits (11a-11d; 11a', 11b') such that an equal current distribution is obtained in the switching elements (13, 14, 15, 16) over a predetermined time period by changing the switching configuration depending on whether a reference signal (FWD) changes sign.

11. Multi-level inverter apparatus as claimed in claim 9,

wherein said control means (10; 20) is adapted for changing the freewheeling path of an inverter circuit synchronized with a zero crossing of the output current (Iinv) of said inverter circuit or synchronized to a predetermined, in particular first, switching state of the sign of the output current (Iinv) of said inverter circuit.

12. Power supply circuit for supplying an AC load voltage (Uload) to a load (4), comprising:

- a multi-level inverter apparatus (6; 8; 9) as claimed in one of the preceding claims for converting a DC input voltage (Udc) provided by a DC voltage source (1) into an AC output voltage (Uout), and
- a filter circuit (3) coupled to the output of said multi-level inverter apparatus for filtering said AC output voltage (Uout) into said AC load voltage (Uload).

13. Power supply circuit as claimed in claim 12, wherein said filter circuit comprises a control loop including:

- a loop control circuit (31) for receiving the difference between said AC load voltage signal and a reference signal and for generating a loop control signal and
- a loop amplifier circuit (32) for generating a correction signal based on said loop control signal for correcting said AC load voltage.

14. Imaging device for imaging an object, in particular a patient, comprising imaging means, in particular an X-ray unit or a magnetic resonance unit, and one or more

power supply circuits as claimed in one of claims 12 or 13 for supplying power to said imaging means.

15. MPI device for influencing and/or detecting magnetic particles in a field of view (28), wherein the field of view comprises an object of interest containing magnetic particles, comprising:

- selection means comprising a selection field signal generator unit (110) and selection field elements (116) for generating a magnetic selection field (50) having a pattern in space of its magnetic field strength such that a first sub-zone (52) having a low magnetic field strength where the magnetization of the magnetic particles is not saturated and a second sub-zone (54) having a higher magnetic field strength where the magnetization of the magnetic particles is saturated are formed in the field of view (28),
- drive means comprising drive field signal generator units (130) and drive field coils (136a, 136b, 136c) for changing the position in space of the two sub-zones (52, 54) in the field of view (28) by means of a magnetic drive field so that the magnetization of the magnetic material changes locally,

wherein said drive field signal generator units (130) comprises one or more power supply circuits as claimed in one of claims 12 or 13.

16. Multi-level inversion method for converting a DC input voltage into an AC output voltage comprising the steps of:

- receiving one or more DC input voltages (Udc) or a supply voltage (Udc1-Udc4; Udc1', Udc2') derived therefrom,
- converting the one or more DC input voltages (Udc; Udc1', Udc2') or said supply voltage (Udc1-Udc4) into a plurality of AC intermediate voltages (Ua1-Ua4),
- generating an AC output voltage (Uout) from said AC intermediate voltages (Ua1-Ua4) by a series coupling of said AC intermediate voltages (Ua1-Ua4),
- controlling the conversion of the one or more DC input voltages (Udc; Udc1', Udc2') or said supply voltage (Udc1-Udc4) into predetermined AC intermediate voltages (Ua1-Ua4).

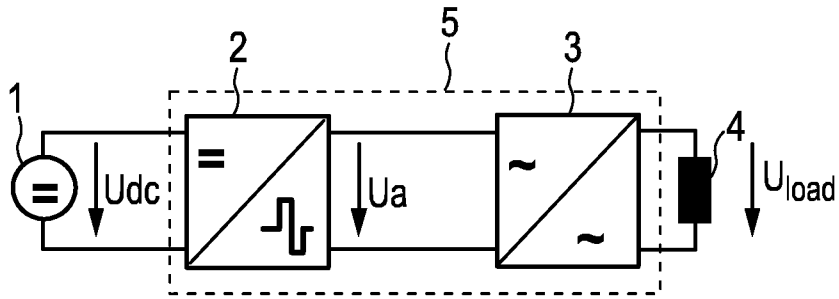


FIG. 1

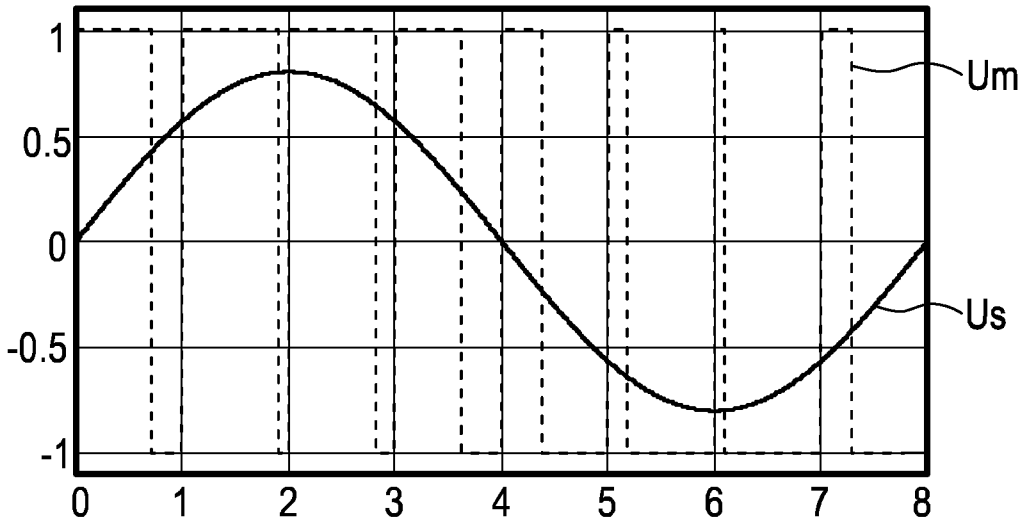


FIG. 2

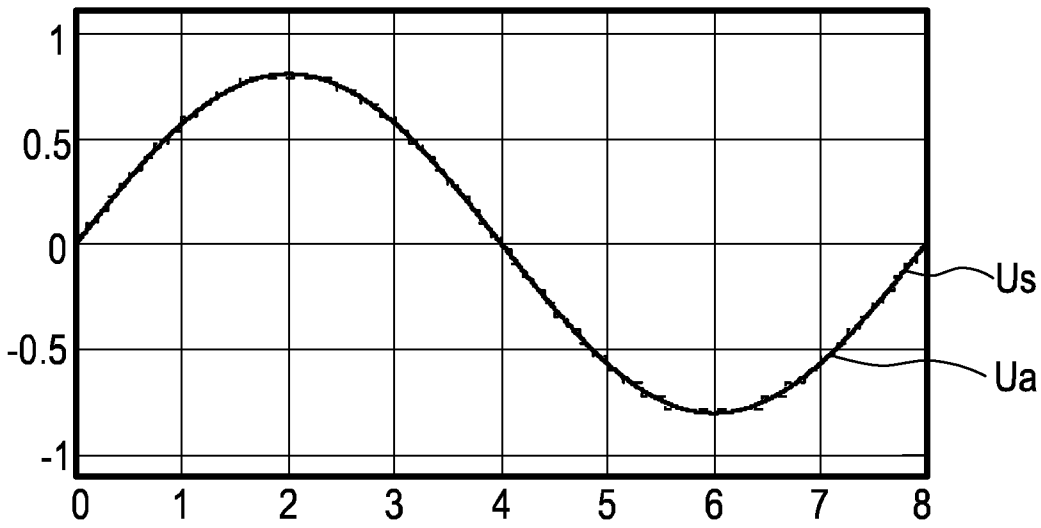
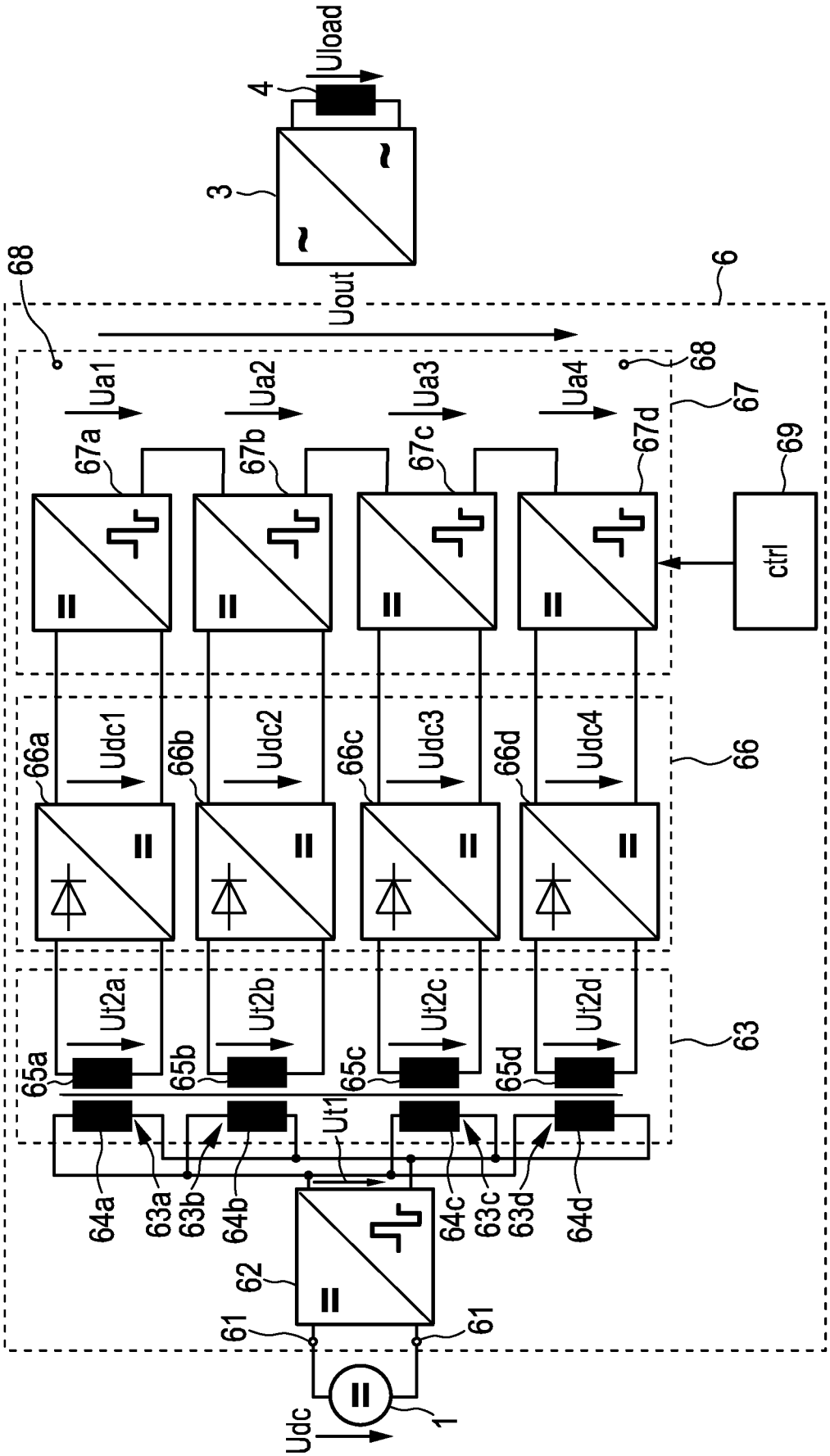


FIG. 3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3
Uout
68
6
Ua1
Ua2
Ua3
Ua4
67
67a
67b
67c
67d
69
ctrl
Udc1
Udc2
Udc3
Udc4
66a
66b
66c
66d
66
Ut2a
Ut2b
Ut2c
Ut2d
63
65a
65b
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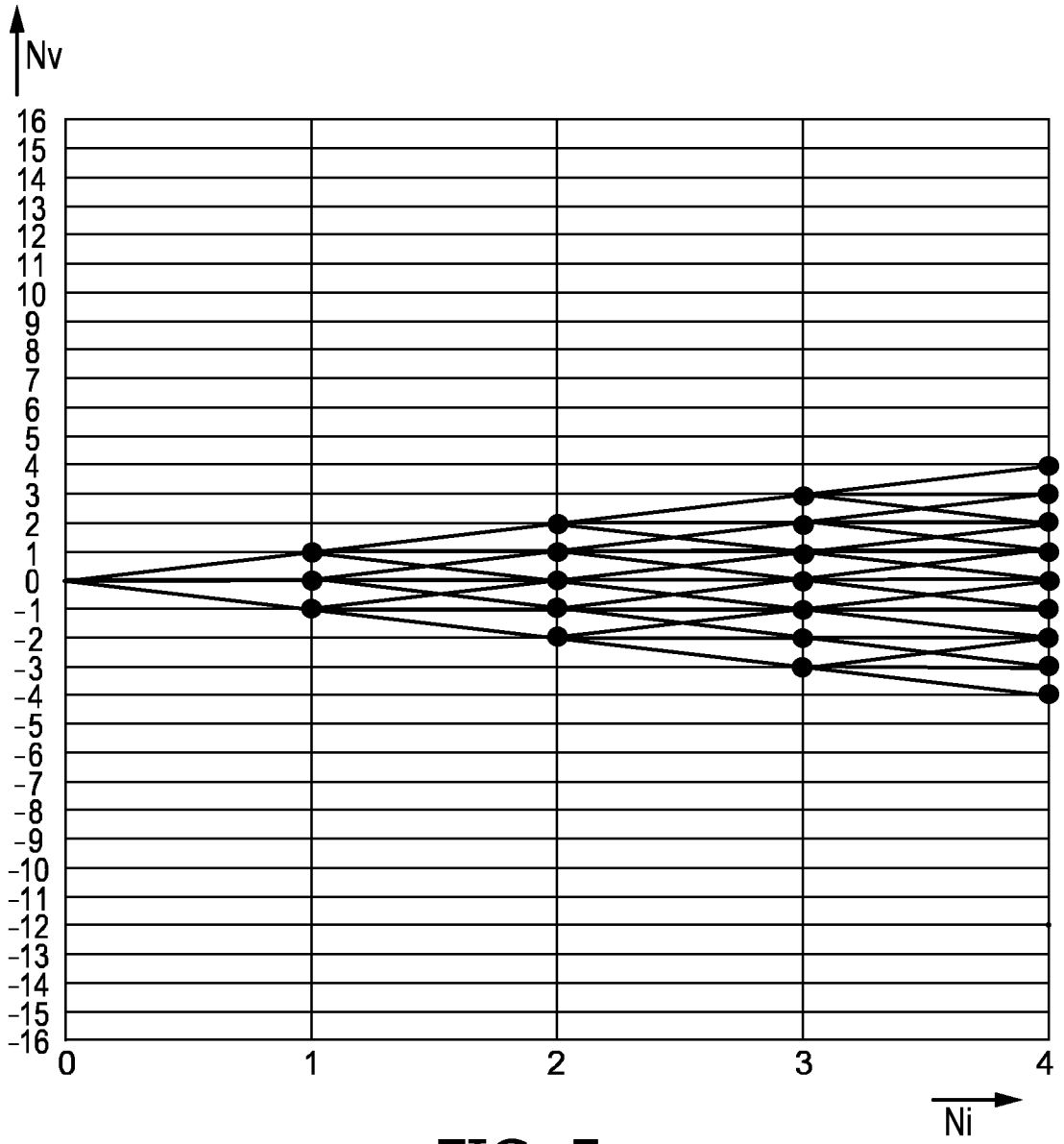
62
61
1
Udc


Nv
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13
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11
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9
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-6
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FIG. 5

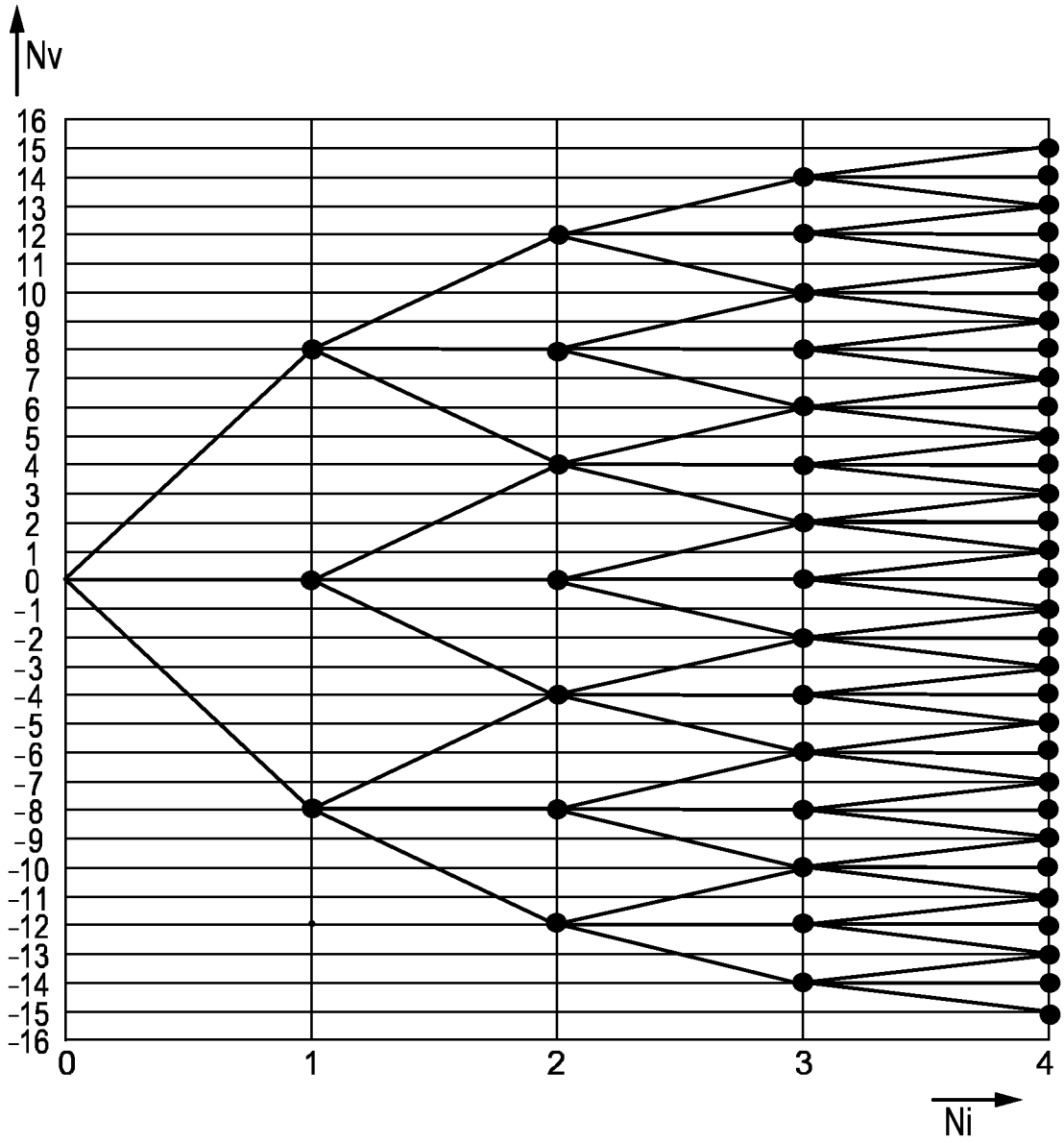
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FIG. 6

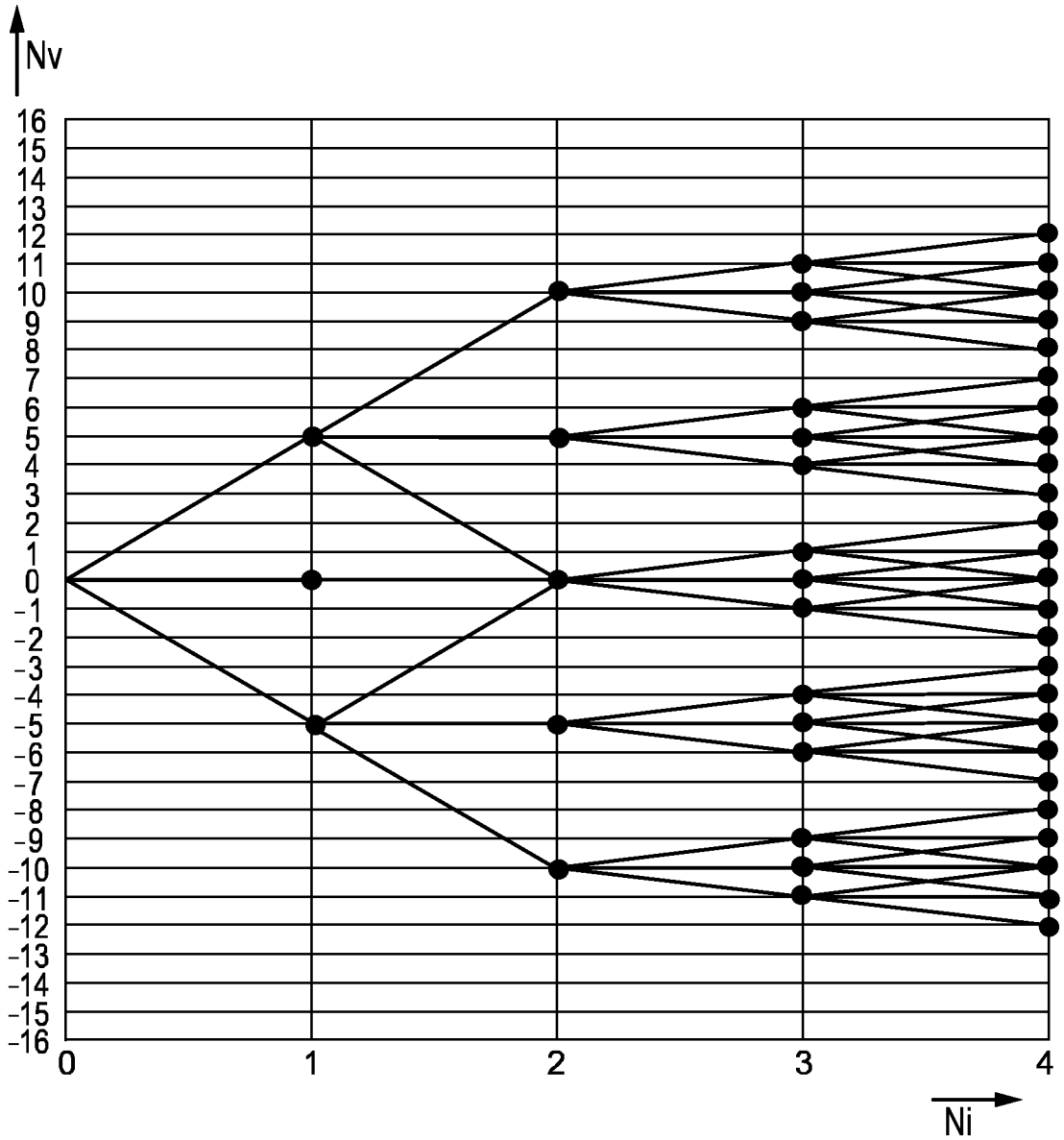
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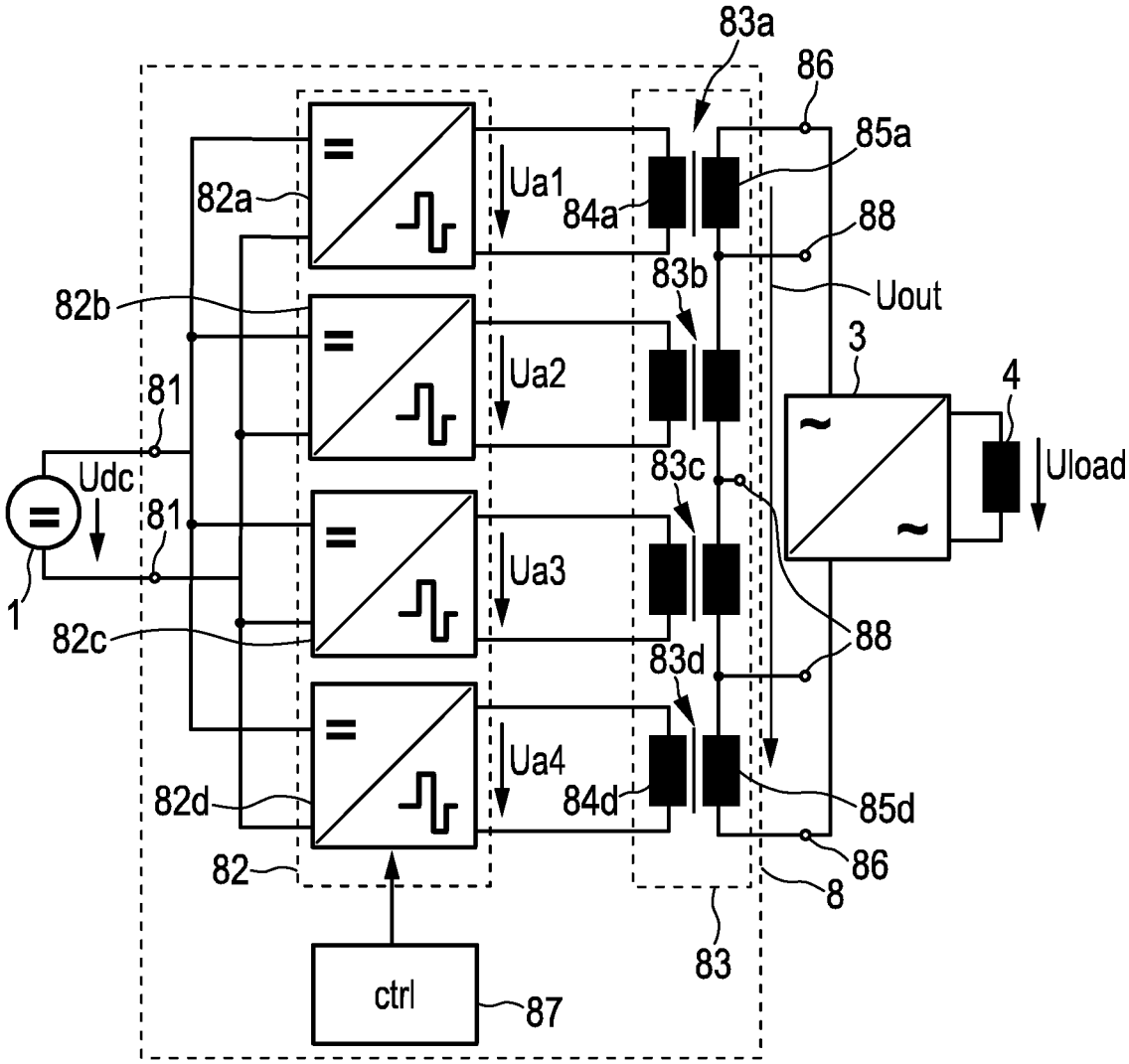
FIG. 7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85a
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Ua1
84a
88
83b
Uout
82b
Ua2
3
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81
Udc
Uload
83c
81
Ua3
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1
82c
83d
Ua4
82d
84d
85d
86
82
8
83
ctrl
87

FIG. 8

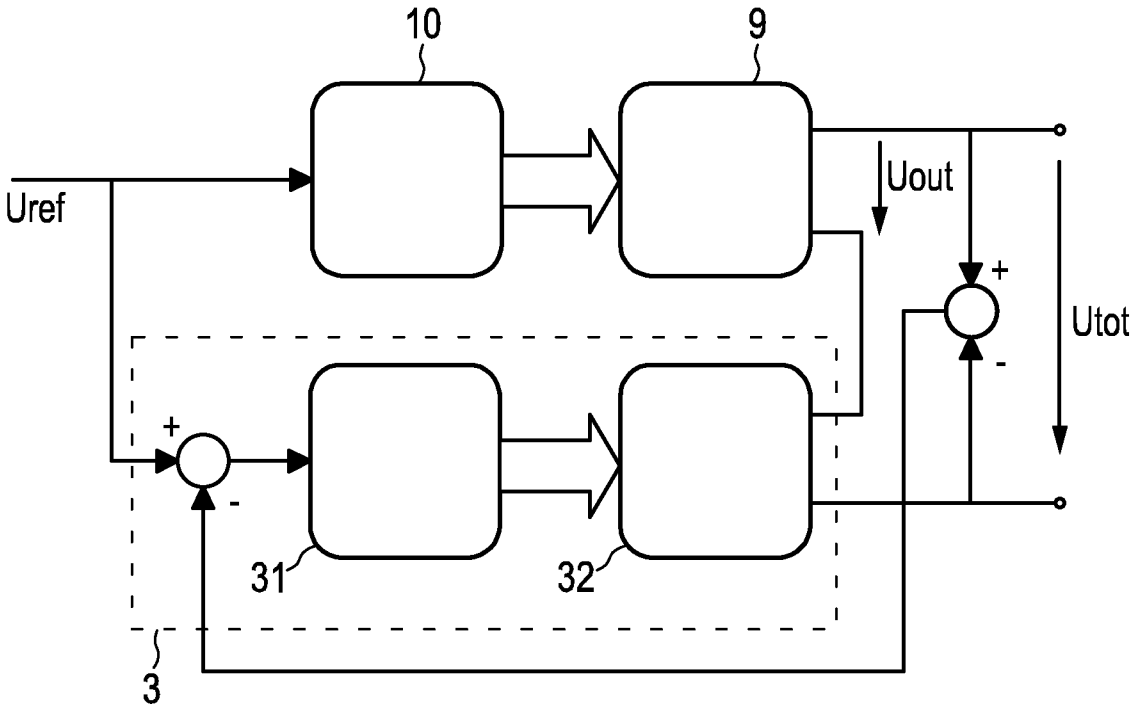
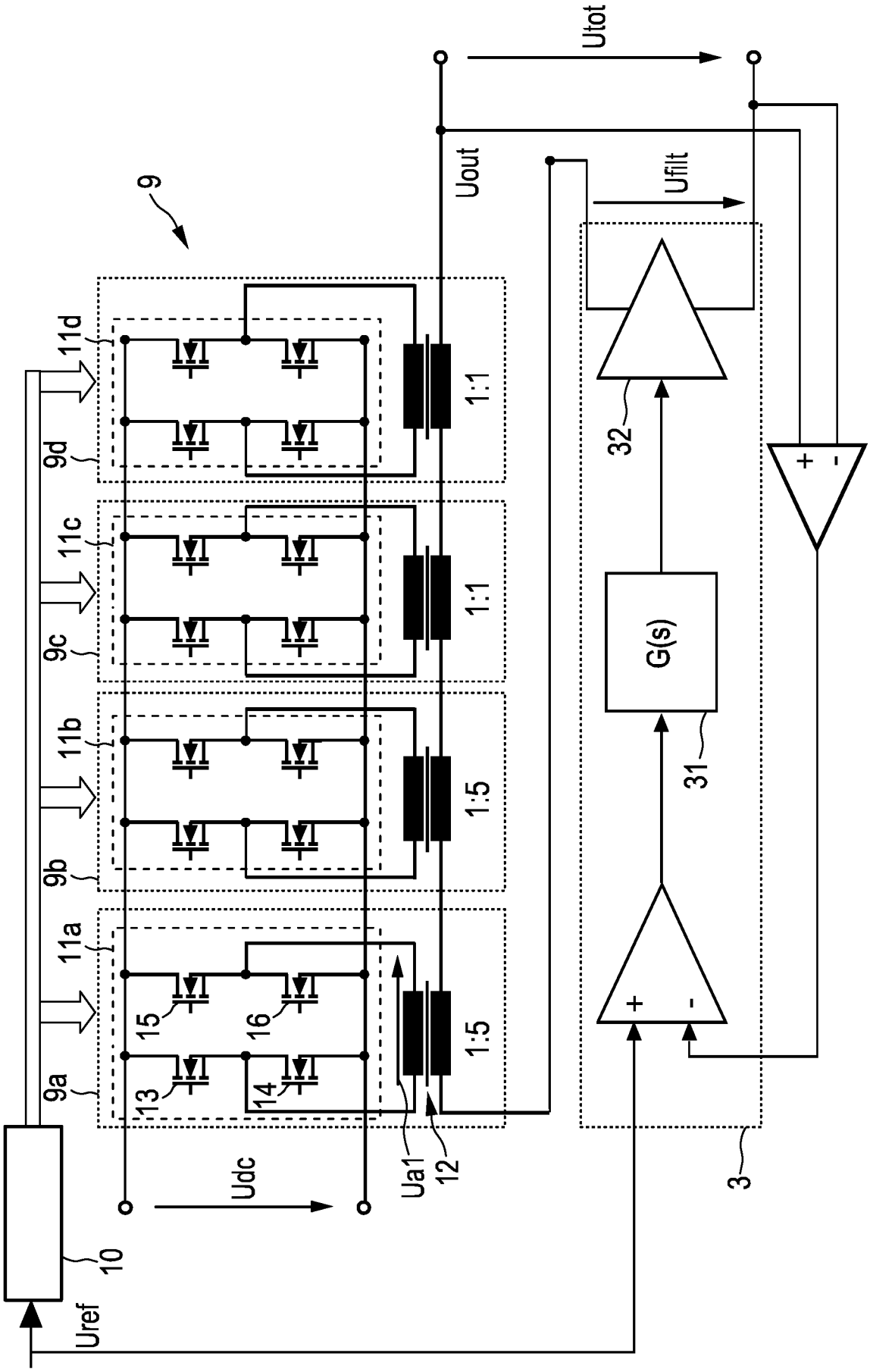


FIG. 9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Uout
Ufilt
9
11d
9d
11c
9c
11b
9b
11a
9a
1:1
1:1
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Udc
10
Uref
32
G(s)
31
3
+
-

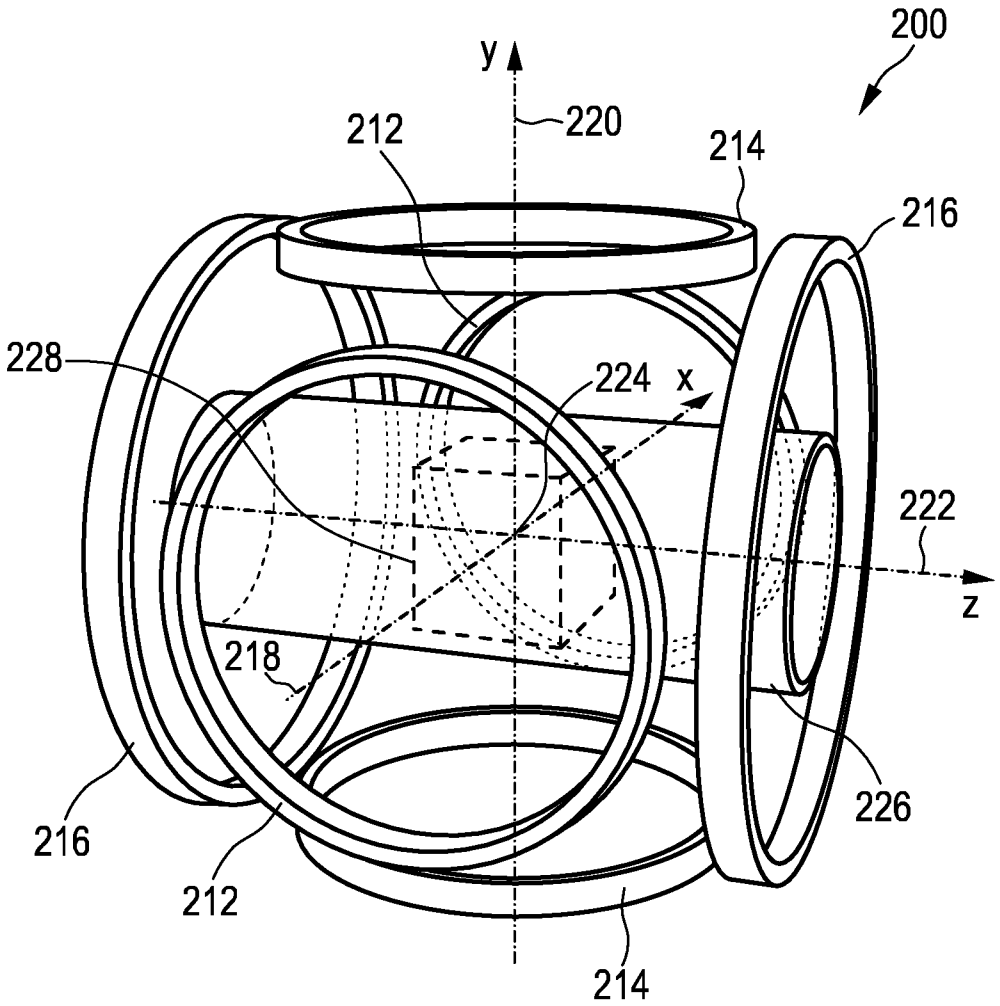


FIG. 11

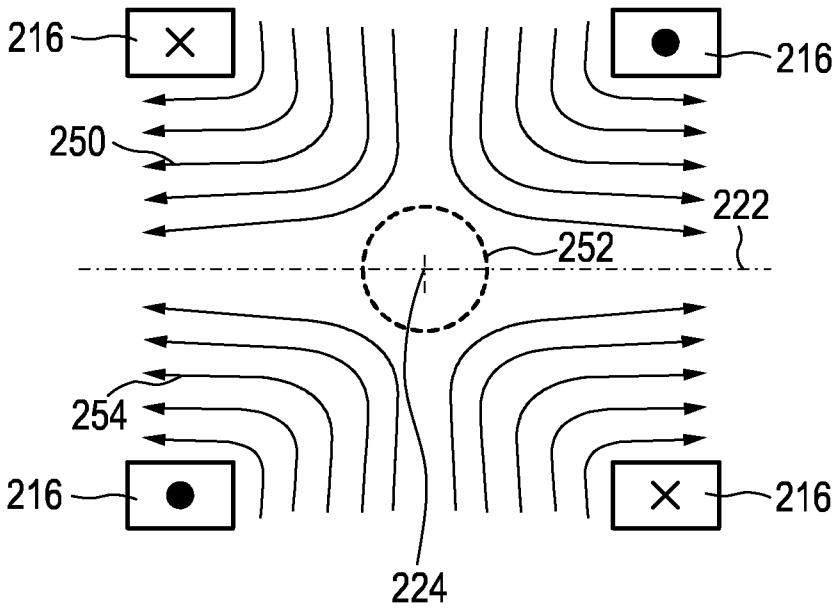
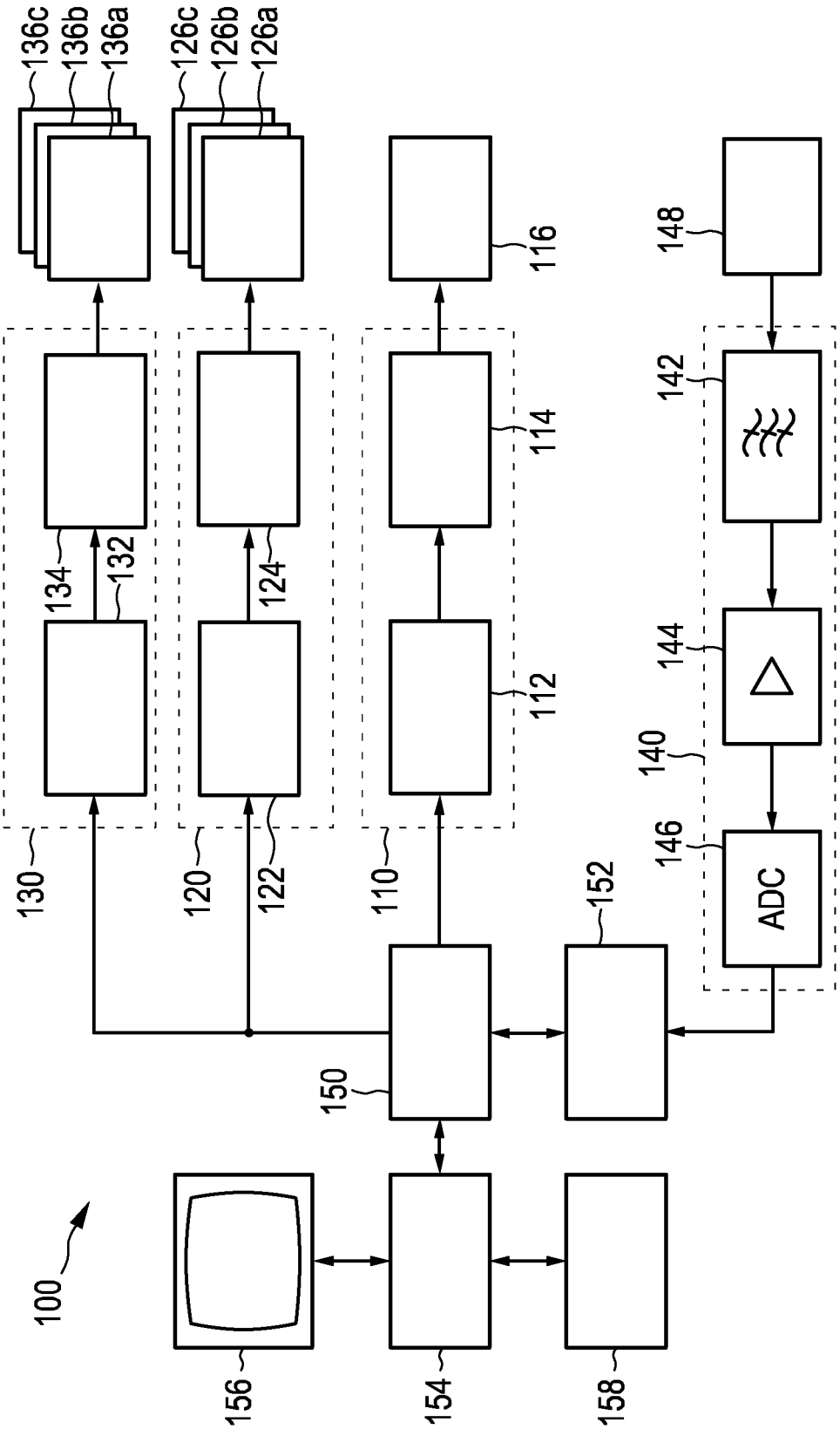


FIG. 12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ADC
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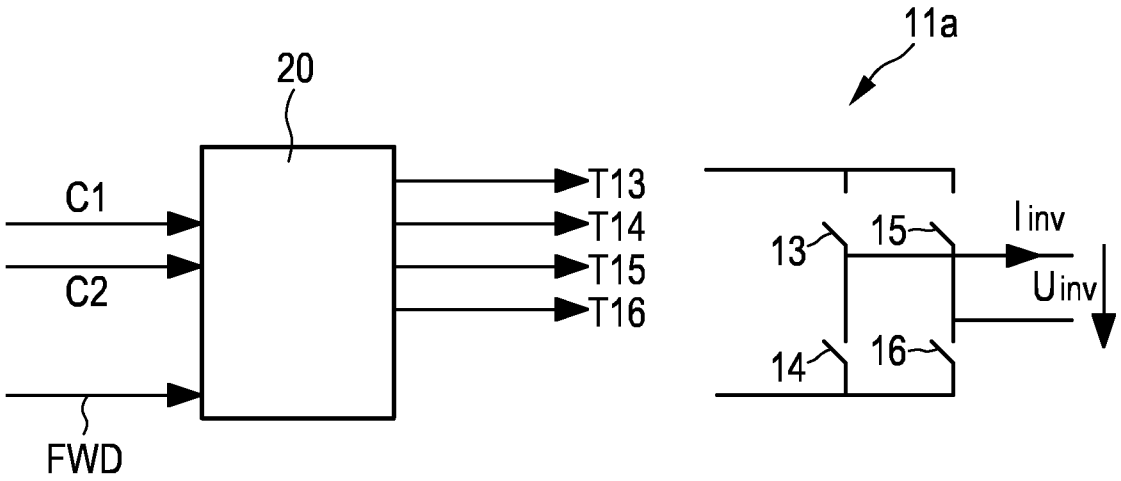

11a
20
C1
C2
FWD
T13
T14
T15
T16
13
15
14
16
Iinv
Uinv

FIG. 14

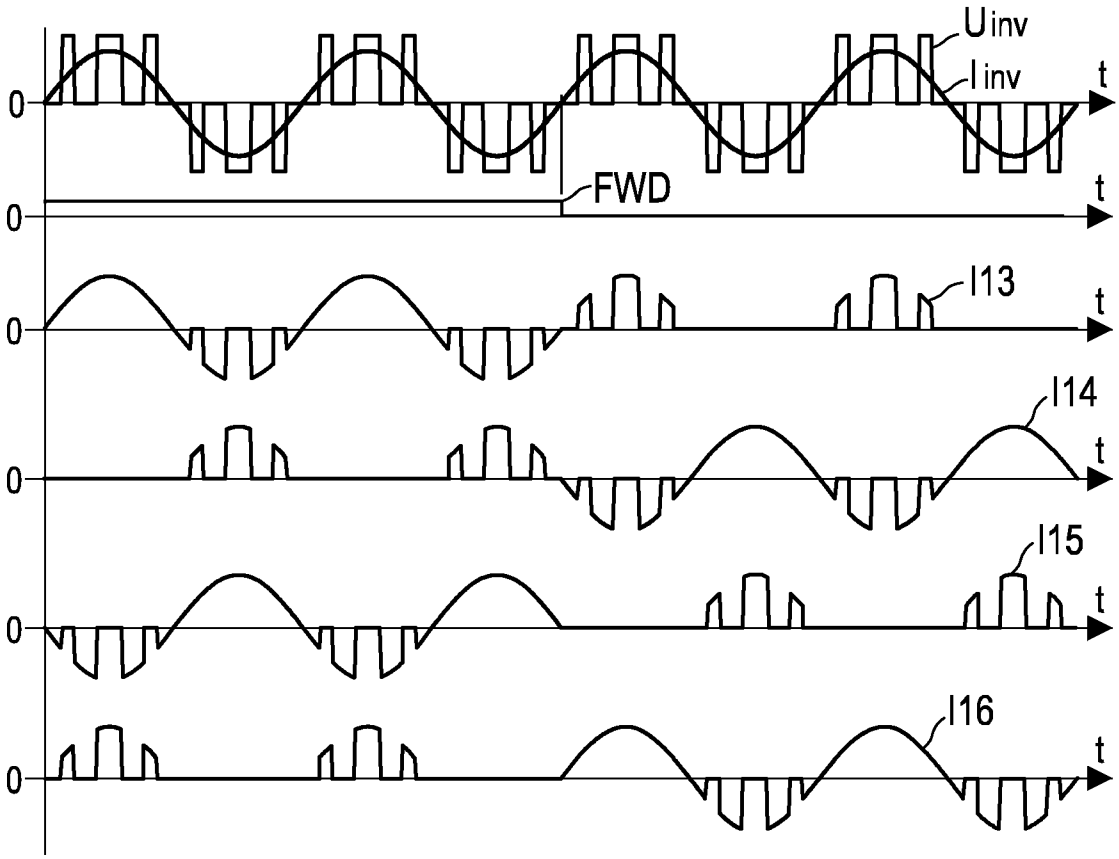

Uinv
Iinv
t
0
FWD
I13
I14
I15
I16

FIG. 15

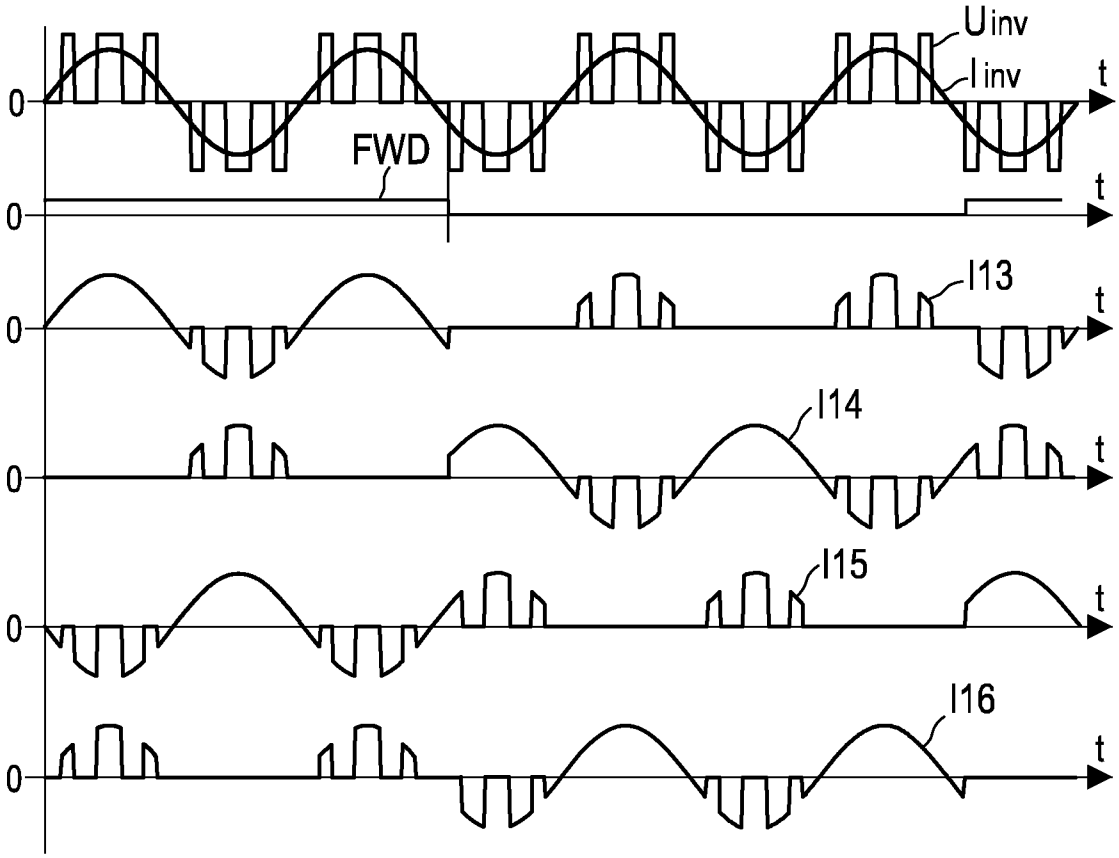
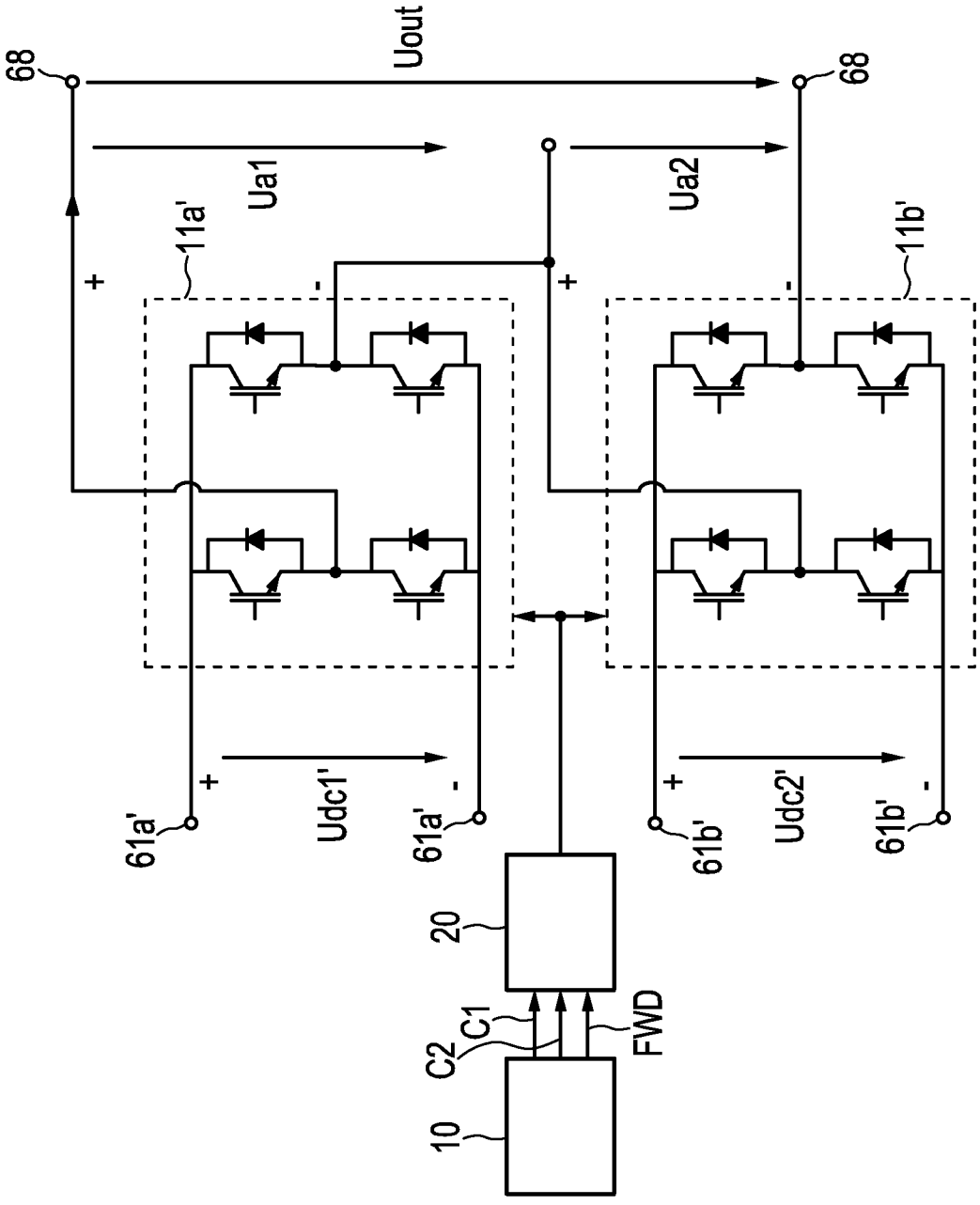


FIG. 16


68
Uout
68
Ua1
Ua2
11a'
11b'
+
-
+
-
61a'
+
Udc1'
61a'
-
61b'
+
Udc2'
61b'
-
20
C1
C2
FWD
10

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2010/053840

A. CLASSIFICATION OF SUBJECT MATTER
INV. H02M7/49
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H02M

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	WO 93/22827 A1 (TRACE ENGINEERING [US]) 11 November 1993 (1993-11-11) page 7, line 12 - line 15; figure 1	1-5,9,16 10-15
X	FR 2 641 912 A1 (FRANCE ETAT ARMEMENT [FR]) 20 July 1990 (1990-07-20) page 6, line 8 - line 10; claim 1; figure 2	1-5,9,12

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 January 2011	19/01/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Imbernon, Lisa

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2010/053840

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	KANG F-S ET AL: "A new control scheme of a cascaded transformer type multilevel PWM inverter for a residential photovoltaic power conditioning system", SOLAR ENERGY, PERGAMON PRESS. OXFORD, GB, vol. 78, no. 6, 1 June 2005 (2005-06-01), pages 727-738, XP004871599, ISSN: 0038-092X, DOI: DOI:10.1016/J.SOLENER.2004.09.008 paragraph [0002]; figure 1; table 1	1-5,9
X	US 5 757 633 A (BOWLES EDWARD E [JP]) 26 May 1998 (1998-05-26) claim 1; figure 2	1,3,6-8
X	GONG G ET AL: "A Multi-Cell Cascaded Power Amplifier", APPLIED POWER ELECTRONICS CONFERENCE AND EXPOSITION, 2006. APEC '06. T WENTY-FIRST ANNUAL IEEE MARCH 19, 2006, PISCATAWAY, NJ, USA,IEEE, PISCATAWAY, NJ, USA, 19 March 2006 (2006-03-19), pages 1550-1556, XP010910152, DOI: DOI:10.1109/APEC.2006.1620746 ISBN: 978-0-7803-9547-3 page 1551, left-hand column; figure 1	1,3,6-8, 12-16
Y	WO 2005/008876 A2 (UNIV TEXAS [US]; DIONG BILL M [US]) 27 January 2005 (2005-01-27) page 9, line 16 - line 20; figures 2,3	10,11
Y	MUELLER O M ET AL: "Quasi-linear IGBT inverter topologies", APPLIED POWER ELECTRONICS CONFERENCE AND EXPOSITION, 1994. APEC '94. C ONFERENCE PROCEEDINGS 1994., NINTH ANNUAL ORLANDO, FL, USA 13-17 FEB. 1994, NEW YORK, NY, USA,IEEE, 13 February 1994 (1994-02-13), pages 253-259, XP010118563, DOI: DOI:10.1109/APEC.1994.316391 ISBN: 978-0-7803-1456-6 figure 15	12-15

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2010/053840

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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FR 2641912 A1	20-07-1990	NONE	
US 5757633 A	26-05-1998	NONE	
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