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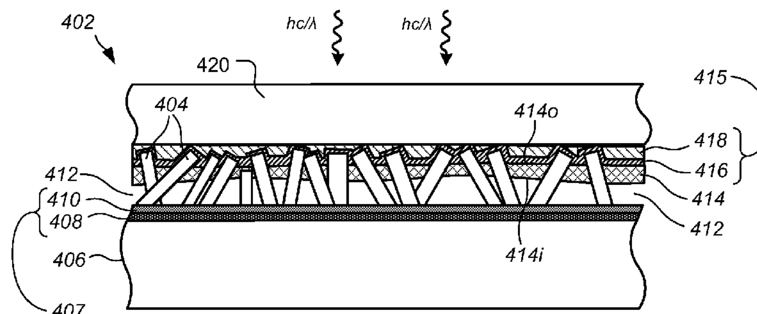

FIG. 4

(57) Abstract: Nanowire-based photovoltaic energy conversion devices and related fabrication methods therefor are described. A plurality of photovoltaic (PV) nanowires extend outwardly from a surface layer of a substrate, each PV nanowire having a root end near the substrate surface layer and a tip end opposite the root end. For some embodiments, a collar material is formed that laterally surrounds and is in contact with the PV nanowires along a portion of one or more of their ends. According to some embodiments, the PV nanowires are formed on a crystalline silicon substrate. According to some other embodiments, the PV nanowires are formed on a roll-sourced continuous substrate.

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PHOTOVOLTAIC NANOWIRE STRUCTURES AND RELATED FABRICATION METHODS

5

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to, and claims the benefit of, each of the following U.S. Provisional Patent Applications: U.S. Prov. Ser. No. 61/381,930, filed September 10, 2010; U.S. Prov. Ser. No. 61/390,732, filed October 7, 2010;
10 U.S. Prov. Ser. No. 61/415,943, filed November 22, 2010; U.S. Prov. Ser. No. 61/450,107, filed March 7, 2011; and U.S. Prov. Ser. No. 61/526,629, filed 23 August 2011. This application is related to the subject matter of the following applications: U.S. Prov. Ser. No. 61/236,144, filed August 24, 2009; U.S. Prov. Ser. No. 61/263,315, filed November 20, 2009; U.S. Prov. Ser. No. 61/264,194, filed
15 November 24, 2009; U.S. Prov. Ser. No. 61/295,500, filed January 15, 2010; U.S. Prov. Ser. No. 61/295,579, filed January 15, 2010; U.S. Prov. Ser. No. 61/295,606, filed January 15, 2010; U.S. Prov. Ser. No. 61/309,414, filed March 1, 2010; International Application No. PCT/US10/46334 filed August 23, 2010; and U.S. Prov. Ser. No. 61/376,358, filed August 24, 2010. Each of the above-referenced
20 applications is incorporated by reference herein in its entirety.

FIELD

[0002] This patent specification relates to photovoltaic energy conversion devices, such as may be used in photovoltaic solar cells and solar panels. More
25 particularly, this patent specification relates to nanowire-based photovoltaic energy conversion devices, as well as systems and methods for fabricating such devices.

BACKGROUND

[0003] Solar electric power generation systems, particularly those based on
30 photovoltaic solar panels, continue to gain popularity in efforts to shift away from supply-limited, greenhouse-gas producing fossil fuels to more environmentally friendly and sustainable forms of energy. Most of today's conventional rooftop photovoltaic solar panels comprise side-by-side arrangements of relatively large (*e.g.*, 5 cm x 5 cm, 10 cm x 10 cm) bulk monocrystalline or bulk multicrystalline
35 silicon wafers processed to form depthwise p-n junctions. Manufacture of the bulk

crystalline silicon wafers is highly energy-intensive and expensive, and the power conversion efficiency of the resultant devices is typically only in the range of 15% to 20%. A chronic shortage in the supply of bulk crystalline silicon wafers has plagued the industry in recent years, a shortage that is expected by some
5 forecasters to reach crisis proportions in coming years. Although thin-film photovoltaic cells fabricated from amorphous silicon or chalcogenide compounds require less semiconductor material than those based on bulk crystalline silicon wafers and are less energy-intensive and less costly to produce, their power conversion efficiencies are even lower, usually in the 6% to 10% range.

10 **[0004]** Proposals have been set forth for using semiconducting nanowires as a basis for photovoltaic solar energy conversion. Nanowires are small self-assembled structures having lengths typically in the range of 0.5 μm – 5 μm and diameters typically in the range of 10 nm – 1000 nm. One method of fabricating nanowires uses a vapor-liquid-solid ("VLS") synthesis process, sometimes termed
15 a catalytic growth process. A catalyst material such as gold or titanium is deposited on a substrate at a large number of spots thereacross, each spot being a location at which a nanowire will be grown. The substrate with the catalyst is then placed in a reaction chamber and heated to high temperatures (*e.g.*, 250° C - 1000° C). Precursor gases, including the elements or compounds that will form the
20 nanowires, are introduced into the chamber. Under the influence of the catalyst, the precursor gases at least partially decompose into their respective elements, some of which are transported on or through the catalyst in liquified phase to the immediately underlying solid surface provided by the substrate. At each spot, a nanowire epitaxially grows outwardly from the substrate as the process proceeds,
25 the catalyst at each spot remaining at the tip of the nanowire and rising away from surface of the substrate as the nanowire grows. The resultant nanowires exhibit a long-range atomic order (i.e., single-crystal) that can potentially be exploited for a variety of different useful applications. So-called self-catalytic growth of nanowires has also been reported in the literature.

30 **[0005]** During nanowire formation, the elements or compounds used to form the nanowires can be varied, such that the material composition and/or semiconductor doping level of each nanowire is variable along the longitudinal length of that nanowire. In one known scenario relevant to the preferred

embodiments herein, the longitudinally varying material and/or doping profile can be designed such that each nanowire exhibits a photovoltaic property, *i.e.*, is capable of absorbing incident photons and providing an associated photocurrent to an external load (if properly electrically connected to that load). As used herein,
5 PV nanowire refers to any of a variety of nanowires themselves or related structures that employ nanowires and are capable of exhibiting photovoltaic properties, such photovoltaic properties arising from any of a variety of different material selections, material compositional and spatial chemical profiles, and/or doping profiles thereof. By way of non-limiting example, PV nanowires can
10 comprise one or more longitudinal homojunctions (*e.g.,* p-n, p-i-n, p-n-p, n-p-n homojunctions), one or more longitudinal heterojunctions (e.g., materials containing various chemical elements and/or various chemical compositions and various bandgaps), and/or portions of such homojunctions or heterojunctions that are completed by virtue of the materials and/or doping profiles immediately opposite
15 the longitudinal end(s) of the nanowire. One example of a PV nanowire-based solar cell is described in US 2007/0267625 A1, which is incorporated by reference herein in its entirety.

[0006] Advantageously, PV nanowire-based solar cells can provide power conversion efficiencies that are as great, or even greater, than solar cells based on
20 bulk crystalline wafers made of a same material. For example, it is believed at least theoretically possible to achieve PV nanowire-based solar cells composed of III-V semiconductor material having 35 percent, and perhaps even 40 percent, energy conversion efficiency, which is as high or better than photovoltaic cells made with bulk crystalline semiconductor wafers. At the same time, because they
25 can be built upon low-cost substrates with low material utilization and comparatively low energy requirements, PV nanowire-based solar cells can be fabricated at a fraction of the cost of comparable solar cells based on bulk crystalline wafers.

[0007] One or more issues may arise in the design and/or fabrication of PV
30 nanowire-based solar cells that is at least partially resolved by one or more of the preferred embodiments described herein. One issue that may arise in PV nanowire-based solar cells relates to the need for an electrode to be provided on each side of the PV nanowire array, including a root-side electrode corresponding

to the roots of the PV nanowires and a tip-side electrode corresponding to the tips of the PV nanowires. The need to provide good electrical contact and conductivity at these electrodes can present substantial limitations on the type, complexity, and orientation of the overall PV nanowire-based solar cells, because structures providing the good electrical contact and conductivity can often prove to be light-absorbing or light-reflecting, thereby reducing the percentage of photons able to reach the PV nanowire junctions. For PV nanowire-based solar cells that are based on longitudinal p-i-n junctions, another issue that may arise relates to the quality of p-type, intrinsic-type, and n-type semiconductor material that physically forms the PV nanowire for achieving optimum photovoltaic performance.

[0008] One issue that can affect the performance of PV nanowire-based solar cells is carrier loss due to charge recombination occurring along the surface of the PV nanowires. Charge recombination is a loss process in which an electron, which has been photo-excited from the valence band to the conduction band of a semiconductor, falls back into an empty state (hole) in the valence band. Charges that recombine do not produce any photocurrent and, hence, do not contribute toward solar cell efficiency. Charge recombination losses can be particularly strong along the surface of a semiconductor material, where dangling bonds give rise to certain surface states that greatly facilitate the electron-hole recombination process. Because the recombination losses associated with surfaces scale with total surface area, the problem becomes particularly amplified for nanowires having high surface-to-volume ratio. Generally speaking, the recombination losses at surfaces tend to be more problematic for III-V compound semiconductor PV nanowires than for silicon PV nanowires for which stable natural oxide (i.e., SiO_2) that can be easily formed on Si surfaces can greatly reduce the density of surface states. Other issues may arise as would be apparent to one skilled in the art upon reading the present disclosure.

SUMMARY

[0009] According to some embodiments, a method for fabricating a photovoltaic energy conversion device is described. The method includes providing a substrate including a substrate surface layer doped in a first dopant type (e.g. n-type or p-type); growing a plurality of photovoltaic (PV) nanowires outwardly from the substrate surface layer, each PV nanowire having a root end

near the substrate surface layer and a tip end opposite the root end; forming a layer of collar material that laterally surrounds and is in contact with the PV nanowires along at least a rootward portion of their lengths, the collar material doped in the first dopant type; and forming a tip-side doped material doped in a
5 second dopant type, the tip-side doped material in contact with the tip ends of the PV nanowires.

[0010] According to some embodiments the layer of collar material is grown in a lateral direction from the PV nanowires, and a layer of optically transparent, electrically insulating solid filler material is provided that laterally surrounds the PV
10 nanowires along an outward portion of their lengths. A longitudinal p-i-n junction is preferably associated with each PV nanowire. According to some embodiments, the growing of PV nanowires is partially carried out before the forming of the collar material and partially carried out after the forming of the collar material, such that a gap between 0.2 microns and 5 microns is formed between an outward-most
15 portion of the collar material a rootward most portion of the tip-side material. The PV nanowires are not intentionally doped, according to some embodiments. In such cases the PV nanowires preferably have impurity levels less than 10^{17} per cubic centimeter.

[0011] According to some embodiments, a method for fabricating a
20 photovoltaic energy conversion device it described that includes: providing a substrate including an n-doped substrate surface layer; growing a plurality of n-doped photovoltaic (PV) nanowires outwardly from the substrate surface layer, each PV nanowire having a root end near the substrate surface layer and a tip end opposite the root end; forming a layer of optically transparent, electrically insulating
25 solid filler material that laterally surrounds the PV nanowires along a portion of their lengths; and forming a tip-side p-doped material in contact with the tip ends of the PV nanowires. According to some embodiments, the tip-side p-doped material is p+ or p++ type doped.

[0012] According to some embodiments, a method for fabricating a
30 photovoltaic energy conversion device is described that includes: providing a 6" by 6" square substrate including a substrate surface layer on which the PV nanowires and other structures are formed.

[0013] According to some embodiments, a method for fabricating a photovoltaic energy conversion device is described, that includes forming a mask layer on the substrate surface layer, the mask having a plurality of spaced apart voids such that portions of the substrate surface layer are exposed at the locations
5 of the voids. The photovoltaic (PV) nanowires are grown outwardly from the exposed portions of the substrate surface layer.

[0014] According to some embodiments, a method for fabricating a photovoltaic energy conversion device is described that includes providing a substrate including a long range atomic order (LRAO) substrate surface layer (such
10 as a highly n-type doped <111> crystallographic plane of the silicon wafer); and growing a plurality of n-doped photovoltaic (PV) nanowires outwardly from the LRAO substrate surface layer.

[0015] According to some embodiments, a method for fabricating a photovoltaic energy conversion device is described that includes providing a roller-
15 based substrate material including a substrate surface layer with short range atomic order (SRAO) such as polysilicon or amorphous silicon, on which the PV nanowires and other structures are formed.

[0016] According to some embodiments, a photovoltaic energy conversion device is provided that is fabricated according to the methods described herein.

20

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Fig. 1 illustrates fabricating a PV nanowire structure according to some preferred embodiments;

[0018] Fig. 2A illustrates a simplified cross-sectional view of one of the PV
25 nanowire structures formed according to the method of Fig. 1;

[0019] Fig. 2B illustrates a simplified perspective view thereof;

[0020] Figs. 3A-C illustrate an alternative method of manufacture using a thin mask structure, according to some embodiments;

[0021] Fig. 4 illustrates a cross-sectional view of a PV nanowire-based solar
30 cell, according to some embodiments;

[0022] Fig. 5 illustrates some fabrication steps of the device of Fig. 4 according to some embodiments;

[0023] Fig. 6 illustrates fabrication of a PV nanowire-based solar cell according to some embodiments;

[0024] Fig. 7 is a block diagram showing stations of a continuous substrate roll manufacturing process for fabricating PV nanowire-based solar cells, according to some embodiments;

[0025] Figs. 8A-B schematically illustrate roll-based continuous substrate manufacturing processes for PV nanowire-based solar cells, according to some embodiments;

[0026] Fig. 9 is diagram schematically illustrating a heating and/or cooling station, according to some embodiments;

[0027] Figs. 10A-B show cross sections of a processing chamber having a moveable lid, according to some embodiments;

[0028] Fig. 11 is a cross section of a processing chamber having high impedance wall section, according to some embodiments;

[0029] Fig. 12 is a cross section of a processing chamber having double rollers, according to some embodiments;

[0030] Fig. 13 is a plan view of a processing station used to spray on nanowire catalyst material, according to some embodiments;

[0031] Fig. 14 schematically illustrates a large area discrete substrate manufacturing process for PV nanowire-based solar cells, according to some embodiments; and

[0032] Fig. 15 illustrate a structure that includes an n-doped PV nanowire and a heavily doped p-type tip-side electrode material, according to some embodiments.

DESCRIPTION

[0033] One or more aspects of the preferred embodiments hereinbelow may be further understood in view of selected background references from the non-patent literature identified in the list that follows. The listed references, each of which is incorporated by reference herein in its entirety, are referenced further hereinbelow by their respective identifying numerals.

[0034] {1} Kobayashi, et. al., “Metal Organic Chemical Vapor Deposition of Indium Phosphide Nanoneedles on Non-Single Crystal Silicon Surfaces,” Proc. SPIE, Vol. 6370, 63700S-1-8 (2006);

[0035] {2} Kobayashi, et. al., “Growth and Characterization of Indium Phosphide Single-Crystal Nanoneedles on Microcrystalline Surfaces,” Appl. Phys. A, Vol. 85, 1-6 (2006);

[0036] {3} Kobayashi, et. al., “Ensembles of Indium Phosphide Nanowires: Physical Properties And Functional Devices Integrated On Non-Single Crystal Platforms,” Appl. Phys. A, Vol. 95, 1005-1013 (2009);

[0037] {4} Goto, et. al., “Growth of Core-Shell InP Nanowires for Photovoltaic Application by Selective-Area Metal Organic Vapor Phase Epitaxy,” Applied Physics Express 2, 035004-1-3 (2009);

[0038] {5} Singh, et. al., “Reduction in Surface Charge Density By New GaAs Passivation Method,” J. Phys. D: Appl. Phys., Vol. 8, L42-43 (1975);

[0039] {6} Kalhor, et. al., “Annealing Effects on Opto-electronic Properties of Thermally-Evaporated ITO/Ag/ITO Multilayered Films for Use in Color Filter Electrodes,” World Applied Sciences Journal 6 (1): 83-87 (2009);

[0040] {7} Perkins, et. al., “Combinatorial Optimization of Transparent Conducting Oxides (TCOs) for PV,” 31st IEEE Photovoltaics Specialists Conference and Exhibition, Lake Buena Vista, Florida, Jan. 3-7, 2005, NREL/CP 520-37420 (2005);

[0041] {8} Pern, et. al., “Accelerated Exposure Tests of Encapsulated Si Solar Cells and Encapsulation Materials,” National Center for Photovoltaics Program Review Meeting, Denver, Colorado, Sept. 8-11, 1998, NREL/CP-520-25361 (1998);

[0042] {9} Guillen, et. al., "ITO/Metal/ITO Multilayer Structures Based On Ag and Cu Metal Films for High Performance Transparent Electrodes," Solar Energy Materials and Solar Cells, Vol. 92, Issue 8, pp. 938-941 (2008);

[0043] {10} Iyer, R., “Sulfur as a Surface Passivation for InP,” Appl. Phys. Lett. 53 (2) (1988);

[0044] {11} Voyles, et. al., “Absence of an Abrupt Phase Change from Polycrystalline to Amorphous in Silicon with Deposition Temperature,” Phys. Rev. Lett. 86 (24), pp. 5514-5517 (2001); and

[0045] {12} Gao, L., et. al., “Self-Catalyzed Epitaxial Growth of Vertical Indium Phosphide Nanowires on Silicon,” Nano Lett. 9 (6), pp 2223–2228 (2009).

[0046] PV nanowires can be formed *(e.g.*, catalytically grown or otherwise generated) upon substrates having different types of surface characteristics. PV nanowires can, of course, be formed upon substrates that exhibit long-range crystallographic order along their surfaces, including cost-intensive bulk crystalline
5 wafer substrates. However, as described in {2}-{3}, *supra*, PV nanowires can also be formed upon substrates that do not exhibit long-range crystallographic order along their surfaces, but that do exhibit short-range crystallographic order along their surfaces at the locations of the nanowires to be formed. For purposes of the present description, the term short range atomic order (SRAO) is used
10 interchangeably with the term short range crystallographic order. The material providing the short-range atomic order, termed herein SRAO material, can be different or the same as the underlying material that forms the bulk of the substrate. When different from the underlying substrate material, the SRAO material can be formed as a very thin layer thereupon, which can be termed a template layer.
15 Advantageously, the substrate material underlying the SRAO template layer can be any material suitable to provide mechanical and/or electrical support for the SRAO template layer regardless of the presence or absence of crystalline character, provided only that its properties are otherwise consistent with the purpose of the apparatus to be built. By way of example, the bulk of the substrate can comprise
20 amorphous silicon dioxide, quartz, stainless steel, or chromium. By way of example, the SRAO template layer can be a 100-nm thick film of hydrogenated amorphous silicon or hydrogenated microcrystalline silicon.

[0047] If the PV nanowires are formed upon a substrate whose surface exhibits long range atomic order, it is more likely that a high percentage of the nanowires
25 will be in geometric alignment with each other and that their tips will rise to similar heights above the substrate surface. If the PV nanowires are formed upon a substrate having an short range atomic order (SRAO) material surface, the population of PV nanowires will be more likely to have a lesser degree of alignment due to the multiple different crystallographic directions imposed upon the
30 population of PV nanowires, and there will be greater variation in the heights of their tips above the substrate surface. The preferred PV nanowire-coupling fabrication methods described hereinbelow are presented in the context of PV nanowires formed upon substrates having SRAO material surfaces. In addition to

representing the more difficult (and more general) case due to greater variation in PV nanowire tip heights, the latter also represents a more commercially desirable case due to the availability of lower-cost fabrication processes, such as roll-based manufacturing processes, associated with the wide flexibility in bulk substrate material choices. It is nevertheless to be appreciated, however, that the described methods are readily applicable in the context of PV nanowires formed upon substrates whose surfaces exhibit long range atomic order, such as bulk crystalline wafer substrates.

[0048] In relation to the description that follows, it is to be readily understood that the “positive” and “negative” electrical polarities can of course be reversed depending on the material structures and doping profiles of the PV nanowires. For one or more of the examples presented herein, the “top” direction corresponds to an outward direction relative to a surface of the substrate from which the PV nanowires are grown. However, it is to be appreciated that the terms “top” and “bottom” are used for convenience of description and do not imply any particular orientation relative to gravity, nor do they imply any particular direction of solar radiation entry into the PV nanowire array.

[0049] Fig. 1 illustrates fabricating a PV nanowire structure according to some preferred embodiments. Fig. 2A illustrates a simplified cross-sectional view of one of the PV nanowire structures formed according to the method of Fig. 1, while Fig. 2B illustrates a simplified perspective view thereof. At step 102, a bottom electrode layer 154 is formed upon a substrate 152, and a layer 156 of n-type amorphous hydrogenated silicon (n-type a-Si:H) is formed on the bottom electrode layer 154. The bulk of the substrate 152 substrate can comprise, for example, amorphous silicon dioxide, quartz, stainless steel, chromium, or an optically transparent glass. The bottom electrode layer can comprise, for example, a metal such as molybdenum or aluminum.

[0050] At step 104 a nanoparticle catalyst island 158, comprising for example gold or platinum, is formed on the n-type a-Si:H layer 156 at each location where a nanowire is to be grown. The catalyst island 158 will be shaped and dimensioned according to the desired profile of the nanowire to be grown. In one example, the catalyst island 158 can be generally circular with a diameter in the range of 50 nm – 500 nm.

[0051] At step 106, catalytic nanowire growth is commenced, for example at a temperature of 430 degrees Celsius for InP nanowires, in conjunction with the introduction of appropriate precursor gases into the growth chamber. However, according to a preferred embodiment, the nanowire growth process proceeds only
5 to a time when the nanowire tips are at a predetermined intermediate height, such as 500 nm, above the surface of the n-type a-Si:H layer. At this point, as illustrated in Fig. 1, only a root section 160a of a nanowire has been formed.

[0052] At step 108, the temperature is then raised to 500-600 degrees, and the precursor gases used in step 106 are kept the same except that n-type dopants
10 are also introduced into the reaction chamber. Due to the raised temperature, the upward nanowire growth, as catalyzed by the nanoparticle catalyst island 158, stops occurring. Instead a more standard (non-catalytic) crystallographic growth of the InP material occurs, with the lateral sides of the root section 160a serving as a "substrate" for that growth. Accordingly, at step 108 the growth proceeds laterally,
15 rather than upwardly, to form what is essentially a cylindrical shell 162 of InP material around the root section 160a, and because n-type dopants are introduced, the InP shell 162 is an n+ type shell. The lateral growth of the n+ type shell 162 proceeds until its thickness (*i.e.,* the amount that it extends laterally outward from the root section 160a) is comparable to the diameter of the root section 160a, *e.g.*,
20 about 500 nm. Suitable n-type dopants for step 108 include, for example, Te, Sn, and Si for the case of InP nanowires. Notably, it is acceptable and can indeed be advantageous if some n-doping of the nanowire root section 160a occurs during the step 108.

[0053] At step 110, subsequent to the formation of the n+ type shell 162, the
25 temperature is again lowered to the previous catalytic nanowire growth temperature, such as 430 degrees Celsius for InP nanowires, and the upward catalytic nanowire growth process is resumed to form upper nanowire portions 160b, proceeding until completed nanowires 160 at their full ultimate intended height (such as between 2 μm to 5 μm, although the scope of the present
30 teachings is not so limited) are formed. Optionally, after nanowire growth, a thin passivation layer can be applied on the surface of the nanowires to chemically and physically protect the nanowires and stabilize the surface of the nanowires to reduce the density of unfavorable surface states. Such thin passivation layer can

be made by a technique such as atomic layer deposition that relies upon self-limiting surface chemical reaction of precursors containing desired chemical elements such that the voids among the nanowires will not be filled.

[0054] At step 112 an optically transparent, electrically insulating solid filler material layer 164 is applied, such as by spinning, such that the tips of the nanowires 160 are covered. For one preferred embodiment, the filler layer 164 comprises a spin-coating material, such as spin-on glass (SOG) or cyclotene, that is applied to the top of the nanowire array and then spun on. Notably, a variety of different materials for the solid filler layer 164 and methods for achieving the result of step 112 are within the scope of the preferred embodiments. For example, the solid filler layer 164 can alternatively comprise one or more of Si oxides, Si nitrides, Al oxide, Al nitride, or other materials that are optically transparent and electrically insulating, and methods of application other than spinning such as spraying and injecting via inkjet could be used.

[0055] At step 114, the solid filler layer 164 is subject to a dry etch, such as with O2 plasma, so that most of the nanowires 160 jut outwardly from an outward surface of the solid filler layer 164 and are available to make good physical and electrical contact with a tip-side electrode layer. Since the nanowires 160 are less affected by the etching, their tip ends will look much like stubble or whiskers sticking out of the solid filler layer 164. The solid filler layer 164 may advantageously provide at least some degree of passivation of the nanowire surfaces.

[0056] At step 116, the temperature is again raised to 500-600 degrees Celsius and the InP precursor gases introduced into the chamber, this time in the presence of p-type dopants, to form a p+ type shell 166 around the tip ends of the nanowires 160 in a lateral non-catalytic growth process similar to that described above for step 108. Suitable dopants for step 116 include, for example, Zn and Mg for the case of InP nanowires. Notably, it is acceptable and can indeed be advantageous if some p-doping of the nanowire tip sections occurs during the lateral growth process of step 116. Moreover, it is also acceptable and can be advantageous, as shown in the progress drawing adjacent to box 116 of Fig. 1, for the p+ type shells 166 of adjacent nanowires 160 to merge together. Alternatively, there can be formed a p+ type layer using any of a variety of materials having a bandgap greater

than the 1.35 eV bandgap of InP, such as InGaP which has a bandgap of 1.82 eV. With reference back to step 108 and as illustrated by the dotted line in the progress drawing adjacent to box 116 of Fig. 1, it is also acceptable and can indeed be advantageous for the n+ type shells 162 to merge together during step 108. Note
5 that although the shells 166 are shown as connected in Fig. 1-2, there may be a gap between them, as shown by the dotted lines 199.

[0057] Finally, at step 118, a transparent conductive oxide layer (TCL) 168 is formed upon and around the p+ type shells 166, and grid-style metal electrode 170 is formed to complete a tip-side electrode for the overall PV nanowire structure. As
10 illustrated in Figs. 2A-2B, each PV nanowire structure takes on an overall shape similar to that of a dumbbell, by virtue of the p+ type shells 166 near the nanowire tip and the n+ type shell 162 near the nanowire root. The resultant PV nanowire-based device provides an advantageously optimized combination of good p-i-n photovoltaic properties, good root-side and tip-side electrode connectivity and
15 conductivity, mechanical and electrical stability, and amenability to roll-based fabrication methods.

[0058] Figs. 3A-C illustrate an alternative method of manufacture using a thin mask structure, according to some embodiments. One or more aspects of such embodiments may be further understood in view of selected background
20 references from the non-patent literature identified in the list that follows. The listed references, each of which is incorporated by reference herein in its entirety, are referenced further hereinbelow by their respective identifying numerals.

[0059] {13} Li, RR and Dapkus, D., et. al., “Dense arrays of ordered GaAs nanostructures by selective area growth on substrates patterned by block
25 copolymer lithography,” App. Phys. Lett. 76(13), pp. 1689-1691 (27 March 2000);

[0060] {14} Zhang, Y., et. al., “Patterned growth and field emission of ZnO nanowires,” Materials Letters 60, pp. 522-526 (2006);

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30 **[0062]** {16} Zhang, Y., et. al., “Selective-area growth and field emission properties of Zinc oxide nanowire micropattern arrays,” Physica B 382, pp. 76-80 (2006);

[0063] {17} Bauer, J., et. al., "GaAs nanowires grown by MOVPE," Phys. Status Solidi B 247, No. 6, 1294–1309 (2010); and

[0064] {18} Dalacu, et. al., "Selective-area vapour–liquid–solid growth of InP nanowires," Nanotechnology 20, 395602 (6 pp.) (2009).

5 **[0065]** Provided according to a preferred embodiment are methods for forming photovoltaic (PV) nanowire-based solar cells, along with the resultant solar cells themselves, based on the methods of the incorporated patent references, together with the selective area growth strategies of the references {13} - {18} above, but with certain key differences as set forth hereinbelow. As illustrated in Fig. 3A, there 10 is provided a short-range atomic order (SRAO) substrate 310, such as n-Si:H. In Fig. 3B, there is then provided a very thin mask layer of SiO2 (or other suitable oxide) 312 above the SRAO layer, a mask layer 312 is preferably so thin (for example, 2-5 nm) that it intrinsically contains a series of randomly and irregularly distributed, sized and shaped openings therethrough. The openings can 15 alternatively be called "holes" or "voids," and the mask layer can be called a "holey film." The SRAO layer is exposed through those openings, and is not exposed elsewhere. In Fig. 3C, the PV nanowire precursor gases are introduced into the chamber at a relatively high temperature as needed for non-catalytic growth (in comparison to catalytic growth), and the PV nanowires grow non-catalytically 20 through the random, irregular openings in the mask layer. The PV nanowires do not grow through the remaining mask areas, but rather only through the openings. The result is photovoltaic nanowires formed in spatially random clusters over the surface, as shown in Fig. 3C.

[0066] Stated differently, there is provided what it believed to potentially be a 25 better alternative to the patterned selective area growth (SAG) method of growing nanowires without using catalyst. In contrast to the Dapkus idea in which a dielectric pattern is provided over a crystalline surface, the nanowires growing through areas not covered by the dielectric, according to some embodiments, a very thin dielectric film with lots of "holes," such as SiO2 (say 3 to 10 nm thick or 30 so), is deposited to serve as a random pattern over crystalline or amorphous Si surface, and the nanowires will grow in areas not covered by the "holey" film.

[0067] Notably, the PV nanowires grown in this fashion could also be encouraged to grow laterally, by changing the growth temperature and other

conditions, so that all the nanowires could become fat. It is also possible that the fat nanowires could simply grow together to form a quasi-continuous layer or film. Again, the nanowires could be made of InP, GaAs, GaN and other III-V materials. Notably, according to some embodiments, the lateral growth techniques described
5 herein can be added to the ideas of the incorporated patent references above. There would be no need to deposit a larger catalyst grain. The nanowires could grow fat by changing the growth conditions and still have a tiny catalyst cap. The fat nanowires could again grow together to form a quasi-continuous film as described above.

10 **[0068]** A method of making III-V microwire solar cell modules compatible to silicon crystal modules will now be described, according to some embodiments. The modules can use minimally modified silicon crystal module manufacturing and handling equipment as well as fitting into the standard panels for silicon crystal modules. This is particularly important for cost and manufacturing yield
15 considerations.

[0069] Since approximately 80% of the solar cell modules are made of silicon crystal and the costs of such manufacturing and handling equipment are well designed and proven at a much lower cost than specialized equipment for typical thin-film solar cell modules. This cost advantage also applies to the standard
20 panels and mounting fixtures.

[0070] A typical silicon solar cell module is six-inch square (6”x6”), made from an eight-inch (8”) silicon wafer. It takes approx. 43 of these modules to add up to a square meter. Thus, each silicon crystal module typically delivers 3.5W or less. Whereas, each such size (6”x6”) III-V microwire solar cell module should deliver
25 7W. For a silicon crystal solar cell manufacturing plant of GW/year (one billion watt/year) capacity, it would have to produce 800,000 such 6”x6” modules per day x 360 days/year. If yield were 80%, then the daily run rate would be over one million modules per day.

[0071] According to one preferred embodiment, III-V microwire solar cells are
30 fabricated according to one or more of the methods described in the above-referenced applications that are incorporated by reference herein, with the additional constraint that they are made in discrete, individually manipulable plates or sections having unit sizes that correspond to the sizes of conventional silicon

crystal wafers. The III-V microwire solar cell units or plates are formed such that they can be “substituted” in place of the conventional silicon crystal wafers in a conventional solar cell module-making process, with only relatively minor modifications to that process. The result is solar panel modules that have the general look, feel, and applicability of conventional solar panels, except that they are advantageously based on III-V microwire-based solar cell technology instead of conventional silicon crystal wafers.

[0072] Thus, for example, according to one preferred embodiment, the III-V microwire solar cell module is made on (A) 6”x6” (or similar size as crystal silicon standards change) glass or other transparent substrate, or on (B) 6”x6” non-glass opaque or metal substrate. A manufacturing process has been disclosed in the above-referenced prior disclosures. A key is to be able to use standard multi-wafer silicon crystal module manufacturing and handling equipment with minimal modifications. This would substantially reduce the equipment costs for III-V microwire solar cell modules.

[0073] An additional benefit is the yield rate will be much higher than making a much larger module than 6”x6”, which most current thin-film solar cell manufacturers do. For example, Applied Material’s thin-film module was recently increased from 1.4 square meters to 5.7 square meters, which is respective equivalent to 60 to 245 times the size of 6”x6” modules. For example, if the yield of a 6”x6” module is 95%, then 1.4 and 5.7 square meter modules would have respective yield of (0.95)60 = 4.6% and (0.95)245 = 0.0003%. The yield is a very important cost factor, especially during the early years of the manufacturing ramp up period.

[0074] A method of forming solar energy conversion devices with III-V photo voltaic nanowires formed on <111> crystalline silicon substrates will now be described, according to some embodiments. The embodiments are related to the teachings of WO2011/025733A1, which is incorporated by reference herein in its entirety, and is more particularly directed to III-V photovoltaic (PV) nanowire-based solar energy conversion devices. Generally speaking, the many examples set forth in WO2011/025733A1 for the growth of PV nanowires and the formation of operable photovoltaic solar panels therefrom, including methods for PV nanowire stabilization and forming operable electrode structures suitable for field use, are

applicable for contexts in which the III-V PV nanowires are formed upon substrates whose surfaces exhibit long range atomic order, such as bulk crystalline wafer substrates. According to one embodiment, it is desirable to leverage the many teachings set forth in WO2011/025733A1 for PV nanowire-based solar cell formation for a particular context in which III-V PV nanowires are grown on a highly n-type (or p-type) doped <111> crystallographic plane of a silicon wafer.

[0075] One way is to grow the PV nanowires using gold catalyst on a highly n-type doped silicon's <111> crystallographic plane of the silicon wafer. The surface could optionally buffed, reactive etched, or slightly mechanically roughened to promote the initiation of growth. Since the growth is on same crystallographic plane, the nanowires will grow more parallel to each another, which is different from the more random orientation on growing on non-crystalline surfaces covered with a layer of amorphous silicon. The growth process could still be similar to that we disclosed for growing on non-crystalline surfaces, using MOCVD for example. After growth, we can do the same atomic layer deposition passivation, fill and etch back, and deposition of p-type Si, TCL, etc. at taught in WO2011/025733A1. Alternatively, we could also dope both ends of the nanowires, p-type and n-type, as we have disclosed before in the commonly assigned U.S. 61/381,930, *supra*.

[0076] Each of the following references discusses one or more aspects of growing III-V nanowires on crystalline silicon <111> substrates, and each of the following references is incorporated by reference herein in its entirety: Bao, X., et. al., "Heteroepitaxial Growth of Vertical GaAs Nanowires on Si (111) Substrates by Metal Organic Chemical Vapor Deposition," Nano Lett. 8 (11), 3755-3760 (2008); and Mi, Z., et. al., "III-V Compound Semiconductor Nanostructures On Silicon: Epitaxial Growth, Properties, And Applications In Light Emitting Diodes And Lasers," J. Nanophotonics, Vol. 3, 031602 (23 January 2009). According to one preferred embodiment, it is desirable to form the PV nanowires such that the i-region of each nanowire is at least 0.2 μm in length.

[0077] Certain cost advantages associated with using SRAO substrates (*e.g.*, compatibility with roll-based processes, etc.) are not shared for the currently disclosed embodiment of using silicon wafers as substrates for growing the III-V PV nanowires, and therefore the costs may be higher in comparison to growing on non-crystalline surfaces. However, since the III-V nanowire PV cell described

herein inherently has much higher conversion efficiency than crystalline silicon, the resultant cost per watt will still be lower than conventional photovoltaic cells made of crystalline silicon.

[0078] Methods for fabricating nanowire-based photovoltaic solar cells on roller-based substrate material will now be described, according to some embodiments. According to some embodiments, high-efficiency solar cells are fabricated on a continuous substrate, such as a roll-to-roll based substrate. According to some embodiments crystallized III-V based solar cells are fabricated on a flexible substrate, such as roll-to-roll based substrates. According to some embodiments, PV nanowire-based solar cells are fabricated on a continuous substrate, such as a roll-to-roll based substrate. According to some embodiments, single crystalline nanostructure-based solar cells are fabricated on a continuous substrate, such as a roll-to-roll based substrate.

[0079] Aspects of the currently disclosed embodiments may be more thoroughly understood in view of the following references, each of which is incorporated by reference herein in its entirety: {19} Goto, et. al., "Growth of Core-Shell InP Nanowires for Photovoltaic Application by Selective-Area Metal Organic Vapor Phase Epitaxy," Applied Physics Express 2, 035004-1-3 (2009); {20} U.S. Patent No. 7,608,530; {21} PCT International Patent Application No. PCT/US10/46334; {22} U.S. Patent No. 7,608,530, issued October 27, 2009 to Kobayashi and Wang, entitled "Hetero-Crystalline Structure and Method of Making Same"; {23} Singh and Hartnagel, "Reduction in Surface Charge Density By New GaAs Passivation Method," J. Phys. D: Appl. Phys., Vol. 8, pp. L42-L43 (1975); and {24} Pern and Glick, "Accelerated Exposure Tests of Encapsulated Si Solar Cells and Encapsulation Materials," National Center for Photovoltaics Program Review Meeting, Denver, Colorado, Sept. 8-11, 1998, NREL/CP-520-25361 (October 1998).

[0080] Fig. 4 illustrates a cross-sectional view of a PV nanowire-based solar cell, according to some embodiments. PV nanowire-based solar cell 402 (PV nanowire-based photovoltaic energy conversion device) includes an array of PV nanowires 404. More specifically, for a preferred embodiment of Fig. 4, the array of PV nanowires 404 is sandwiched between a root-side electrode 407 and a tip-side electrode 415. The root-side electrode 407 includes an SRAO layer 410 (for

example, n-type amorphous hydrogenated silicon or a-Si:H) and a metallic layer 408 (for example, molybdenum or aluminum). The root-side electrode 407 is disposed upon a continuous substrate 406, which according to some embodiment is stainless steel. According to some embodiments, substrate 406 is taken from a
5 roll and cell 402 is manufactured on substrate 406 as part of a roll manufacturing process. According to some embodiments, the substrate 406 is electrically conductive, and can be considered as part of the root-side electrode. Tip-side electrode 415 comprises a layer 416 of an optically transparent electrically conductive material, such as an optically transparent electrically conductive
10 semiconductor material including p-type a-Si:H, and a transparent conductive layer (TCL) 418. Although the PV nanowires 404 are shown as having rectangular cross-sections, they can likewise have a nanoneedle character, without departing from the scope of the preferred embodiments. According to some embodiments, a solid layer 414 of transparent insulating filler material is disposed in the space
15 between the root-side electrode 407 and tip-side electrode 415, but it does not fill all of the air space among the PV nanowires 404, whereby there is an air gap layer 412 disposed between an inwardly facing surface 414i of the solid filler layer 414 and the root-side electrode 407. The tip ends of the PV nanowires 404 jut outwardly beyond an outwardly facing surface 414o of the solid filler layer 414 into
20 physical and electrical contact with the tip-side electrode layer 415.

[0081] The design of Fig. 4 can be advantageous in reducing the adverse effects, such as absorption, heating, and darkening over time, that would be brought about by an insulator material that fully extends over the lengths of the PV nanowires, while at the same time providing good lateral stabilization of the PV
25 nanowires and providing a stable platform upon which to fabricate the tip-side electrode layers of the device. Additionally, by the juttable extension of the tip ends of the PV nanowires 404 beyond the outwardly facing surface 414o of the solid filler layer 414 and well into the material of the tip-side electrode layer 415, superior electrical contact with the tip-side electrode layer 415 is achieved for
30 promoting superior overall performance.

[0082] According to some embodiments, the air gap 412 occupies at least twenty-five percent of the vertical space between the solid filler layer 414 and the root-side electrode 407. For another preferred embodiment, the air gap 412

occupies at least fifty percent of the vertical space between the solid filler layer 414 and the root-side electrode 407. For another preferred embodiment, the air gap 412 occupies at least seventy-five percent of the vertical space between the solid filler layer 414 and the root-side electrode 407. Notably, in view of the material characteristics of the solid filler layer 414 (optically transparent, electrically insulating), it is not required that the air gap 412 be provided over one hundred percent of the lateral extent of the root-side electrode 407, because the device would still be substantially operable in the event there is contact between portions of the solid filler layer 414, although the advantages of the air gap would not be enjoyed at those contact locations. Accordingly, some drooping or sagging of the solid filler layer 414 toward the root-side electrode 407 as may occur during device fabrication, including some areas of contact therebetween that are not statistically overwhelming relative to the overall lateral extent of the device, may be acceptable.

[0083] According to some embodiments, each of the PV nanowires 404 is intrinsically doped along all or substantially all of its length between the root-side electrode 407 and tip-side electrode 415, with a photovoltaic cell being formed by virtue of the p-doped layer 416 at the tip end and the n-doped layer 410 at the root end. For this preferred embodiment the nanowire array 404 acts as the i-region, that is, each PV nanowire 404 is an i-region along its entire length. As used herein, i-region refers to a semiconductor region that is an intrinsically doped semiconductor region, or a semiconductor region that is not intentionally doped, as contrasted with p-region or p-doped region (intentionally p-doped) and n-region or n-doped region (intentionally n-doped). According to some other embodiments, the tips of the PV nanowires 404 can be doped of a similar type as the corresponding electrode. For embodiments having an opaque substrate 406 such as in Figs. 4-5, the light photons enter the device from the top (tip-side) through the transparent conductive layer (TCL) 418, then through the thin (10 to 20 nm) transparent p-type electrode layer 416, and then to the array of PV nanowires 404. TCL 418 can comprise a transparent conductive oxide, such as ITO (indium tin oxide), or alternatively any of a variety of different materials known to be both conductive and transparent, preferably with more than 80% light transmission. It is to be appreciated that it is within the scope of the preferred embodiments for the described doping configurations to be reversed, for example, for the p-type

electrode layer (and p-type nanowire tips) to be at the root side of the device of Fig. 4 and n-type electrode layer (and n-type nanowire tips) to be near the tip side of the device. According to some embodiments, the cell 402 includes a protective glass layer 420 on top (*i.e.*, on the tip-side of the PV nanowire-based solar cell 5 device).

[0084] Fig. 5 illustrates some fabrication steps of the device of Fig. 4 according to some embodiments. According to these embodiments stainless steel substrate 506 in a continuous form such as a roll is used. At step 552, the stainless steel surface can be textured or roughened, which will increase light trapping by allowing 10 the incident light photons to back-reflect. When the PV nanowires to be grown will have high aspect ratios (greater than 20:1, for example), they will generally be naturally light trapping and so the texturing of the substrate may be less beneficial. However, when the PV nanowires to be grown will be short and stubby according to some embodiments (less than 20:1, for example), they may be less naturally 15 light-trapping and therefore it will be more beneficial to texturize the stainless steel surface as in step 552.

[0085] At step 554, the stainless steel surface is sputtered or evaporation coated with a layer of metal 408 such as molybdenum or aluminum or other metals, the layer 408 thus also facilitates bottom electrode (root-side electrode) 20 functionality in conjunction with the n-type electrode layer 410. The metal layer 408, on the textured substrate surface, could also reflect back into the nanowire array any transmitted photons. Also at step 554, the electrode layer 410 of n-type a-Si:H is deposited, for example by PECVD (plasma enhanced chemical vapor deposition). Also at step 554, the PV nanowires 404 are grown, such as by 25 MOCVD (metal organic chemical vapor deposition) or CVD (chemical vapor deposition) outwardly from the electrode layer 410 with or without the need of catalysts, using for example one or more techniques discussed in U.S. Patent No. 7,608,530. The nanowires grown by such technique could allow for the design of PV nanowire arrays with better geometry. According to some embodiments, the 30 PV nanowires 404 should have a diameter in the range of 100 to 500 nm. Broader ranges, such as 20 to 1000 nm are also usable. One particularly important feature is the cross-sectional aspect ratio of the PV nanowires 404 (ratio of length to root cross-sectional dimension). For better performance, lower aspect ratios are more

desirable, preferably in the range of 1:1 to 20:1, which is in contrast to known prior art PV nanowire aspect ratios that are much larger than 20:1.

[0086] At steps 556-558, the layer 414 of optically transparent, electrically insulating solid filler material is formed that laterally surrounds the PV nanowires 404 along a portion of their lengths, wherein the forming is carried out such that (i) the air gap 412 remains between the root-side electrode 407 and an inwardly facing surface 414i of the solid filler layer 414, and (ii) the tip ends of the PV nanowires 104 are juttedly exposed beyond an outwardly facing surface 414o of the solid filler layer 414. At step 556, the optically transparent, electrically insulating solid filler material is applied, such as by spaying or injecting via inkjet. For one preferred embodiment, the filler material comprises a spray-coating material, such as spray-on glass, that is applied to the top of the PV nanowire array via one or more sprayer heads. Note that according to some preferred embodiments, the filler material is sprayed on such that the air gap 412 remains. At step 558, the solid filler layer 414 is subject to a dry etch, such as with O_2 plasma, so that most of the PV nanowires 404 jut outwardly from the outward surface 414o of the solid filler layer 414 and are available to make good physical and electrical contact with the tip-side electrode layer 415. Since the PV nanowires 404 are less affected by the etching, their tip ends look much like stubble or whiskers sticking out of the solid filler layer 414.

[0087] Notably, a variety of different materials for the solid filler layer 414 and methods for achieving the result of steps 556-558 are within the scope of the preferred embodiments. For example, the solid filler layer 414 can alternatively comprise one or more of Si oxides, Si nitrides, Al oxide, Al nitride, or other materials that are optically transparent and electrically insulating. According to some embodiments, the depth space between the PV nanowires is left partially unfilled, thereby leaving the air gap 412. In this way, the filler material will not absorb substantial amounts of the incident photons before reaching the i-region of the PV nanowires. An optically transparent, electrically insulating filler material that is somewhat phobic to the PV nanowires so that it does not “wet” well to the nanowires may be preferred. Advantageously, upon completion of step 558, the outwardly facing surface 414o of the solid filler layer 414 is available as a stable platform for the formation of the tip-side electrode layers 416 and 418. As used

herein, the term “layer” should not be construed as limiting such item to a single material, but rather a layer recited herein such as the solid filler layer 414, the passivation layer 656 (in Fig. 6), root-side electrode layer 407, or tip-side electrode layer 415 can comprise multiple sublayers of different materials.

5 **[0088]** At step 560, for this preferred embodiment, a p-type layer 416 of amorphous Si:H is deposited on the outwardly facing surface 414o of the solid filler layer 414 by a PECVD process. Finally, at step 562, the TCL 418 (transparent conductive layer) is deposited. There are a number of well-known materials that can be used for the TCL 418 that are suitable in photovoltaic cells, such as SnO
10 (tin oxide), indium-tin oxides (ITO), ZnO, etc., as well as non-oxide materials that are substantially conductive and substantially transparent.

[0089] In another preferred embodiment as will be discussed further *infra*, before forming the solid filler layer 414, an atomic layer of Si oxide or Al oxide is deposited onto the nanowires to coat the PV nanowires using atomic layer
15 deposition method for passivating the surfaces of the PV nanowires and increasing overall efficiency.

[0090] Presented by way of example, and not by way of limitation, are typical dimensions and materials for the various layers of the PV nanowire-based solar cell 402 of Fig. 4. The metal layer 408 will typically be greater than 100 nm thick
20 and comprise a metal and/or metallic alloy such as Mo, Cr, NiSi, etc. The n-electrode layer 410 will typically be n-type a-Si:H (B doped a-Si-H, etc.) having a thickness greater than 50 nm. The PV nanowires 404, which have the preferred dimensions and aspect ratios described *supra*, can comprise Group IV, II-VI, or III-V semiconductors and related alloys. For one preferred embodiment, the
25 nanowires 404 will have lengths and diameters of about 10 nm or greater, again so as preferably to keep their aspect ratios low to make their surface area to volume ratios low. The p-electrode layer 416 will typically have a thickness greater than 10 nm and may comprise wide bandgap non-single-crystal semiconductors such as p-type a-Si:H, p-type mc-Si:H, p-type SiC, etc. The TCL 418 will typically have a
30 thickness greater than about 500 nm and will preferably comprise a wide bandgap transparent semiconductor (ITO, ZNO, etc.). The PV nanowire-based solar cell 402 will also comprise a mesh-style electrode layer (not shown in Fig. 4) atop the TCL 418, the mesh-style electrode layer being optimally designed to provide

electrical connectivity to the various areas of TCL 418, while at the same time not covering too much lateral area so as to allow most of the incident light to pass through to the TCL 418 and the underlying layers.

[0091] Fig. 6 illustrates fabrication of a PV nanowire-based solar cell according to some embodiments. At step 602, PV nanowires 652 are formed upon a continuous substrate 654, such as stainless steel from a roll source. The substrate 654 includes a root-side electrode structure (not shown) including an SRAO surface (not shown) similar to those described above from which the PV nanowires 652 are grown, these elements being omitted from the present description for clarity of disclosure. PV nanowires amenable to passivation methods according to one or more of the preferred embodiments can be formed upon substrates that exhibit long-range atomic order, substrates having SRAO material surfaces, or other suitable substrates.

[0092] At step 604, the PV nanowires 652 are passivated by forming a passivation layer 656 (which may itself comprise multiple individual passivation layers) on each individual PV nanowire 652. The passivation layer 656 can be formed using methods including, but not limited to, atomic layer deposition. Atomic layer deposition can be particularly advantageous for randomly oriented ensembles of nanowires with high aspect ratio for which conventional chemical vapor deposition may not be sufficiently functional. Atomic layer deposition will provide conformal deposition that uniformly covers complicated geometrical surfaces resulting from randomly oriented ensembles of nanowires. Suitable materials for the passivation layer 656 include, but are not limited to, aluminum oxide, tin oxide, titanium oxide, silicon oxide and certain nitrides. In one preferred embodiment for which the PV nanowires 652 are formed from InP material, the passivation process comprises depositing a thin layer of SiO_2 on the PV nanowires 652 by placing the assembly in an atomic layer deposition reactor and introducing two precursors containing silicon and oxygen that react spontaneously even at room temperature. Prior to the deposition of a passivation layer, the surfaces of the PV nanowires 652 could be chemically pretreated to saturate dangling bonds on the surface. For instance, a process that employs chemicals that contain sulfur using ammonium sulfide was found very effective way to reduce adverse surface effects as described in Iyer, R., “Sulfur as a Surface Passivation for InP,” Appl. Phys. Lett. 53

(2) (1988), which is incorporated by reference herein in its entirety. However, an ensemble of nanowires is inherently hydrophobic, thus a surface treatment based on solution will not work as uniformly on all nanowires within an ensemble. Instead, it is more preferable to place a small amount of solid sulfur in atomic layer
5 deposition reaction chamber during the deposition of a passivation layer. The sulfur pretreatment process serves to protect, or at least stabilize, the surface of the PV nanowires 652 against thermal degradation during the deposition of a passivation layer.

[0093] Subsequent to the passivation of the PV nanowires 552 at step 604, the
10 remainder of the solar cell fabrication process can proceed according to one or more methods described above with respect to Fig. 5. The remainder of steps of Fig. 6 are similar to the latter steps of the fabrication method of Fig. 5 that results in the device of Fig. 4. At step 606, a layer of substantially transparent insulating filler material 658 is applied, preferably in a manner that leaves an air gap 660. At step
15 608, the filler layer 658 is subject to a dry etch, such as with O_2 plasma. Since the PV nanowires 652 are less affected by the dry etch, the appearance is much like whiskers sticking out of the transparent insulating filler 658. Advantageously, a significant longitudinal portion of the PV nanowires 652 are now available to make electrical contact with the top layers, rather than just the top tips of the PV
20 nanowires. In addition to etching back the filler material 658, the dry etch step 608 should also serve to etch back the passivation layer 656 above the surface of the filler material 658 so to expose the tips and upper sidewalls of the PV nanowires 652, to facilitate electrical contact with the subsequently applied p-type layer of amorphous Si:H. At step 612, the p-type layer 662 of amorphous Si:H is deposited
25 on the filler layer by PECVD process. Advantageously, by virtue of the etching step 608, a better ohmic contact is established between each PV nanowire 652 and the a-Si:H layer 662, since the a-Si:H layer 662 now can make substantial contact with the upper side walls of the PV nanowires 652 rather than just the very tips of the PV nanowires 652. Finally, at step 614, a transparent conductive layer
30 664 (*e.g.*, comprising tin oxide, indium-tin oxides, zinc oxide, or other substantially conductive and substantially transparent material) is formed above the Si:H layer 662.

[0094] Conventional uses of a passivation layer on a semiconductor surface is rather passive in the sense that electronic states associated with the presence of a surface are inactivated so that they do not contribute to the electrical transport properties of bulk semiconductor underneath the surface. In contrast, within our
5 frame work of passivation of PV nanowires, we explicitly control the electrical transport properties of PV nanowires by tuning the electronic structures established between a passivation layer and a semiconductor surface.

[0095] Explicit control of the electronic structures can be established between a passivation layer and a semiconductor surface by controlling, for instance,
10 bandgap of a passivation layer or the density of built-in ionized impurities in a passivation layer, which can be very advantageous for PV nanowires. Unlike a semiconductor surface that exists on a bulk semiconductor that has infinite thickness, the diameter of a nanowire is very small, thus an electronic band that deforms at the surface of a nanowire can be interacted inside of a nanowire. As a
15 result, photo-generated excess electron and holes can be confined either near the center of a nanowire or near the surface of a nanowire. The band bending at the surface of a nanowire can be intentionally controlled by, for instance, having a passivation layer contain either negatively or positively charged ions.

[0096] In the PV structure that employs PV nanowires described hereinabove,
20 all nanowires in an ensemble of nanowires have a built-in electric field parallel to the long axis of nanowires, thus, charged carriers confined near the center of a nanowire can be swept away by drift without getting scattered at the surface of a nanowire while charged carriers confined near the surface of a nanowire will be swept away by drift in quasi-two dimensional channel (i.e., two-dimensional
25 electron or hole gas), which improves overall PV properties.

[0097] The term “micro-wires” or “microwires” can be used to refer to the PV nanowires 652 where their root dimensions approach the order of hundreds of nanometers.

[0098] Fig. 7 is a block diagram showing stations of a continuous substrate roll
30 manufacturing process for fabricating PV nanowire-based solar cells, according to some embodiments. According to some embodiments, each station has the same length and the process is carried out at each station while the substrate is stationary. Following a set amount of time, for example 5 minutes, the processes

at each station are complete and the substrate is advanced and stopped such that the portion of substrate that was processed by the previous station is aligned for processing at the following station. Through this start-stop process of indexed advancements, the PV nanowire based solar cells are fabricated on a continuous
5 substrate such as rolled stainless steel.

[0099] At station 710, the root side electrode is deposited. Station 710 corresponds to part of step 554 in Fig. 5 in which a layer of metal such as molybdenum or aluminum or other metals form a part or all of the root side electrode. According to some embodiments, the processing temperature is about
10 250°C. Prior to station 710, a pre-heating station may be used to raise the temperature from room temperature to close to 250°C. At station 712 an amorphous silicon, for example n-type, is formed via a PECVD process at approximately 250°C, which also corresponds to part of step 554 in Fig. 5.

[00100] At station 714, the substrate is actively cooled in preparation for the
15 application of micro-particles used as a catalyst for nanowire growth. The active cooling can be, for example, by convection with a gas such as helium gas and/or conduction such as with cooling rollers as will be described in further detail herein. At station 716, a catalyst material such as gold or titanium is deposited at a large number of spots, with each spot being a location at which a nanowire will be grown.
20 According to some embodiments, gold suspended in a suitable organic solvent is sprayed on the substrate so as to uniformly distribute the nano particles of gold. According to some embodiments, the spray on catalyst can be performed at about 150°C. At station 718, the substrate is heated in preparation for the nanowire growth process. Heating can be carried out, for example using convection,
25 conduction via heated rollers as is described in further detail herein and/or radiation such as with IR lamps as is known in rapid thermal annealing processes.

[00101] At station 720, the nanowires are grown at temperatures of about 450°C. Station 720 corresponds with part of step 554 in Fig. 5 and with step 602 in Fig. 6. Precursor gases, including the elements or compounds that will form the
30 nanowires, are introduced into a chamber. Under the influence of the catalyst, the precursor gases at least partially decompose into their respective elements, some of which are transported on or through the catalyst in liquified phase to the immediately underlying solid surface provided by the substrate. At each spot, a

nanowire epitaxially grows outwardly from the substrate as the process proceeds, the catalyst at each spot remaining at the tip of the nanowire and rising away from surface of the substrate as the nanowire grows. The resultant nanowires exhibit a long-range atomic order (i.e., single-crystal) that can potentially be exploited for a variety of different useful applications.

[00102] By way of example, the VLS synthesis process can be carried out in a metalorganic chemical vapor deposition (MOCVD) process, which is sometimes alternatively termed a metalorganic vapor phase epitaxy (MOVPE) process, an organometallic vapor phase epitaxy (OMVPE) process, or an organometallic chemical vapor deposition (OMCVD) process. Exemplary precursors for InP nanowires can be trimethylindium ($(CH_3)_3In$) and phosphine (PH_3). During a first phase of nanowire growth corresponding to the root region, n-type doping can be achieved during the MOCVD process by introducing an Si-containing gas, such as silane (SiH_4), or other suitable n-dopant. During a second phase of nanowire growth corresponding to the intrinsic region, no dopants would be introduced. During a third root region phase of nanowire growth corresponding to the tip region, p-type doping can be achieved during the MOCVD process by introducing a metalorganic vapor containing Zn, or other p-type dopants such as Be in a Be-containing metalorganic vapor. In other preferred embodiments, the PV nanowires can comprise another III-V material such as GaAs, together with suitable associated complementary dopants for the root and tip ends.

[00103] A variety of different material systems and doping schemes for the PV nanowires are generally within the scope of the preferred embodiments. According to some embodiments, the root ends of the PV nanowires correspond to the n-doped side of the device, while the tip ends correspond to the p-doped side of the device.

[00104] It has been found particularly advantageous for the PV nanowires to comprise high-purity intrinsic InP along most or all of their vertical height (length). Thus, according to some embodiments, in which these InP nanowires have root diameters in the range of 400 nm – 750 nm, aspect ratios in the range of 2.0 – 5.0, and therefore nanowire lengths in the range of 0.8 μm – 3.75 μm, high-purity intrinsic InP extends along most or all of the 0.8 μm – 3.75 μm length of the nanowire. The photovoltaic character of the overall device is provided by virtue of

the tip-side p-i junctions formed with the p-doped a-Si:H layer at the tip end, and the root-side i-n junctions formed with the n-doped a-Si:H layer at the root end.

[00105] At station 722, the substrate is actively cooled in preparation for the application of the passivation layer. The active cooling can be, for example, by convection with a gas such as helium gas and/or conduction such as with cooling rollers as will be described in further detail herein. At station 724, a passivation layer of a material such as aluminum oxide, tin oxide, titanium oxide, silicon oxide or other nitride is applied via atomic layer deposition. The passivation layer can be deposited, using atomic layer deposition at range of temperatures from about room temperature to about 400°C. According to some embodiments a temperature of about 250°C so as to minimize the need to heat and/or cool the substrate in subsequent processing steps. Station 724 corresponds with step 604 in Fig. 6.

[00106] At station 728, the substrate is heated or cooled in preparation for the application of the filler layer. At station 730, the filler material is applied preferably using a spray-coating material, such as spray-on glass. The filler material is uniformly applied to the top of the PV nanowire array via one or more sprayer heads in station 730. Station 730 corresponds to step 556 in Fig. 5 and to step 606 in Fig. 6. The liquid used in station 730 can be similar or identical to known spin-on glass formulations. However, due to the highly viscous nature of many such liquids, a higher application temperature is preferred when spraying on rather than spinning on the glass. According to some embodiments, filler material may be applied at a temperature of about 250°C so as to lower the viscosity of the filler material and also to minimize the need to heat and/or cool the substrate in subsequent processing steps. At station 732, the substrate is heated or cooled in preparation for the etching step. Note that in the case where stations 724, 730 and 734 are all carried out at close to 250°C, the additional heating/cooling stations 728 and 732 can be eliminated. At station 734, the filler layer is subject to a dry etch, such as with O2 plasma, at approximately 250°C. Station 734 corresponds to step 558 in Fig. 5 and to step 608 in Fig. 6.

[00107] At station 736, a p-type layer of amorphous Si:H is deposited on the solid filler layer by a PECVD process at approximately 250°C. Station 736 corresponds to step 560 in Fig. 5 and to step 612 in Fig. 6. At station 738, the TCL (transparent conductive layer) is deposited at approximately 250°C. There are a

number of well-known materials that can be used for the TCL that are suitable in photovoltaic cells, such as SnO (tin oxide), indium-tin oxides (ITO), ZnO, etc., as well as non-oxide materials that are substantially conductive and substantially transparent. Station 738 corresponds to step 562 in Fig. 5 and to step 614 in Fig. 6. At station 740, a metal layer is sputter deposited to create one or more metal electrodes on the tip side. Since the metal electrode will block light from entering the cell, the shape of the metal should be designed, such as a grid-pattern, so as to minimize the amount of surface area covered.

[00108] Figs. 8A-B schematically illustrate roll-based continuous substrate manufacturing processes for PV nanowire-based solar cells, according to some embodiments. In Fig. 8A, the roll-based fabrication line 800 is shown that includes a large continuous substrate 842 that passes through a number of processing stations such as those described with respect to Fig. 7. According to some embodiments, substrate 842 is thin stainless steel that is sourced from source roll 850. According to some embodiments substrate 842 is 1 meter wide and about 5 km long. According to some embodiments, each processing station processes about 1 square meter of substrate material in a stop-start fashion. The processing stations, such as stations 810, 812, 814, 838 and 840 are housed within respective housings to provide the environment (e.g. pressure, temperature and gasses) used for the particular process carried out at the station. For example, station 810, which corresponds to station 710 in Fig. 7, is used to sputter deposit the root side electrode layer at about 250°C; station 812, which corresponds to station 712 in Fig. 7 is used to form an amorphous silicon layer via a PECVD process at approximately 250°C; station 814, which corresponds to station 714 in Fig. 7 is used to actively cool the substrate 842 in preparation for the application of micro-particles used as a catalyst for the nanowire growth; station 538, which corresponds to station 738 in Fig. 7, is used deposit the TCL (transparent conductive layer) at approximately 250°C; and in station 840, which corresponds to station 740 in Fig. 7, a metal layer is sputter deposited to create one or more metal electrodes.

[00109] In Fig. 8A, the fabricated solar cells are collected on a roll 870. In the case of Fig. 8B, the fabricated solar cells are cut using cutter 880 into sheets corresponding to the size of the processing stations. In the example of each

processing station covering a 1m x 1m are of the substrate 842, for example, the cut size of sheets 882 is also 1m x 1m.

[00110] According to some embodiments, one or more buffer chambers 860 are used to collect any gases that may have leaked from the individual processing
5 stations. The buffer chambers, such as buffer chamber 860, can be used to (1) recycle escaped gasses for subsequent use; and/or (2) collect gases for subsequent treatment to decrease the likelihood of a hazardous gas escaping into the environment. A number of rollers are provided at the entrances and exits of each processing station and to the buffer chamber(s) so as to provide sufficient
10 impedance for gas leakage, and to prevent cross-contamination as will be described in further detail herein. The upper rollers are preferably made from a soft elastic material having low hardness so as not to damage the formed structures (e.g. the nanowires) during the fabrication process, and appropriate temperature resistance for the processes being carried out.

15 **[00111]** When operating in a start-stop processing arrangement, the stationary time allowed for processing at each station should be set according to the most time consuming process. In one example, the MOCVD nanowire growth station, such as station 720 in Fig. 7, is the most time consuming station and uses about 5 minutes. In this example, the substrate is advanced by 1 meter plus the distance
20 between the stations and then stopped for 5 minutes, then advanced and then stopped for 5 minutes, and so on. In the case where fabrication line 800 uses a 1 meter wide substrate and 1 meter long processing stations, the throughput is approximately:

$$\frac{1\ \text{meter}^2}{5\ \text{min}} \times 60\frac{\text{min}}{\text{hr}} \times 24\frac{\text{hr}}{\text{day}} \times 365\frac{\text{days}}{\text{year}} \cong 100{,}000\,\text{m}^2/\text{year}$$

25 Assuming in this example, 1 square meter generates about 200 watts for 20% efficiency at 1000 watts/square meter, such a line would produce about 20 Megawatts / Year. According to some embodiments, a wider substrate media could be used, such as 2 meters wide, and the processing stations could be 2 meters long, which would produce 4 square meters per 5 minutes equaling about
30 80MW per year.

[00112] According to some embodiments, a continuous process could be used instead of a start-stop process.

[00113] Fig. 9 is diagram schematically illustrating a heating and/or cooling station, according to some embodiments. In Fig. 9, a heating station 918 is used to raise the temperature of the substrate 942 from the liquid spray catalyst stage 916 to the MOCVD nanowire growth stage 920. According to these embodiments,
5 heated rollers such as rollers 910 are used to heat the substrate using conduction. the rollers can be heated for example via electric resistance coils and/or by passing heated liquid through portions of the rollers. According to some embodiments, the same type of arrangement of rollers could be used for cooling the substrate 942 via conduction in which case the rollers are cooled for example by passing a cool liquid
10 through portions thereof.

[00114] Figs. 10A-B show cross sections of a processing chamber having a moveable lid, according to some embodiments. Processing station 1000 has an upper lid 1010 and a lower housing 1012. A start-stop process is used to fabricate PV nanowire-based solar cells on a continuous substrate 1042. The substrate
15 1042 is held flat in part by rollers within the chamber such as roller 1030. The portion of the substrate 1050 is where the solar cells are being fabricated. In between processing stages, when the substrate is being advanced, the moveable lid 1010 is raised by a distance d, as shown in Fig. 10A. During processing at station 1000, the lid 1010 is lowered to contact the substrate 1042 such that the
20 processing chamber is relatively air tight between the walls of the lid 1010 and lower rollers 1020 and 1022. In this way, very little gas will escape from the chamber during processing. Prior to raising the lid 1010, the chamber can be flushed such that contaminating gases can be removed. Note that in a start-stop fabrication method, fabrication only takes place in some locations on the substrate,
25 such as location 1050, so that contact by the wall portions of the lid 1010 will not damage any structures being fabricated.

[00115] Fig. 11 is a cross section of a processing chamber having high impedance wall section, according to some embodiments. Processing station 1100 has a wall 1110 that forms a processing chamber 1102 with slots on the left and
30 right sides for entry and exit of a continuous substrate 1142 on which solar cells are fabricated. The substrate 1142 is held flat in part by rollers within the chamber such as roller 1130. Gas communication between the chamber 1102 and the outside 1104, which could be still within a buffer chamber, is controlled by contact

rollers 1120 and 1122 and wall sections 1112 and 1114. Wall sections 1112 and 1114 have a width ***w*** and a distance ***d*** from the surface of the substrate 1142 such that there is sufficient impedance for gas communication between the chamber 1102 and the outside 1104. According to some embodiments, station 1100 is used
5 in a start-stop fabrication process. However, according to some embodiments, station 1100 is used in a continuous processing method in which the substrate 1142 is continuously advanced without stopping.

[00116] Fig. 12 is a cross section of a processing chamber having double rollers, according to some embodiments. Processing station 1200 has a wall 1210 that
10 forms a processing chamber 1202 with slots on the left and right sides for entry and exit of a continuous substrate 1242 on which solar cells are fabricated. The substrate 1242 is held flat in part by rollers within the chamber such as roller 1230. Gas communication between the chamber 1202 and the outside 1204, which could be still within a buffer chamber, is controlled by contact rollers 1220, 1222, 1260
15 and 1262. The upper rollers 1260 and 1262 are preferably made from a soft elastic material having low hardness so as not to damage the formed structures (e.g. such as the nanowires) during the fabrication process, and appropriate temperature resistance for the processes being carried out. According to some embodiments, station 1200 is used in a start-stop fabrication process. However, according to
20 some embodiments, station 1200 is used in a continuous processing method in which the substrate 1242 is continuously advanced without stopping.

[00117] Fig. 13 is a plan view of a processing station used to spray on nanowire catalyst material, according to some embodiments. The processing station 1300 corresponds, for example, to station 716 in Fig. 7 and is used for uniformly
25 depositing a catalyst material such as gold or titanium is at a large number of spots on substrate 1342, with each spot being a location at which a nanowire will be grown. Processing chamber 1302 is defined by chamber wall 1310 and gas communication between the chamber 1302 and the outside, which could be a buffer chamber, is controlled by rollers such as rollers 1320 and 1322. The area
30 1344 on continuous substrate 1342 is where the PV solar cells are being fabricated. A spray assembly 1330 includes a wide spray head 1332 that is made up of a large number of nozzles. According to some embodiments, the nozzles are similar to inkjet nozzles used in inkjet technology. During operation, the spray

assembly 1330 is translated across fabrication area 1344 (as denoted by the arrows and small dotted lines in Fig. 13) such that the liquid spray, and therefore the suspended nano particles of catalyst material, is uniformly deposited across the area 1344.

5 **[00118]** According to some embodiments, a processing station similar to that shown in Fig. 13 is used for depositing spray on glass. In such embodiments, the nozzles 1332 in head 1330 are dimensioned and spaced according to the viscosity of the liquid being deposited.

[00119] Fig. 14 schematically illustrates a large area discrete substrate 10 manufacturing process for PV nanowire-based solar cells, according to some embodiments. Fabrication line 1400 is similar to line 800 shown in Figs. 8A and 8B except that prior to processing, the substrate is cut into discrete pieces corresponding to the size of the processing stations. For example, according to some embodiments, the processing stations 1410, 1412, 1414, 1438 and 1440 are 15 all 1meter x 1meter format, and the discrete substrate pieces, such as piece 1442, 1444, and 1446 are also 1m x 1m.

[00120] Fig. 15 illustrates a structure that includes a lightly n-doped PV nanowire and a more heavily doped p-type tip-side electrode material, according to some embodiments. Instead of an intrinsic PV nanowire, as described herein according 20 to some other embodiments, the PV nanowire 1510 is intentionally lightly doped n-type (e.g. n^- type) on an n-type substrate 1520. For example, the n-type doping of PV nanowire 1510 can be intentionally doped to an impurity level in the range of 10^{14} to 10^{16} per cubic centimeter. A heavily p+ type cap 1530 is formed, which can be p+ or p++ type doping. Due to heavily doped p-type cap 1530, the tip region 25 1512 of the nanowire becomes p-type. Furthermore, a depletion region 1514 is caused in the lightly doped PV nanowire due to field strength and the relative doping levels. The depletion region 1514, can range in size, for example, from 0.2 microns to 3 microns. According to some embodiments, a depletion region of about 1 micron in height can result from an PV nanowire intentionally doped to an 30 impurity level of about 10^{16} per cubic centimeter. According to some embodiments, lightly-doped PV nanowires such as the one shown in Fig. 15 can be combined with the other teachings and techniques as described herein.

[00121] Although the description herein is directed primarily to PV nanowires made of III-V compound semiconductors such as InP, the scope of the present teachings is not necessarily so limited. More generally, the PV nanowires can be composed of various combinations of elemental and compound semiconductors
5 optimized for different spectrum ranges in the solar spectrum. The elemental semiconductors include silicon ("Si") and germanium ("Ge"), and compound semiconductors include group III-V and II-VI materials (the Roman numerals III and V representing elements in the group IIIa and Va on the periodic table). Compound semiconductors can be composed of group IIIa elements, such as
10 Aluminum ("Al"), Gallium ("Ga"), and Indium ("In"), in combination with group Va elements, such as Nitrogen ("N"), Phosphorus ("P"), Arsenic ("As"), and Antimony ("Sb"). Compound semiconductors can be classified according the relative quantities of III and V elements. By way of example, binary compound semiconductors include GaAs, InP, InAs, GaN, and GaP; ternary compound
15 semiconductors include $GaAs_yP_{1-y}$, where y ranges between 0 and 1; and quaternary compound semiconductors include $In_xGa_{1-x}As_yP_{1-y}$, where both x and y independently range between 0 and 1. Other types of suitable compound semiconductors include II-VI materials, the Roman numerals II and VI representing elements in group IIb and VIa on the periodic table. By way of example, CdSe,
20 ZnSe, ZnS, and ZnO are examples of binary II-VI compound semiconductors.

[00122] In the case of using a stainless steel substrate or other non-transparent substrate, it is beneficial to optimize the filler layer, the dry etch to expose a large percentage of the micro-wires, the deposition of the a-Si layer to provide a p-type (or n-type) junction, and finally the TCL layer to optimize conductivity and optical
25 transmissivity.

[00123] According to some embodiments, a protective encapsulation on the light incident side is provided, which consists of a sun-resistant transparent overcoat of polymer. See, for example, Pern and Glick, “Accelerated Exposure Tests of Encapsulated Si Solar Cells and Encapsulation Materials,” National Center for
30 Photovoltaics Program Review Meeting, Denver, Colorado, Sept. 8-11, 1998, NREL/CP-520-25361 (October 1998), which is incorporated by reference herein in its entirety.

[00124] Whereas many alterations and modifications of the present invention will no doubt become apparent to a person of ordinary skill in the art after having read the foregoing description, it is to be understood that the particular embodiments shown and described by way of illustration are in no way intended to be considered
5 limiting. By way of example, in another preferred embodiment, the i-region portion of each nanowire can be made very short, and the device can be operable as a light-emitting diode (LED) rather than a photovoltaic energy generation device. Therefore, reference to the details of the preferred embodiments is not intended to limit their scope.

10

What is claimed is:

1. A method for fabricating a photovoltaic energy conversion device, comprising:

5 providing a substrate including a substrate surface layer doped in a first dopant type;

growing a plurality of photovoltaic (PV) nanowires outwardly from the substrate surface layer, each PV nanowire having a root end near said substrate surface layer and a tip end opposite said root end;

10 forming a layer of collar material that laterally surrounds and is in contact with the PV nanowires along at least a rootward portion of their lengths, the collar material doped in the first dopant type; and

forming a tip-side doped material doped in a second dopant type, the tip-side doped material in contact with said tip ends of the PV nanowires.

15

2. A method according to claim 1 wherein the layer of collar material is grown in a lateral direction from the PV nanowires.

3. A method according to claim 1 further comprising forming a layer of

20 optically transparent, electrically insulating solid filler material that laterally surrounds the PV nanowires along an outward portion of their lengths.

4. A method according to claim 1 wherein the first dopant type is n-type and second dopant type is p-type.

25

5. A method according to claim 1 wherein the first dopant type is p-type and second dopant type is n-type.

6. A method according to claim 1 wherein the collar material is in

30 contact with the substrate surface layer.

7. A method according to claim 1 wherein a longitudinal p-i-n junction is associated with each PV nanowire.

8. A method according to claim 1 wherein said growing of PV nanowires is partially carried out before said forming of the collar material and partially carried out after said forming of the collar material.

5 9. A method according to claim 8 wherein a gap between 0.2 microns and 5 microns is formed between an outward-most portion of the collar material a rootward most portion of the tip-side material.

10. A method according to claim 9 wherein said gap is between 0.2
10 microns and 2 microns.

11. A method according to claim 1 wherein the PV nanowires are not intentionally doped.

15 12. A method according to claim 1 wherein the PV nanowires have impurity levels less than 10^{17} per cubic centimeter.

13. A photovoltaic energy conversion device fabricated according to the method of claim A1.

20

14. A photovoltaic energy conversion device comprising:

a substrate including an electrically conductive substrate surface layer doped in a first dopant type;

a plurality of photovoltaic (PV) nanowires extending outwardly from
25 the substrate surface layer, each PV nanowire having a root end near said substrate surface layer and a tip end opposite said root end, said substrate surface layer forming at least a portion of a root-side electrode layer of the device;

a collar material laterally surrounding the PV nanowires along at least
30 a rootward portion of their lengths, the collar material doped in the first dopant type; and

a tip-side electrode material doped in a second dopant type, the tip-side electrode material being in contact with said tip ends of the PV nanowires.

5 15. A device according to claim 14 further comprising a layer of optically transparent, electrically insulating solid filler material laterally surrounding the PV nanowires along an outward portion of their lengths.

16. A device according to claim 14 wherein a longitudinal p-i-n junction is 10 associated with each PV nanowire.

17. A device according to claim 14 wherein a gap between 0.2 microns and 5 microns is formed between an outward-most portion of the collar material a rootward most portion of the tip-side material.

15

18. A device according to claim 14 wherein the PV nanowires are not intentionally doped.

19. A method for fabricating a photovoltaic energy conversion device, 20 comprising:

providing a substrate including an n-doped substrate surface layer;

growing a plurality of n-doped photovoltaic (PV) nanowires outwardly from the substrate surface layer, each PV nanowire having a root end near said substrate surface layer and a tip end opposite said root end;

25 forming a layer of optically transparent, electrically insulating solid filler material that laterally surrounds the PV nanowires along a portion of their lengths; and

forming a tip-side p-doped material in contact with said tip ends of the PV nanowires.

30

20. A method according to claim 19 wherein said tip-side p-doped material is p+ type doped.

21. A method according to claim 19 wherein said tip-side p-doped material is p++ type doped.

22. A method according to claim 19 wherein said n-doped PV nanowires
5 and said tip-side p-doped material form radial and longitudinal p-n junctions.

23. A method according to claim 19 wherein said n-doped PV nanowires are intentionally lightly doped n- type to an impurity level of between 10^{14} to 10^{16} per cubic centimeter.
10

24. A method according to claim 19 wherein a depletion region within each n-doped PV nanowire is formed of between 0.2 and 3.0 microns in longitudinal distance.

15 25. A photovoltaic energy conversion device fabricated according to the method of claim C9.

26. A method for fabricating a photovoltaic energy conversion device, comprising:
20 providing a 6” by 6” square substrate including a substrate surface layer;

growing a plurality of photovoltaic (PV) nanowires outwardly from the square substrate surface layer, each PV nanowire having a root end near said substrate surface layer and a tip end opposite said root end;
25 forming a layer of optically transparent, electrically insulating solid filler material that laterally surrounds the PV nanowires along a portion of their lengths; and

forming a tip-side electrode upon said outwardly facing surface of the solid filler layer in contact with said tip ends of the PV nanowires.
30

27. A method according to claim 26 wherein said forming the layer of optically transparent material is carried out such that an air gap remains between the substrate surface layer and an inwardly facing surface of the solid filler layer.

28. A method according to claim 26 wherein said forming the layer of optically transparent material is carried out such that the tip ends of the PV nanowires are juttedly exposed beyond an outwardly facing surface of the solid
5 filler layer.

29. A photovoltaic energy conversion device fabricated according to claim 26.

10 30. A method for fabricating a photovoltaic energy conversion device, comprising:

providing a substrate including a substrate surface layer;

forming a mask layer on the substrate surface layer, the mask having a plurality of spaced apart voids such that portions of the substrate surface
15 layer are exposed at the locations of the voids;

growing a plurality of photovoltaic (PV) nanowires outwardly from said exposed portions of the substrate surface layer, each PV nanowire having a root end near said substrate surface layer and a tip end opposite said root end;

20 forming a layer of optically transparent, electrically insulating solid filler material that laterally surrounds the PV nanowires along a portion of their lengths; and

forming a tip-side electrode upon said outwardly facing surface of the solid filler layer in contact with said tip ends of the PV nanowires.

25

31. A method according to claim 30 wherein the voids are located randomly within the mask layer.

32. A method according to claim 30 wherein the mask layer is within a
30 thickness range of 3 to 10 nm.

33. A photovoltaic energy conversion device fabricated according to claim 30.

34. A method for fabricating a photovoltaic energy conversion device, comprising:

providing a substrate including a long range atomic order (LRAO) substrate surface layer;

growing a plurality of n-doped photovoltaic (PV) nanowires outwardly from the LRAO substrate surface layer, each PV nanowire having a root end near said substrate surface layer and a tip end opposite said root end;

forming a layer of optically transparent, electrically insulating solid filler material that laterally surrounds the PV nanowires along a portion of their lengths; and

forming a tip-side electrode upon said outwardly facing surface of the solid filler layer in contact with said tip ends of the PV nanowires.

35. A method according to claim 34 wherein the substrate is a bulk crystalline wafer substrate.

36. A method according to claim 34 wherein the PV nanowires are III-V PV nanowires, and the LRAO substrate surface layer is a highly n-type doped <111> crystallographic plane of a silicon wafer.

37. A method according to claim 36 wherein a gold catalyst is formed upon said a highly n-type doped <111> crystallographic plane of the silicon wafer.

38. A photovoltaic energy conversion device fabricated according to claim 34.

39. A method for fabricating a photovoltaic energy conversion device, comprising:

providing a roller-based substrate material including a substrate surface layer;

growing a plurality of photovoltaic (PV) nanowires outwardly from the square substrate surface layer, each PV nanowire having a root end near said substrate surface layer and a tip end opposite said root end;

forming a layer of optically transparent, electrically insulating solid filler material that laterally surrounds the PV nanowires along a portion of their lengths; and

forming a tip-side electrode upon said outwardly facing surface of the solid filler layer in contact with said tip ends of the PV nanowires.

40. A method according to claim 39 wherein a plurality of fabrication stations are used, each station being adapted to completing a process upon a fixed length of the roller-based substrate material within a predetermined amount of time.

41. A method according to claim 39 wherein the method includes actively cooling the substrate material using rollers.

42. A method according to claim 39 wherein the method includes actively heating the substrate material using rollers.

43. A method according to claim 39 wherein the filler material is applied using a spray-coating process.

44. A method according to claim 39 wherein the roller based substrate material is at least about 1 meter wide.

45. A photovoltaic energy conversion device fabricated according to claim 39.

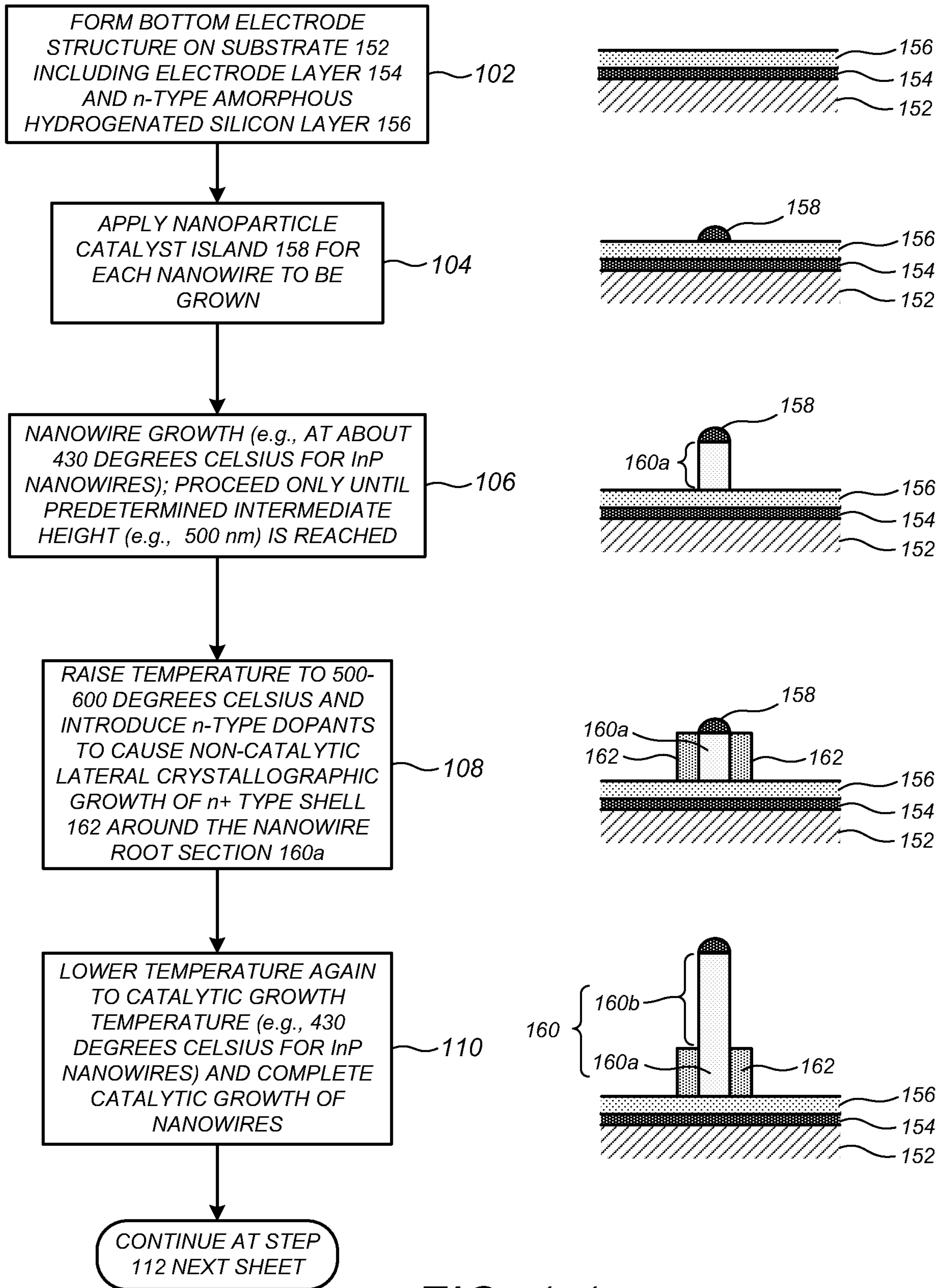

FIG. 1-1

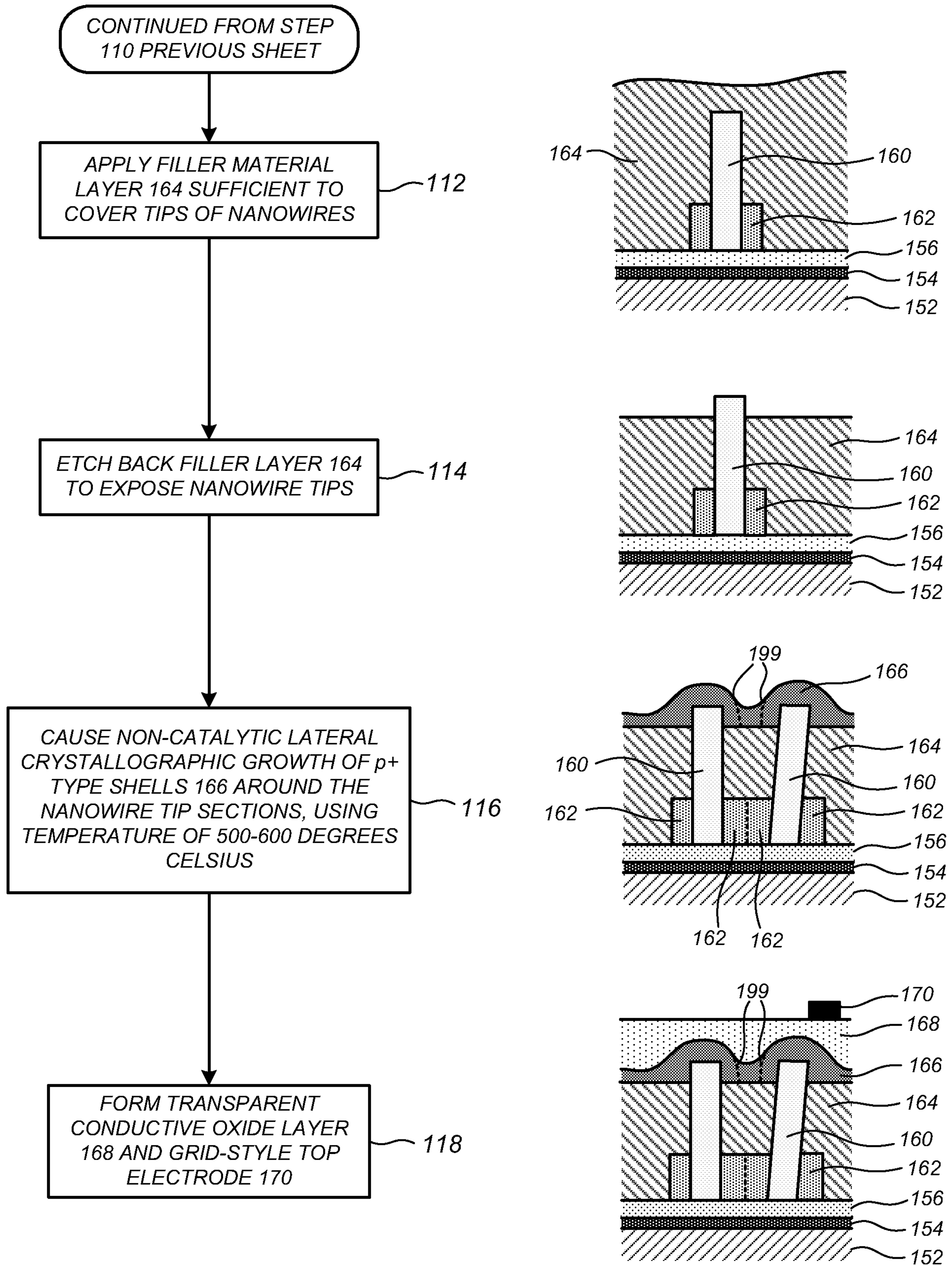

FIG. 1-2

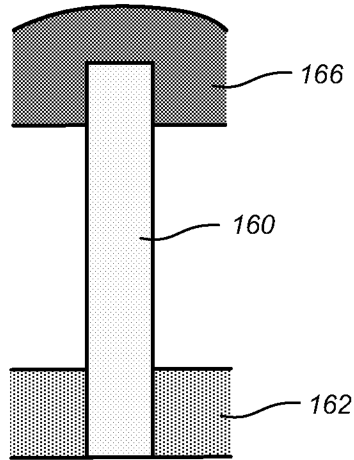

FIG. 2A

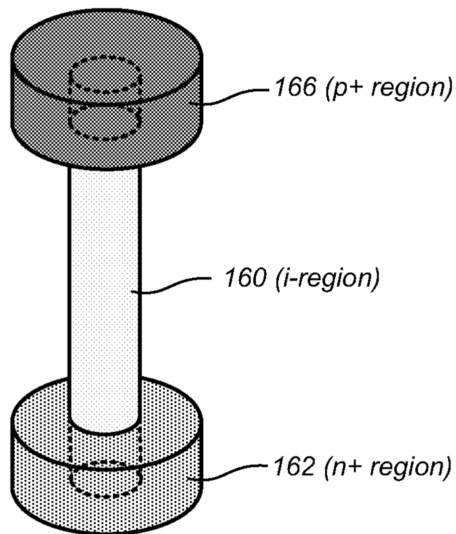

FIG. 2B

STEP 1: FORM LAYER OF n-TYPE AMORPHOUS Si

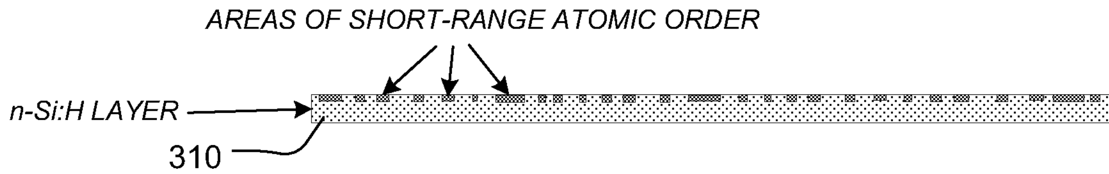

FIG. 3A

STEP 2: FORM VERY THIN MASK LAYER OF SiO2 (OR OTHER OXIDE)

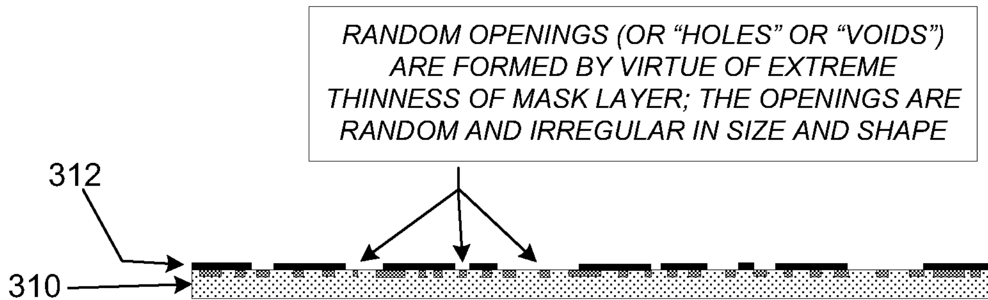

FIG. 3B

STEP 3: INTRODUCE NANOWIRE PRECURSOR GASES AT HIGH TEMPERATURE TO GROW NANOWIRES THROUGH THE RANDOM, IRREGULARLY SHAPED MASK LAYER OPENINGS

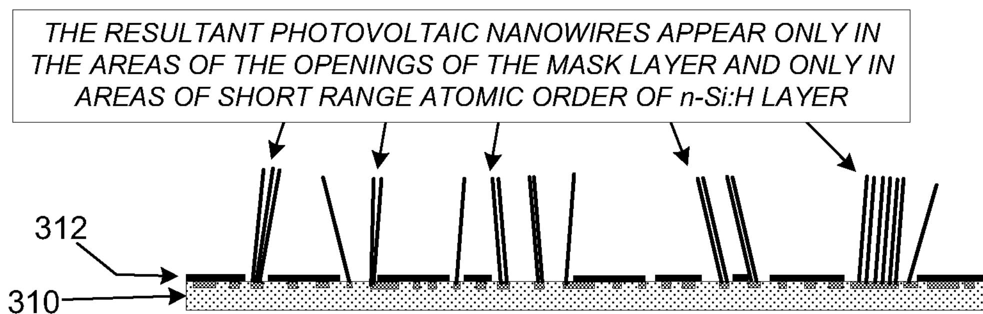

FIG. 3A

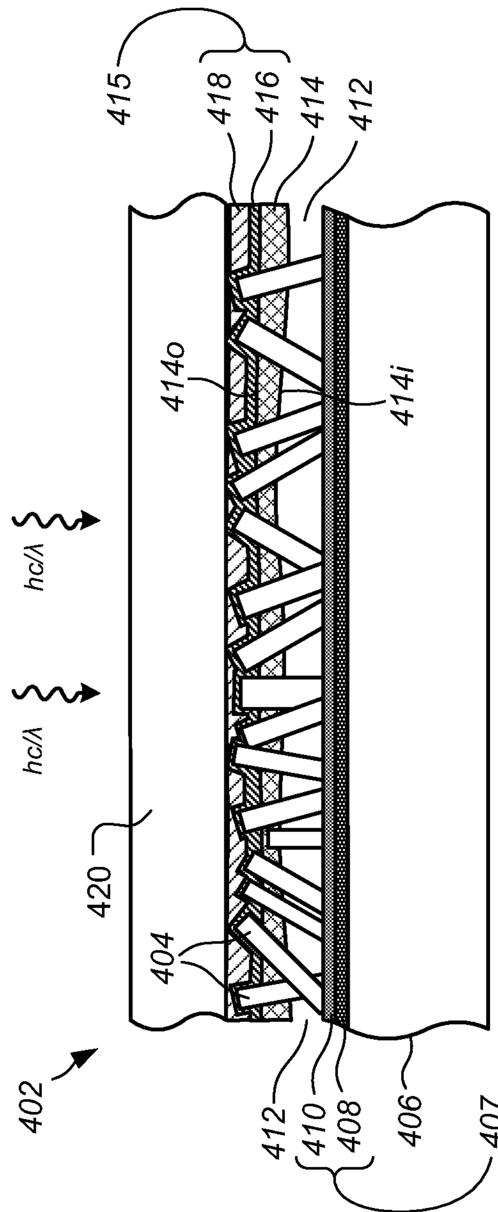

FIG. 4

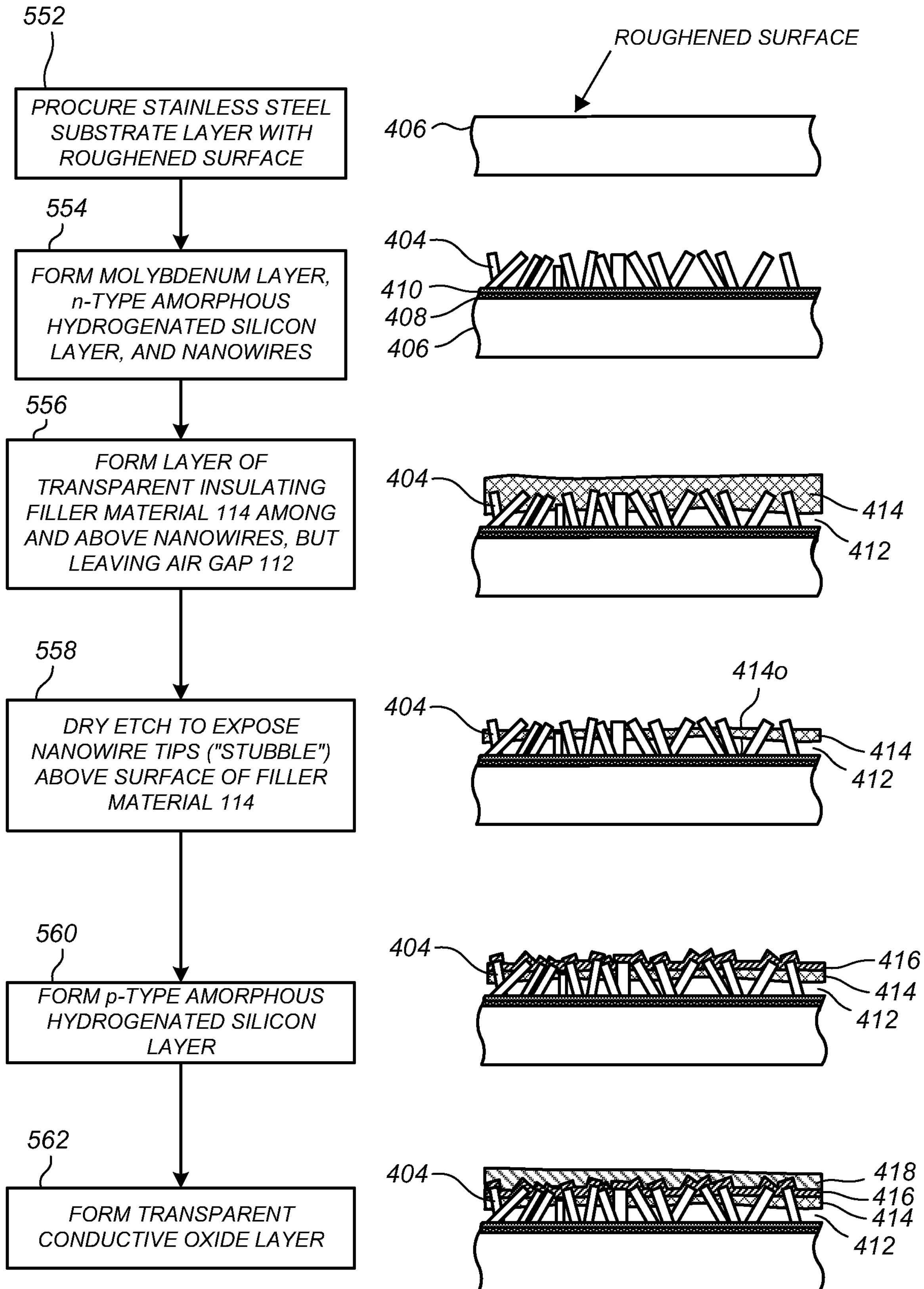

FIG. 5

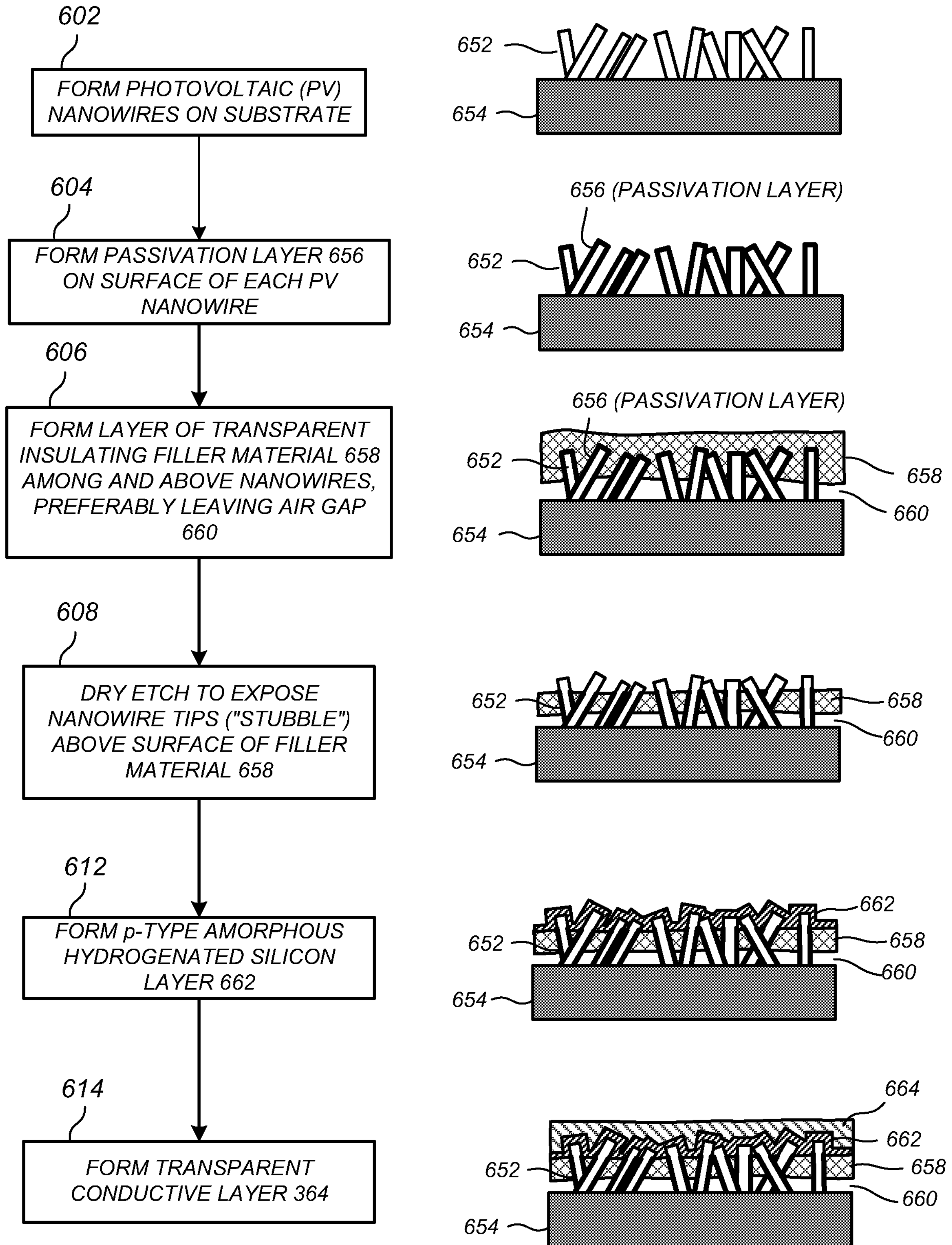

FIG. 6

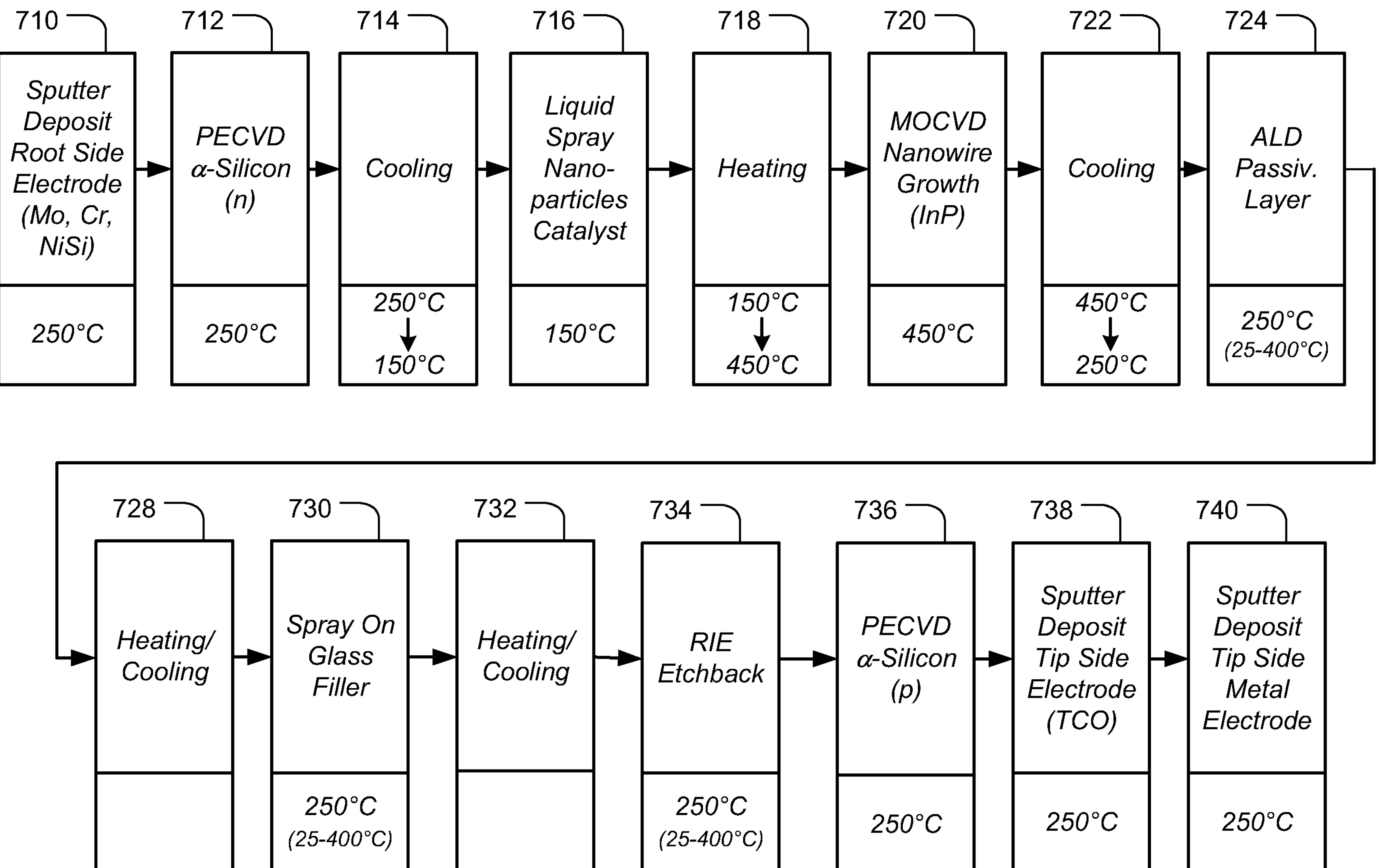

FIG. 7

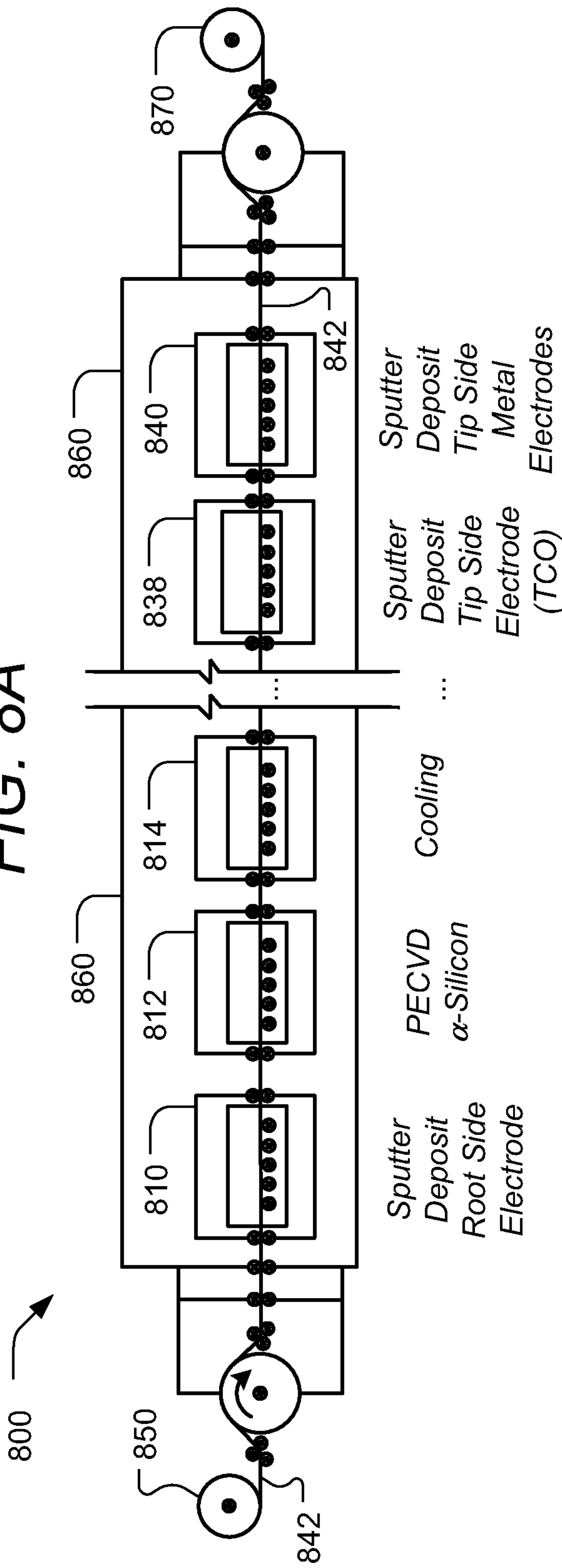

FIG. 8A

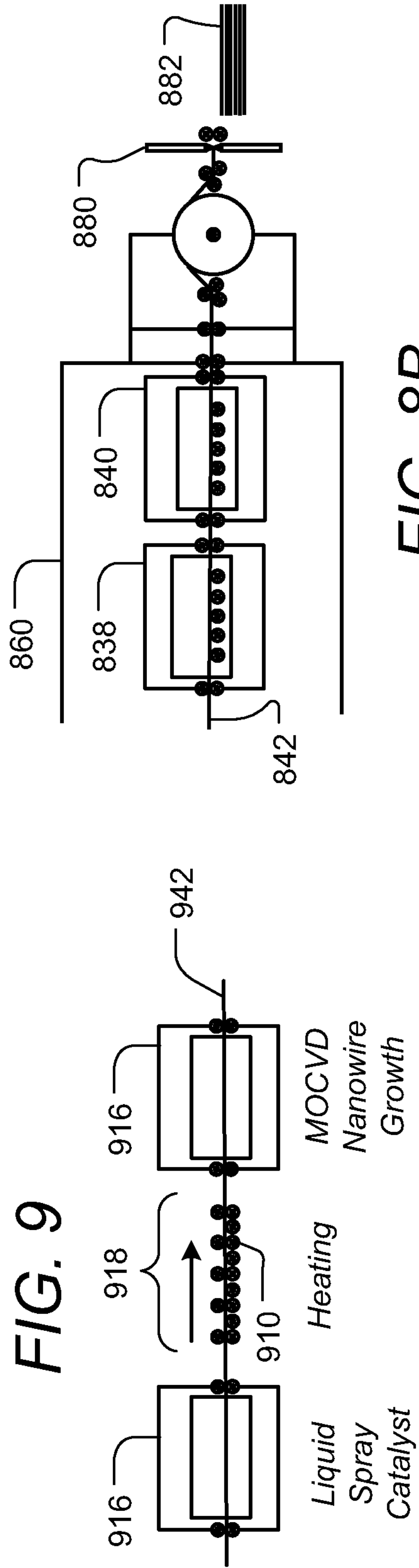

FIG. 8B

FIG. 9

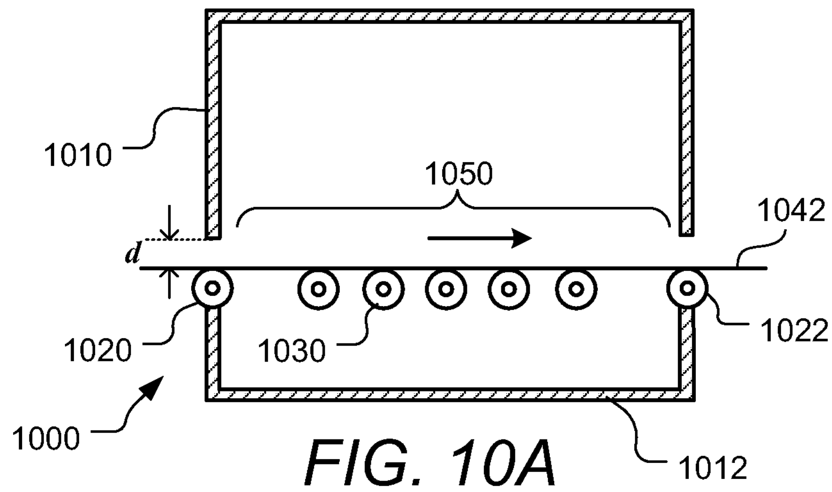

FIG. 10A

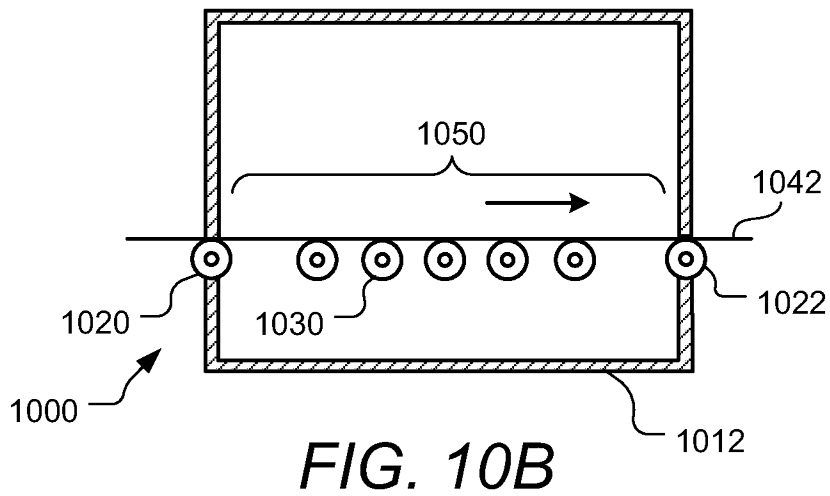

FIG. 10B

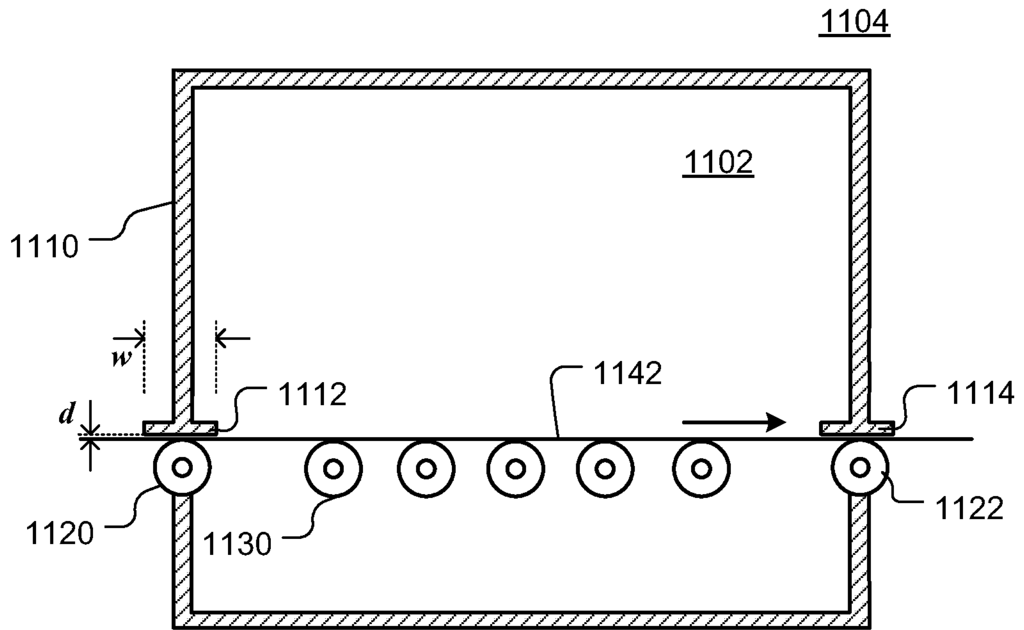

FIG. 11

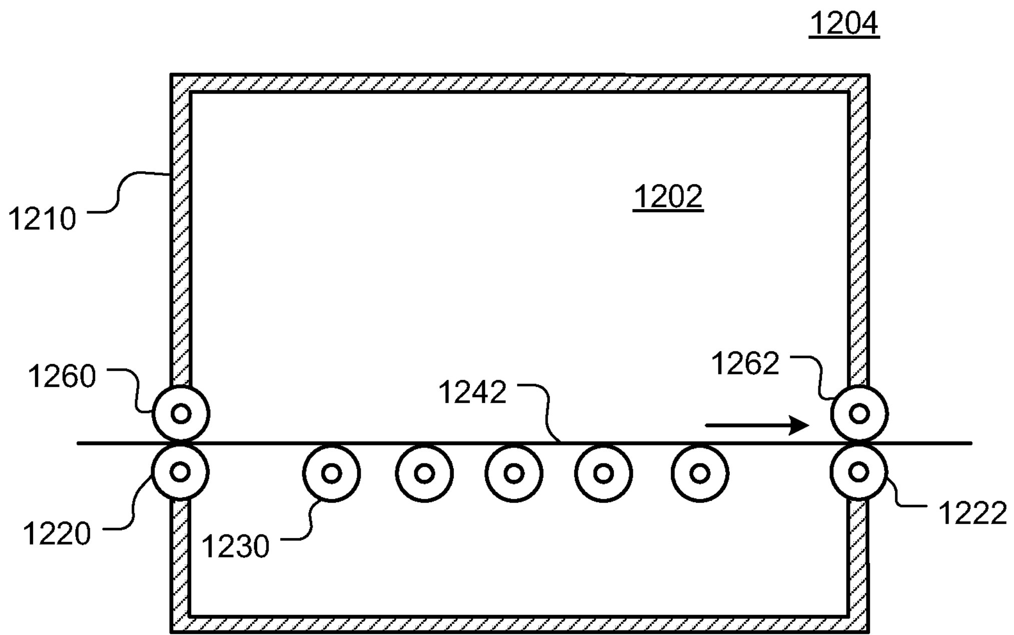

FIG. 12

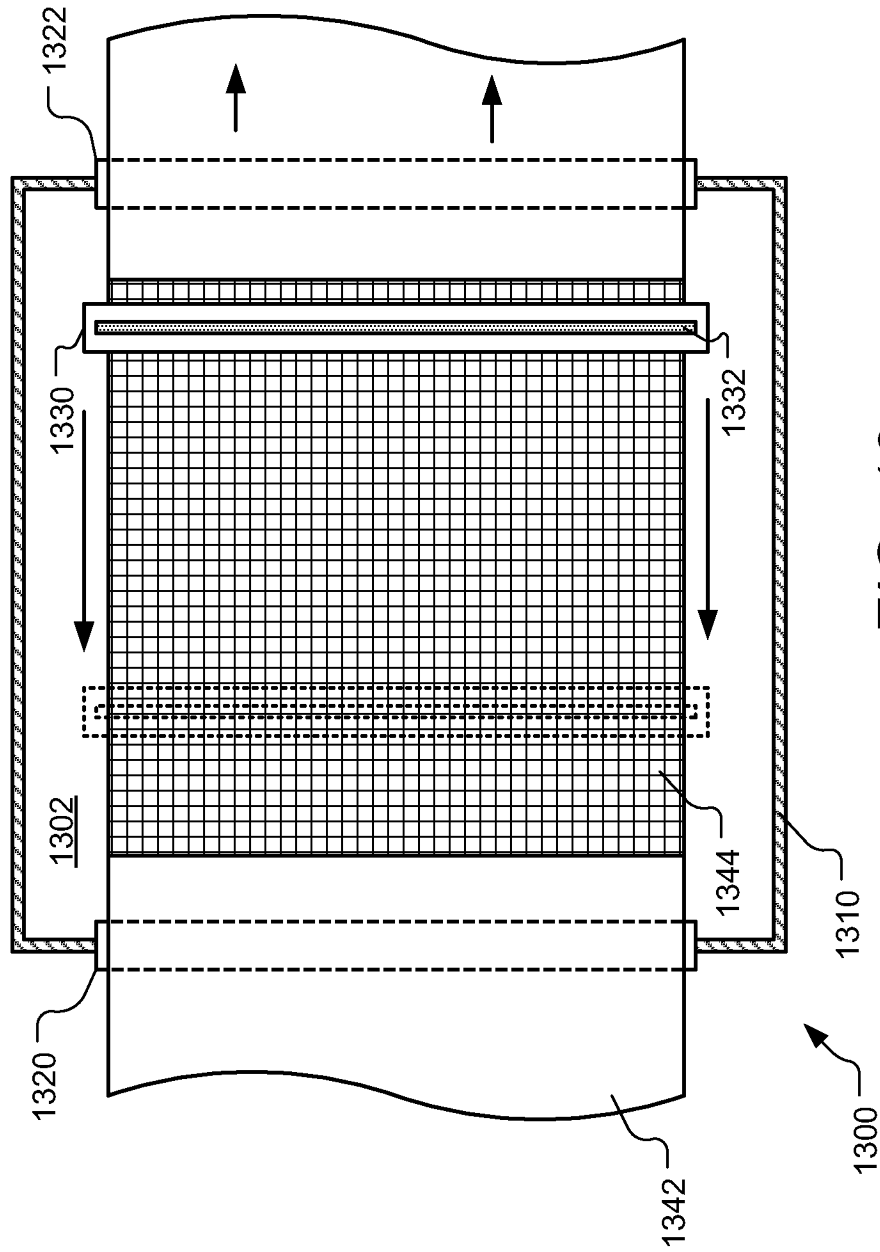

FIG. 13

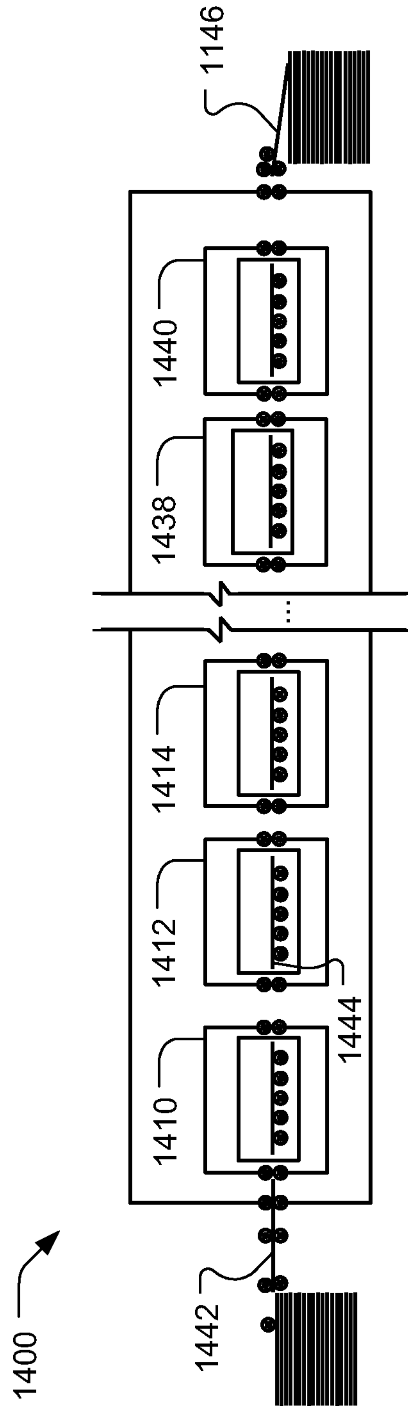

FIG. 14

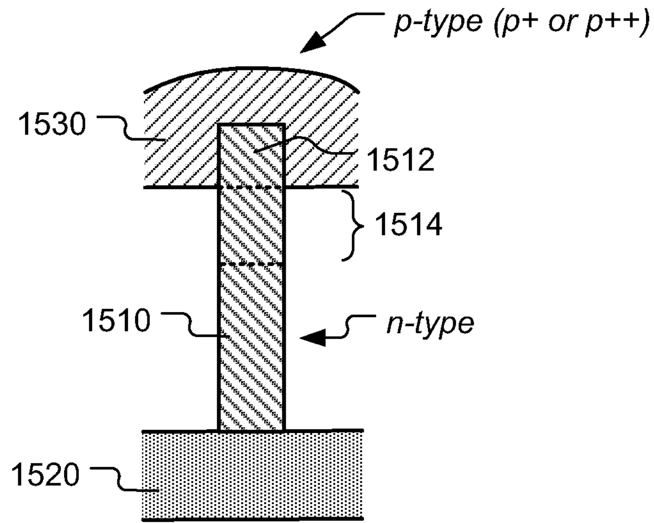

FIG. 15

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2011/051091

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - H01L 31/00 (2011.01)
USPC - 136/255
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8) - H01L 31/00, H01L 31/042, and H02N 6/00 (2011.01)
USPC - 136/244, 136/251, and 136/255

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent, Google Patent, and ACM

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2008/0047604 A1 (KOREVAAR et al) 28 February 2008 (28.02.2008) entire document	1-45
Y	US 2010/0193768 A1 (HABIB) 05 August 2010 (05.08.2010) entire document	1-45
Y	US 2010/0197068 A1 (POON et al) 05 August 2010 (05.08.2010) entire document	9-10 and 17
Y	US 2009/0267049 A1 (CHO et al) 29 October 2009 (29.10.2009) entire document	11, 18, 20-21
Y	US 2010/0126548 A1 (JANG et al) 27 May 2010 (27.05.2010) entire document	12
Y	US 2008/0102582 A1 (TAKEI) 01 May 2008 (01.05.2008) entire document	23, 30-33
Y	US 7,115,971 B2 (STUMBO et al) 03 October 2006 (03.10.2006) entire document	24
Y	US 2008/0265449 A1 (MEINDERS et al) 30 October 2008 (30.10.2008) entire document	32
Y	US 2007/0190434 A1 (SUDA) 16 August 2007 (16.08.2007) entire document	26-29
Y	US 2009/0188557 A1 (WANG et al) 30 July 2009 (30.07.2009) entire document	34-38
Y	US 2008/0265449 A1 (HEIDARI) 25 September 2008 (25.09.2008) entire document	39-45

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"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
09 December 2011	23 DEC 2011

Name and mailing address of the ISA/US	Authorized officer:
Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Blaine R. Copenheaver PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774