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(72) Inventeurs/Inventors:
WU, YIFENG, US;
ZHANG, NAIQIAN, US;
XU, JIAN, US;
MCCARTHY, LEE, US

(73) Propriétaires/Owners:
THE REGENTS OF THE UNIVERSITY OF CALIFORNIA, US;
CREE, INC., US

(74) Agent: OYEN WIGGS GREEN & MUTALA LLP

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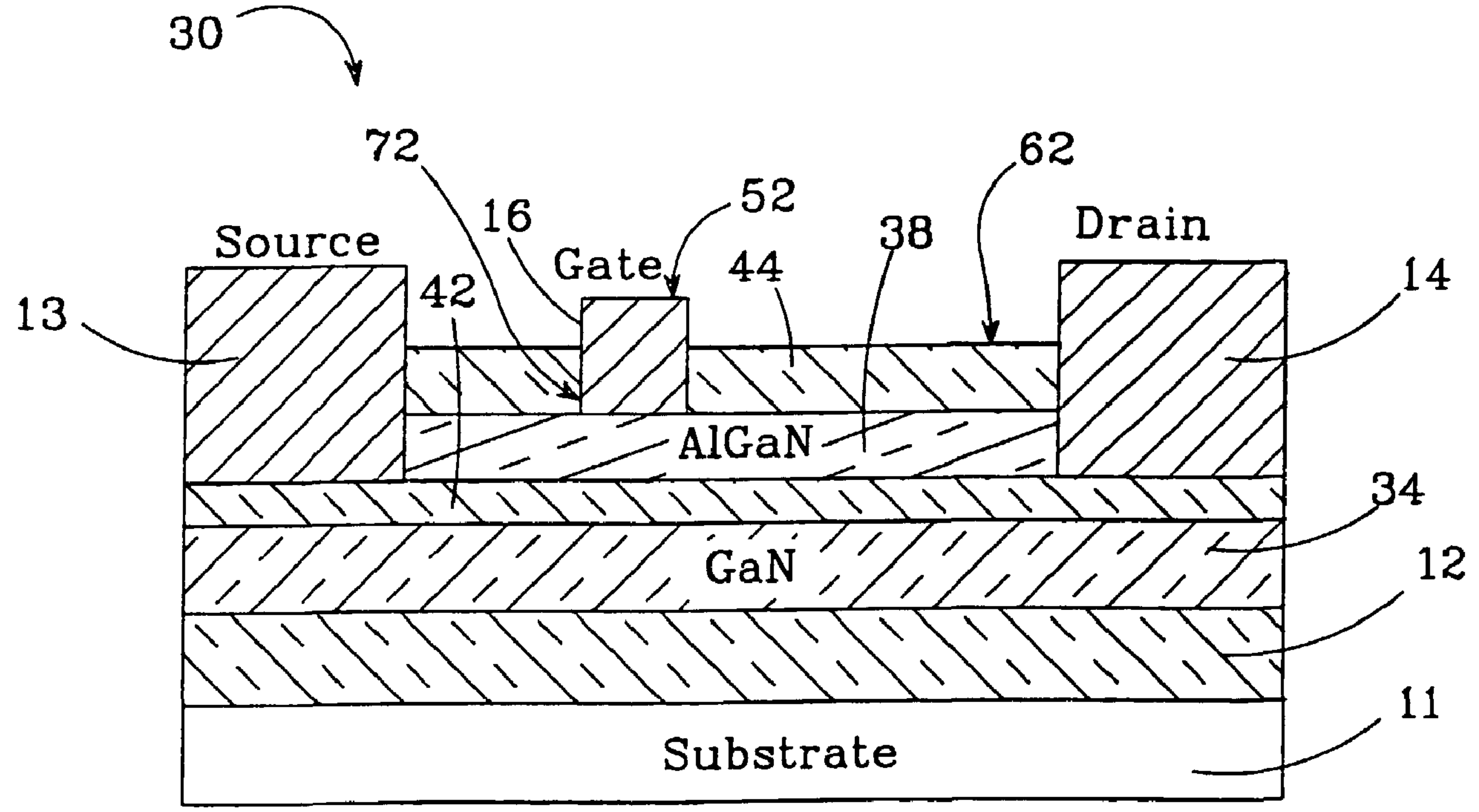
(54) Title: GROUP III NITRIDE BASED FETs AND HEMTs WITH REDUCED TRAPPING AND METHOD FOR PRODUCING THE SAME



(57) Abrégé/Abstract:
New Group III nitride based field effect transistors (10) and high electron mobility transistors (30) are disclosed that provide enhanced high frequency response characteristics. The preferred transistors (10, 30) are made from GaN/AlGaN and have a dielectric layer (22, 44) on the surface of their barrier layer (18, 38). The dielectric layer (22, 44) has a high percentage of donor electrons (68) that neutralize traps (69) in the barrier layer (18, 38) such that the traps (69) cannot slow the high frequency response of the transistors (10, 30). A new method of manufacturing the transistors (10, 30) is also disclosed, with the new method using sputtering to deposit the dielectric layer (18, 38).

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(71) Applicant: **CREE LIGHTING COMPANY** [US/US]; 340 Storke Road, Goleta, CA 93117 (US).

(72) Inventors: **WU, Yifeng**; 7170 Davenport Road #103, Goleta, CA 93117 (US). **ZHANG, Naiqian**; 789 Laurel Walk #A, Goleta, CA 93117 (US).

(74) Agents: **HEYBL, Jaye, G.** et al.; Koppel & Jacobs, Suite 107, 555 St. Charles Drive, Thousand Oaks, CA 91360 (US).

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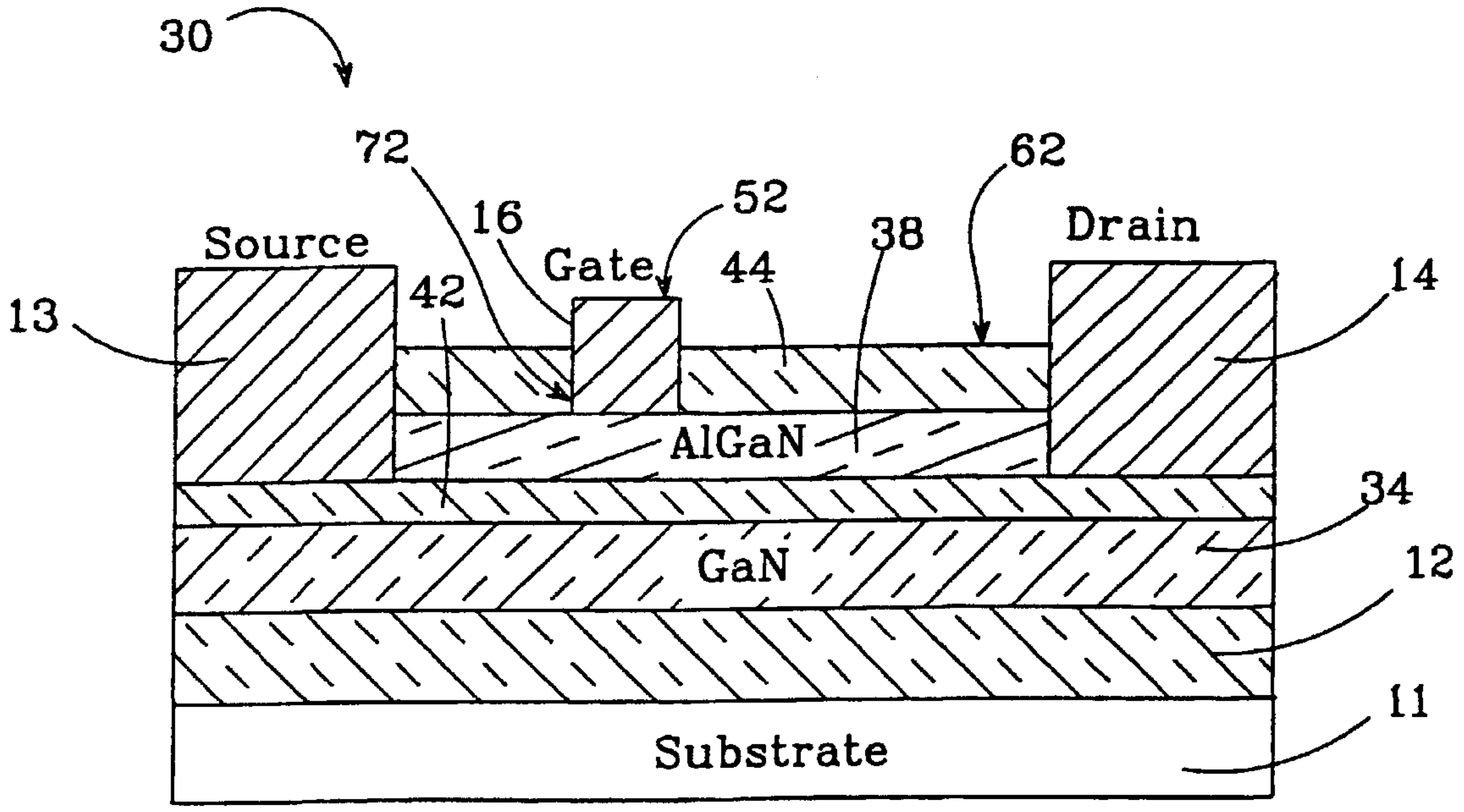
(54) Title: GROUP III NITRIDE BASED FETS AND HEMTS WITH REDUCED TRAPPING AND METHOD FOR PRODUCING THE SAME



(57) Abstract: New Group III nitride based field effect transistors (10) and high electron mobility transistors (30) are disclosed that provide enhanced high frequency response characteristics. The preferred transistors (10, 30) are made from GaN/AlGaN and have a dielectric layer (22, 44) on the surface of their barrier layer (18, 38). The dielectric layer (22, 44) has a high percentage of donor electrons (68) that neutralize traps (69) in the barrier layer (18, 38) such that the traps (69) cannot slow the high frequency response of the transistors (10, 30). A new method of manufacturing the transistors (10, 30) is also disclosed, with the new method using sputtering to deposit the dielectric layer (18, 38).

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GROUP III NITRIDE BASED FETs AND HEMTs WITH REDUCED TRAPPING AND METHOD FOR PRODUCING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to high frequency solid state transistors, and more particularly to Group III nitride based field effect transistors and high electron mobility transistors.

Description of the Related Art

Microwave systems commonly use solid state transistors as amplifiers and oscillators, which has resulted in significantly reduced system size and increased reliability. To accommodate the expanding number of microwave systems, there is an interest in increasing their operating frequency and power. Higher frequency signals can carry more information (bandwidth), allow for smaller antennas with very high gain, and provide radar with improved resolution.

Field effect transistors (FETs) and high electron mobility transistors (HEMTs) are common types of solid state transistors that are fabricated from semiconductor materials such as Silicon (Si) or Gallium Arsenide

(GaAs). One disadvantage of Si is that it has low electron mobility (approximately 1450 $cm^2/V\text{-}s$), which produces a high source resistance. This resistance seriously degrades the high performance gain otherwise possible from Si based FETs and HEMTs. [CRC Press, The Electrical Engineering Handbook, Second Edition, Dorf, p.994, (1997)]

GaAs is also a common material for use in FETs and HEMTs and has become the standard for signal amplification in civil and military radar, handset cellular, and satellite communications. GaAs has a higher electron mobility (approximately 6000 $cm^2/V\text{-}s$) and a lower source resistance than Si, which allows GaAs based devices to function at higher frequencies. However, GaAs has a relatively small bandgap (1.42 eV at room temperature) and relatively small breakdown voltage, which prevents GaAs based FETs and HEMTs from providing high power at high frequencies.

Improvements in the manufacturing of GaN/AlGaN semiconductor materials have focussed interest on the development of GaN/AlGaN based FETs and HEMTs. These devices can generate large amounts of power because of their unique combination of material characteristics including high breakdown fields, wide bandgaps (3.36 eV for GaN at room temperature), large conduction band offset, and high saturated electron drift velocity. The same size GaN amplifier can produce up to ten times the power of a GaAs amplifier operating at the same frequency.

U.S. Patent number 5,192,987 to Khan et al discloses GaN/AlGaN based HEMTs grown on a buffer and a substrate, and a method for producing them. Other HEMTs have been described by Gaska et al., "High-Temperature Performance of AlGaN/GaN HFET's on SiC Substrates," IEEE Electron Device Letters, Vol. 18, No 10, October 1997, Page 492; and Ping et al., "DC and Microwave Performance of High Current AlGaN Heterostructure Field Effect Transistors Grown on P-type SiC Substrates," IEEE Electron Devices Letters, Vol. 19, No. 2, February 1998, Page 54. Some of these devices have shown a gain-bandwidth product (f_T) as high as 67 gigahertz (K. Chu et al. WOCSEMMAD, Monterey, CA, February 1998) and high power densities up to 2.84 W/mm at 10 GHz (G. Sullivan et al., "High Power 10-GHz Operation of AlGaN HFET's in Insulating SiC," IEEE Electron Device Letters, Vol. 19, No. 6, June 1998, Page 198; and Wu et al., IEEE Electron Device Letters, Volume 19, No. 2, Page 50, February 1998.)

Despite these advances, GaN/AlGaN based FETs and HEMTs have been unable to produce significant amounts of total microwave power with high efficiency and high gain. They produce significant power gain with DC gate drives, but with frequency step-ups as low as a millihertz to a few kilohertz, their amplification drops off significantly.

It is believed that the difference between AC and DC amplification is primarily caused by surface traps in the device's channel. Although the nomenclature varies somewhat, it is common to refer to an impurity or defect center as a trapping center (or simply trap) if, after capture of one type carrier, the most probable next event is re-excitation. In general, trapping levels located deep in a band gap are slower in releasing trapped carriers than other levels located near the conduction of valence bands. This is due to the increased energy that is required to re-excite a trapped electron from a center near the middle of the band gap to the conduction band, compared to the energy required to re-excite the electron from a level closer to the conduction band.

$Al_XGa_{1-X}N$ (X=0~1) has a surface trap density comparable to the channel charge of the transistor with the traps in deep donor states with activation energy ranging from 0.7 to 1.8 eV (depending on X). During FET and HEMT operation, the traps capture channel electrons. The slow trapping and deep trapping process degrades transistor speed, which largely degrades the power performance at microwave frequencies.

SUMMARY OF THE INVENTION

The present invention provides an improved Group III nitride based FETs and HEMTs that are preferably formed of GaN/AlGaN and exhibit improved amplification characteristics in response to AC gate drives. The invention also provides a new method for producing the new GaN/AlGaN FET and HEMT.

The new FET comprises a barrier layer on a high resistivity, non-conducting layer. Source, drain and gate contacts are included, with each contacting the barrier layer. A electron donor layer is formed on the surface of the barrier layer between the contacts, the donor layer preferably being a dielectric layer with a high percentage of donor electrons.

For the new HEMT, the barrier layer has a wider bandgap than the non-conducting layer and, as a result, a two dimensional electron gas (2DEG) forms at the junction between the barrier layer and the non-conducting layer. The 2DEG has a high concentration of electrons which provide an increased device transconductance. The new HEMT has contacts that are similar to those on the FET's conducting channel and a similar dielectric layer is included on the HEMT's conducting channel.

In each device, it is believed that the barrier layer has surface traps that are positively charged. It is also believed that the dielectric layer's donor electrons migrate to the device's barrier layer and fill the surface traps. This causes them to become neutral and prevents them from capturing free electrons. The new dielectric coating also increases sheet electron density in the un-gated regions of the devices and protects the devices from undesirable passivation, impurities and damage during handling.

The present invention also provides a method for producing the new GaN FET or HEMT. The new method relies on sputtering techniques and results in little to no damage to the surface of the conduction channel. It also provides a strong and stable bond between the dielectric layer and the surface of the channel.

These and other further features and advantages of the invention would be apparent to those skilled in the art from the following detailed description, taking together with the accompanying drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a sectional view of a new GaN/AlGaN FET with a dielectric layer on its surface;

FIG. 2 is a sectional view of a new GaN/AlGaN HEMT with a dielectric layer on its surface;

FIG. 3 is a band energy diagram for the new GaN/AlGaN HEMT, taken through its gate;

FIG. 4 is a band diagram of the new GaN/AlGaN HEMT, taken through one of its access regions;

FIG. 5 is a band diagram of the new GaN HEMT, taken along the junction between the dielectric layer and the channel;

FIG. 6 is a set of graphs showing the output characteristics of the new GaN/AlGaN HEMT compared to one without the dielectric layer;

FIG. 7 is a set of graphs showing the difference in performance of the new HEMT as a function of the dielectric layer thickness;

FIG. 8 is a sectional view of a conventional sputtering chamber; and

FIG. 9 is a flow diagram for the new method of producing a transistor with a dielectric layer.

DETAILED DESCRIPTION OF THE INVENTION

New GaN/AlGaN FET and HEMT

FIG. 1 shows the new Group III nitride based FET 10 constructed in accordance with this invention. It comprises a substrate 11 that can be either sapphire (Al_2O_3) or silicon carbide (SiC), with the preferred substrate being a 4H polytype of silicon carbide. Other silicon carbide polytypes can also be used including 3C, 6H and 15R polytypes. An $Al_xGa_{1-x}N$ buffer layer 12 (where x in between 0 and 1) is included on the substrate 11 and provides an appropriate crystal structure transition between the silicon carbide substrate and the remainder of the FET 10.

Silicon carbide has a much closer crystal lattice match to Group III nitrides than sapphire and results in Group III nitride films of higher quality. Silicon carbide also has a very high thermal conductivity so that the total output power of Group III nitride devices on silicon carbide is not limited by the thermal dissipation of the substrate (as is the case with some devices formed on sapphire). Also, the availability of silicon carbide substrates provides the capacity for device isolation and reduced parasitic capacitance that make commercial devices possible. SiC substrates are available from Cree Research, Inc., of Durham, North Carolina and methods for producing them are set forth in the scientific literature as well as in a U.S. Patents, Nos. Re. 34,861; 4,946,547; and 5,200,022.

Group III nitrides refer to those semiconductor compounds formed between nitrogen and the elements in Group III of the periodic table, usually aluminum (Al), gallium (Ga), and indium (In). The term also refers to ternary and tertiary compounds such as AlGaN and AlInGaN.

The FET 10 has a barrier layer 18 made of $Al_xGa_{1-x}N$, that is on a high resistivity, non-conducting layer 20 made of GaN. The high resistivity layer 20 is sandwiched between the barrier layer 18 and the buffer layer 12. The barrier layer is typically about 0.1 to 0.3 micrometers thick and the barrier layer 18, high resistivity layer

20, and buffer layer 12, are preferably formed on the substrate 11 by epitaxial growth or ion implantation.

The FET also has a source and a drain contact 13 and 14, that are that are on the surface of the high resistivity layer 20. The barrier layer 12 is disposed between the contacts 13 and 14, with each contacting the edge of the barrier layer. The contacts 13 and 14 are usually separated by a distance in the range 3 to 10 micrometers for microwave devices. A rectifying Schottky contact (gate) 16 is located on the surface of the barrier layer 12 between the source and drain contacts 13 and 14, and it typically has a length in the range of 0.1 to 2 micrometers. The total width of the FET depends on the total power required. It can be wider than 30 millimeters, with the typical width being in the range of 50 to 100 microns. The area of the barrier layer's surface between the contacts is referred to as the barrier layer's access region.

The source and drain contact 13 and 14, are preferably formed of alloys of titanium, aluminum, nickel and gold, and the gate 16 is preferably formed of titanium, platinum, chromium, nickel, alloys of titanium and tungsten, and platinum silicide. In one embodiment, the contacts comprise an alloy of nickel, silicon, and titanium that is formed by depositing respective layers of these materials, and then annealing them. Because this alloy system eliminates aluminum, it avoids unwanted aluminum contamination over the device surface when the anneal temperature exceeds the melting point of aluminum (660°C).

During operation, the drain contact 14 is biased at a specified potential (positive drain potential for an n-channel device) and the source is grounded. This causes current to flow through the channel, from the drain to the source. The flow of current is controlled by the bias and frequency potentials applied to the gate 16, which modulate the channel current and provide gain.

The present invention is also applicable to GaN/AlGaN based HEMTs. FIG. 2 shows a HMET 30 that also had a source contact 13, a drain contact 14 and a Schottky gate 16 similar to those on the FET 10. It also has an $Al_xGa_{1-x}N$ semiconductor barrier layer 32 on a high resistivity, non-conducting GaN layer 34. Both these layers are formed on an aluminum nitride buffer layer 12 and a substrate 11 similar to those in FIG. 1.

However, in this embodiment, the layer 32 has a wider bandgap than the GaN layer 34 and this discontinuity in energy band gaps results in a free charge transfer from the wider band gap to the lower band gap material. A charge accumulates at the interface between the two and creates a two dimensional electron gas (2DEG) 36 that allows current to flow between the source and drain contacts 13 and 14. The 2DEG has very high electron mobility which gives the HEMT a very high transconductance at high frequencies. The voltage applied to the gate 16 electrostatically controls the number of electrons in the 2DEG directly under the gate, and thus controls the total electron flow.

Both the new FET 10 and HEMT 30 also include a layer of dielectric material 22 and 44 on the surface of their respective barrier layers 18 and 38, in the barrier layer's access regions. The dielectric layer is preferably silicon nitride (Si_xN_y), with silicon being the source of the donor electrons. To be most effective the layer 22 and 44 should meet the following four conditions. First, it should have a dopant that provides a high source of donor electrons. For silicon nitride, the layer should have a high percentage of Si. Although the applicant does not wish to be bound by any theory of operation, it is presently believed that electrons from the layer fill surface traps such that they become neutral and do not capture barrier layer electrons during operation.

Second, the energy level of the dopant should be higher than the energy level in the trap and for optimal results, the energy should be higher than the energy level of the barrier layer's conduction band edge. It is believed that this reduces the possibility of an electron from the gate metal giving to the donor states and prevents the trapping and de-trapping at that energy level. The layer will also work if the dopant's energy level is slightly below the energy level in the barrier layer's conduction band, but the higher its energy the better.

Third, there should be little or no damage to the device's surface and the forming of the dielectric layer should not increase the surface damage. It is believed that surface damage can create more surface traps. Fourth, the bond between the coating and the surface of the barrier layer should be stable under stress. If the bond is unstable, it is believed that the layer may fail under actual device operation when subjected to the stress created by increases in the electron field, voltage or temperature.

FIG. 3 shows a band diagram 50 for the new HEMT 30 taken at point 52 in FIG. 2, and vertically through the device's Schottky gate 16, barrier layer 38, 2DEG 42 and GaN layer 34. The diagram 50 shows the HEMT in equilibrium with no bias applied and no current flowing though the barrier layer. It shows the HEMT's barrier layer 54, GaN layer 56, and 2DEG 58 band energy. It is similar to a band diagram from a HEMT without the dielectric coating 44. The Schottky gate 58 covers the barrier layer below it, blocking the dielectric layer's electrons from reaching the barrier layer below it.

FIG. 4 shows another band diagram 60 for the HEMT 30 (again at equilibrium) taken at point 62 in FIG. 2 and vertically through its dielectric layer 44, barrier layer 38, 2DEG 42 and GaN layer 34. The diagram again shows the HEMT's barrier layer 63, GaN layer 64 and 2DEG 65 band energy, and it shows the dielectric layer's band energy 66. In the barrier layer's access region there are typically surface traps 69 that reduce the frequency characteristics by trapping electrons. This diagram shows the dielectric layer's band energy 66 with a source of donor electrons 68 at a higher energy state than the traps 69. The electrons 68 migrate to the barrier layer and fill the surface traps 69 causing then to become neutral and reducing their ability to capture electrons during operation.

FIG. 5 shows a third band diagram 70 for the HEMT (at equilibrium) taken at point 72 in FIG. 2, and horizontally along the junction between the dielectric layer 44 and the barrier layer 38. It begins from the gate 36 and continues into the region between the gate and drain. At the gate there is no dielectric layer and the band energy 72 remains constant. Outside of the gate, at the barrier layer's access region, shallow donor electrons 74 from the dielectric layer are available to fill surface traps 76 causing them to become neutral. The band energy falls near the edge of the gate as the traps are filled and then levels off 78 in the access region.

FIG. 6 shows the output characteristics 80 of the new HEMT with and without the dielectric layer. The gate sweep begins as a gate voltage of 2.0 volts followed by steps of 1 volt to generate the family of curves. The HEMT with or without the dielectric layer has the same DC high power output characteristics 82 (shown in bold lines). However, with AC gate drives applied to the device without the dielectric layer, the output response is significantly degraded 84 (normal lines). With the dielectric layer, the HEMT's AC output characteristics 86 (dashed lines) are nearly the same as its DC output characteristics 82, providing high power AC outputs.

FIG. 7 shows a graph 90 illustrating the drain current ratio (at V_{ds}=6V) under AC and DC drives (I_{AC}/I_{DC}) verses the thickness of the dielectric layer 92, and power density (at f=8GHz, V_{ds}=20V) verses the thickness of a silicon nitride dielectric layer 94. As the thickness of the layer increases from 0Å the preferred thickness of approximately 1500Å, the AC power density 94 increases. Around the preferred thickness, the graphs shows a point 96 where the AC power is equal to the DC power density and the drain current ratio is equal to one. At thicknesses less than 1500Å the AC power density decreases and the current ratio is less than one. It is believed that this difference is caused by thinner layers not having a sufficient percentage of donor electrons to neutralize all the channel traps. This leaves a percentage of charged traps that are available to capture electrons during operation. However, if the layer is too thick, it will result in too much capacitance on the device's surface. At 1500Å there is a sufficient percentage of donor electrons and any increase in the thickness does not appreciably improve the device's performance characteristics.

New Method of Manufacturing

As described above, the dielectric layer should have a strong bond with the surface of its FET and HEMT that is stable under stress. Various methods for depositing the layer can be used, including but not limited to sputtering, PECVD, MOCVD in situ at the of HEMT growth.

The preferred method for depositing a layer 108 on the FET and HEMT having a strong bond this is also stable, is through sputtering. FIG. 8 shows a simplified sputtering chamber 100 that can be used to deposit material on a substrate. In operation, a semiconductor device 101 is placed on an anode 102. The chamber 103 is then evacuated and an inert gas 104 such as argon is bled through the valve 105 to maintain a background pressure. The cathode 106 is made of the material to be deposited on the substrate/device. With the application of a high voltage 107 between the electrodes, the inert gas is ionized and the positive ions 110 excel to the cathode

106. On striking the cathode 106, they collide with the cathode atoms 112, giving them sufficient energy to be ejected. The sputtered cathode atoms 112 travel through space, eventually coating the anode 102 and the semiconductor device 101 on it. Other sputtering units can be more complex and detailed, but they work on much the same basic physical mechanisms. Using the more complex sputtering systems, it is possible to sputter and deposit a range of metals and dielectric layers.

FIG. 9 shows a flow diagram 120 for the new method of producing a transistor with a donor electron rich silicon nitride dielectric layer. The first step 122 is to form the device. The device is preferably an GaN/AlGaN FET or HEMT and it is preferably formed on a semiconductor wafer by a process such as metal-organic chemical vapor deposition (MOCVD). The wafer is then cleaned 124, with the preferred cleaning process being rinsing it with $NH_4OH:H_2O$ (1:4) for approximately 10 to 60 seconds. The wafer is then loaded into a sputtering chamber 126 having a silicon source.

In the next step 128, the Si_xN_y dielectric layer is deposited on the wafer by sputtering. The preferred sputtering process includes the specific steps of pumping down the chamber to a low pressure of about $3x10^{-7}$ Torr. Using a source gas having a flow of 20-100 sccm and a pressure of 5-10 mTorr the plasma is then started with RF power of 200-300W for about 2 minutes. This bombards the silicon at the cathode, cleaning its surface. The sputtering conditions are then changed such that the argon gas flow is 10-12 sccm, the nitrogen gas flow of 8-10 sccm, the chamber pressure of 2.5-5 mTorr, and the RF power of 200-300W. This condition is maintained for 2 minutes to sputter the Si cathode. The sputtered silicon reacts with the nitrogen and the resulting silicon nitride deposits on the wafer.

After sputtering, the next step 130 is to turn off the nitrogen gas and turn up the argon gas flow to 20-100 sccm for 2 minutes to clean the Si surface. All gas and power are then turned off and the chamber is allowed to cool down for five minutes and vent. The device can then be removed from the sputtering chamber. Windows are etched in the device for contacts and gate. An additional step in the process could include depositing the contacts and gate on the device's surface and attaching leads 134. Alternatively, the contacts and gate could be deposited on the device before depositing the dielectric layer in the sputtering chamber. The dielectric layer over the contacts and gate could then be etched to allow for the connection of leads.

In embodiments using T-gates instead of conventional gates, there may be some difficulty fully covering the transistors surface. This is due to the shadowing that can occur when the top of the T blocks sputtered materials from reaching areas around the footprint of the T-gate. To ensure full coverage, the transistor can be loaded at an angle and rotated during sputtering deposition.

In any of the deposition methods, it is important that the environment be hydrogen free, particularly when sputtering. Hydrogen atoms diffuse into the semiconductor material, where they can neutralize dopants. This can leave the dopants inactive, resulting in the material becoming insulating or weakly doped in its as grown state. This can result in critical performance problems for the new FET or HEMT.

Although the present invention has been described in considerable detail with reference to certain preferred configurations thereof, other versions are possible. Therefore, the spirit and scope of the appended claims should not be limited to the preferred versions contained described in the specification.

WE CLAIM:

1. A field effect transistor (FET), comprising:

a high resistivity, non-conducting layer (20);

a barrier layer (18) on said non-conducting layer (20);

respective source, drain and gate contacts (13,14,16) contacting said barrier layer (18), with part of the surface of said barrier layer (18) uncovered by said contacts (13,14,16); and

an electron source layer (22) formed on the surface of said barrier layer (18) between said contacts (13,14,16) said electron source layer (22) having a high percentage of donor electrons (68).

2. The FET of claim 1, wherein said barrier layer (18) has positive charged surface traps (69) and wherein said donor electrons (68) neutralize said traps (69) and said donor electrons (68) have a higher energy state than said traps (69).

3. The FET of claim 1, wherein said electron source layer (22) is a layer of dielectric material.

4. The FET of claim 1, wherein said electron source layer (22) has a stable bond with said barrier layer (18) under stresses created by increases in electron fields, voltage or temperature.

5. The FET of claim 1, wherein the surface of said barrier layer (22) is substantially free of damage.

6. The FET of claim 1, further comprising a substrate (11) of sapphire or silicon carbide, said substrate (11) being adjacent to said non-conducting layer (20), opposite said barrier layer (18).

7. The FET of claim 6, further comprising a buffer layer (12) between said non-conducting layer (20) and said substrate (11).

8. The FET of claim 1, wherein said non-conducting layer (20) and said barrier layer (18) are made of Group III nitride semiconductor materials.

9. The FET of claim 1, wherein said barrier layer (38) has a wider energy bandgap than said non-conducting layer (34), said FET further comprising a 2 dimensional electron gas (2DEG) (42) between said barrier layer (38) and non-conducting layer (34).

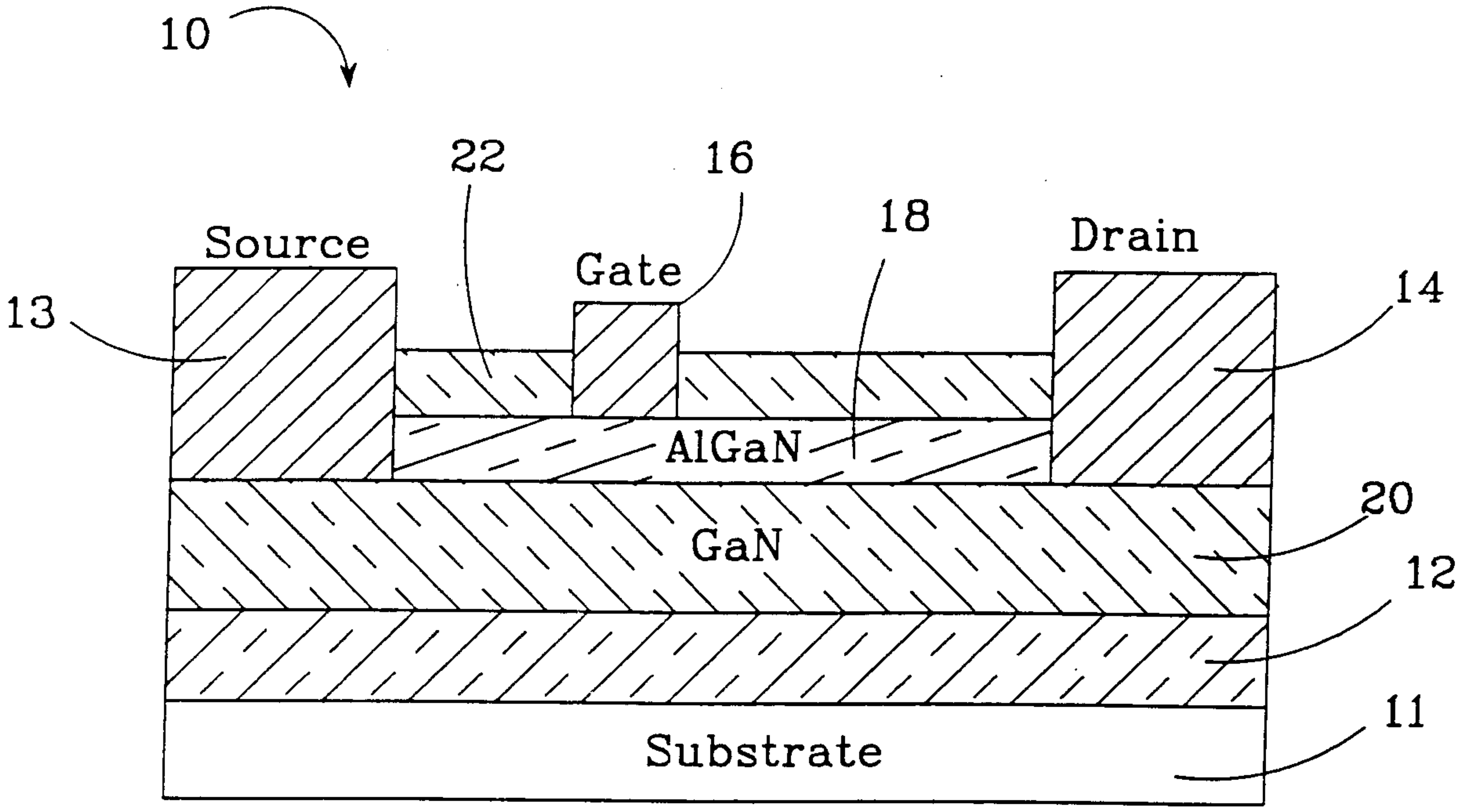
10
22
16
Source
Gate
18
Drain
13
14
AlGaN
20
GaN
12
11
Substrate

FIG.1

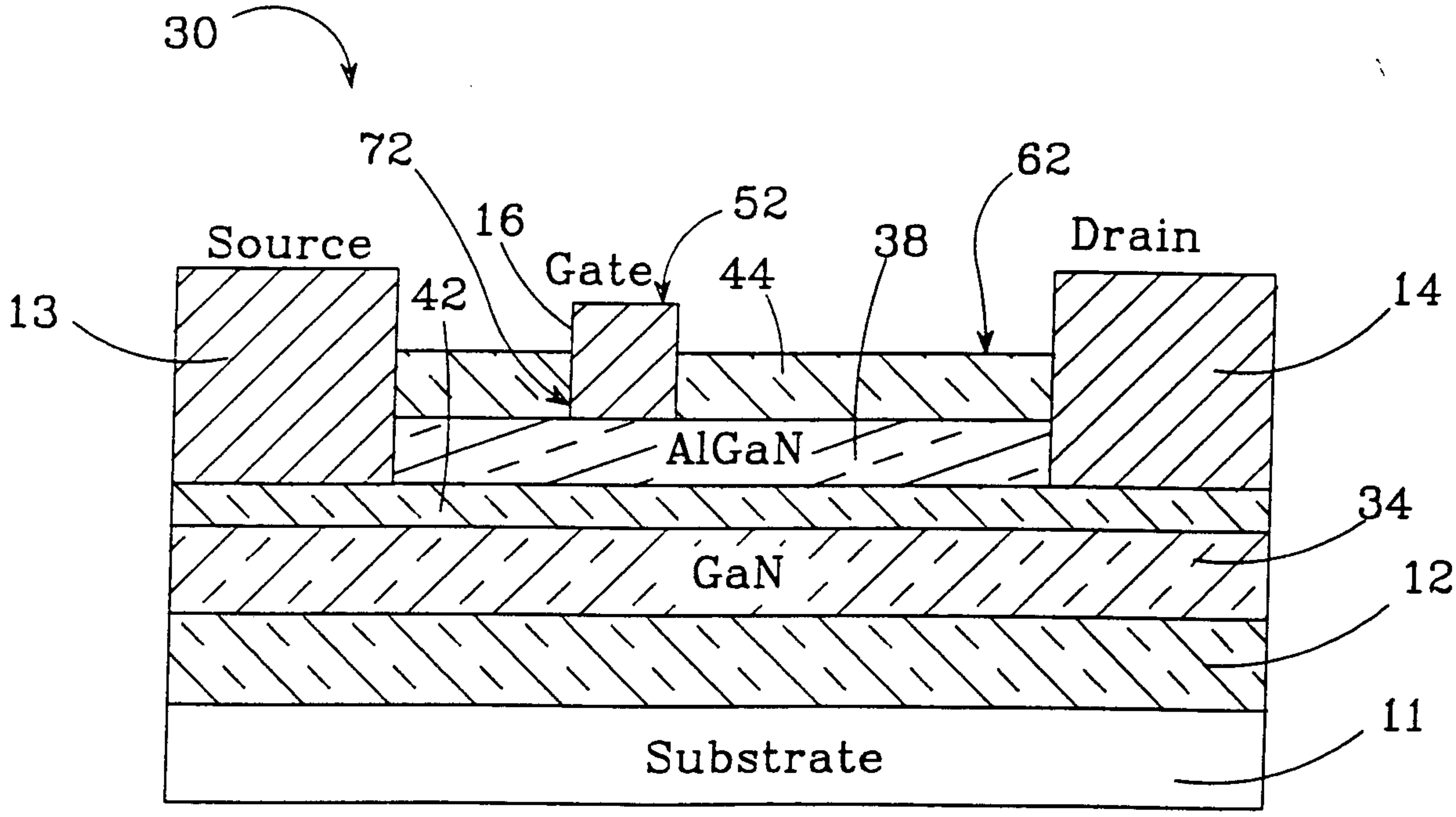
30
72
62
52
16
Source
Gate
44
38
Drain
13
42
14
AlGaN
34
GaN
12
11
Substrate

FIG.2

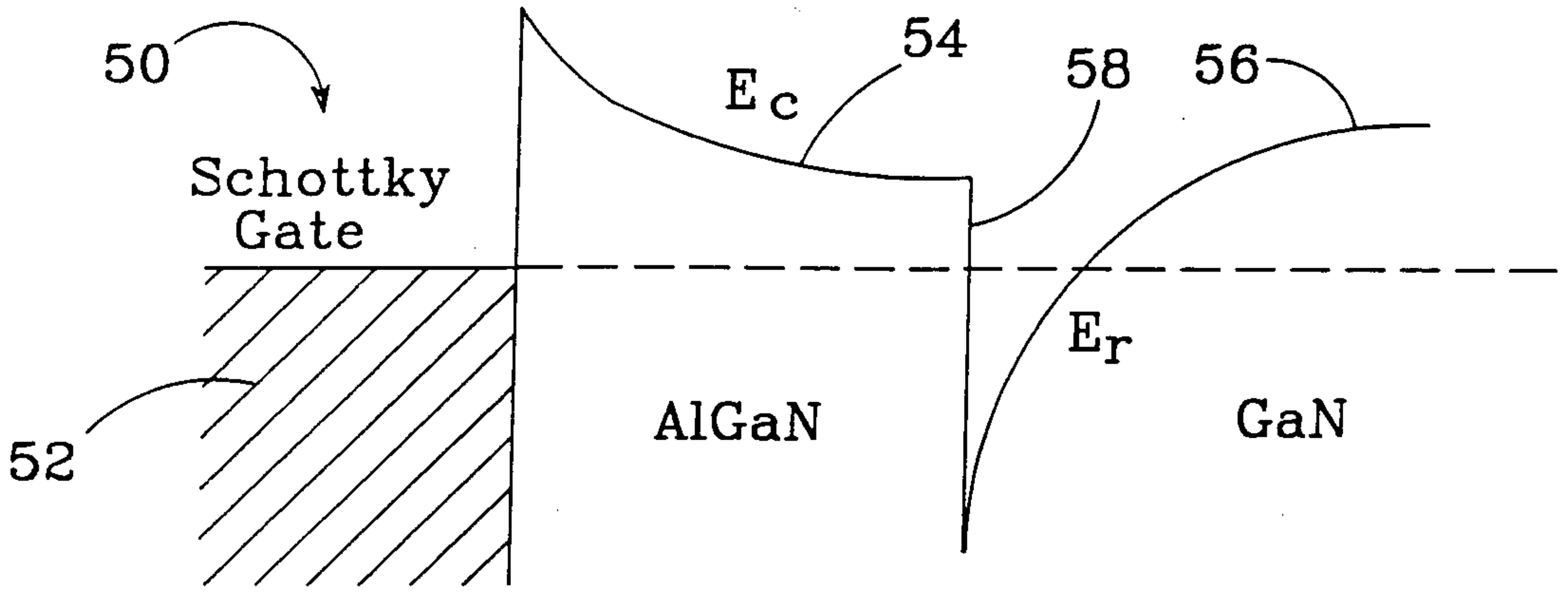

FIG.3

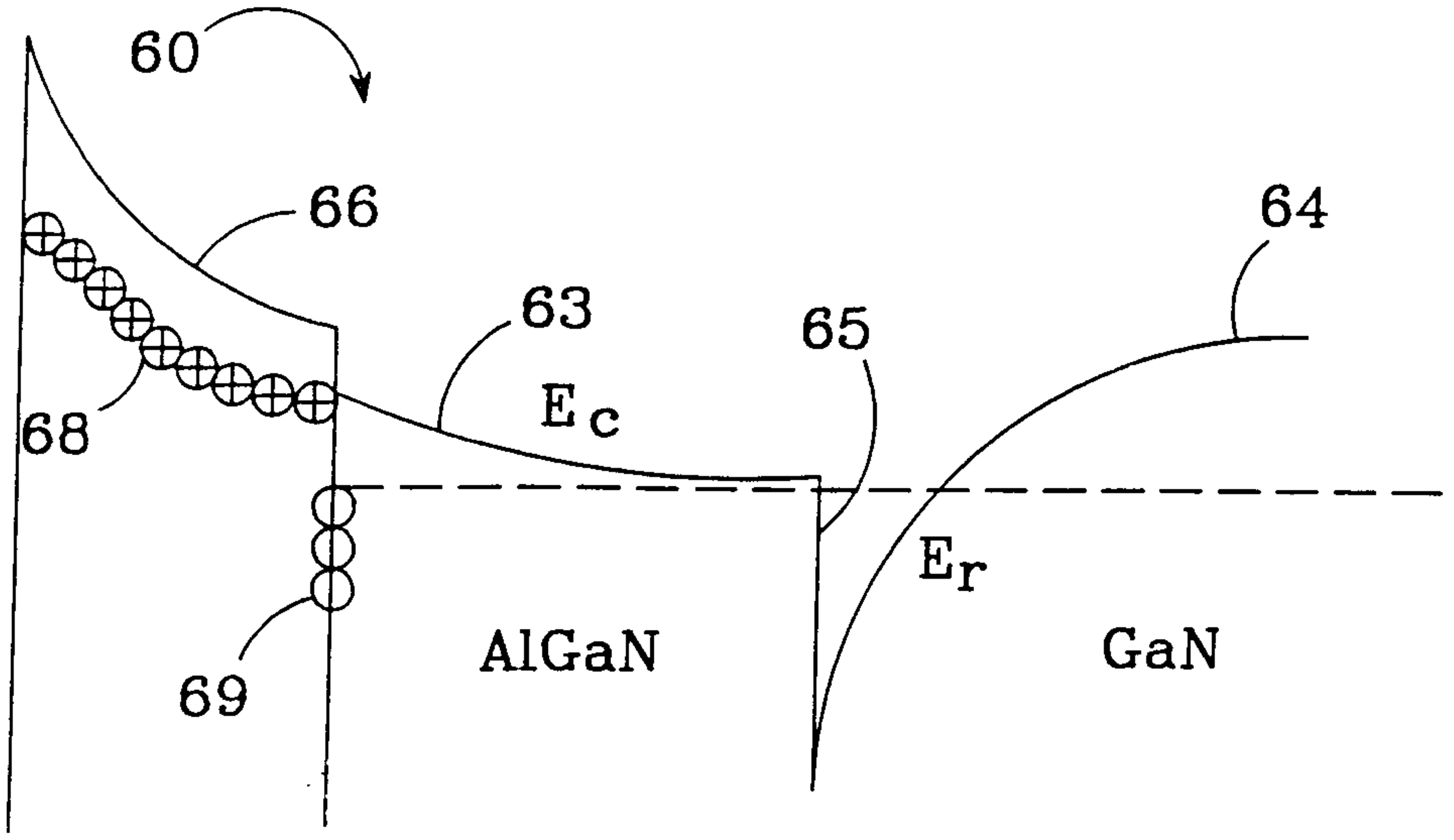

FIG.4

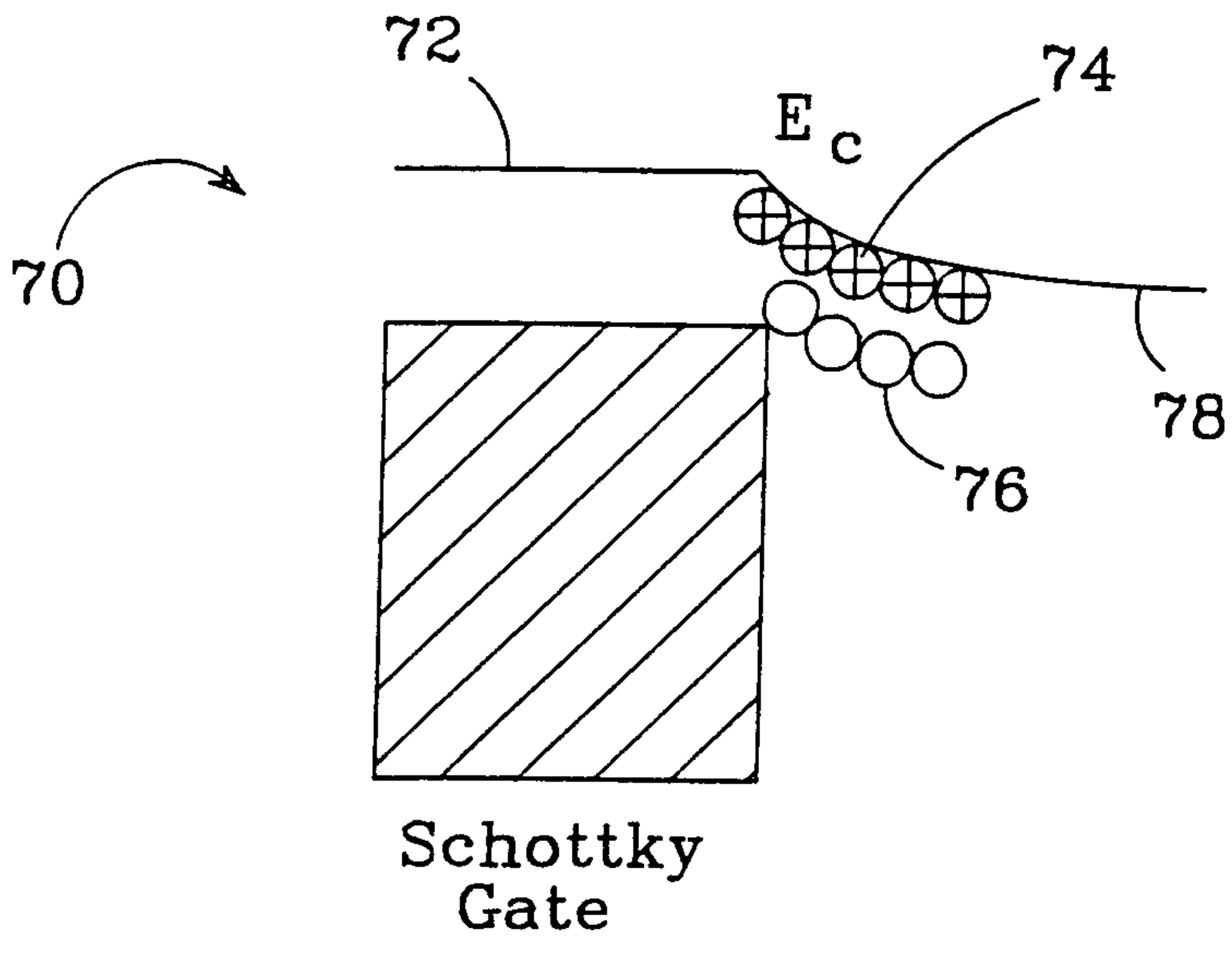

FIG.5

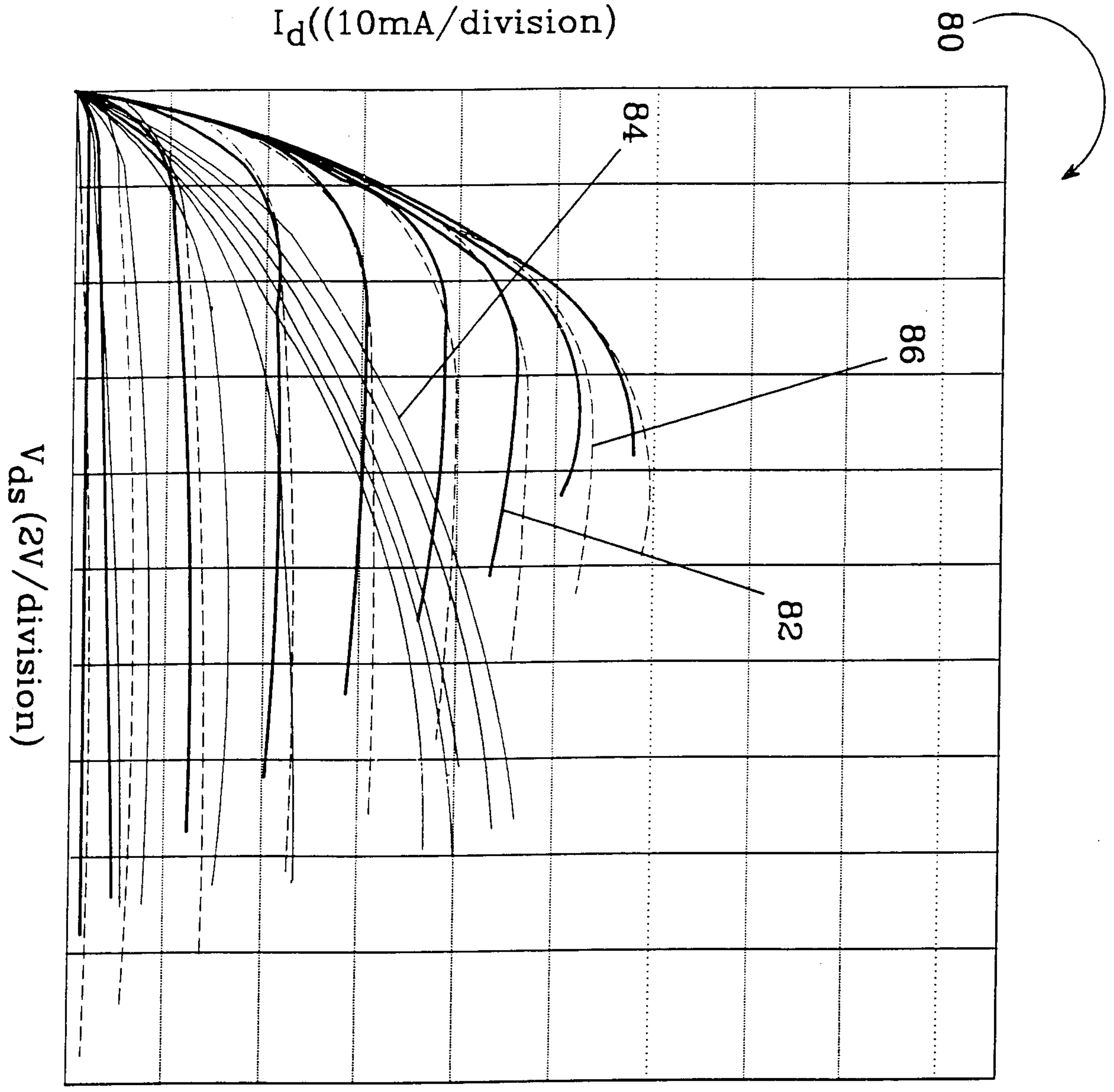

FIG.6

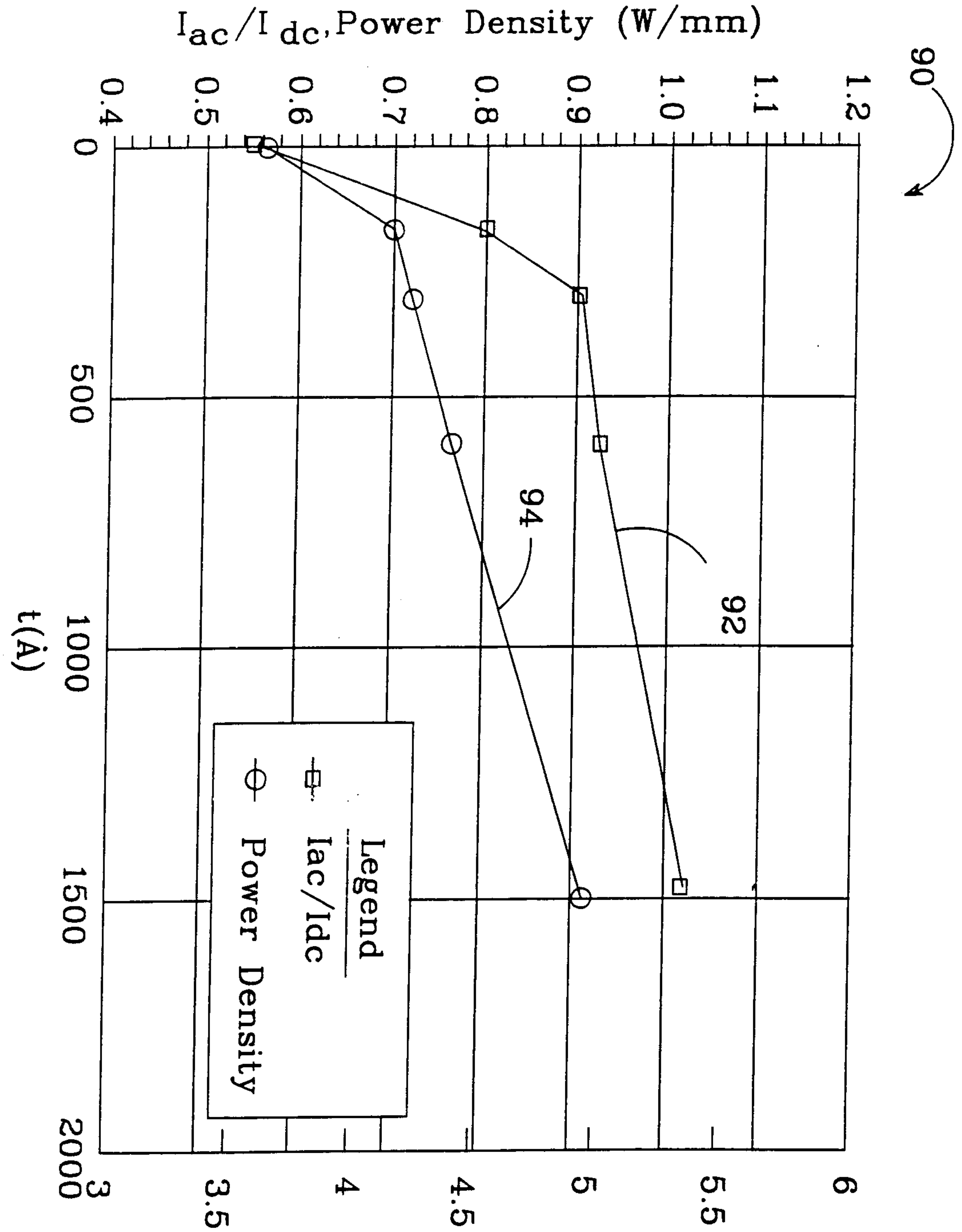
90
I_{ac}/I_{dc}, Power Density (W/mm)
0.4
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2
0
500
1000
1500
2000
t(Å)
3
3.5
4
4.5
5
5.5
6
92
94
Legend
Iac/Idc
Power Density

FIG.7

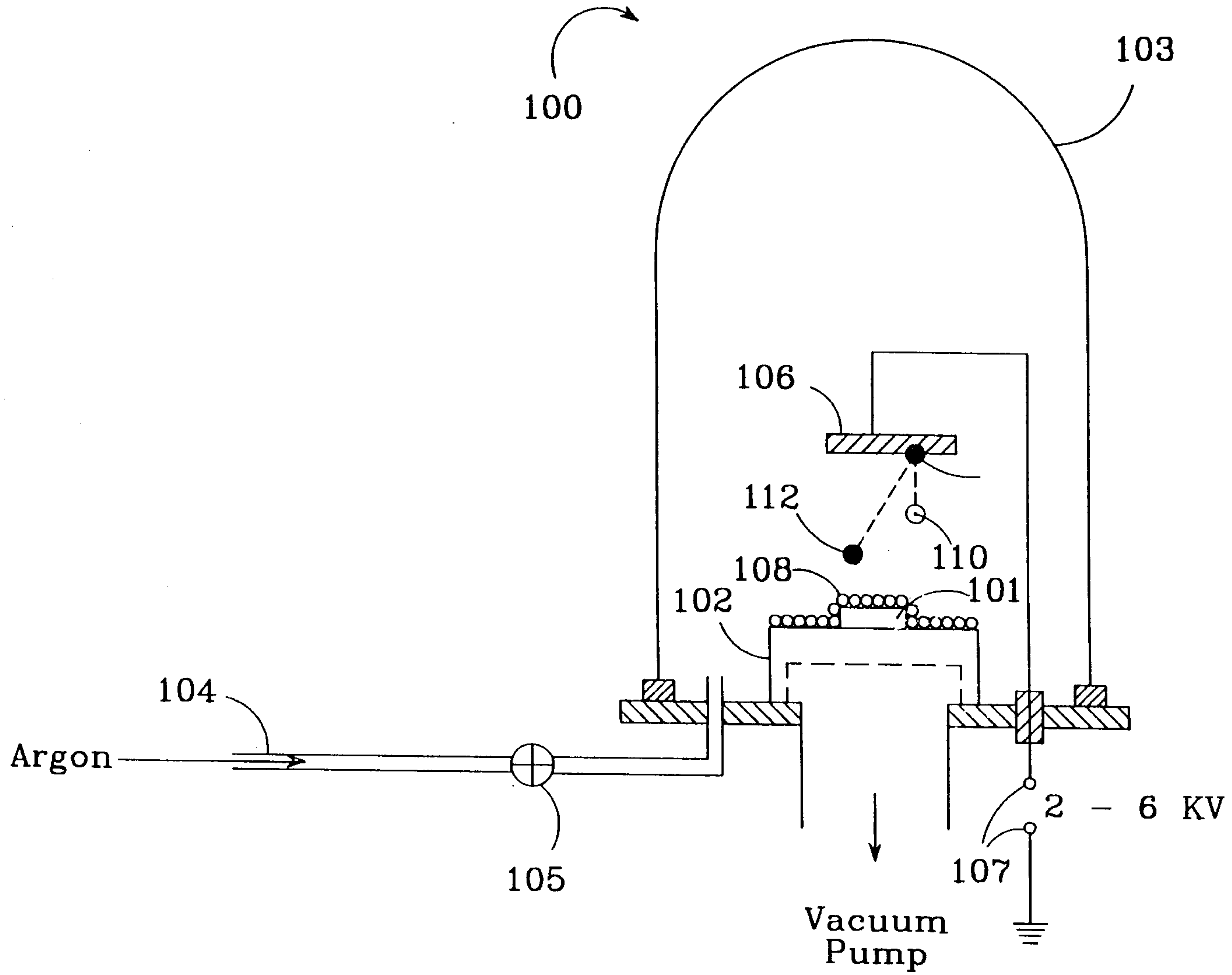
100
103
106
112
110
108
101
102
104
Argon
105
2 – 6 KV
107
Vacuum
Pump

FIG.8

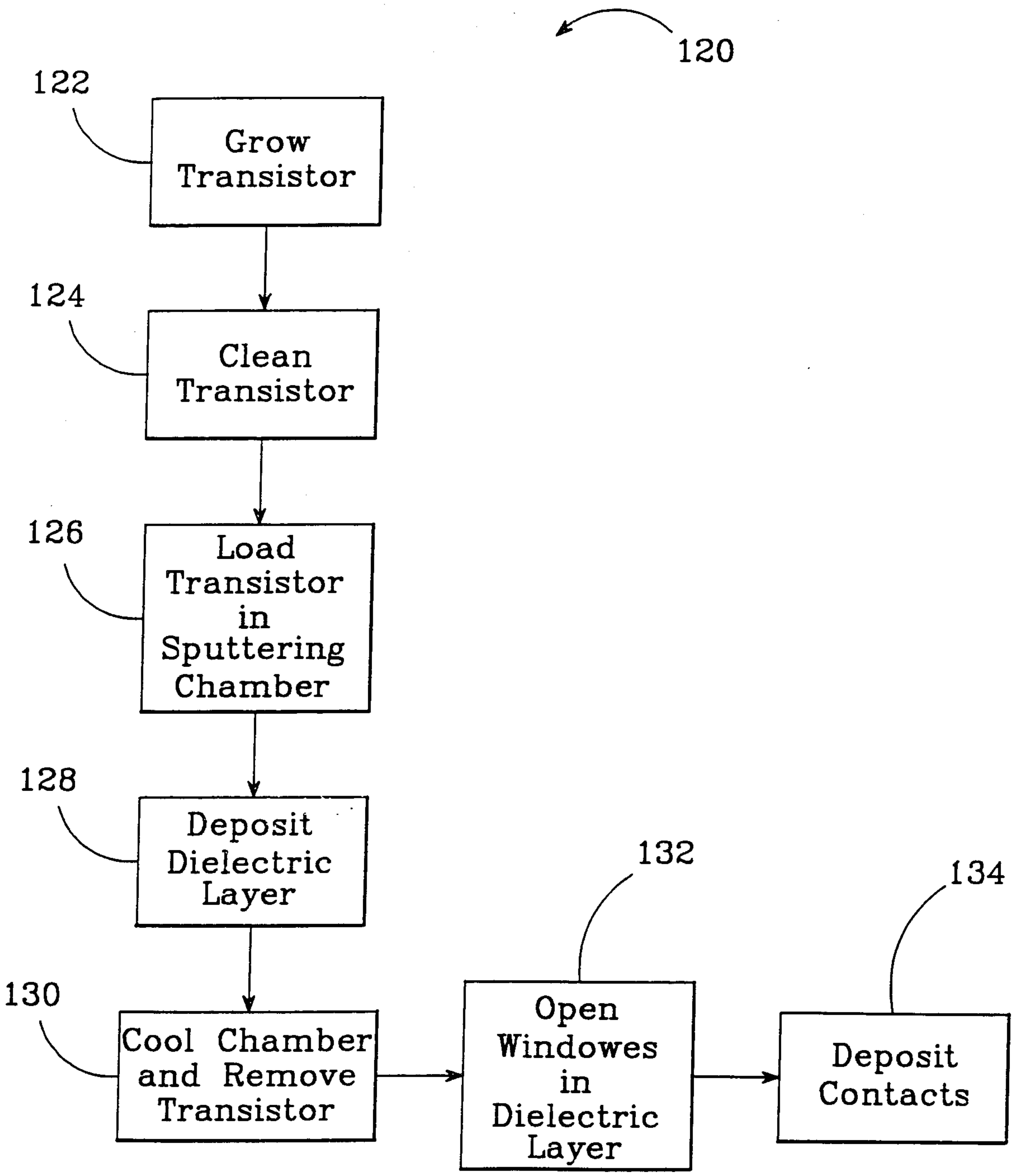
120
122
Grow Transistor
124
Clean Transistor
126
Load Transistor in Sputtering Chamber
128
Deposit Dielectric Layer
130
Cool Chamber and Remove Transistor
132
Open Windowes in Dielectric Layer
134
Deposit Contacts

FIG.9


30
72
62
52
16
38
Source
Drain
Gate
44
42
14
13
AlGaN
34
GaN
12
11
Substrate