(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
25 May 2023 (25.05.2023)

WIPO | PCT

(10) International Publication Number
WO 2023/088617 A1

(51) International Patent Classification:
H01L 23/535 (2006.01) *H01L 29/78* (2006.01)
H01L 21/768 (2006.01) *H01L 23/528* (2006.01)

(21) International Application Number:
PCT/EP2022/078559

(22) International Filing Date:
13 October 2022 (13.10.2022)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
17/527,229 16 November 2021 (16.11.2021) US

(71) Applicant: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, New York, 10504 (US).

(71) Applicant *(for MG only)*: **IBM UNITED KINGDOM LIMITED** [GB/GB]; PO Box 41, North Harbour, Portsmouth, Hampshire PO6 3AU (GB).

(72) Inventors: **XIE, Ruilong**; IBM CORPORATION, 257 Fuller Road, Albany, New York 12203-3654 (US). **SIEG, Stuart**; IBM CORPORATION, 257 Fuller Road, Albany, New York 12203-3654 (US). **GHOSH, Somnath**; IBM CORPORATION, 257 Fuller Road, Albany, New York 12203-3654 (US). **CHOI, Kisik**; IBM CORPORATION, 257 Fuller Road, Albany, New York 12203-3654 (US). **PETRARCA, Kevin, Shawn**; IBM CORPORATION, 1101 Kitchawan Road, PO Box 218, Yorktown Heights, New York 10598-0218 (US).

(74) Agent: **LITHERLAND, David**; IBM United Kingdom Limited, Intellectual Property Law, Hursley Park, Hursley, Winchester Hampshire SO21 2JN (GB).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG,

(54) Title: REPLACEMENT BURIED POWER RAIL

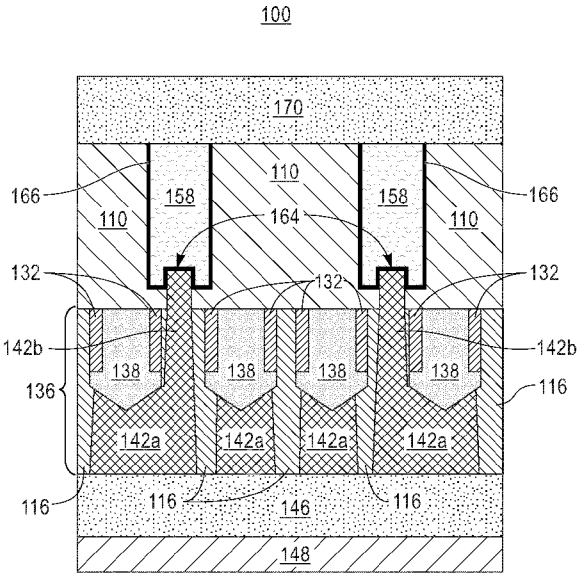

FIG. 12

(57) Abstract: Embodiments disclosed herein describe a semiconductor structure. The semiconductor structure may include a device region with a first source/drain (S/D) and a second S/D. The semiconductor structure may also include a buried power rail (BPR) under the device region. A critical dimension of the BPR may be larger than a distance between the first S/D and the second S/D. The semiconductor structure may also include a via-contact-to-buried power rail (VBPR) between the BPR and the S/D.

WO 2023/088617 A1

[Continued on next page]

NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) **Designated States** *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

REPLACEMENT BURIED POWER RAIL

BACKGROUND

[0001] The present invention relates generally to the field of fabrication of semiconductor devices, and more particularly to forming a buried power rail with increased critical dimension by forming a dummy buried power rail with small dimensions at an earlier stage of fabrication, and increasing the dimensions after the dummy buried power rail is removed at later stage of fabrication.

[0002] In fabricating semiconductor devices, millions of devices can be located together on a single substrate. Useful control of these millions of devices relies on the application of electrical signals to specific devices while insulting the electrical signals from shorting to anything else (e.g., other devices). Within standard logic cells, power rails in back-end of line (BEOL) metal layers deliver current to source/drains that power the individual devices (e.g., transistors). The power rails carry a higher current than standard routing tracks/signal lines to maintain adequate power distribution targets, and therefore require a larger space in the cell. In many designs, a power rail can be four times larger than a normal routing line.

[0003] Reducing a lateral dimension of the power rails and extending a vertical dimension deeper into the cell can keep the total metal volume in the power rail high while making room for other components. Increasing the depth of the power rail, however, can cause higher via resistance, or can cause the signal lines to carry increased capacitance between tracks in the BEOL. Burying the power rails underneath a physical device (e.g. transistor) enables the depth of the power rail to be increased independent of the signal lines in the BEOL. Buried power rails (BPR) provide significantly lower resistance through the power rail without driving any negative impact to either via resistance or capacitance in the BEOL.

SUMMARY

[0004] According to an aspect of the present invention, a semiconductor structure is disclosed. The semiconductor structure may include a device region with a first source/drain (S/D) and a second S/D. The semiconductor structure may also include a buried power rail (BPR) under the device region. A critical dimension of the BPR may be larger than a distance between the first S/D and the second S/D. The semiconductor structure may also include a via-contact-to-buried power rail (VBPR) between the BPR and the S/D.

[0005] According to another aspect of the present invention, a method is disclosed. The method may include forming a dummy buried power rail (BPR) in an insulator layer between a first fin field-effect transistor (FET) and a second fin FET, forming a first source/drain (S/D) electrically connected to the first fin FET, and a second S/D electrically connected to the second fin FET, forming a via-contact-to-buried power rail (VBPR) that contacts a top surface of the dummy BPR and the first S/D, selectively etching the dummy BPR from a bottom surface opposite the top surface to form a BPR trench, widening the BPR trench, and metalizing the BPR trench to form a BPR.

[0006] According to another aspect of the present invention, a semiconductor structure is disclosed. The semiconductor structure may include a back side power delivery network (BSPDN), a buried power rail (BPR) coupled to the BSPDN, a via-contact-to-buried power rail (VBPR) coupled to the BPR, wherein the BPR wraps around a bottom of the VBPR, a first source/drain (S/D) coupled to a middle of the VBPR, and a back-end-of-line layer coupled to a top of the VBPR.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Figure 1 is a schematic cross-sectional side view of a semiconductor structure, in accordance with one embodiment of the present invention;

[0008] Figure 2 is a schematic cross-sectional side view of the semiconductor structure of Figure 1 at a subsequent fabrication stage, in accordance with one embodiment of the present invention;

[0009] Figure 3 is a schematic cross-sectional side view of the semiconductor structure of Figure 1 at a subsequent fabrication stage, in accordance with one embodiment of the present invention;

[0010] Figure 4 is a schematic cross-sectional side view of the semiconductor structure of Figure 1 at a subsequent fabrication stage, in accordance with one embodiment of the present invention;

[0011] Figure 5A and 5B are schematic cross-sectional side views of the semiconductor structure of Figure 1 at a subsequent fabrication stage, in accordance with one embodiment of the present invention;

[0012] Figure 6 is a schematic cross-sectional side view of the semiconductor structure of Figure 1 at a subsequent fabrication stage, in accordance with one embodiment of the present invention;

[0013] Figure 7 is a schematic cross-sectional side view of the semiconductor structure of Figure 1 at a subsequent fabrication stage, in accordance with one embodiment of the present invention;

[0014] Figure 8 is a schematic cross-sectional side view of the semiconductor structure of Figure 1 at a subsequent fabrication stage, in accordance with one embodiment of the present invention;

[0015] Figure 9 is a schematic cross-sectional side view of the semiconductor structure of Figure 1 at a subsequent fabrication stage, in accordance with one embodiment of the present invention;

[0016] Figure 10 is a schematic cross-sectional side view of the semiconductor structure of Figure 1 at a subsequent fabrication stage, in accordance with one embodiment of the present invention;

[0017] Figure 11 is a schematic cross-sectional side view of the semiconductor structure of Figure 1 at a subsequent fabrication stage, in accordance with one embodiment of the present invention; and

[0018] Figure 12 is a schematic cross-sectional side view of the semiconductor structure of Figure 1 at a subsequent fabrication stage, in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0019] In the following detailed description, reference is made to the accompanying drawings, which show specific examples of embodiments of the invention. These embodiments are described in sufficient detail to enable those skilled in the art to practice them, and it is to be understood that other embodiments may be utilized and that

structural, logical and electrical changes may be made without departing from the described embodiments. The following detailed description is, therefore, not to be taken in a limiting sense, and the included embodiments are defined by the appended claims.

[0020] Detailed embodiments of the claimed structures and methods are disclosed herein; however, it is to be understood that the disclosed embodiments are merely illustrative of the claimed structures and methods that may be embodied in various forms. In addition, each of the examples given in connection with the various embodiments are intended to be illustrative, and not restrictive. Further, the figures are not necessarily to scale, some features may be exaggerated to show details of particular components. Therefore, specific structural and functional details disclosed herein are not to be interpreted as limiting, but merely as a representative basis for teaching one skilled in the art to variously employ the methods and structures of the present disclosure. It is also noted that like and corresponding elements are referred to by like reference numerals.

[0021] In the following description, numerous specific details are set forth, such as particular structures, components, materials, dimensions, processing steps and techniques, in order to provide an understanding of the various embodiments of the present application. However, it will be appreciated by one of ordinary skill in the art that the various embodiments of the present application may be practiced without these specific details. In other instances, well-known structures or processing steps have not been described in detail in order to avoid obscuring the present application.

[0022] References in the specification to “one embodiment,” “an embodiment,” “an example embodiment,” etc., indicate that the embodiment described may include a particular feature, structure, or characteristic. Moreover, such phrases are not necessarily referring to the same embodiment. Further, when a particular feature, structure, or characteristic is described in connection with an embodiment, it is submitted that it is within the knowledge of one skilled in the art to affect such feature, structure, or characteristic in connection with other embodiments whether or not explicitly described.

[0023] For purposes of the description hereinafter, the terms “right,” “left,” “vertical,” “horizontal,” “top,” “bottom,” and derivatives thereof shall relate to the disclosed structures and methods, as oriented in the drawing Figures. The terms “overlaying,” “atop,” “positioned on,” or “positioned atop” mean that a first element, such as a first structure, is present on a second element, such as a second structure, wherein intervening elements, such as an interface structure may be present between the first element and the second element. The term “direct contact” means that a first element, such as a first structure, and a second element, such as a second structure, are connected without any intermediary conducting, insulating or semiconductor layers at the interface of the two elements.

[0024] It will be understood that when an element as a layer, region or substrate is referred to as being “on” or “over” another element, it can be directly on the other element or intervening elements may also be present. In

contrast, when an element is referred to as being “directly on” or “directly over” another element, there are no intervening elements present. It will also be understood that when an element is referred to as being “beneath” or “under” another element, it can be directly beneath or under the other element, or intervening elements may be present. In contrast, when an element is referred to as being “directly beneath” or “directly under” another element, there are no intervening elements present.

[0025] With regard to the fabrication of transistors and integrated circuits, major surface refers to that surface of the semiconductor layer in and about which a plurality of transistors are fabricated, e.g., in a planar process. As used herein, the term “vertical” means substantially orthogonal with respect to the major surface and “horizontal” means substantially parallel to the major surface. Typically, the major surface is along a plane of a monocrystalline silicon layer on which transistor devices are fabricated.

[0026] For integrated circuits, the masking, patterning, and etching of device components makes possible the fabrication of semiconductor devices at the micro and nano scale. As devices, components, and layers continually decrease in size and pitch, however, the etching techniques that have been used in the past can cause unintended consequences. As a specific example, buried power rails of a semiconductor structure can suffer from thermal instability caused during annealing processes. Any metal present in buried power rails can suffer issues during subsequent FEOL thermal processing, such as metal migration and metal diffusion, while the semiconductor structure is heated for the annealing. Additionally or alternatively, the semiconductor structure can stress and/or bow the wafer due to the expansion and contraction of the metals during heating. This unwanted stress/bowing could result in lithography misalignment errors in subsequent mask levels.

[0027] The devices and methods disclosed below address the problems associated with annealing the semiconductor structure and the buried power rail. Rather than forming the buried power rail with metals right after fin formation, therefore, the embodiments disclosed herein fabricate a dummy buried power rail, which is replaced later in the fabrication process by the metalized buried power rail.

[0028] Figure 1 is a schematic cross-sectional side view of a semiconductor structure 100, in accordance with one embodiment of the present invention. The schematic view shows a of row 102 that may include fins 104 fabricated as eventually becoming part of a field-effect transistor (FET) region (e.g., n-type FET (NFET) and p-type FET (PFET)). The illustrated embodiment of the semiconductor structure 100 includes four FET regions: a first NFET region 106a, a second NFET region 106b, a first PFET region 106c, and a second PFET region 106d. The fins 104 are fabricated on a substrate 108 and a BOX SiO2 layer 110, and include layers 112 for controlling signals through a device region of the semiconductor structure 100. The layers 112 may be fabricated by forming epitaxial semiconductor layers sequentially above the bottom-most semiconductor layer above the dielectric layer 110. In one embodiment, the starting wafer is a silicon-on-insulator (SOI) wafer. The substrate 108 can be silicon, and there’s a BOX SiO2 layer 110 above the substrate 108. In certain embodiments, an additional silicon layer (not shown) may be fabricated above the BOX SiO2 layer 110. Firstly, the additional silicon layer above is thinned down

to about 5~10nm, followed by growing a SiGe layer and SiGe condensation process to convert the bottom most semiconductor layer above the BOX to SiGe. After that, the oxide above the SiGe is removed, followed by alternative layers of Si and SiGe layer growth. After that, a hard mask 114 is deposited. A patterning process is applied to the hard mask to define the active regions by conventional lithographical and etch processes. Then the area of the layers 112 that are not protected by the hard mask 114 may be etched away to form the fins 104. Though not illustrated, the layers 112 may be laterally cut in a direction perpendicular to the illustrated direction such that the semiconductor structure 100 may include several fins 104 along a column (i.e., into and out of the page). The open spaces between the fins 104 are then filled with dielectric116, such as SiO2, or a combination of SiN and SiO2 layers. The semiconductor structure 100 may then be planarized, for example with chemical-mechanical planarization (CMP).

[0029] Figure 2 is a schematic cross-sectional side view of the semiconductor structure 100 of Figure 1 at a subsequent fabrication stage, in accordance with one embodiment of the present invention. Figure 2 shows buried power rail (BPR) trenches 118a, b etched through the length of the semiconductor structure 100 (i.e., into and out of the page). Since the BPR trenches 118a, b are continuous along the length of the semiconductor structure 100, the BPR trenches 118a, b may be patterned to a line shape which passed several, or all, of the fins 104 along the direction into and out of the page. The BPR trenches 118a, b may be patterned using a conventional lithographical and etch process, and may be patterned using a different hard mask (not illustrated). First, the hard mask may be patterned (e.g., using lithography and etch processes) so that the BPR trenches 118a, b may be subsequently formed through an etching process. In some embodiments, this etching can be performed using an anisotropic etch such as reactive ion etching (RIE). The BPR trenches 118a, b may be etched through the oxide 116, BOX SiO2 layer 110, and may partially cut into the substrate 108. The BPR trenches 118a, b do not require a large width 120. A narrower BPR trench 118a, b helps protect the fins 104 from being damaged by the BPR patterning process, even at worst case lithographic misalignment.

[0030] The BPR trenches 118a, b are formed between FET regions 106a-d. In the illustrated embodiment of Figure 2, the first BPR trench 118a is formed between the first FET region 106a and the second FET region 106b, which are both NFET region. Likewise, the second BPR trench 118b is formed between the third FET region 106c and the fourth FET region 106d, which are both PFET region. Other embodiments may be conceived in which the BPR trench 118a, b are formed between FET regions that differ in device type.

[0031] Figure 3 is a schematic cross-sectional side view of the semiconductor structure 100 of Figure 1 at a subsequent fabrication stage, in accordance with one embodiment of the present invention. The semiconductor structure 100 includes a dummy buried power rail (BPR) 122a, b within each BPR trench 118a, b. The dummy BPR 122a, b may be formed of a sacrificial material, such as amorphous silicon, which can be selectively etched relative the BOX SiO2 layer 110, and the oxide 116. The dummy BPR 122a, b may be formed using chemical-vapor deposition (CVD), Plasma-enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), or

sputtering. After deposition, the dummy BPR 122a, b may be recessed partially so that a top surface 124a, b is at a height below the top of the BOX SiO2 layer 110. The dummy BPR 122a, b may be etched using a selective etch. Selective in the context of this application means that the etch process etches one material significantly faster than another material. In the instance illustrated in Figure 3, the selective etch process etches the amorphous silicon of the dummy BPR 122a, b significantly faster than the exposed portions of the oxide 116, hard mask 114, or BOX SiO2 layer 110. The amount of recessing of the dummy BPR 122 may change depending on the embodiment, and a recession 126 that is larger or smaller than the illustrated embodiment will not diverge from the disclosed embodiments herein.

[0032] Figure 4 is a schematic cross-sectional side view of the semiconductor structure 100 of Figure 1 at a subsequent fabrication stage, in accordance with one embodiment of the present invention. Figure 4 shows the recession 126 filled with a fill 128 that covers the dummy BPR 122a, b. The fill 128 may include the same, or similar, material to the BOX SiO2 layer 110, and may fill the recession 126 to a top of the hard mask 114 so that the semiconductor structure 100 can then be planarized (e.g., CMP). Following planarization, a FIN reveal process is performed to selectively recess the dielectric 116, 128 (e.g., dilute hydrofluoric (DHF) or buffered oxide etch (BHF) wet etch; or SiCoNi/COR dry etching process can be used) such that the nanosheet stacks (comprising alternative SiGe and Si) are fully exposed while keeping the dummy BPR 122 covered. After that, the hard mask layer 114 can be selectively removed.

[0033] Figures 5A and 5B are schematic cross-sectional side views of the semiconductor structure 100 of Figure 1 at a subsequent fabrication stage, in accordance with one embodiment of the present invention. Figure 5A shows the cross-sectional location of the location illustrated in Figures 1-4, and Figure 5B shows a second view angle that is perpendicular to the view of Figures 1-4. Line A-A in Figure 5B shows the location of Figures 1-4, Figure 5A, and 6-13.

[0034] Figure 5A and 5B shows a process stage after forming a dummy gate 130 with a hard mask 134, spacers 132, inner spacers 135 and S/D epi formation in a device region 136. The gate, spacer and inner spacer formation can be achieved using conventional nanosheet fabrication process. Between the exposed nanosheets, the semiconductor structure 100 has source/drains (S/D) 138, that are formed epitaxially to form a crystalline layer onto the BOX SiO2 layer 110 and between the gates. Epitaxial layers of the S/Ds 138 may be grown from gaseous or liquid precursors. Epitaxial silicon may be grown using vapor-phase epitaxy (VPE), molecular-beam epitaxy (MBE), liquid-phase epitaxy (LPE), or other suitable process. The epitaxial silicon, silicon germanium, and/or carbon doped silicon (Si:C) silicon can be doped during deposition by adding a dopant or impurity to form a silicide. The silicon may be doped with an n-type dopant (e.g., phosphorus or arsenic) or a p-type dopant (e.g., boron or gallium), depending on the type of transistor.

[0035] The epitaxial layers forming the S/Ds 138 may be grown using a suitable growth process, for example, CVD, liquid phase (LP) or reduced pressure chemical vapor deposition (RPCVD), vapor-phase epitaxy (VPE),

molecular-beam epitaxy (MBE), liquid-phase epitaxy (LPE), metal organic chemical vapor deposition (MOCVD), or other suitable processes.

[0036] Figure 6 is a schematic cross-sectional side view of the semiconductor structure 100 of Figure 1, in accordance with one embodiment of the present invention. Figure 6 shows the device region 136 covered by an interlayer dielectric (ILD) 140. The device region 136 may have several stages completed before the ILD 140 is formed. After ILD 140 is formed, several conventional processes are further performed to fabricate the device. For example, gate cut and single diffusion break can be patterned and filled with dielectric, CMP process can be used to polish the ILD and remove the gate hard mask 134 to expose the dummy gate, and the dummy gate 130 and sacrificial SiGe between the Si sheets may be etched away and replaced by a high-k metal gate. The steps of fabricating the high-k gate dielectric and the S/Ds 138 may typically involve heat treatment for steps such as annealing, and the amorphous silicon of the dummy BPR 122a, b does not inhibit the annealing process by diffusing or by buckling. That is, unlike a metal BPR, the dummy BPR 122a, b does not have atoms the spread or diffuse during the annealing process. And since the coefficient of expansion is smaller and closer to the rest of the semiconductor structure 100 (and the wafer on which the semiconductor structure 100 is fabricated), the dummy BPR 122a, b will not cause stress or bow the semiconductor structure 100 during heating stages of the fabrication process.

[0037] Figure 7 is a schematic cross-sectional side view of the semiconductor structure 100 of Figure 1, in accordance with one embodiment of the present invention. Figure 7 shows contacts 142a, b through which controlling signals are sent when the semiconductor structure 100 is finished. The contacts 142a, b include S/D contacts 142a and via-contacts-to-buried power rail (VBPRs) 142b. The contacts 142a, b are formed using conventional lithographic and etch processes through the ILD 140. In certain embodiments, openings for the S/D contacts 142a are formed with one mask, followed by a different mask for the openings of the VBPR 142b. In other embodiments, openings for the S/D contacts 142a and the VBPR 142b may be formed using the same mask. After the S/D contacts 142a,b are etched through the ILD 140 to expose the S/Ds 138 and/or the dummy BPR 122a, b, the openings are metalized to form the contacts 142a, b. The VBPRs 142b contact the dummy BPR 122a, b at a top surface 144.

[0038] Figure 8 is a schematic cross-sectional side view of the semiconductor structure 100 of Figure 1, in accordance with one embodiment of the present invention. Figure 8 shows addition of middle-of-line (MOL) and/or back-end-of-line (BEOL) layers 146 and a carrier wafer 148 bonded to a top surface 150 of the BEOL layer 146. The MOL/BEOL layers 146 include the signal and power wires for controlling the transistors in the device region 136 through the contacts 142a, b. The MOL/BEOL layers 146 include contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections. While the illustrated embodiment is not drawn to scale, modern processes for fabricating the MOL/BEOL layers 146 may include more than ten metal layers. The carrier wafer 148 is bonded to enable the wafer flip and backside processing, including the steps illustrated below. In

certain embodiments, the carrier wafer 148 may be bonded to the BEOL layers 146 through dielectric-dielectric bonding or Cu-Cu bonding.

[0039] Figure 9 is a schematic cross-sectional side view of the semiconductor structure 100 of Figure 1, in accordance with one embodiment of the present invention. Figure 9 shows the semiconductor structure 100 flipped over to complete the steps for power delivery. The carrier wafer 148 supports the semiconductor structure 100 while the substrate 108 is removed from a bottom surface 152, which reveals the dummy BPRs 122a, b. The dummy BPRs 122a, b are then selectively etched from the bottom surface 152 opposite the top surface 150, leaving the BOX SiO2 layer 110 and the VBPR 142b intact and forming a BPR trench 154.

[0040] Figure 10 is a schematic cross-sectional side view of the semiconductor structure 100 of Figure 1, in accordance with one embodiment of the present invention. Figure 10 shows the BPR trench 154 being widened. The BPR trench 154 may be widened using an isotropic etch, which can be controlled to uniformly etch the surfaces inside the BPR trench 154. The etch process may be selective to the BOX SiO2 layer 110 so that the VBPR 142b is not affected, and protrudes into the BPR trench 154. A longer etch of the BPR trench 154 exposes more of the VBPR 142b, while a shorter etch will expose less of the VBPR 142b.

[0041] Figure 11 is a schematic cross-sectional side view of the semiconductor structure 100 of Figure 1, in accordance with one embodiment of the present invention. Figure 11 shows the BPR trench 154 filled to form a BPR 158. The BPR trench 154 may be filled with metals such as copper, cobalt, tungsten, and ruthenium. Prior to the metal fill, a metal adhesion liner 166 is deposited, such as a thin TiN or TaN liner. The BPR 158 is filled with metal or metals so that power may flow through with the least amount of resistance. The BPR 158 is thus able to supply voltage to a number of S/Ds 138 along the length (i.e., in/out of the page) without costing a lot in terms of lost power. This can translate into cooler operation of the semiconductor structure 100 and longer battery life for device utilizing the semiconductor structure 100.

[0042] To further increase efficiency of the BPR 158, the embodiments disclosed herein have a critical dimension 160 that is greater than a distance 162 between the S/Ds 138 above the BPR 158. The critical dimension 160 is determined by the amount of etching of the BPR trench 154. The larger critical dimension 160 is possible due to the etching from the bottom surface 152 rather than trying to etch the BPR trench 154 before forming the contacts 142a, b.

[0043] The BPR 158 also forms a wrap-around contact over the VBPR 142b, which increase the contact area between the VBPR and BPR, which mitigates the concern that VBPR 142b bottom CD is too small that could lead a poor contact between VBPR and BPR.

[0044] While certain embodiments may include the BPR 158 directly contacting the VBPR 142b, the illustrated embodiment includes an adhesion liner 166 between the BPR 158 and the BOX SiO2 layer 110. The adhesion liner

166 may be formed from titanium nitride and tantalum nitride, or similar materials that help the BPR 158 better adhere to the BOX SiO2 layer 110 without deteriorating, diffusing, or shorting to other components of the semiconductor structure 100. As illustrated, the adhesion liner 166 may wrap around the VBPR 142b, and the BPR 158 may wrap around the adhesion liner 166 rather than directly wrapping around the VBPR 142b.

[0045] Figure 12 is a schematic cross-sectional side view of the semiconductor structure 100 of Figure 1, in accordance with one embodiment of the present invention. Figure 12 shows a back side power delivery network (BSPDN) 170 that coupled to the BPR 158 and contains the power delivery components needed for the semiconductor structure 100. The goal of the BSPDN 170 is to provide power and reference voltage to the S/Ds 138 and other devices in the device region 136, in the most efficient way. The BSPDN 170 is a network of interconnects that is separate from the MOL/BEOL layer 146 contained on the opposite side of the device region 136. Traditionally, the power components and the signals components are fabricated through back-end-of-line (BEOL) processing on the frontside (i.e., below the contacts 142a, b in the configuration illustrated in Figure 12). Separating the BSPDN 170 to the backside (i.e., opposite the frontside so the device region 136 is between the frontside and the backside) enables direct power delivery to the device region 136, which enhances system performance, increases chip area utilization, and reduces complexity in the MOL/BEOL layers 146.

[0046] The integrated circuit chips resulting from the processes described herein can be distributed by the fabricator in raw wafer form (that is, as a single wafer that has multiple unpackaged chips), as a bare die, or in a packaged form. In the latter case the chip is mounted in a single chip package (such as a plastic carrier, with leads that are affixed to a motherboard or other higher level carrier) or in a multichip package (such as a ceramic carrier that has either or both surface interconnections or buried interconnections). In any case the chip is then integrated with other chips, discrete circuit elements, and/or other signal processing devices as part of either (a) an intermediate product, such as a motherboard, or (b) an end product. The end product can be any product that includes integrated circuit chips, ranging from toys and other low-end applications to advanced computer products having a display, a keyboard or other input device, and a central processor.

[0047] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms “a,” “an,” and “the” are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms “comprises” and/or “comprising,” when used in this specification, specify the presence of stated features, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0048] While the present application has been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the scope of the present application. It is therefore intended that

the present application to not be limited to the exact forms and details described and illustrated but fall within the scope of the appended claims.

[0049] The descriptions of the various embodiments of the present invention have been presented for purposes of illustration but are not intended to be exhaustive or limited to the embodiments disclosed. Many modifications and variations will be apparent to those of ordinary skill in the art without departing from the scope of the described embodiments. The terminology used herein was chosen to best explain the principles of the embodiments, the practical application or technical improvement over technologies found in the marketplace, or to enable others of ordinary skill in the art to understand the embodiments disclosed herein.

CLAIMS

1. A semiconductor structure, comprising:

a device region comprising a first source/drain (S/D) and a second S/D;

a buried power rail (BPR) under the device region, wherein a critical dimension of the BPR is larger than a distance between the first S/D and the second S/D;

a via-contact-to-buried power rail (VBPR) between the BPR and the S/D.

2. The semiconductor structure of claim 1, wherein the BPR wraps around the VBPR.

3. The semiconductor structure of claim 1, further comprising an adhesion liner between the BPR and an insulator.

4. The semiconductor structure of claim 3, wherein the adhesion liner wraps around the VBPR, and the BPR wraps around the adhesion liner.

5. The semiconductor structure of claim 3, wherein (i) the BPR comprises a selection from the group consisting of: copper, cobalt, tungsten, and ruthenium; and (ii) the adhesion liner comprises a selection from the group consisting of: titanium nitride and tantalum nitride.

6. The semiconductor structure of claim 1, further comprising a back side power delivery network (BSPDN) electrically coupled to the BPR.

7. The semiconductor structure of claim 6, further comprising back-end-of-line (BEOL) layers electrically coupled to the VBPR, wherein the device region is between the BSPDN and the BEOL layers.

8. A method, comprising:

forming a dummy buried power rail (BPR) in an insulator layer between a first fin field-effect transistor (FET) and a second fin FET;

forming a first source/drain (S/D) electrically connected to the first fin FET, and a second S/D electrically connected to the second fin FET;

forming a via-contact-to-buried power rail (VBPR) that contacts a top surface of the dummy BPR and the first S/D;

selectively etching the dummy BPR from a bottom surface opposite the top surface to form a BPR trench; widening the BPR trench; and

metalizing the BPR trench to form a BPR.

9. The method of claim 8, further comprising:

forming the first fin field-effect transistor (FET) of a first doping type before forming the dummy BPR; and forming the second fin FET of the first doping type before forming the dummy BPR.

10. The method of claim 8, wherein forming the dummy BPR comprises depositing amorphous silicon into a dummy BPR trench between the first fin FET and the second fin FET.

11. The method of claim 8, wherein widening the BPR trench comprises selectively etching the insulator layer without etching the VBPR.

12. The method of claim 8, wherein widening the BPR trench comprises widening to a critical dimension that is greater than a distance between the first S/D and the second S/D.

13. The method of claim 8, further comprising forming an adhesion liner within the BPR trench before metalizing the BPR trench.

14. The method of claim 13, wherein the adhesion liner wraps around the VBPR, and the BPR wraps around the adhesion liner.

15. A semiconductor structure, comprising:

a back side power delivery network (BSPDN);

a buried power rail (BPR) coupled to the BSPDN;

a via-contact-to-buried power rail (VBPR) coupled to the BPR, wherein the BPR wraps around a bottom of the VBPR;

a first source/drain (S/D) coupled to a middle of the VBPR; and

a back-end-of-line layer coupled to a top of the VBPR.

16. The semiconductor structure of claim 15, further comprising a second S/D, wherein a critical dimension of the BPR is larger than a distance between the first S/D and the second S/D.

17. The semiconductor structure of claim 16, wherein the VBPR passes between the first S/D and the second S/D to connect to the BPR.

18. The semiconductor structure of claim 15, further comprising an adhesion liner between the BPR and an insulator.

19. The semiconductor structure of claim 18, wherein the adhesion liner wraps around the VBPR, and the BPR wraps around the adhesion liner.

20. The semiconductor structure of claim 18, wherein (i) the BPR comprises a selection from the group consisting of: copper, cobalt, tungsten, and ruthenium; and (ii) the adhesion liner comprises a selection from the group consisting of: titanium nitride and tantalum nitride.

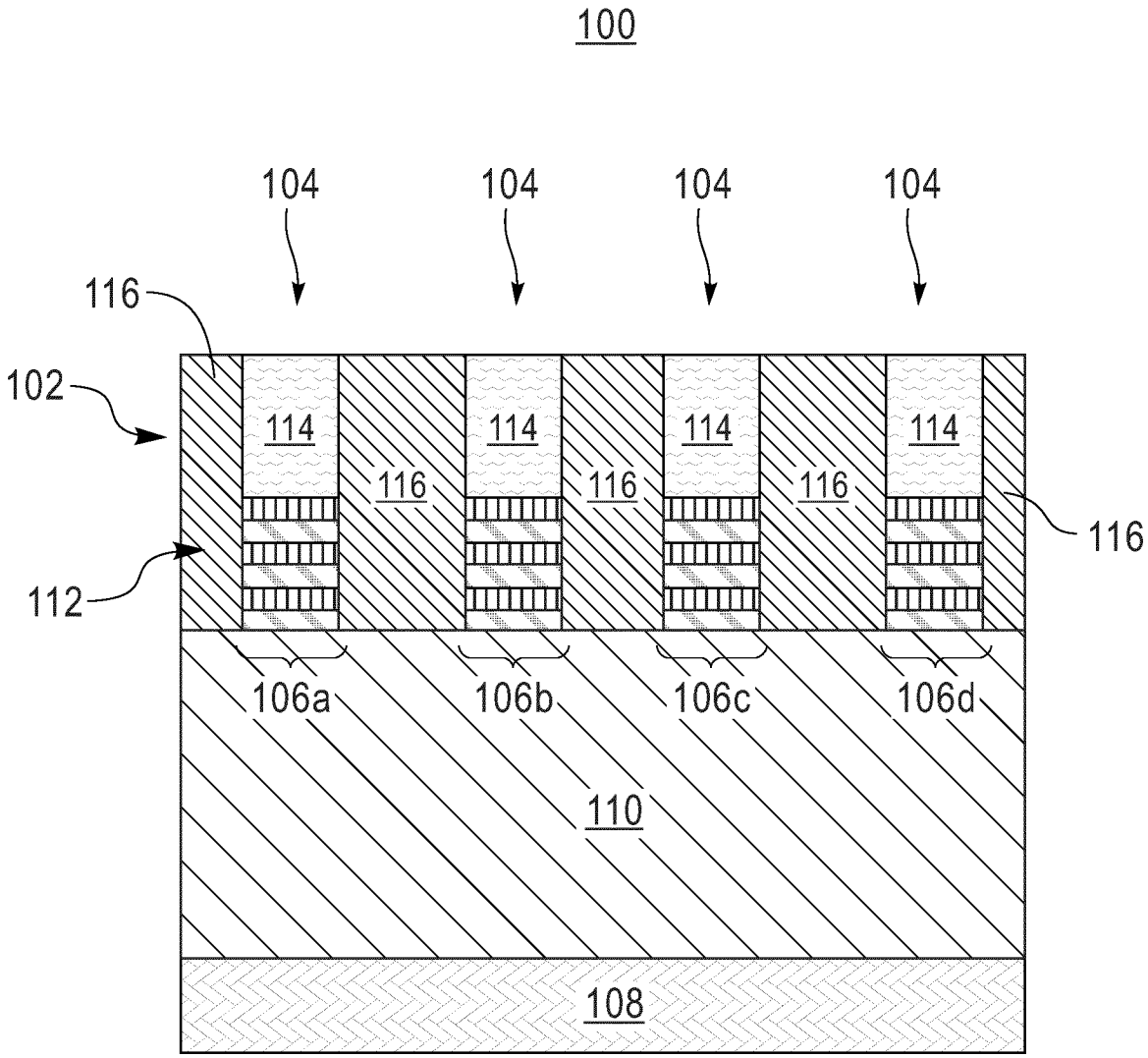
100
104
104
104
104
116
102
114
114
114
114
116
116
116
116
112
106a
106b
106c
106d
110
108

FIG. 1

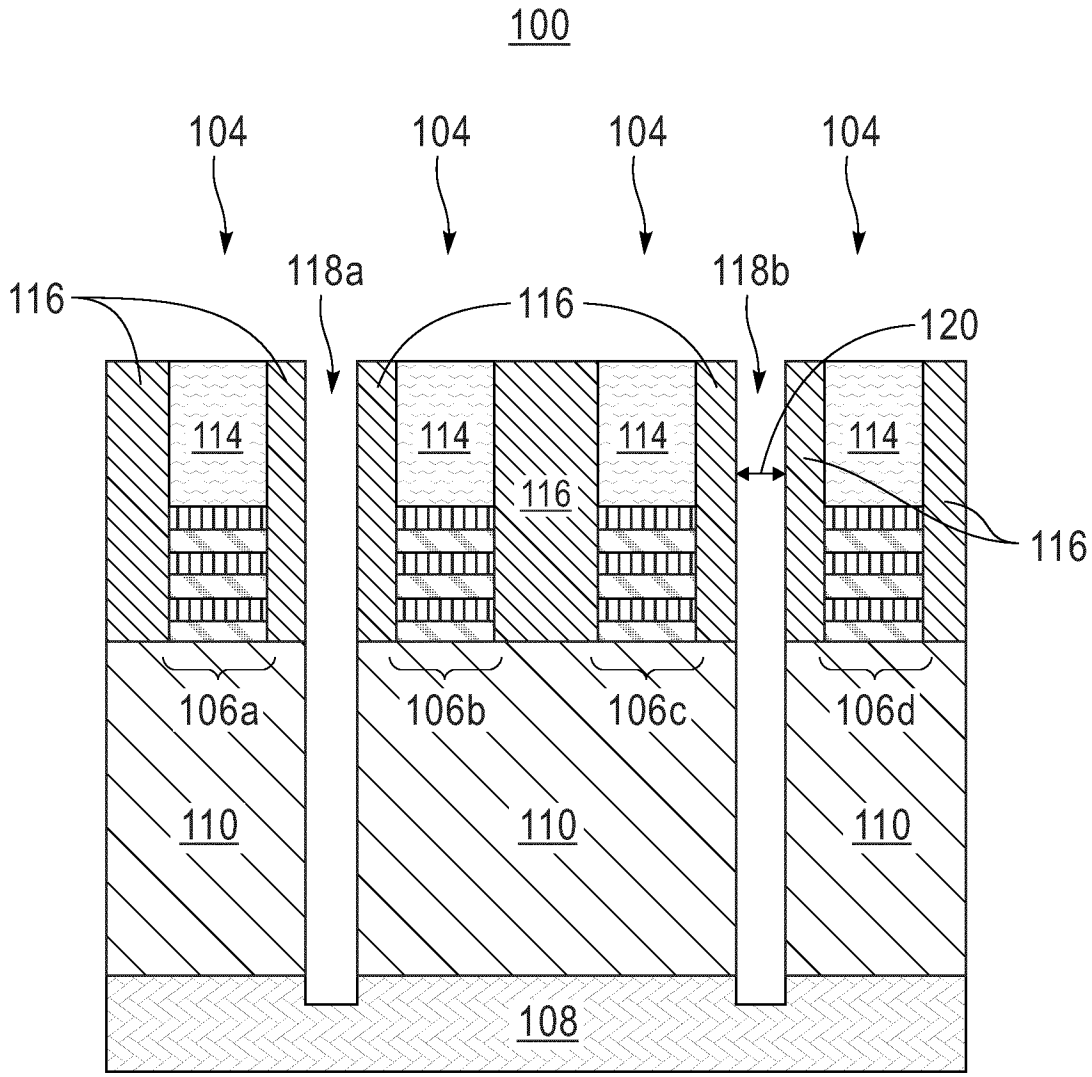
100
104
104
104
104
118a
118b
116
116
120
114
114
114
114
116
116
106a
106b
106c
106d
110
110
110
108

FIG. 2

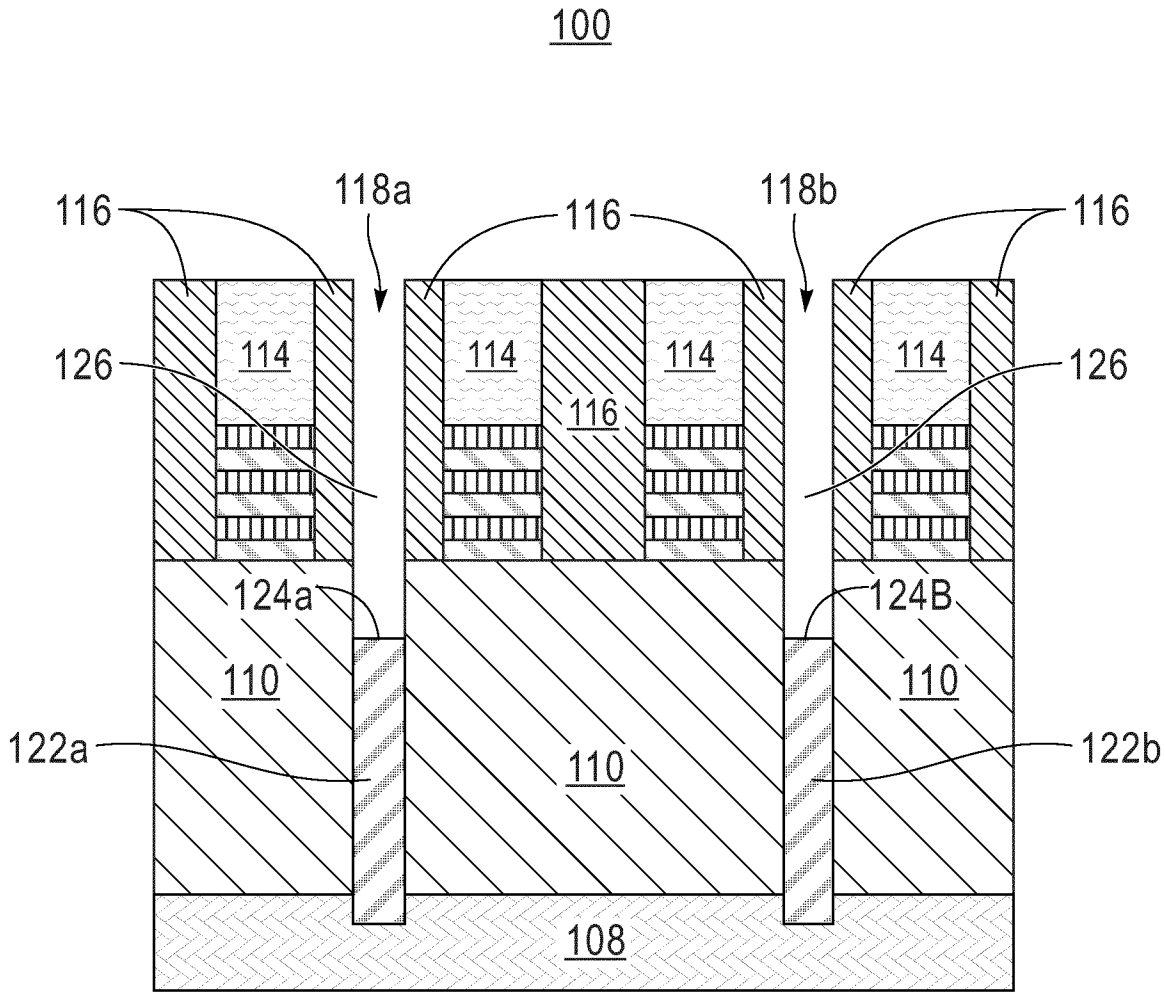
100
116
118a
116
118b
116
114
114
114
114
126
126
116
124a
124B
110
110
122a
110
122b
108

FIG. 3

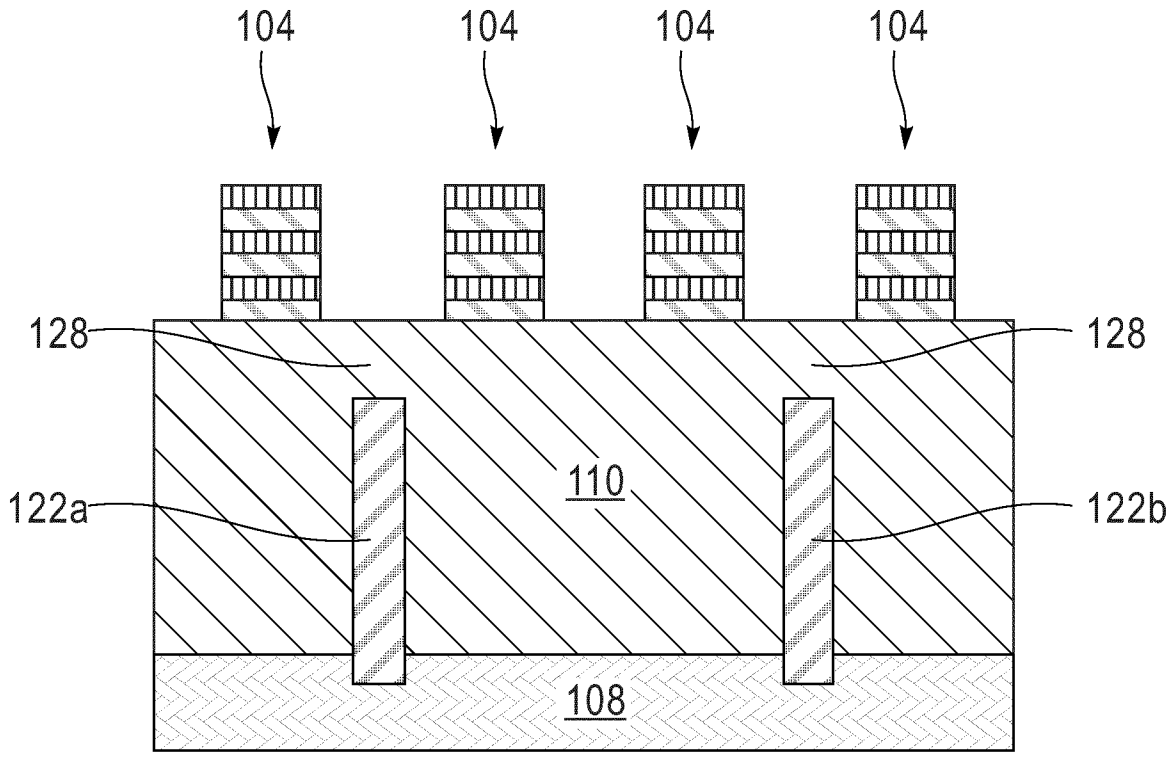
104
104
104
104
128
128
110
122a
122b
108

FIG. 4

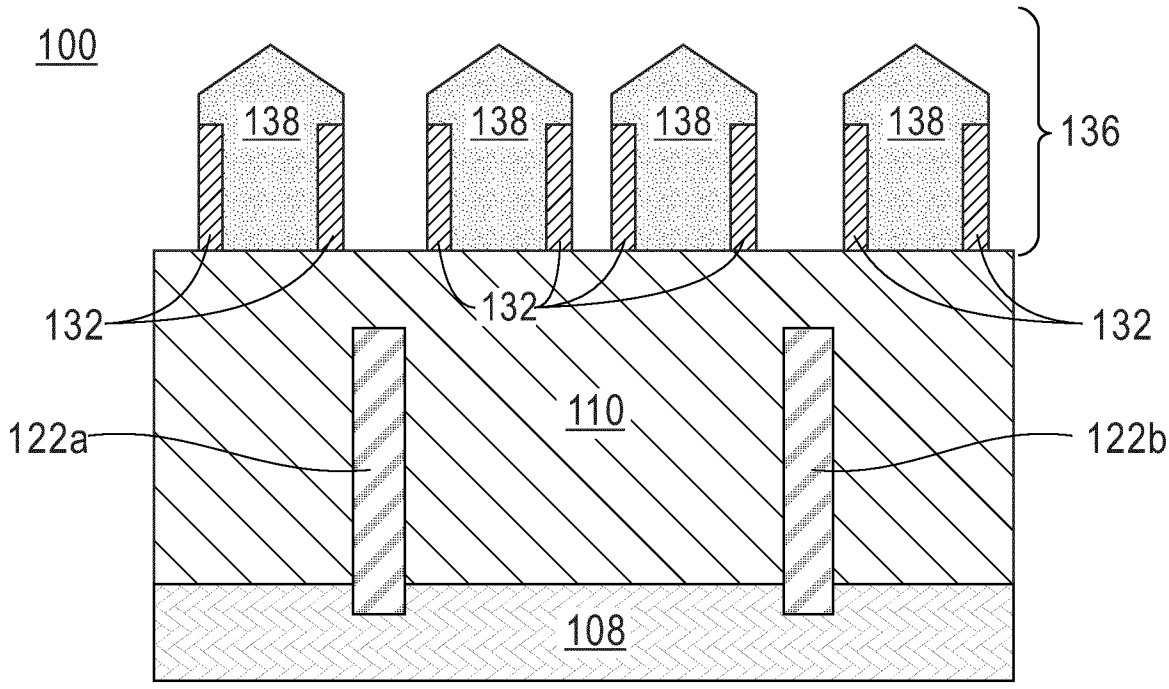
100
138
138
138
138
136
132
132
132
110
122a
122b
108

FIG. 5A

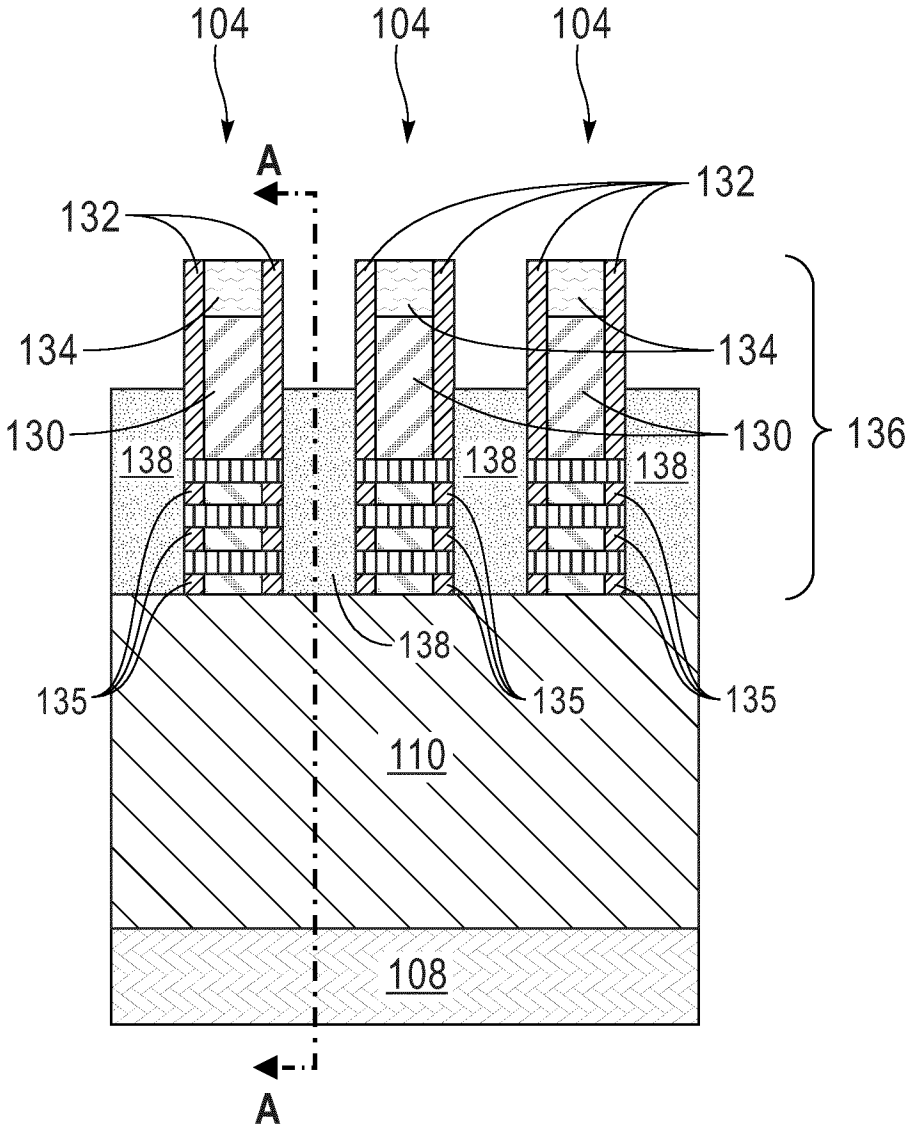
104
104
104
A
132
132
134
134
130
130
136
138
138
138
138
135
135
135
110
108
A

FIG. 5B

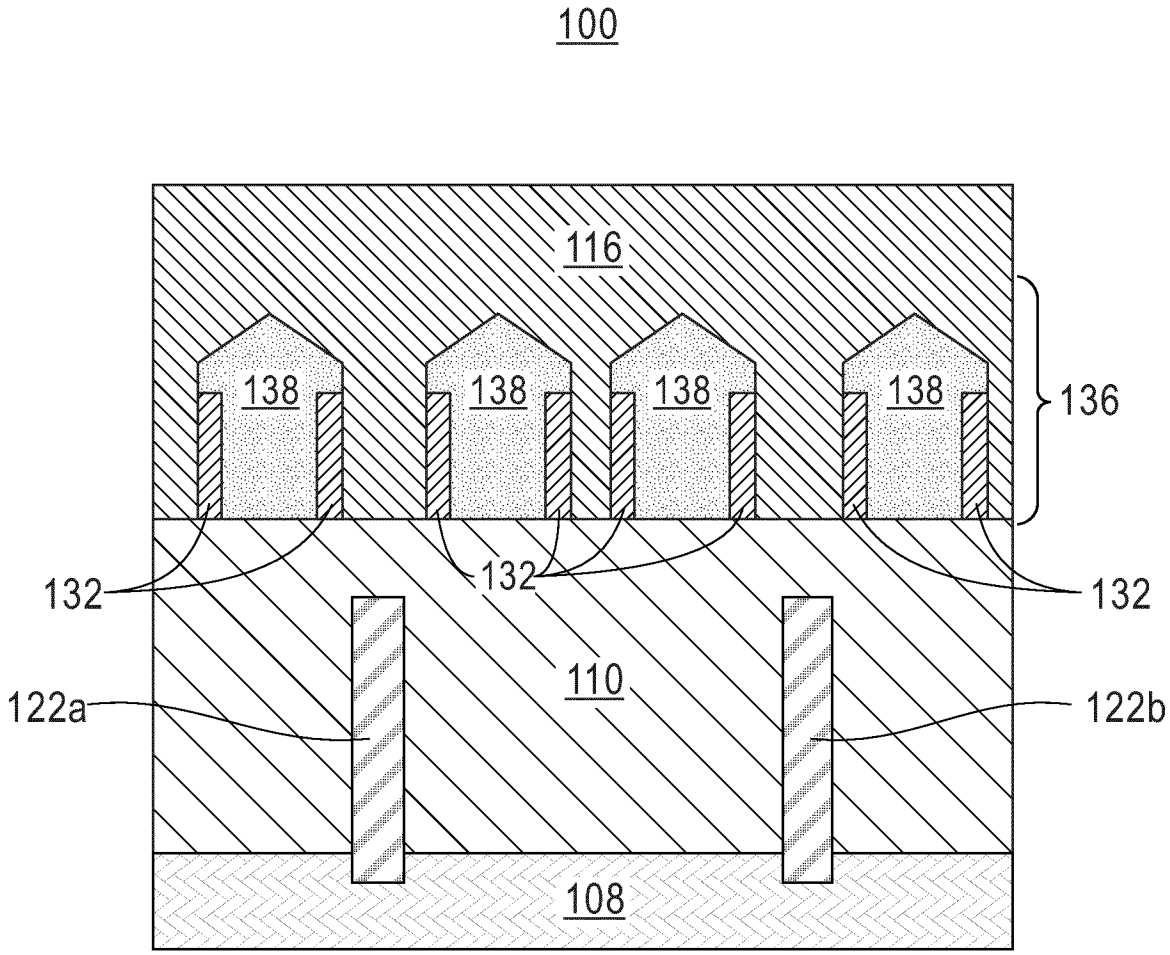

FIG. 6

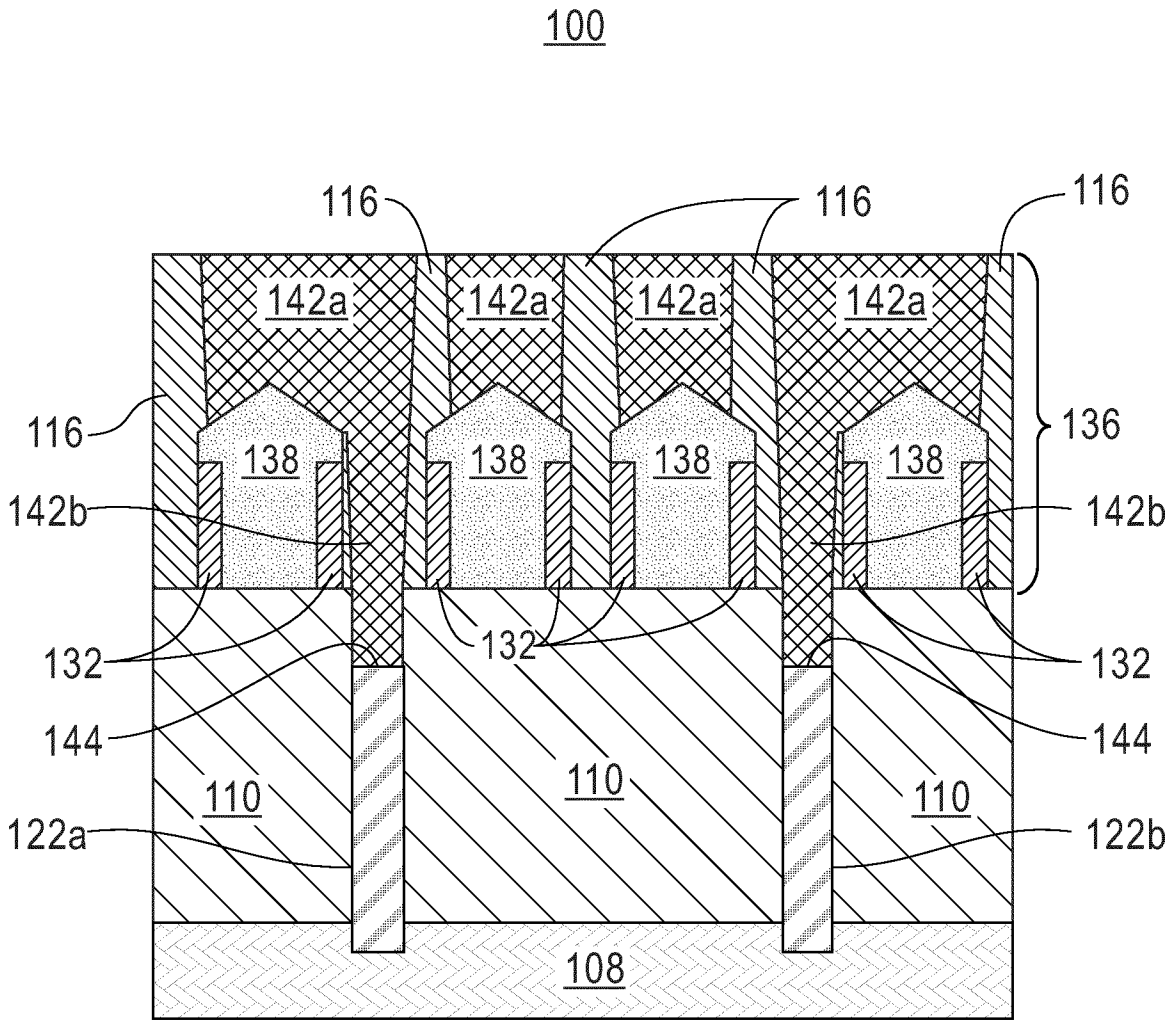
100
116
116
116
142a
142a
142a
142a
116
136
138
138
138
138
142b
142b
132
132
132
144
144
110
110
110
122a
122b
108

FIG. 7

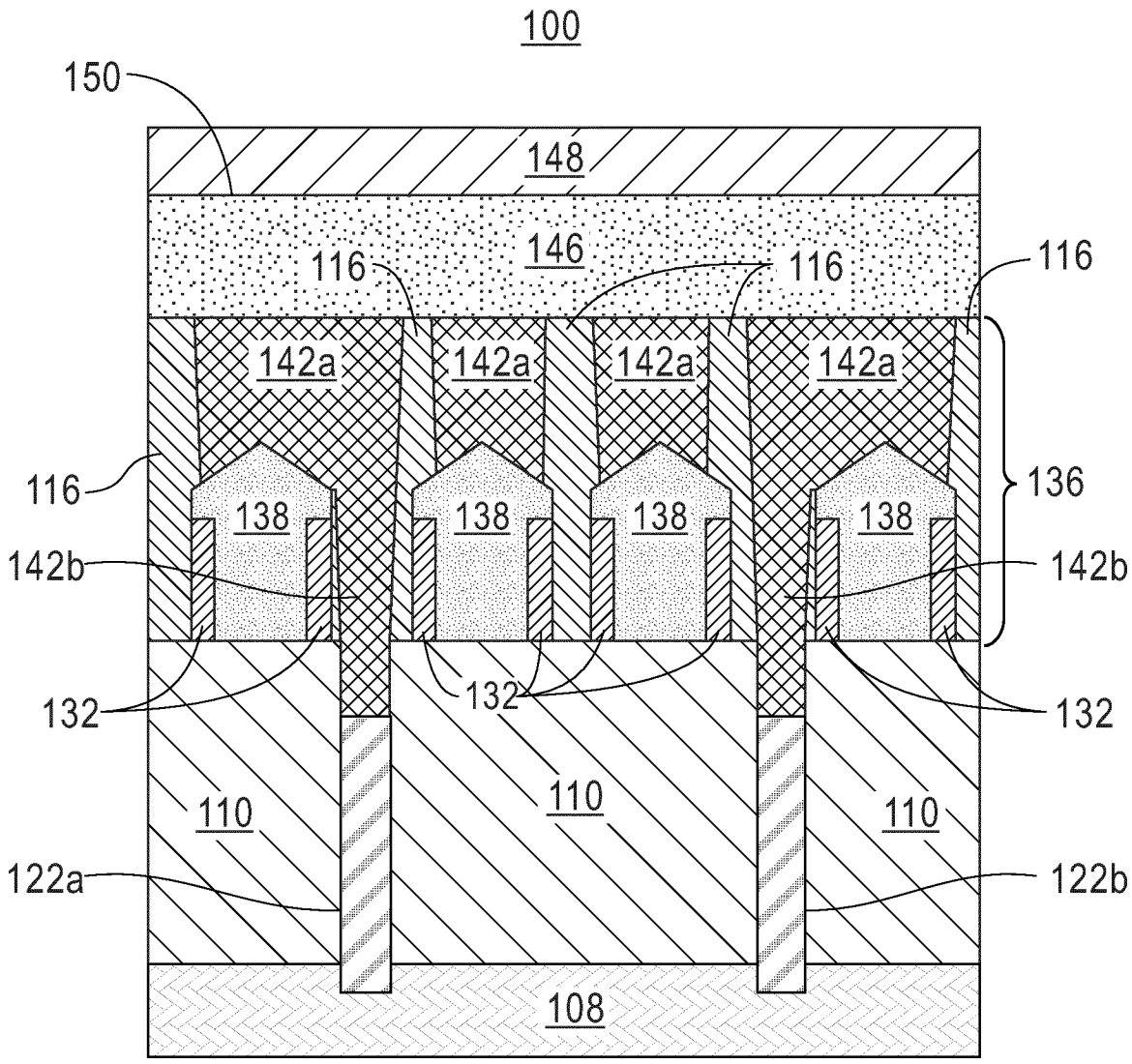
100
150
148
146
116
116
116
142a
142a
142a
142a
116
136
138
138
138
138
142b
142b
132
132
132
110
110
110
122a
122b
108

FIG. 8

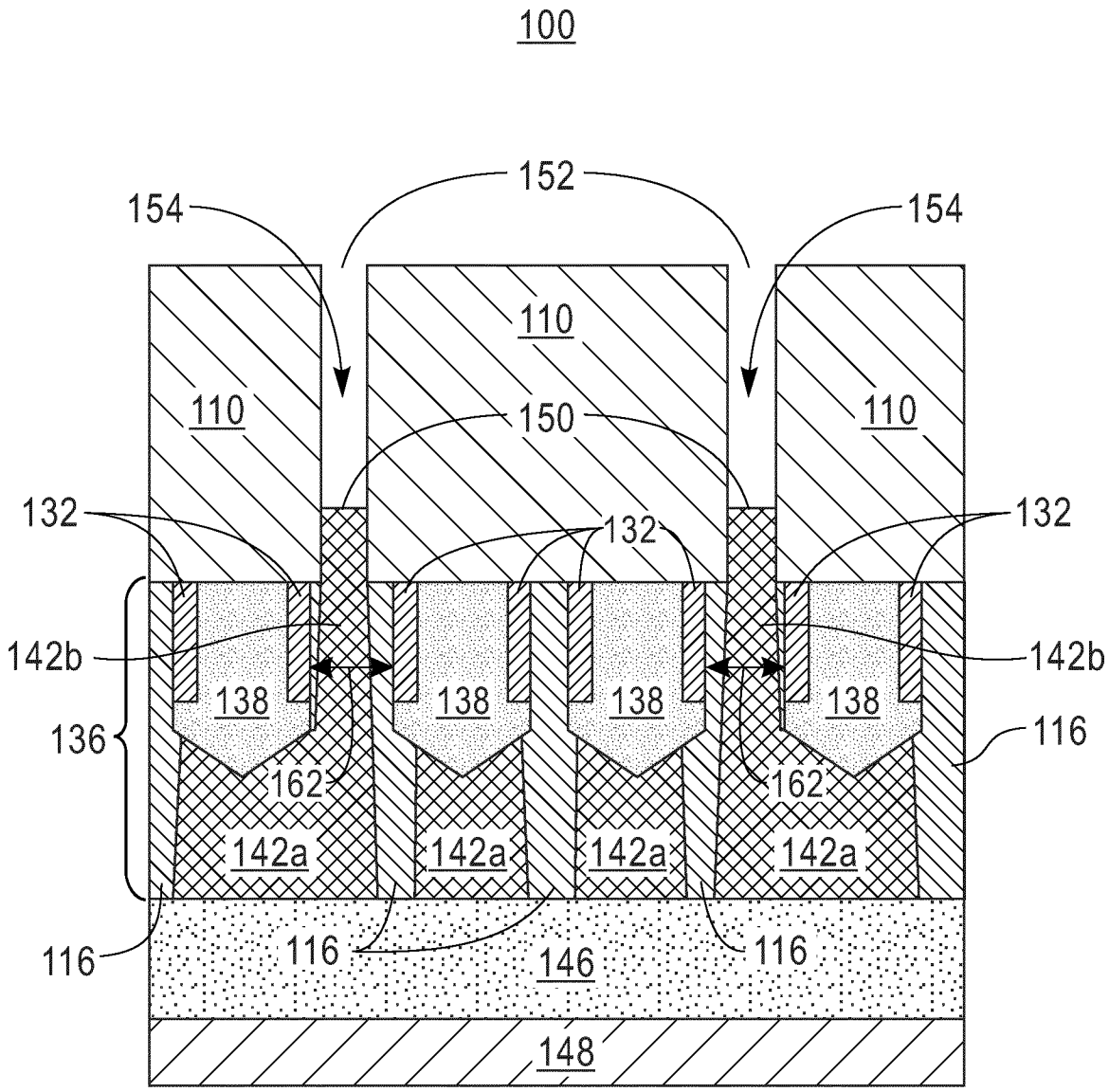
100
152
154
154
110
110
110
150
132
132
132
142b
142b
138
138
138
138
136
116
162
162
142a
142a
142a
142a
116
116
116
146
148

FIG. 9

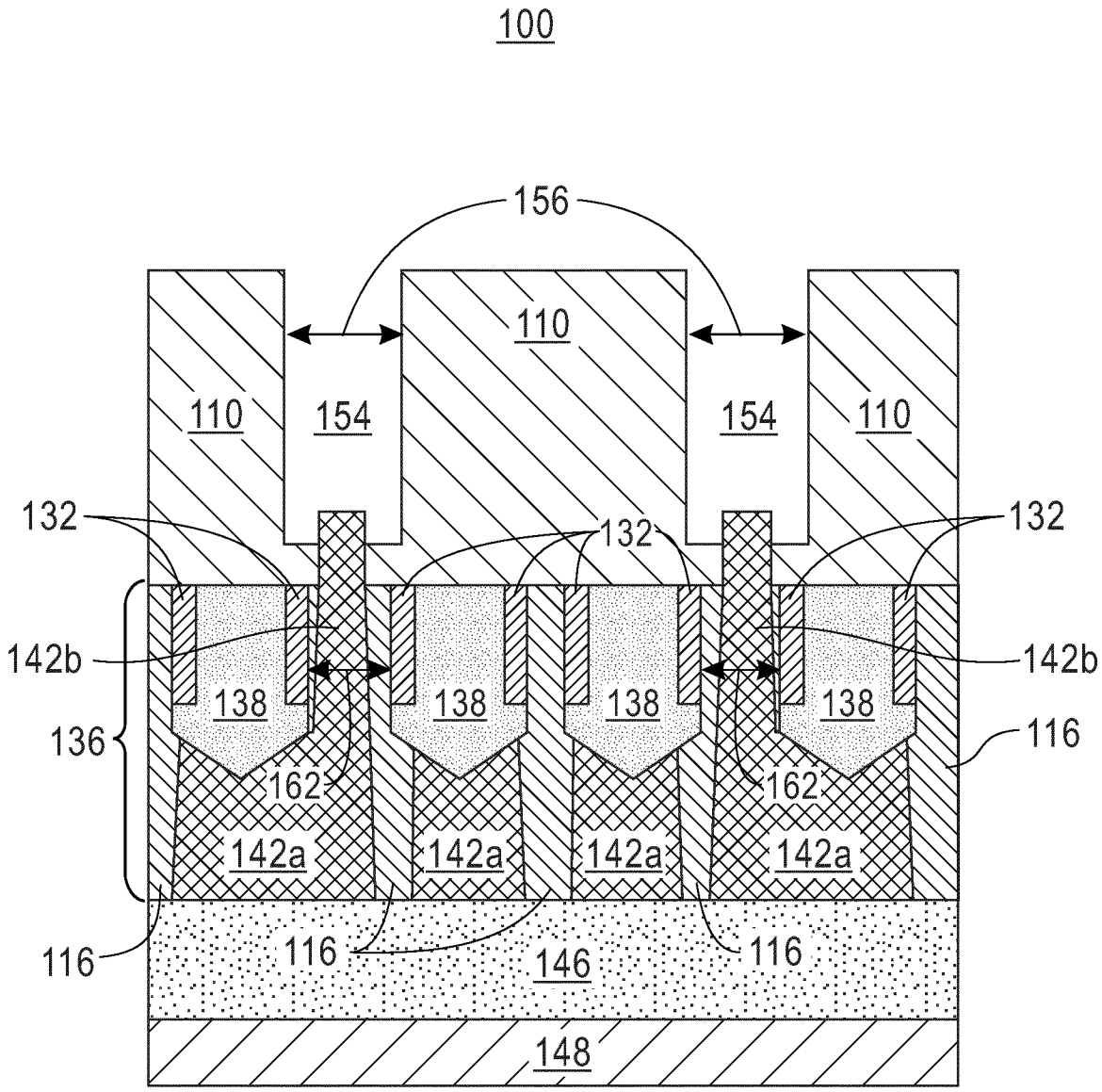
100
156
110
110
154
154
110
132
132
132
142b
142b
138
138
138
138
136
116
162
162
142a
142a
142a
142a
116
116
116
146
148

FIG. 10

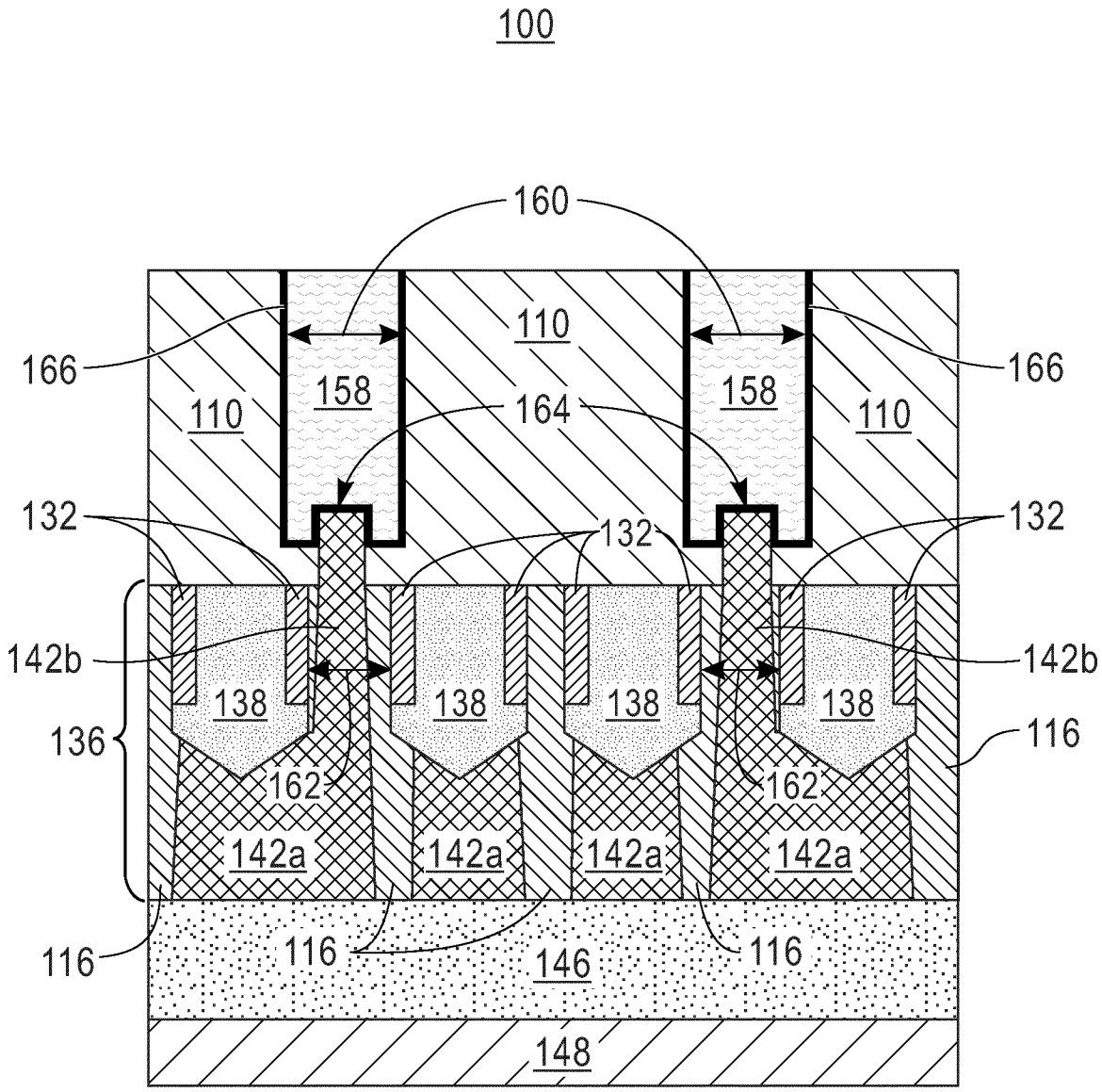
100
160
166
110
158
158
166
110
164
110
132
132
132
142b
142b
138
138
138
138
136
116
162
162
142a
142a
142a
142a
116
116
116
146
148

FIG. 11

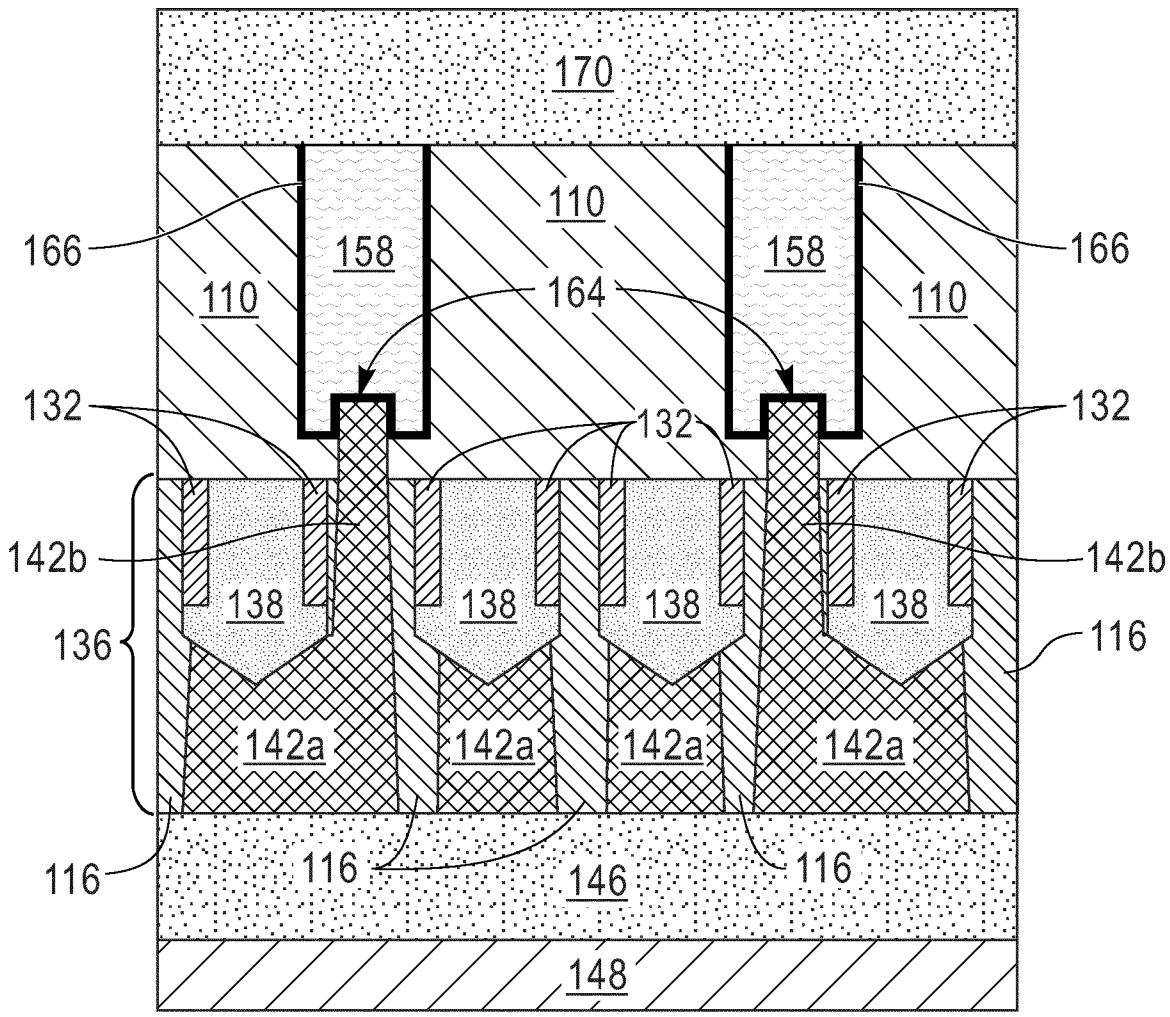
100
170
110
166
158
158
166
110
164
110
132
132
132
142b
142b
138
138
138
138
136
116
142a
142a
142a
142a
116
116
116
146
148

FIG. 12

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2022/078559

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L23/535 H01L21/768 H01L29/78 H01L23/528
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GUPTA ANSHUL ET AL: "Buried Power Rail Integration With FinFETs for Ultimate CMOS Scaling", IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE, USA, vol. 67, no. 12, 16 November 2020 (2020-11-16), pages 5349-5354, XP011821463, ISSN: 0018-9383, DOI: 10.1109/TED.2020.3033510 [retrieved on 2020-11-23] page 5349 - page 5350; figure 1 -----	1-7, 15-20
X	US 2021/336019 A1 (SU HUAN-CHIEH [TW] ET AL) 28 October 2021 (2021-10-28) paragraphs [0048] - [0062]; figures 19-29 -----	8-14

-/--

[x] Further documents are listed in the continuation of Box C.

[x] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 January 2023	07/02/2023

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Franche, Vincent

1

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No
PCT/EP2022/078559

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PRASAD DIVYA ET AL: "Buried Power Rails and Back-side Power Grids: Arm CPU Power Delivery Network Design Beyond 5nm", 2019 IEEE INTERNATIONAL ELECTRON DEVICES MEETING (IEDM), IEEE, 7 December 2019 (2019-12-07), XP033714522, DOI: 10.1109/IEDM19573.2019.8993617 [retrieved on 2020-02-10] the whole document -----	1-20

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/EP2022/078559

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2021336019 A1	28-10-2021	DE 102020135005 A1	28-10-2021
		KR 20210132587 A	04-11-2021
		US 2021336019 A1	28-10-2021