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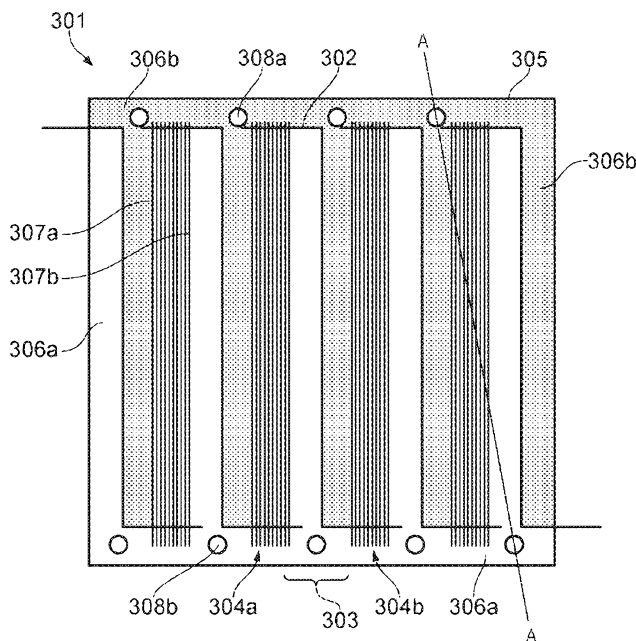


FIG. 1a

(57) Abstract: An optoelectronic device and method of producing the same. The optoelectronic device comprises a substrate having a first and a second substantially planar face. A series of grooves in the first substantially planar face, the series of grooves including a first outermost groove and a second outermost groove and a first and a second aperture in the substrate. The first aperture provides electrical communication between the first outermost groove and the second substantially planar face of the substrate and the second aperture provides separate electrical communication between the second outermost groove and the second substantially planar face of the substrate. The second substantially planar face of the substrate further comprises a first and a second electrical conductor, the first and second electrical conductors being electrically insulated from one another.



OPTOELECTRONIC DEVICE AND METHOD OF PRODUCING THE SAME

The present invention relates to an optoelectronic device and more specifically a solar photovoltaic cell.

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The term photovoltaic refers to the production of electricity, normally direct electrical current, from light at the junction between two materials that are exposed to the light. The light is normally sunlight and therefore photovoltaic is often referred to as solar photovoltaic. It is known to use semiconductors for the two materials. The
10 semiconductor materials used exhibit a photovoltaic effect.

The two materials are usually semiconductors, a p-type and an n-type semiconductor material. When joined together the boundary or interface between the two types of semiconductor material is referred to as a p-n junction. This type of p-n junction is
15 usually created by doping one material with the other material. The doping may be by diffusion, ion implantation or epitaxy. The later involves growing a second layer of crystal doped with one type of dopant on top of a first layer of crystal doped with a different type of dopant.

20 The p-n junction can be found in most optoelectronic devices that use semiconductors. These optoelectronic devices include photovoltaic or solar photovoltaic cells, diodes, light-emitting diodes (LEDs) and transistors. The p-n junction can be thought of as the active site where the generation or consumption of electrical energy occurs.

25 The demand for sources of renewable energy has driven significant improvements in the cost and efficiency of solar photovoltaic cells but existing technology still represents a relatively expensive method of generating electricity. Also, existing solar photovoltaic cells are relatively inefficient compared to other methods of generating electricity and are relatively fragile, that is they are relatively easily damaged.

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One of the problems with existing solar photovoltaic cells is the difficulty in extracting and/or collecting electrical charge from the solar photovoltaic cell. The present invention aims to mitigate one or more of the disadvantages of existing solar photovoltaic cells.

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In accordance with a first aspect of the present invention there is provided an optoelectronic device comprising:

a substrate having a first and a second substantially planar face;

a series of grooves in the first substantially planar face, the series of grooves including a first outermost groove and a second outermost groove; and

a first and a second aperture in the substrate;

wherein the first aperture provides electrical communication between the first outermost groove and the second substantially planar face of the substrate and the second aperture provides separate electrical communication between the second outermost groove and the second substantially planar face of the substrate.

In use, the first and second apertures are typically used to carry electrical charge between the first and the second substantially planar faces of the substrate, and typically from the first to the second substantially planar face of the substrate.

The first and second apertures typically each have a side or sides. The side or sides may be referred to as an internal surface/internal surfaces. The side or sides of the first and second apertures typically comprise the substrate. The side or sides of the first and second apertures, and therefore the substrate that the side or sides comprise, may provide the electrical communication. The first and second apertures may be empty and/or hollow.

The second substantially planar face of the substrate typically further comprises a first and a second electrical conductor. The first and second electrical conductors are normally electrically insulated from one another, thereby helping to provide the separate electrical communication between the second outermost groove and the second substantially planar face of the substrate.

The first aperture typically passes through the first substantially planar face of the substrate proximate to the first outermost groove and through the first electrical conductor on the second substantially planar face of the substrate. The second aperture typically passes through the first substantially planar face of the substrate proximate to the second outermost groove and through the second electrical conductor on the second substantially planar face of the substrate.

The first and second electrical conductors may provide and/or be part of the positive and negative poles of an electrical circuit. The first and second electrical conductors may comprise one or more of aluminium, copper, silver, zinc, lead, antimony, gold, nickel, bismuth, and indium.

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It may be an advantage of the present invention that in use, the first and second electrical conductors are used to collect from and/or convey an electrical charge along a length of the optoelectronic device, these electrical conductors having a lower electrical resistance compared to the first substantially planar face and/or the series of
10 grooves. This typically means that the length of the optoelectronic device and hence the number of grooves and/or number of series of grooves can be increased without an otherwise corresponding decrease in the electrical charge that can be collected.

The first and second apertures may be two of the plurality of apertures. The plurality of
15 apertures may comprise a first group of apertures including the first aperture and a second group of apertures including the second aperture. The apertures of the first group of apertures may all pass through and/or be in electrical communication with the first electrical conductor. The apertures of the second group of apertures may all pass through and/or be in electrical communication with the second electrical conductor.

20

The first and second apertures may have a diameter of from 0.5 to 2000 microns, typically from 10 to 50 microns. There may be at least one aperture for every from 3 to 10cm² of the substrate, typically at least one aperture for every 5cm² of the substrate. It may be an advantage of the present invention that the number of apertures in the
25 substrate is such that the substrate is not structurally weakened. The substrate is typically flexible.

The apertures of the first group of apertures may be connected in parallel to the first electrical conductor. The apertures of the second group of apertures may be
30 connected in parallel to the second electrical conductor.

The first and second electrical conductors may be referred to as first and second bus bars. The first and second electrical conductors may be referred to as first and second collecting strips.

35

The first and second apertures may holes and/or slots. The first and second holes may have a circular cross-section. The first and second holes may be square and/or have a square cross-section. The first and second slot may be elongate in one dimension. The first and second slot may be elongate in the x-axis or y-axis.

5

The first and second apertures in the substrate typically have the same shape and/or design. The first and second apertures may be described as passing through the substrate.

10 The first and second apertures may be at least partially, typically substantially filled with a filler material. The filler material is typically an electrical conductor. The electrical conductor may be an ink. The ink may be a conductive ink. The filler material, typically the ink, may be substantially organic or substantially inorganic. The filler material, typically the ink, may comprise an organic binder. The filler material, typically the ink,
15 may comprise one or more of carbon, silver, copper and lead.

In use, the electrical communication may include the transfer of an electrical charge. The electrical charge typically includes an electrical current.

20 The series of grooves may comprise a first and a second series of grooves. The substrate may further comprise a channel between the first and second series of grooves.

Each groove of the series of grooves or the first and second series of grooves typically
25 has a first and a second face and a cavity therebetween. The cavity is normally at least partially filled with a first semiconductor material. The first face is normally coated with a conductor material and the second face coated with a second semiconductor material. The channel typically also transects the grooves of the first and second series of grooves.

30

The side or sides of the first and second apertures are normally coated with the conductor material and/or the semiconductor material. The aspect ratio of the depth to the width of the first and second apertures is typically such that the conductor material and/or the semiconductor material coats enough of the side or sides of the first and
35 second apertures to establish the electrical communication between the first and second outermost grooves and the second substantially planar face of the substrate.

The first and second apertures may be at least partially filled with the filler material to increase the reliability and/or effectiveness of the electrical communication between the first and second outermost grooves and the second substantially planar face of the substrate.

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The first and second apertures may have been formed by an elongate member being pushed through the substrate from the first and/or second substantially planar face. The elongate member may remain in the substrate during use. The elongate member may provide the electrical communication between the first or second outermost
10 groove and the second substantially planar face of the substrate.

The elongate member may be a pin or a nail. The elongate member may be sized such that when it is in the aperture, the elongate member is in contact with the conductor material and/or the semiconductor material on the sides of the aperture.

15

Contact between the elongate member and the conductor material and/or the semiconductor material on the sides of the aperture typically helps provide the electrical communication between the first and second outermost grooves and the second substantially planar face of the substrate.

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The side or sides of the first and second apertures extending between, and in electrical communication with, the first and second substantially planar faces of the substrate may be coated with one or more of the conductor material, the first semiconductor material and the second semiconductor material. It is typically one or more of the conductor material, the first semiconductor material and the second semiconductor
25 material that provides the electrical communication between the first outermost groove and the second substantially planar face of the substrate and the second outermost groove and separately the second substantially planar face of the substrate.

25

When the first and second apertures are at least partially filled with the filler material, it
30 may be the filler material that provides the electrical communication between the first outermost groove and the second substantially planar face of the substrate and the second outermost groove and the second substantially planar face of the substrate.

30

When the side or sides of the first and second apertures extending between, and in
35 electrical communication with, the first and second substantially planar faces of the substrate are coated with one or more of the conductor material, the first

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semiconductor material and the second semiconductor material and the first and second apertures are at least partially filled with the filler material, it may be one or more of the conductor material, the first semiconductor material and the second semiconductor material and the filler material that provides the electrical
5 communication between the first outermost groove and the second substantially planar face of the substrate and the second outermost groove and the second substantially planar face of the substrate.

The channel typically separates the first and second series of grooves such that an
10 electrical current can be taken from or supplied to the first series of grooves in isolation from the second series of grooves.

The first and second series of grooves are typically elongate grooves. The channel
15 between the first and second series of grooves is typically an elongate channel.

The channel typically transects the grooves of the first and second series of grooves at or towards an end of each groove. The channel typically transects or crosses the grooves of the first series of grooves towards an end of each groove and then passes
20 between the first and second series of grooves before transecting or crossing the grooves of the second series of grooves towards an opposite and/or opposing end of each groove.

The first and second faces of each of the grooves of the first and second series of grooves may be coated with the conductor material. The first and second faces of
25 each of the grooves of the first and second series of grooves may be coated with the second semiconductor material.

The second face may be coated with the second semiconductor material and the first face coated with a third semiconductor material. The first semiconductor material at
30 least partially filling the cavity may be an intrinsic semiconductor.

The first and second faces of each of the grooves of the first and second series of grooves may be referred to as the integral first and integral second faces respectively. The integral first face is normally at a first angle relative to a normal from the substrate
35 and the integral second face at a second angle relative to a normal from the substrate.

The first angle is normally from 45 to less than 90°. The second angle is normally from 45 to less than 90°.

The first semiconductor material is typically a p-type semiconductor material. The
5 second semiconductor material is typically an n-type semiconductor material. The p-type semiconductor is therefore normally in the cavity of the grooves.

In an alternative embodiment the first semiconductor material is an n-type
10 semiconductor material and the second semiconductor material is a p-type semiconductor material.

The n-type and p-type semiconductors may comprise one or more of silicon,
amorphous silicon, hydrogenated amorphous silicon, aluminium, germanium, gallium
nitride, gallium arsenide, aluminium phosphide, aluminium arsenide, copper iodide,
15 zinc oxide and any other semiconductor.

The n-type semiconductor typically comprises one or more of silicon, germanium,
phosphorus, selenium, tellurium, cadmium sulphide, Copper Zinc Tin Sulfide (CZTS),
Quantum Dot (QD) materials for example lead sulphide and organic materials for
20 example perovskites.

The p-type semiconductor typically comprises one or more of silicon, germanium,
cadmium telluride, copper indium gallium selenide, lead sulphide, cadmium telluride,
copper indium gallium diselenide ('CIGS'), copper oxide, boron, beryllium, zinc,
25 cadmium, Copper Zinc Tin Sulfide (CZTS), Quantum Dot (QD) materials for example
lead sulphide and organic materials for example perovskites.

The first and second semiconductor materials may meet at an interface and/or
boundary. The interface is typically referred to as a p-n junction. The first and second
30 semiconductor materials may together be referred to as an active material.

The active material may be deposited in the cavity and on the first and/or second face
of the cavity and may provide ohmic and rectifying contacts for insertion or extraction of
charge from the active material. The active material may be one or more of
35 photovoltaic, light emitting and ion conducting.

The second face may be coated with a conductor material and the second semiconductor material. The conductor material coated on the first face may be the same as the conductor material coated on the second face but it may be different. The conductor material coated on the first and/or second face may comprise one or more of
5 aluminium, bismuth, cadmium, chromium, copper, gallium, gold, indium, lead, magnesium, manganese, samarium, scandium, silver, tin and zinc.

The second semiconductor material may be an electron blocking material such as molybdenum trioxide. The first semiconductor material may be a heterojunction, that is
10 a mixture of one or more of a p-type semiconductor, n-type semiconductor and donor acceptor material.

Typically a portion, normally a substantial portion, of the first and second series of grooves and channel therebetween are substantially parallel, typically parallel to one
15 another. The channel may extend across the first and second series of grooves and typically across the end of the first and second series of grooves. The channel may extend across the first and second series of grooves and typically across opposing ends of the first and second series of grooves.

In an alternative embodiment a portion, normally a substantial portion, of the first and second series of grooves and channel therebetween may be offset from one another, that is not parallel to one another.
20

The channel may extend both perpendicular to and parallel to the first and second series of grooves. Normally the channel is perpendicular to the first and second series
25 of grooves when it extends across the ends of the first and second series of grooves. Normally the channel is parallel to the first and second series of grooves when it extends between the first and second series of grooves. The angle at which the channel may extend across the ends of the first and second series of grooves can be
30 variable and optionally be from 0 to 90°, normally from 35 to 55° and typically be 45°.

When the channel extends both perpendicular to and parallel to the first and second series of grooves, the channel may be referred to as running in at least two directions to connect said first and second series of grooves. When the channel extends
35 substantially perpendicular and across the ends of the first and second series of grooves, it may also extend in at least two directions relative to the first and second

series of grooves. When the channel extends in at least two directions relative to the first and second series of grooves it typically forms a zigzag shape.

5 A surface of the substrate comprising the first and second series of grooves and a channel therebetween may be referred to as a structured surface. The structured surface is typically not flat. The substrate may have another surface that is flat.

10 The channel may be referred to as a delineation feature. The channel typically separates the first and second series of grooves. The channel typically has a first and a second face and a channel cavity therebetween. At least the first face of the channel may be coated with the conductor material and the second face of the channel may be coated with the second semiconductor material. The second face of the channel may also be coated with the conductor material. The channel cavity between the first and second faces of the channel is normally at least partially filled with the first
15 semiconductor material.

The channel typically has a first face at a first angle relative to a normal from the substrate and a second face at a second angle relative to a normal from the substrate. The first face of the channel and the second face of the channel may be perpendicular
20 to the plane of the substrate. The first angle is normally from 45 to less than 90°. The second angle is normally from 45 to less than 90°.

The first semiconductor material in the cavity, second semiconductor material on the second face and conductor material on at least the first face of each groove of the first
25 and second series of grooves are normally all in electrical communication. The electrical communication is such that normally an electrical current can flow between the first and second semiconductor materials and the conductor material.

30 There is usually no electrical communication between the first semiconductor material in the channel cavity, second semiconductor material on the second face and conductor material on at least the first face of the channel.

The depth of the first semiconductor material in the cavity between the first and second faces of each of the first and second series of grooves is substantially the same or at
35 least similar to the depth of the first semiconductor material in the channel cavity between the first and second faces of the channel.

A first side and a second side of the channel may provide the positive and negative poles of an electrical circuit. The first and second sides may be in electrical communication with the conductor material on the first and second faces of the channel. The first side of the channel may be in electrical communication, typically attached to, the positive pole of the electrical circuit. The second side of the channel may be in electrical communication, typically attached to, the negative pole of the electrical circuit.

Electricity in the electrical circuit may have one or more of a current of from 1 milliamp to 1 amp, a potential of from 0.1 to 3 volts and a power of from 1×10^{-6} to 3 watts.

The first and second sides of the channel may be adjacent to the channel. The first and second sides of the channel may be at least substantially parallel to the plane of the substrate.

The channel is typically non-conductive. The channel typically separates and/or insulates the first and second sides of the channel from one another.

The optoelectronic device may be referred to as a two terminal device. The first and second series of grooves may be referred to as cascaded groove structures. In use the device may be fabricated in a series arrangement and operated in a parallel or a combined series and parallel arrangement.

The cavity between the first and second faces of the first and second series of grooves may be any shape and is normally U-shaped, V-shaped or semi-spherical. The cavity between the first and second faces of the first and second series of grooves may have a flat bottom. The channel cavity between the first and second faces of the channel may be any shape and is normally U-shaped, V-shaped or semi-spherical. The channel cavity between the first and second faces of the channel may have a flat bottom. The shape of the cavity between the first and second faces of the first and second series of grooves may be the same or different to the shape of the channel cavity between the first and second faces of the channel.

The bottom of the channel cavity may be flat or may be rutted. The rutted bottom of the channel cavity may be referred to as uneven or rough. The rutted bottom of the

channel cavity typically increases the surface area of the bottom of the channel cavity. Increasing the surface area of the bottom of the channel cavity may help to ensure the channel separates and/or insulates the first and second sides of the channel from one another.

5

The channel and grooves of the first and second series of grooves typically have a depth measured from an upper surface of the substrate to a point in the channel or groove furthest from the upper surface.

10 The depth of the channel is typically greater than the depth of the grooves of the first and second series of grooves. The depth of the channel may be at least twice the depth of the grooves of the first and second series of grooves.

The channel has a depth and a width. The depth of the channel is typically twice the
15 width of the channel. The aspect ratio for the depth to the width of the channel is therefore typically 2:1.

The first and second series of grooves typically form a series of ridges and cavities. The first and second series of grooves may comprise from 2 to 500 cavities.

20

The inventor of the present invention has appreciated that, in contrast to the usual trend towards reducing the cost and increasing the efficiency of optoelectronic devices, if the costs are significantly reduced, may be by up to an order of magnitude, then the efficiency may be less important. When the optoelectronic device is a solar
25 photovoltaic cell, this is particularly useful if the durability of the solar photovoltaic cells can be improved so that installation is relatively easy and therefore low cost and the solar photovoltaic cells have a greater range of application.

The optoelectronic device according to the first aspect of the present invention may be
30 one or more of attached, secured and applied to a vehicle, for example a car or lorry, a house, for example a roof, and any other surface of a permanent structure. The permanent structure may be man-made or natural.

A surface that the optoelectronic device is one or more of attached, secured and
35 applied to may be flat or uneven, that is one or more of rough, bumpy, irregular and/or rutted. The surface may be part of a building including a house and/or a domestic roof.

Each of the grooves of the first and second series of grooves is typically from 5 to 200mm long, normally from 5 to 1000mm long. Each of the grooves of the first and second series of grooves is typically from 0.1 to 100µm wide, normally from 0.3 to 5µm wide.

The substrate may comprise a curable resin and in particular a UV curable resin. The substrate may comprise one or more of an acrylic resin coated onto polyvinyl chloride (PVC), acrylic resin coated onto polyethylene terephthalate (PET), acrylic resin coated onto polyethylene naphthalate (PEN), a biopolymer coated onto polyvinyl chloride (PVC), a biopolymer coated onto polyethylene terephthalate (PET) and a biopolymer coated onto polyethylene naphthalate (PEN).

The first and second series of cascaded groove structures may comprise the substrate.

In accordance with a second aspect of the present invention there is provided a method of producing an optoelectronic device, the method including the steps of:

providing a substrate comprising a first and a second substantially planar face, a first and a second aperture in the substrate, and a series of grooves in the first substantially planar face, the series of grooves including a first outermost groove and a second outermost groove, each groove of the series of grooves having a first and a second face and a cavity therebetween;

coating at least the first face with a conductor material and coating the second face with a semiconductor material; and

at least partially filling the cavity with another semiconductor material.

The step of coating at least the first face with the conductor material and coating the second face with the semiconductor material and/or the step of at least partially filling the cavity with the another semiconductor material, may also at least partially coat a side or sides of the first and/or second aperture and/or fill the first and/or second aperture with one or more of the conductor material, the semiconductor material and the another semiconductor material.

The method may separately include the step of creating the first and the second aperture in the substrate. The step of creating the first and the second aperture in the substrate may be before or after the step of coating at least the first face with the

conductor material and coating the second face with the semiconductor material and/or the step of at least partially filling the cavity with the another semiconductor material.

5 It may be an advantage of the present invention that when the substrate is provided with the first and second aperture therein, and/or the method separately includes the step of creating the first and the second aperture in the substrate before the coating and filling steps, and then the first and/or second aperture is at least partially filled with one or more of the conductor material, the semiconductor material and the another semiconductor material, these materials provide the first and/or second aperture and/or
10 substrate surrounding the first and/or second aperture with additional structural strength.

The first aperture typically provides electrical communication between the first outermost groove and the second substantially planar face of the substrate and the
15 second aperture provides separate electrical communication between the second outermost groove and the second substantially planar face of the substrate.

The substrate typically also comprises a channel between the first and second series of grooves. The channel typically also transects the grooves of the first and second
20 series of grooves.

The semiconductor material coated on the second face of each groove may be referred to as a second semiconductor material. The another semiconductor material at least partially filling the cavity may be referred to as a first semiconductor material.
25

The step of coating the at least first face of each groove with the conductor material and coating the second face of each groove with the semiconductor material is normally before the step of at least partially filling the cavity with the another semiconductor material.
30

The channel typically has a first and a second face and a channel cavity therebetween.

The step of at least partially filling the cavity between the first and second faces of the grooves with the another semiconductor material also typically at least partially fills the
35 channel cavity with the another semiconductor material.

The first and second semiconductor materials are typically different. The first semiconductor material is typically a p-type semiconductor material. The second semiconductor material is typically an n-type semiconductor material.

5 The step of coating at least the first face of each groove of the first and second series of grooves with the conductor material and coating the second face of each groove of the first and second series of grooves with the semiconductor material typically comprises an off-axis directional coating process. The step of at least partially filling the cavity of each groove with the another semiconductor material typically comprises
10 one or more of an off-axis directional coating process, directional coating process and uniform coating process.

The first and second faces and cavity of each groove of the first and second series of grooves are normally configured to be coated by an off-axis directional coating
15 process.

The method step of coating at least the first face of each groove of the first and second series of grooves with the conductor material is typically before the step of coating the second face of each groove of the first and second series of grooves with the
20 semiconductor material. The method step of at least partially filling the cavity with the another semiconductor material typically follows these coating steps.

The off-axis directional coating process may include spraying the conductor material and/or the semiconductor material at an angle relative to the plane of the substrate,
25 and therefore also each of the grooves of the first and second series of grooves, such that only the first or second face of each groove of the first and second series of grooves is coated. This is typically because the coating is substantially restricted by viewing angle of the coating process to only one of the first or second face.

30 The off-axis directional coating is typically performed in a partial vacuum. The partial vacuum normally ensures the coating material, typically a vapour, has a mean free path from a source to the substrate, that is a direct and un-diverted path free from interactions with gas molecules. The coating material may be the conductor material, the semiconductor material or the another semiconductor material.

35

Generally the mean free path of travel of atomised coating material is comparable to the distance between the source and the surface of the substrate to be coated. Off-axis directional coating in a partial vacuum, also referred to as vacuum evaporation coating, at pressures below 10^{-4} mbar is typically directional due to the mean free path being approximately 600mm. The source can be angled to the first or second substantially planar face of the substrate so that a restricted view of the surface of the substrate is presented and this restricted view allows for coating on selective parts of the substrate by a process of self-shadowing. The mean free path may also be defined as the length of a path an atom or molecule can travel before it is expected to have interacted with another atom or molecule. At atmospheric pressure the mean free path is typically 67nm. Calculated using nitrogen as the total atmosphere and a partial vacuum level of 0.0001mbar, the mean free path is typically 66cm. At a partial vacuum of 0.00001mbar, the mean free path increases to 6.6 meters.

The conductor material, the semiconductor material and/or the another semiconductor material may be sprayed onto and/or towards the substrate at an angle relative to the plane of the substrate of from 25° to 90° , normally from 35° to 55° , and typically 45° . When the conductor material, the semiconductor material and/or the another semiconductor material is sprayed onto the substrate at an angle relative to the plane of the substrate of from 25° to 90° , normally from 35° to 55° and typically 45° , coating the side or sides of the first and second apertures with the conductor material, the semiconductor material and/or the another semiconductor material coats the side or sides at least 25%, normally more than 50% of the length of the first and/or second apertures away from the surface of the substrate nearest the source.

It may be an advantage of the present invention that coating the side or sides of the first and second apertures with the conductor material, the semiconductor material and/or the another semiconductor material at least 25%, normally more than 50% of the length of the apertures away from the surface of the substrate nearest the source helps to provide adequate, typically good electrical conduction from the first to the second substantially planar face of the substrate, and/or from the second to the first substantially planar face.

The angle at which conductor material, the semiconductor material and/or the another semiconductor material is sprayed onto and/or towards the first substantially planar face of the substrate, may be the same, typically different from the angle at which

conductor material, the semiconductor material and/or the another semiconductor material is sprayed onto and/or towards the second substantially planar face of the substrate.

- 5 The aperture may be a hole and/or a slot. It may be an advantage of the present invention that when the aperture is a slot, the aspect ratio for the depth to the width of the slot may improve the viewing angle of the coating process for at least one, normally at least two, of the sides of the slot.
- 10 The off-axis directional coating process may include using a shield to restrict the coating of the conductor material and/or the semiconductor material onto the at least first and/or second face of each groove of the first and second series of grooves. The off-axis directional coating process may be repeated using more than one conductor material and/or semiconductor material.
- 15 The step of providing the substrate typically includes patterning a surface of the substrate to produce a structured surface.
- The optional features of the first aspect of the present invention can be incorporated
- 20 into the second aspect of the present invention and vice versa.

An embodiment of the invention will now be described by way of example only and with reference to the accompanying drawings, in which:

Figure 1a is a plan view of an optoelectronic device of the present invention;

5 Figure 1b is a plan view of an alternative optoelectronic device of the present invention;

Figure 2a is a cross-sectional view of part of the optoelectronic device shown in Figures 1a and 3a;

Figure 2b is a cross-sectional view of part of the alternative optoelectronic device shown in Figures 1a and 3a;

10 Figure 3a is a plan view of a reverse or second side of the optoelectronic device shown in Figure 1a; and

Figure 3b is a plan view of a reverse or second side of the optoelectronic device shown in Figure 1b.

15 Figure 1a shows a plan view of the optoelectronic device 301 comprising a substrate 305. Only the first substantially planar face of the substrate is shown in Figure 1a. The substrate 305 has a surface comprising a first 304a and a second 304b series of grooves and a channel 302 therebetween. Figure 1a also shows a first outermost groove 307a and a second outermost groove 307b of the first series of grooves 304a
20 and a first 308a and a second 308b aperture in the substrate 305.

The optoelectronic device 301 is a solar photovoltaic cell. The optoelectronic device 301 includes a mixture of interdigitated (parallel connected) and cascaded (series connected) grooves 304. The operating voltage of the optoelectronic device 301 can
25 be controlled by changing the number of series of grooves 304a & 304b. Increasing the number of series of grooves 304a & 304b increases the operating voltage of the optoelectronic device 301. The optoelectronic device 301 can be operated in parallel or a combination of series and parallel arrangement. It may be an advantage of the optoelectronic device 301 that this removes the need for extra process steps to be
30 used to connect the cascaded groove structures in series to achieve the desired output voltage.

The channel 302 is a means to separate but also connect the cascaded (series connected) grooves 304a & 304b in parallel, in order to make it possible to extract the
35 desired electric charge generated at the voltage designed by the number of cascaded groove structures 304a & 304b.

The channel 302, also referred to as the delineation or structural delineation feature first crosses the first series 304a of cascaded grooves towards the edge of the structured web and then crosses a space 303 between the cascaded grooves 304a & 304b, and subsequently crosses the second series of cascaded grooves 304b towards the opposite edge of the structured web. Since many of these structural delineation features 302 are used, each series of cascaded grooves, 304a & 304b for example, are crossed towards each edge by elements of two successive individual delineation features 302, as depicted in Figure 1a.

The spaces 303 are divided into first 306a and second 306b areas. The first area 306a carries a positive charge and the second area 306b carries a negative charge 306b.

The first aperture 308a provides electrical communication between the first outermost groove 307a and the second substantially planar face of the substrate (as shown in Figure 3a). The second aperture 308b provides separate electrical communication between the second outermost groove 307b and the second substantially planar face of the substrate (as shown in Figure 3a).

A first group of apertures including the first aperture 308a is shown at the top of Figure 1a and a second group of apertures including the second aperture 308b is shown at the bottom of Figure 1a. The group of apertures are shown horizontally spaced in Figure 1a.

The first aperture 308a passes through the first substantially planar face (shown in Figure 1a) of the substrate 305 proximate to the first outermost groove 307a and through the first electrical conductor on the second substantially planar face of the substrate (as shown in Figure 3a). The second aperture 308b passes through the first substantially planar face (shown in Figure 1a) of the substrate 305 proximate to the second outermost groove 307b and through the second electrical conductor on the second substantially planar face of the substrate (as shown in Figure 3a).

It may be an advantage that the optoelectronic device of the present invention does not suffer from the same sensitivity to defects in its structure compared to other known optoelectronic devices of the prior art. Any defect in the structure of a typical known planar sandwich construction solar photovoltaic cell for example will severely affect the

overall performance of the cell into which the sandwich construction is incorporated. This means the fabrication processes must be kept very clean and any subsequent coating process must be highly uniform. These requirements reduce the process yields and throughputs as materials deposited in the sandwich construction must be
5 very uniform and this requires the processing to be carefully controlled.

Furthermore, the typical known planar sandwich construction has a transparent conducting layer, which may be, for example, zinc oxide or indium oxide based, which is expensive. Also, any error made during the subsequent manufacturing processes to
10 produce the desired voltage from the sandwich construction are therefore costly. The transparent conducting layer requires a high temperature for its deposition in order to achieve the required performance for commercial products, further increasing the cost of fabrication of the device.

15 The optoelectronic device of the present invention may mitigate some or all of the above disadvantages of known solar photovoltaic cells having a planar sandwich construction. The channel or delineation feature 302 is created with the grooves 304, before coating. Some known systems first produce the grooves, then coat the grooves before producing the delineation feature 302.

20 Figure 1b shows a plan view of an alternative optoelectronic device 301 comprising a substrate 305. Only the first substantially planar face of the substrate is shown in Figure 1a. The substrate 305 has a surface comprising a first 304a and a second 304b series of grooves and a channel 302 therebetween. Figure 1b also shows a first
25 outermost groove 307a and a second outermost groove 307b of the first series of grooves 304a. Figure 1b shows a first 308a and a second 308b aperture in the substrate 305. Alternatively, apertures 308c and 308d may be referred to as the first and second apertures respectively.

30 Other features of the optoelectronic device 301 shown in Figure 1b are the same as those shown in Figure 1a.

Figure 2a shows a cross-sectional view of part of the optoelectronic device 301 shown in Figures 1a and 3a along the line A-A. Each groove 320a & 320b for example, of a
35 series of grooves 304b has a first face 312a and a second face 312b and a cavity 314 therebetween.

Figure 2a shows the apertures 308a and 308b filled with filler material 315. Figure 2a shows the first substantially planar face 309a of the substrate 305 (as shown in Figure 1b) and the second substantially planar face 309b of the substrate 305 (as shown in Figure 3b).

The filler material 315 is an electrical conductor. The filler material 315 provides the electrical communication between the first and second outermost grooves 307a and 307b and the second substantially planar face 309b.

The cavities 314 are partially filled with a first semiconductor material 316. The first face 312a is coated with a conductor material 318 and the second face 312b is coated with a second semiconductor material 317.

The first face 312a is coated with the conductor material 318 and the second face 312b is coated with the second semiconductor material 317 using an off-axis coating technique. The cavity 314 is partially filled with the first semiconductor material using a uniform coating technique.

The off-axis directional coating requires that the coating occurs from an angle relative to each groove 320a & 320b for example, of the series of grooves 304b. The coating is sprayed into the grooves and deposited from either side of a vertical axis. The off-axis directional coating is performed in a partial vacuum. The partial vacuum ensures the coating material from the source has a sufficient mean free path, that is a direct and un-diverted path, and that the substrate is substantially free from interactions with gas or atmospheric molecules.

Spray is used herein to refer to any type of directional coating of individual elements and/or droplets, the dimensions of which are smaller than the dimensions of each groove 320a & 320b for example, of the series of grooves 304b.

The off-axis directional coating means that the coating of conductor material 318 and second semiconductor material 317 is largely restricted by viewing angle to only one side of each groove 320a & 320b for example, of the series of grooves 304b. The acceptable limits of off-axis directional coating are defined by the type of structure and/or substrate onto which the coating is deposited. The coating may be either

continuous or discontinuous over a surface of the structure and/or substrate depending on its fine structure or the type of structure or substrate used.

5 The shape of the cavity 314 formed by and between the first and second faces 312a & 312b of the series of grooves 304b is such that the viewing angle is restricted. The restricted viewing angle is the result of the upper edges of the neighbouring groove.

The process of off-axis directional coating is further described in WO 2012/175902A1. The process of off-axis directional coating may be referred to as Glancing Angle
10 Deposition (GLAD).

The conductor material 318 and second semiconductor material 317 are deposited on the cascaded groove structured surface 304b using off-axis directional coating, enabling the fabrication of non-contacting interdigitated conductors having defined
15 geometries along the surface presented to the source of coating materials.

The second face 312b is often coated with a second conductor material (not shown) and then the semiconductor material 317. Both coats are applied using the off-axis coating technique. The semiconductor material 317 is then coated on top of the
20 second conductor material (not shown). The conductor material 318 and second conductor material (not shown) are then used as connections, sometimes for input and output connections, to the first 316 and second 317 semiconductor materials deposited in the space between the conductor material 318 and second conductor material (not
25 shown) on the structured surface, that is the surface of the substrate.

The second conductor material and the first conductor material are usually the same material, as shown in Figure 2a. The apertures 308a and 308b are filled by a uniform coating technique.

30 Cascaded groove structured surfaces address some of the problems associated with standard planar sandwich constructed devices, however these cascaded groove structured surfaces of the prior art are either interdigitated (parallel connected) or cascaded (series connected). The optoelectronic device 301 provides a mixture of interdigitated and cascaded groove structures. This allows the operating voltage of the
35 optoelectronic device 301 to be designed and controlled by the number of series of grooves, for example 304b. Any number of series of grooves, for example 304b, can

be produced and operated in parallel to provide the desired voltage output and series to provide the desired current output. The number of grooves affects the voltage and the number of series of grooves affects the current.

- 5 A conventional post off-axis directional coating demetallisation technique requires significant space to be set aside between a series of cascaded groove structures so that two properties can be maintained. The first property is a physical one in that there must be sufficient space to accommodate the delineation feature between the series of cascaded groove structures and also sufficient space to allow for registration
- 10 tolerances of the technique chosen for the demetallisation technique, which may be, for example, a laser technique. The second property is that the space left after the post off-axis directional coating demetallisation process still needs to be capable of passing current of sufficient conductance to allow efficient use of the cascaded devices.
- 15 When a post off-axis directional coating demetallisation technique is used, the delineation feature or region between the series of cascaded grooves could be formed, for example, by laser cutting through the deposited conductor material whilst avoiding cutting through the supporting substrate or by the printing of metal etching material onto the deposited metals. Following the use of these techniques, the resulting
- 20 delineation feature prevents the short circuiting of the positive output of one series of cascaded grooves with the negative output of the next series of cascaded grooves and prevents the lateral conduction from the individual cascaded grooves to the edge contacts.
- 25 The space required for the delineation feature to be introduced after the off-axis directional coating metallisation is relatively large and has no active function. Therefore, there is a reduction in active cascaded groove area since the delineation feature and the resulting charge extraction areas must be large enough to both allow the registration of the delineation feature with its associated tolerances and provide a
- 30 low enough resistance pathway so that charge can be extracted without excessive internal losses. Consequently, for a solar photovoltaic cell, this region reduces the active area of the overall roll-to-roll fabricated product.

The optoelectronic device 301 increases the speed of, and decreases the cost of, manufacture of devices such as solar photovoltaic cells, with a concomitant increase in product yield due to reduced wastage during the manufacturing process.

Figure 2b shows a cross-sectional view of part of the optoelectronic device 301 shown in Figures 1a and 3a along the line A-A. Each groove 320a & 320b for example, of a series of grooves 304b has a first face 312a and a second face 312b and a cavity 314
5 therebetween.

Figure 2b shows the sides of the apertures 308a and 308b coated with conductor materials 310a and 310b. The conductor materials 310a and 310b contact each other at 313. This contact at 313 and the extension of the conductor materials 310a and
10 310b out of the apertures 308a and 308b provides the electrical communication between the first and second outermost grooves 307a and 307b and the second substantially planar face 309b. The apertures 308a and 308b may or may not be filled with the filler material referred to in Figure 2a.

Figure 3a shows the second substantially planar face 309b of the substrate 305 shown in Figure 1a. The second substantially planar face 309b also comprises a first 311a and a second 311b electrical conductor. The first and second electrical conductors 311a and 311b are electrically insulated from one another by the area 305a of the
15 second substantially planar face 309b of the substrate 305.

Figure 3a also shows the first 308a and second 308b apertures in the substrate 305, the other ends of which are shown in Figure 1a.
20

Figure 3b shows the second substantially planar face 309b of the substrate 305 shown in Figure 1b. The second substantially planar face 309b also comprises a first 311a and a second 311b electrical conductor. The first and second electrical conductors 311a and 311b are electrically insulated from one another by the area 305a of the
25 second substantially planar face 309b of the substrate 305.

Figure 3b shows the first 308a and second 308b apertures in the substrate 305, the other ends of which are shown in Figure 1b. Figure 3b also shows the apertures 308c and 308d also referred to as the first and second apertures respectively.
30

Modifications and improvements can be incorporated herein without departing from the
35 scope of the invention.

THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:-

1. An optoelectronic device comprising:
a substrate having a first and a second substantially planar face;
a series of grooves in the first substantially planar face, the series of grooves including a first outermost groove and a second outermost groove; and
a first and a second aperture in the substrate;
wherein the first aperture provides electrical communication between the first outermost groove and the second substantially planar face of the substrate and the second aperture provides separate electrical communication between the second outermost groove and the second substantially planar face of the substrate;

wherein the second substantially planar face of the substrate further comprises a first and a second electrical conductor, the first and second electrical conductors being electrically insulated from one another; and

wherein each groove of the series of grooves has a first and a second face and a cavity therebetween, the cavity at least partially filled with a first semiconductor material, the first face coated with a conductor material and the second face coated with a second semiconductor material, sides of the first and second apertures coated with one or more of the conductor material, the first semiconductor material and the second semiconductor material.

2. An optoelectronic device as claimed in claim 1, wherein the first aperture passes through the first substantially planar face of the substrate proximate to the first outermost groove and through the first electrical conductor on the second substantially planar face of the substrate.

3. An optoelectronic device as claimed in claim 1 or claim 2, wherein the second aperture passes through the first substantially planar face of the

substrate proximate to the second outermost groove and through the second electrical conductor on the second substantially planar face of the substrate.

4. An optoelectronic device as claimed in any one of the preceding claims, wherein the apertures have a diameter of from 0.5 to 2000 microns.
5. An optoelectronic device as claimed in any one of the preceding claims, wherein the aperture is a hole or a slot.
6. An optoelectronic device as claimed in any one of the preceding claims, wherein the first and second apertures are at least partially filled with an electrical conductor material.
7. An optoelectronic device as claimed in claim 6, wherein the electrical conductor material is a conductive ink.
8. An optoelectronic device as claimed in any one of the preceding claims, wherein the series of grooves comprises a first and a second series of grooves and a channel therebetween, the channel transecting the grooves of the first and second series of grooves.
9. An optoelectronic device as claimed in claim 8, wherein the channel transects the grooves of the first series of grooves towards an end of each groove and then passes between the first and second series of grooves before transecting or crossing the grooves of the second series of grooves towards an opposite end of each groove.

10. An optoelectronic device as claimed in any one of the preceding claims, wherein the first semiconductor material is a p-type semiconductor material and the second semiconductor material is an n-type semiconductor material.

11. An optoelectronic device as claimed in claim 10, wherein the n-type semiconductor comprises one or more of silicon, germanium, phosphorus, selenium, tellurium, cadmium sulphide, Copper Zinc Tin Sulfide (CZTS), a Quantum Dot (QD) material and an organic material.

12. An optoelectronic device as claimed in claim 10 or claim 11, wherein the p-type semiconductor comprises one or more of silicon, germanium, cadmium telluride, copper indium gallium selenide, copper indium gallium diselenide ('CIGS'), copper oxide, boron, beryllium, zinc, cadmium, Copper Zinc Tin Sulfide (CZTS), a Quantum Dot (QD) material and an organic material.

13. An optoelectronic device as claimed in claim 8, wherein the channel has first and second faces and a channel cavity therebetween, the channel cavity being Ushaped, V-shaped or semi-spherical.

14. An optoelectronic device as claimed in claim 13, wherein a bottom of the channel cavity is ruttled.

15. A method of producing an optoelectronic device, the method including the steps of:

providing a substrate comprising a first and a second substantially planar face, the second substantially planar face comprising a first and a

second electrical conductor, the first and second electrical conductors being electrically insulated from one another

providing a first and a second aperture in the substrate, and a series of grooves in the first substantially planar face, the series of grooves including a first outermost groove and a second outermost groove, each groove of the series of grooves having a first and a second face and a cavity therebetween, the first aperture providing electrical communication between the first outermost groove and the second substantially planar face of the substrate and the second aperture providing separate electrical communication between the second outermost groove and the second substantially planar face of the substrate;

coating at least the first face with a conductor material and coating the second face with a semiconductor material; and

at least partially filling the cavity with another semiconductor material.

16. A method of producing an optoelectronic device according to claim 15, wherein the step of coating at least the first face with the conductor material and coating the second face with the semiconductor material or the step of at least partially filling the cavity with the another semiconductor material, also at least partially coats a side of or fills the first or second aperture with one or more of the conductor material, the semiconductor material and the another semiconductor material.

17. A method of producing an optoelectronic device according to claim 15 or claim 16, the method separately including the step of creating the first and the second aperture in the substrate, the step being before or after the step of coating at least the first face with the conductor material and coating the

second face with the semiconductor material or the step of at least partially filling the cavity with the another semiconductor material.

18. A method of producing an optoelectronic device according to any one of claims 15 to 17, wherein the step of coating at least the first face of each groove of the first and second series of grooves with the conductor material and coating the second face of each groove of the first and second series of grooves with the semiconductor material comprises an off-axis directional coating process.

19. A method of producing an optoelectronic device according to any one of claims 15 to 18, wherein the step of at least partially filling the cavity of each groove with the another semiconductor material comprises one or more of an off-axis directional coating process, directional coating process and uniform coating process.

20. A method of producing an optoelectronic device according to claim 18 or claim 19, wherein the off-axis directional coating process includes spraying the conductor material or the semiconductor material at an angle relative to the plane of the substrate, and therefore also each of the grooves of the first and second series of grooves, such that only the first or second face of each groove of the first and second series of grooves is coated.

Dated this 25th day of February 2019

Power Roll Limited

Patent Attorneys for the Applicant

PETER MAXWELL AND ASSOCIATES

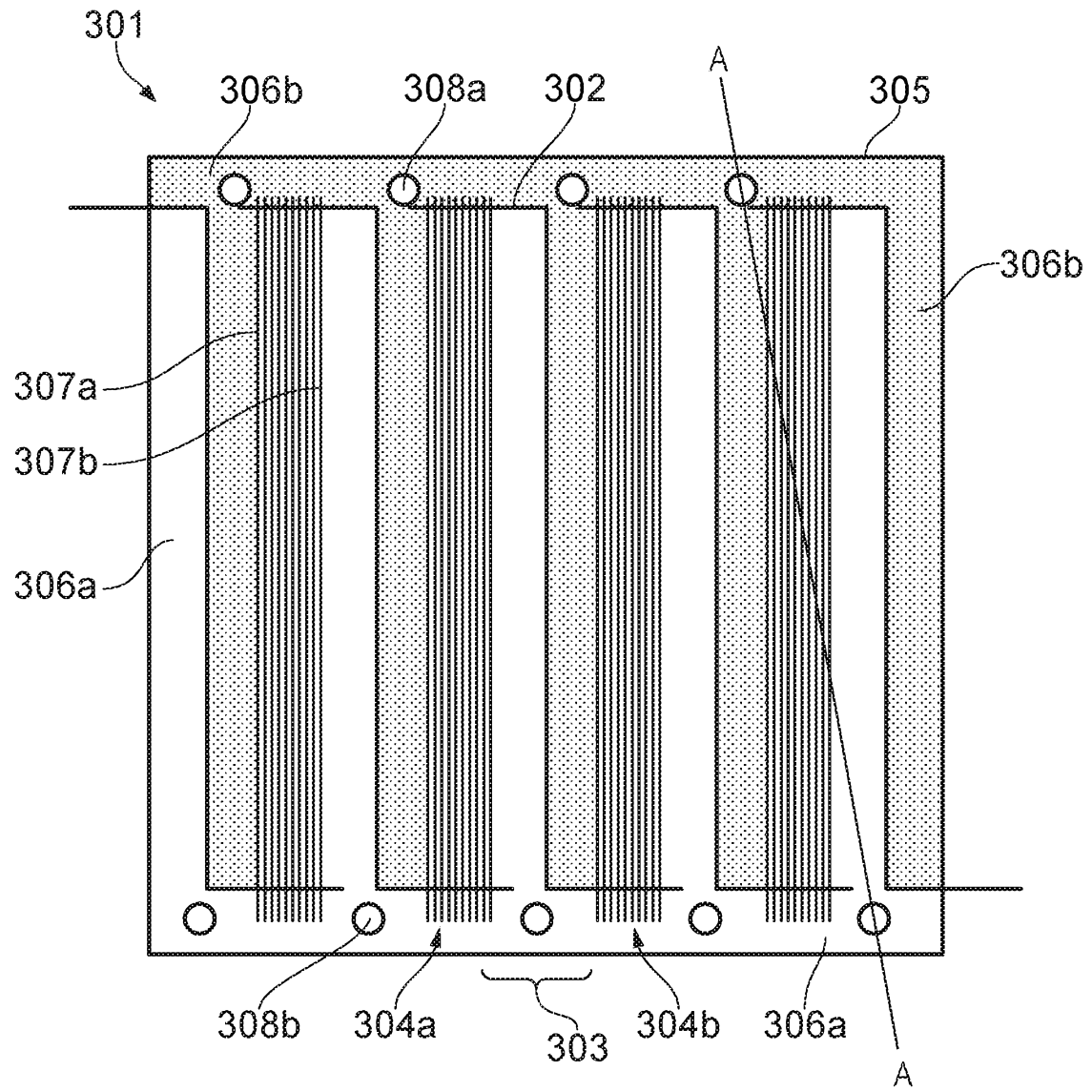


FIG. 1a

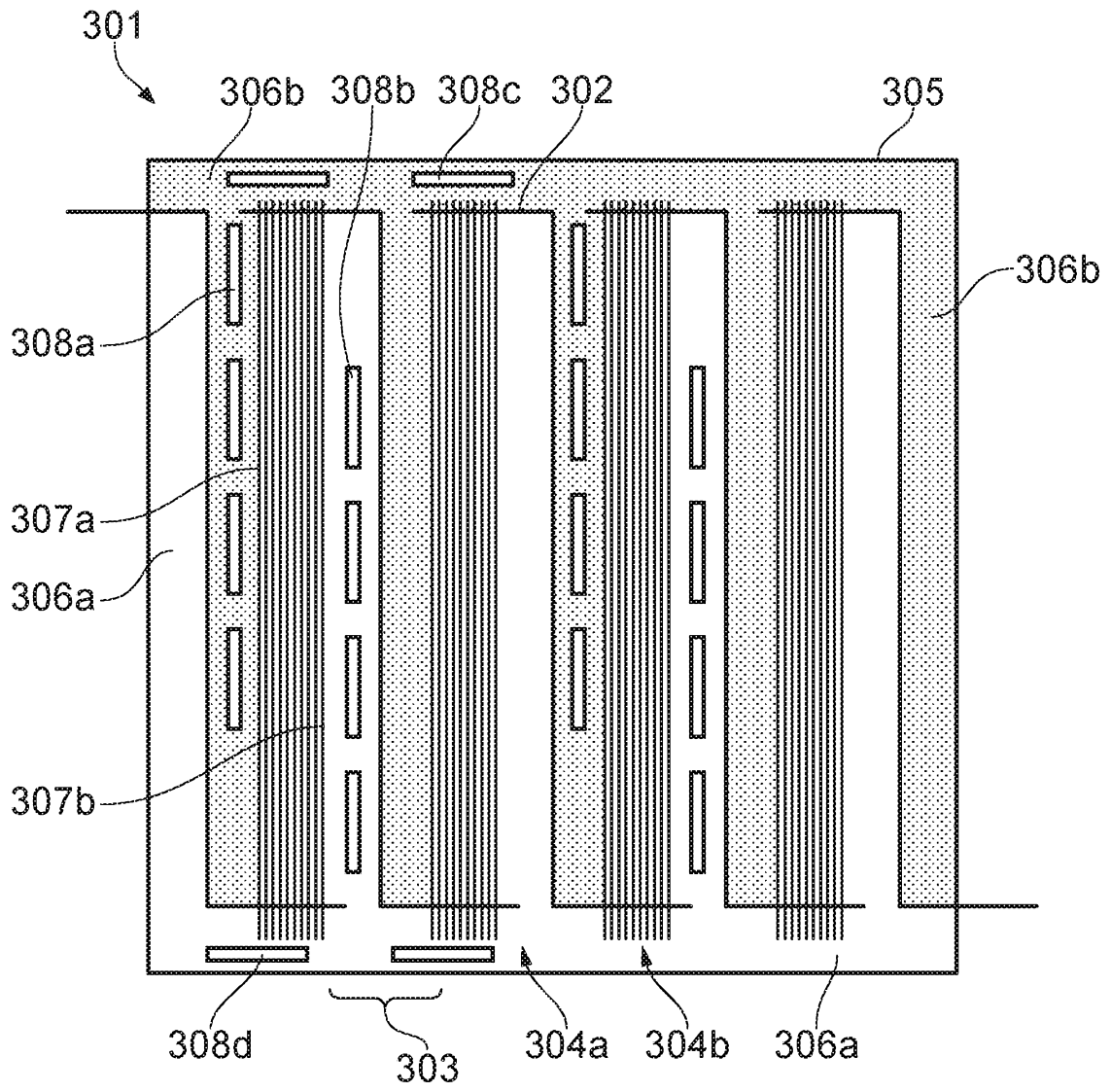


FIG. 1b

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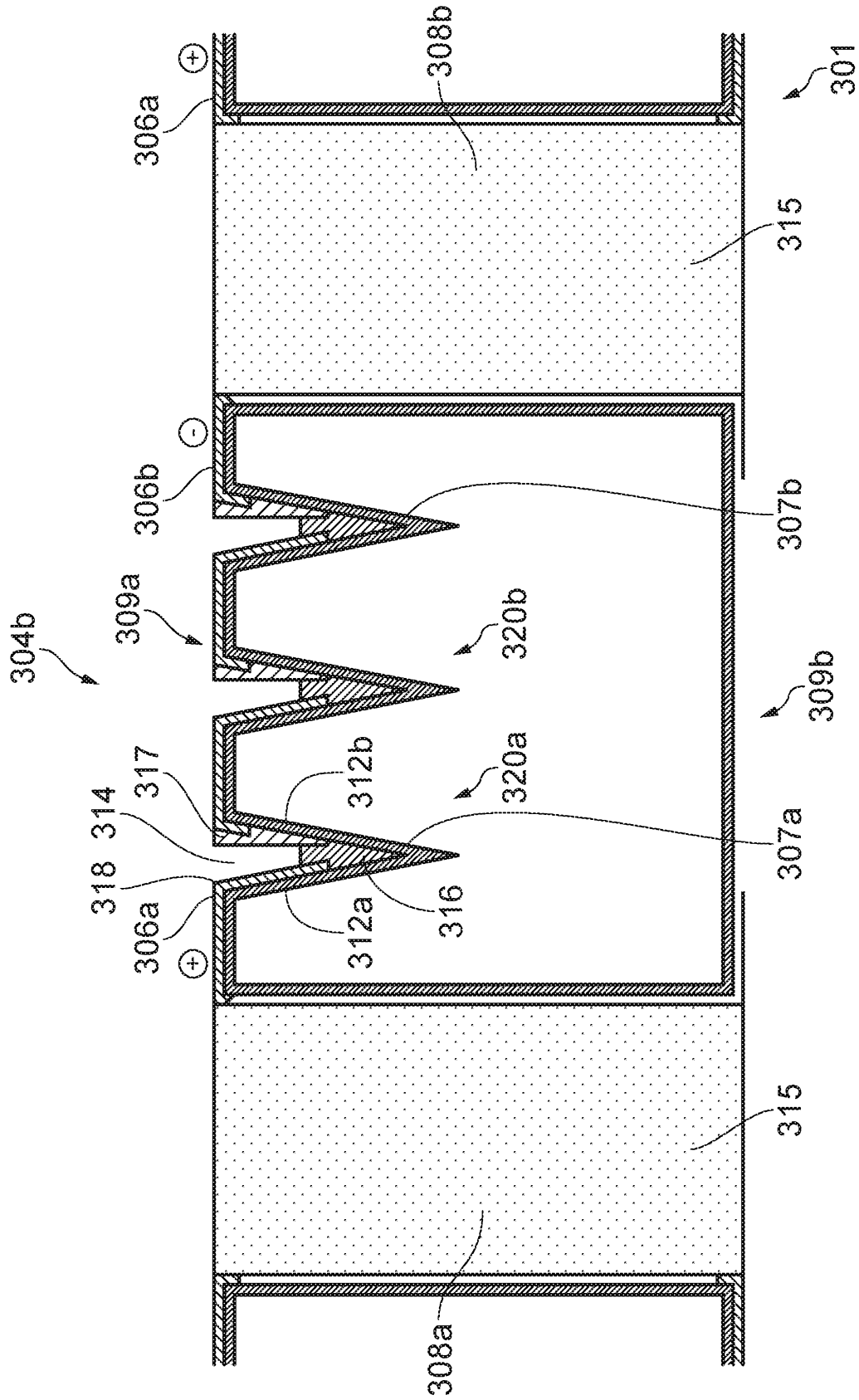


FIG. 2a

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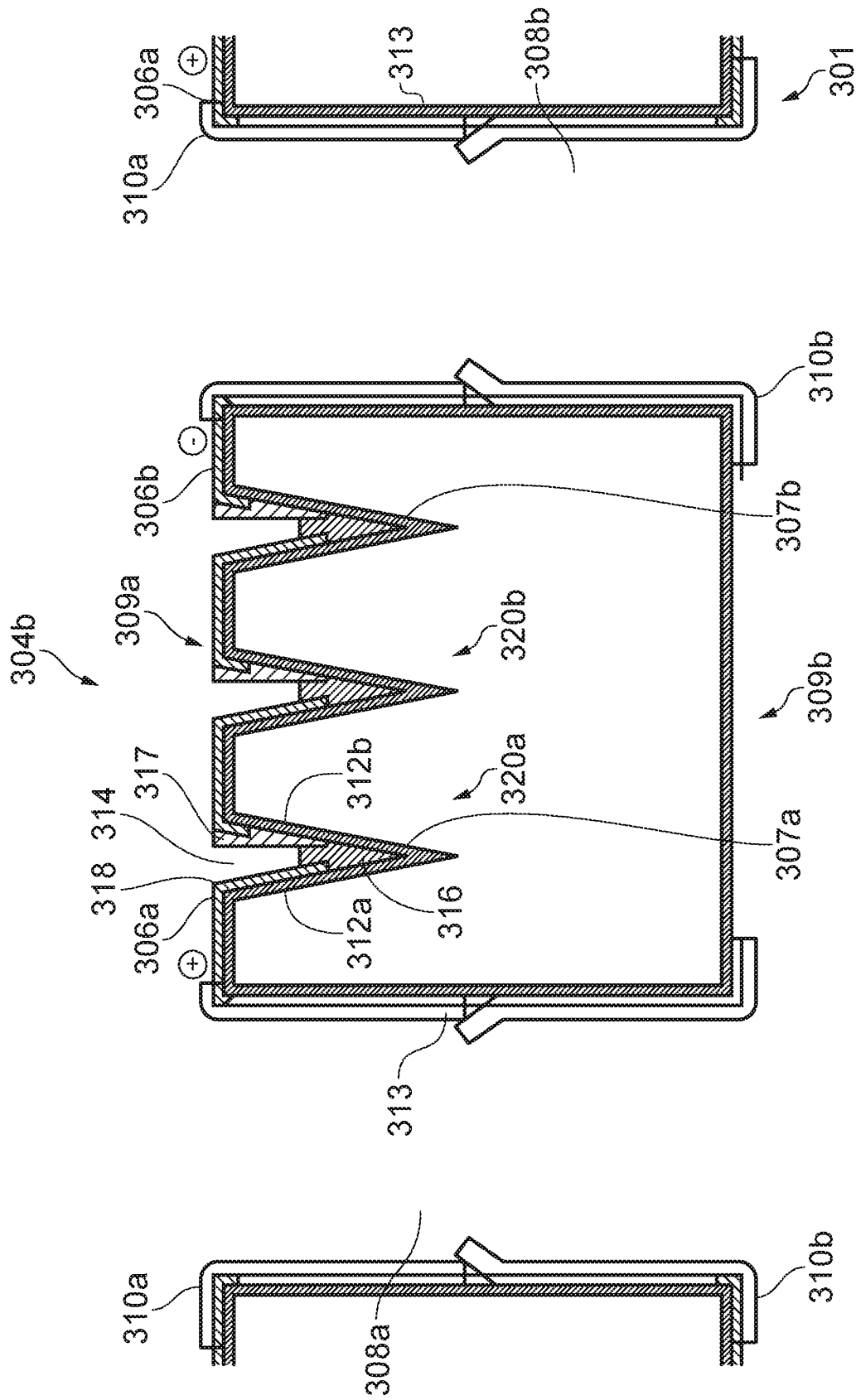


FIG. 2b

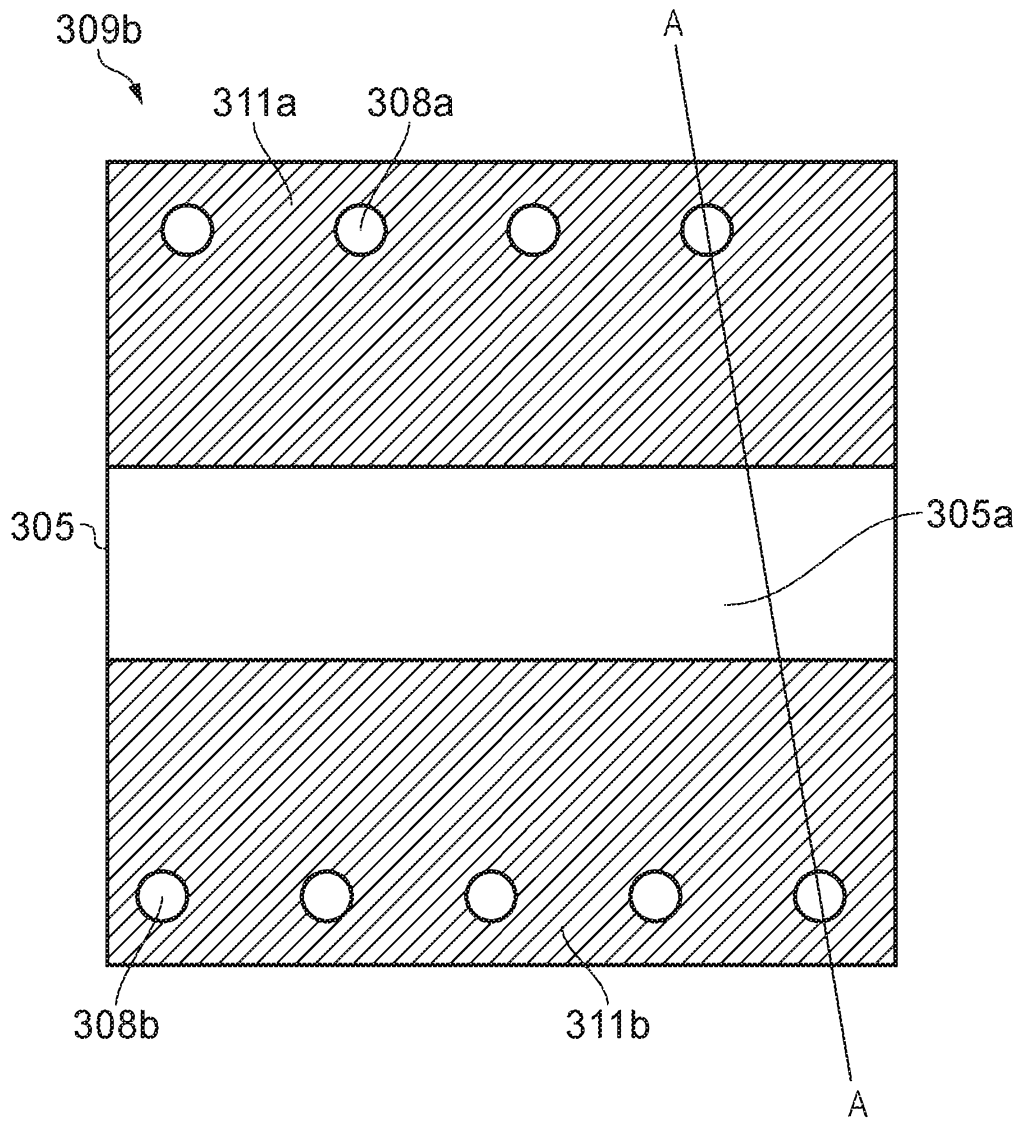


FIG. 3a

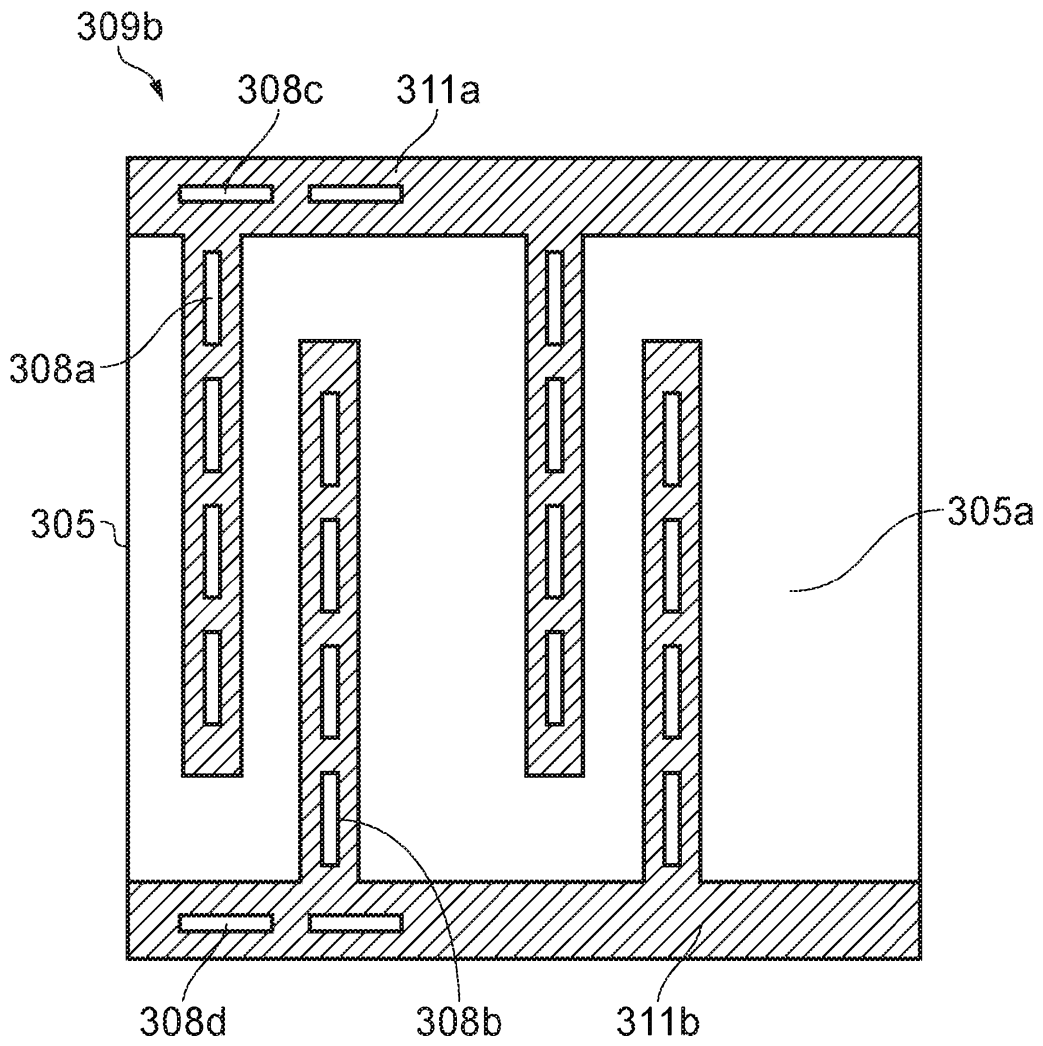


FIG. 3b