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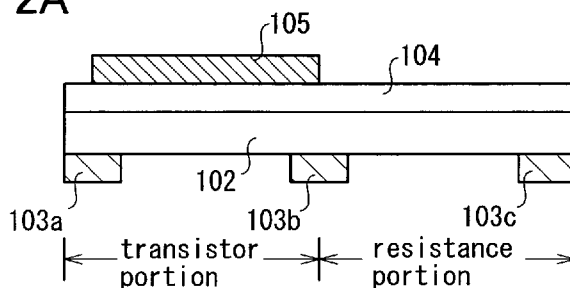
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(54) Title: FIELD EFFECT TRANSISTOR AND SEMICONDUCTOR DEVICE

FIG. 2A



(57) Abstract: An object is to provide a field effect transistor (FET) having a conductor-semiconductor junction, which has excellent characteristics, which can be manufactured through an easy process, or which enables high integration. Owing to the junction between a semiconductor layer and a conductor having a work function lower than the electron affinity of the semiconductor layer, a region into which carriers are injected from the conductor is formed in the semiconductor layer. Such a region is used as an offset region of the FET or a resistor of a semiconductor circuit such as an inverter. Further, in the case of setting up such an offset region and a resistor in one semiconductor layer, an integrated semiconductor device can be manufactured.

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## DESCRIPTION

## FIELD EFFECT TRANSISTOR AND SEMICONDUCTOR DEVICE

## 5 TECHNICAL FIELD

[0001]

The present invention relates to a field effect transistor (FET) including a semiconductor and a semiconductor device including a field effect transistor.

## 10 BACKGROUND ART

[0002]

A field effect transistor (FET) is a device in which regions called a source and a drain are provided in a semiconductor, in which each of the regions is provided with an electrode, potentials are supplied to the electrodes, and an electric field is applied to the semiconductor with the use of an electrode called a gate through an insulating film or a Schottky barrier so that the state of the semiconductor is controlled, whereby current flowing between the source and the drain is controlled. As the semiconductor, Group IV elements (Group 14 elements) such as silicon and germanium, Group III-V compounds such as gallium arsenide, indium phosphide, and gallium nitride, Group 15 II-VI compounds such as zinc sulfide and cadmium telluride, and the like can be given.

[0003]

In recent years, FETs in which an oxide such as zinc oxide or an indium gallium zinc oxide-based compound is used as a semiconductor have been reported (Patent Document 1 and Patent Document 2). In an FET including such an oxide semiconductor, relatively high mobility can be obtained, and such a material has a wide bandgap of greater than or equal to 3 electron volts; therefore, application of the FET including an oxide semiconductor to displays, power devices, and the like is discussed.

[0004]

The fact that the bandgap of such a material is greater than or equal to 3 electron volts means that the material transmits visible light, for example; thus, in the case where the material is used in a display, even an FET portion can transmit light and the aperture ratio is expected to be improved.

[0005]

Further, such a wide bandgap is common to silicon carbide, which is used in power devices; therefore, the oxide semiconductor is also expected to be applied to a power device.

5 [0006]

Furthermore, a wide bandgap means few thermally excited carriers. For example, silicon has a bandgap of 1.1 electron volts at room temperature and thus thermally excited carriers exist therein at approximately  $10^{11}$  /cm<sup>3</sup>, while in a semiconductor with a bandgap of 3.2 electron volts, thermally excited carriers exist at  
10 approximately  $10^{-7}$  /cm<sup>3</sup> according to calculation.

[0007]

In the case of silicon, carriers generated by thermal excitation exist as described above even in silicon including no impurities, and thus the resistivity of the silicon cannot be higher than or equal to  $10^5$  Ωcm. In contrast, in the case of the  
15 semiconductor with a bandgap of 3.2 electron volts, a resistivity of higher than or equal to  $10^{20}$  Ωcm can be obtained in theory. When an FET is manufactured using such a semiconductor and its high resistivity in an off state (a state where the potential of a gate is the same as the potential of a source) is utilized, it is expected that electric charge can be retained semipermanently.

20 [0008]

Meanwhile, there are few reports on an oxide semiconductor which includes zinc or indium in particular and has p-type conductivity. Accordingly, an FET using a PN junction like an FET of silicon has not been reported, and a conductor-semiconductor junction as disclosed in Patent Document 1 and Patent  
25 Document 2, where a conductor electrode is in contact with an n-type oxide semiconductor, has been used for forming a source or a drain.

[0009]

Note that in general academic books about semiconductors, the "conductor-semiconductor junction" is expressed as a "metal-semiconductor junction."  
30 In this case, metal means a conductor. For example, a semiconductor which is doped at a high concentration and whose resistivity is significantly lowered, metal nitrides

such as titanium nitride and tungsten nitride, metal oxides such as indium tin oxide and aluminum zinc oxide, and the like are also regarded as metal in "metal-semiconductor junctions." However, the term "metal" might generally cause misunderstanding; therefore, the term "conductor-semiconductor junction" is used instead of the term "metal-semiconductor junction" in this specification.

[0010]

For example, Patent Document 1 discloses an FET like the one illustrated in FIG. 5A, that is, an FET in which a first conductor electrode 103a called a source electrode and a second conductor electrode 103b called a drain electrode are provided in contact with one surface of a semiconductor layer 102 and a gate 105 is provided on the other surface side of the semiconductor layer 102 with a gate insulating film 104 interposed therebetween. Conductors are used for the first conductor electrode 103a, the second conductor electrode 103b, and the gate 105.

[0011]

The gate 105 needs to have a portion overlapping with the first conductor electrode 103a and a portion overlapping with the second conductor electrode 103b, as shown by a width  $c$  in FIG. 5A. In other words, it is necessary in Patent Document 1 that  $c$  is larger than zero.

[0012]

In an FET where a source electrode and a drain electrode are formed with the use of a conductor-semiconductor junction, when the carrier concentration of the semiconductor is high, current (off-state current) flows between the source electrode and the drain electrode even in an off state. Thus, the off-state current needs to be reduced by lowering the concentration of a donor or an acceptor in the semiconductor so that an i-type semiconductor (in this specification, an i-type semiconductor is a semiconductor whose carrier concentration derived from a donor or an acceptor is lower than or equal to  $10^{12}/\text{cm}^3$ ) is obtained.

[0013]

Note that a concentration of a donor (or an acceptor) in this specification is a concentration of an element, a chemical group, or the like which could be a donor (or an acceptor) multiplied by an ionization rate thereof. For example, in the case where a donor element is included at 2 % and the ionization rate thereof is 0.005 %, the donor

concentration is 1 ppm ( $= 0.02 \times 0.00005$ ).

[0014]

By the way, in a semiconductor circuit including an FET, especially in a semiconductor circuit in which either a p-channel FET or an n-channel FET can be used, an inverter which is one of fundamental circuits has a structure in which a resistor is connected in series with an FET as illustrated in FIG. 6A.

[0015]

Alternatively, in some cases, the inverter may have a structure in which two FETs are connected in series and a short circuit between a drain and a gate of one of the FETs (typically, the one on the VH side) is caused so that a diode is formed, as illustrated in FIG. 6B. However, the inverter of FIG. 6B has a disadvantage in that a contact at a portion expressed by  $X$  in the drawing needs to be made in order to cause the short circuit between the drain and the gate of the FET and thereby high integration cannot be achieved.

[0016]

In the inverter of the type of FIG. 6A, under the assumption that the resistance when the FET is on is  $R_{ON}$  and the resistance when the FET is off is  $R_{OFF}$ , a resistor having a resistance value  $R$  which satisfies the relation,  $R_{ON} \ll R \ll R_{OFF}$ , is connected to the FET. Here, it is preferable that  $R$  is higher than  $10R_{ON}$  and lower than  $R_{OFF}/10$ , and further preferable that  $R$  is higher than  $100R_{ON}$  and lower than  $R_{OFF}/100$ .

[0017]

In this type of inverter, if the input is High, a current flows through the resistor and the on-state FET. At this time, the resistance between the VH and the VL in the inverter is  $R + R_{ON}$ . If the relation,  $R \gg R_{ON}$ , is satisfied, the resistance of the inverter can approximate to  $R$ . Accordingly, when the power supply voltage of the inverter is assumed to be  $V_{dd}$ , power consumption can be expressed as  $V_{dd}^2/R$ . Further, the output voltage can approximate to zero.

[0018]

Even if the input is Low, a current flows through the resistor and the FET. At this time, the resistance of the inverter is  $R + R_{OFF}$ . If the relation,  $R \ll R_{OFF}$ , is satisfied, the resistance of the inverter can approximate to  $R_{OFF}$ . Accordingly, power

consumption of the inverter can be expressed as  $V_{dd}^2/R_{OFF}$ . Further, the output voltage can approximate to  $V_{dd}$ .

[0019]

As is apparent from the above relations, when  $R$  and  $R_{OFF}$  are large values, power consumption can be reduced. In addition, in terms of the output voltage, it is preferable that  $R$  has an intermediate value between  $R_{ON}$  and  $R_{OFF}$ , and it is ideal that  $R$  is  $(R_{ON} \times R_{OFF})^{1/2}$ . Accordingly, it is preferable that  $R_{OFF}/R_{ON}$  is a large value.

[0020]

Among conventional semiconductor circuits, a circuit including an amorphous silicon FET is known as such a semiconductor circuit in which either a p-channel FET or an n-channel FET can be used.

[0021]

In an inverter circuit including an amorphous silicon FET, n-type amorphous silicon is used for a resistor. The n-type amorphous silicon is used as a material of a source and a drain of an FET and part of the amorphous silicon is processed so as to be used as a resistor. Since the n-type amorphous silicon does not have a high resistivity, the size of the resistor is larger than that of the FET.

[0022]

By the way, an FET in which the carrier concentration is reduced by using an intrinsic (i-type) semiconductor having a band gap of 2 electron volts or more has an extremely small off-state current, that is, an extremely high  $R_{OFF}$  and also has a mobility that is significantly high as compared to that of amorphous silicon, that is, a low  $R_{ON}$ ; thus, the value of  $R_{OFF}/R_{ON}$  is larger than or equal to  $10^{10}$ . With such a large value of  $R_{OFF}/R_{ON}$ , the margin in forming or designing a resistor is increased.

[0023]

However, in the FETs in which a conductor is directly in contact with a semiconductor as in Patent Document 1 and Patent Document 2, a material appropriate for a resistor cannot be found, unlike the case of the FET including amorphous silicon. In particular, an i-type semiconductor formed through reduction of the carrier concentration is considered as having an extremely high resistivity; therefore, usage of the i-type semiconductor for a resistor has not been assumed at all.

[Reference]

[Patent Document]

[0024]

[Patent Document 1] United States Published Patent Application No. 2005/0199879

[Patent Document 2] United States Published Patent Application No. 2007/0194379

5

## DISCLOSURE OF INVENTION

[0025]

It is an object of the present invention to provide an excellent FET, semiconductor device, or semiconductor circuit, or a manufacturing method thereof by devising the circuit design of the FET having a conductor-semiconductor junction as described above. Another object is to provide an FET or semiconductor device having excellent characteristics or a manufacturing method thereof by utilizing features of the conductor-semiconductor junction. Further, it is an object to provide an FET or semiconductor device which can be manufactured through an easy process or a manufacturing method thereof. Furthermore, another object is to provide an FET or semiconductor device with high integration or a manufacturing method thereof. The present invention achieves at least one of the above objects.

10

15

[0026]

Before the present invention is described, terms used in this specification will be briefly explained. First, as for a source and a drain of a transistor in this specification, a terminal supplied with a higher potential is referred to as a drain and the other terminal is referred to as a source in an n-channel FET, and a terminal supplied with a lower potential is referred to as a drain and the other terminal is referred to as a source in a p-channel FET. In the case where the same potential is supplied to the two terminals, one of them is referred to as a source and the other is referred to as a drain.

20

25

[0027]

Instead of the terms "source electrode" and "drain electrode", those portions are referred to as a "first conductor electrode" and a "second conductor electrode" in some cases. In such a case, the names are not interchanged between those portions depending on the potential level.

30

[0028]

A first embodiment of the present invention is an FET including a

semiconductor layer, a first conductor electrode and a second conductor electrode provided in contact with one surface of the semiconductor layer, and a gate provided on the other surface side of the semiconductor layer. An offset region is formed in at least one of a region between the first conductor electrode and the gate and a region between  
5 the second conductor electrode and the gate.

[0029]

A second embodiment of the present invention is an FET including a semiconductor layer, a first conductor electrode and a second conductor electrode provided in contact with one surface of the semiconductor layer, and a gate provided  
10 over the same surface. An offset region is formed in at least one of a region between the first conductor electrode and the gate and a region between the second conductor electrode and the gate.

[0030]

In the above-described first and second embodiments of the present invention,  
15 the width of the offset region is preferably more than or equal to 10 nm and less than or equal to 100 nm, further preferably more than or equal to 10 nm and less than or equal to 50 nm, and still further preferably more than or equal to 10 nm and less than or equal to 20 nm. In addition, the thickness of the semiconductor layer is preferably less than or equal to the width of the offset region and further preferably less than or equal to half  
20 of the width of the offset region. Moreover, the width of the gate is preferably more than or equal to the width of the offset region.

[0031]

A third embodiment of the present invention is a semiconductor device including a semiconductor layer, a first conductor electrode, a second conductor  
25 electrode, and a third conductor electrode which are in contact with one surface of the semiconductor layer, and a gate provided on the other surface side of the semiconductor layer.

[0032]

A fourth embodiment of the present invention is a semiconductor device  
30 including a semiconductor layer, a first conductor electrode, a second conductor electrode, and a third conductor electrode which are in contact with one surface of the semiconductor layer, and a gate provided over the same surface.



[0033]

In the above first to fourth embodiments of the present invention, it is preferable that the portions of the first to third conductor electrodes, which are in contact with the semiconductor layer, have a work function of lower than the sum of the electron affinity of the semiconductor layer and 0.3 electron volts (i.e., the electron  
5 affinity + 0.3 electron volts). Alternatively, it is preferable that ohmic junctions be formed between the first and second conductor electrodes and the semiconductor layer.

[0034]

In the above-described first to fourth embodiments of the present invention, the work function of a portion that is the closest to the semiconductor layer in the gate is preferably higher than the sum of the electron affinity of the semiconductor layer and 0.6 electron volts (i.e., the electron affinity + 0.6 electron volts). In addition, it is preferable that the semiconductor layer is an i-type semiconductor layer.  
10

[0035]

In the above-described first to fourth embodiments of the present invention, the FET or the semiconductor circuit may be provided over an appropriate substrate. In such a case, a structure in which the semiconductor layer is provided between the gate and the substrate or a structure in which the gate is provided between the semiconductor layer and the substrate may be employed.  
15

[0036]

As examples of a material of the substrate, a semiconductor such as single crystal silicon, insulators such as various kinds of glasses, quartz, sapphire, and various types of ceramics, and conductors such as aluminum, stainless steel, and copper can be given. In the case where a semiconductor or a conductor is used as a substrate, it is preferable that an insulating layer is provided on a surface of the substrate.  
20  
25

[0037]

Furthermore, a gate insulating film may be provided between the semiconductor layer and the gate. Alternatively, a Schottky barrier junction may be formed between the semiconductor layer and the gate. In addition, it is not necessary that the first to third conductor electrodes are all formed using the same material. Each  
30 of the first to third conductor electrodes may be formed using different materials, or two

of them may be formed using the same material.

[0038]

Note that the kind of the semiconductor layer is not limited to an oxide, and a Group II-VI compound such as a sulfide may be used. In addition, to reduce carriers  
5 generated by thermal excitation as described above, the bandgap of the semiconductor is preferably greater than or equal to 2 electron volts and less than 4 electron volts, further preferably greater than or equal to 2.9 electron volts and less than 3.5 electron volts.

[0039]

At least one of the above objects can be achieved by employing any of the  
10 above-described structures. In the present invention, an appropriate resistance region is formed by utilizing properties of the conductor-semiconductor junction and the resistance region is utilized to form an offset region of an FET, a semiconductor circuit, or a semiconductor device.

[0040]

15 In the FETs as disclosed in Patent Document 1 and Patent Document 2, the source electrode, the drain electrode, and the gate are formed of conductors. However, an influence of the conductor on a semiconductor has not been fully considered so far.

[0041]

In this respect, it is found out from the consideration of the present inventor  
20 that in the case where the work function of a conductor is lower than the electron affinity of a semiconductor layer in the conductor-semiconductor junction, electrons flow into the semiconductor layer and thereby an ohmic junction is formed.

[0042]

In an FET, since it is preferable that a junction between a source electrode and  
25 a semiconductor or between a drain electrode and the semiconductor be formed so that current flows easily, a material of the source electrode or the drain electrode is selected so that an ohmic junction is formed. For example, titanium and titanium nitride are given. When a junction between an electrode and a semiconductor is an ohmic junction, there are advantages of stable characteristics of an FET to be obtained and of  
30 high percentage of non-defective products.

[0043]

In such a conductor-semiconductor junction, the concentration of electrons is

higher in a region closer to the conductor and is roughly calculated to be  $10^{20}/\text{cm}^3$  in several nanometers,  $10^{18}/\text{cm}^3$  in several tens of nanometers,  $10^{16}/\text{cm}^3$  in several hundreds of nanometers,  $10^{14}/\text{cm}^3$  even in several micrometers from the interface of the conductor-semiconductor junction. That is, even if the semiconductor itself is intrinsic (i-type), a region having a high carrier concentration is formed by the contact with the conductor. Formation of such a region including many carriers in the vicinity of the interface of the conductor-semiconductor junction can make the conductor-semiconductor junction an ohmic junction.

[0044]

Further, it is also made clear that when a conductor having an electron affinity higher than the work function of the semiconductor layer is used as a material of the gate, the gate can have a function of eliminating electrons in the semiconductor. For example, tungsten and platinum can be given as examples of the material of the gate. It is found out that the off-state current can be made extremely small when using such a gate material.

[0045]

On the basis of the above consideration, a conceptual distribution of the carrier concentration in the semiconductor layer 102 of the FET illustrated in FIG. 5A in the case where the first conductor electrode 103a, the second conductor electrode 103b, and the gate 105 have the same potential is illustrated in FIG. 5B. Here, assuming that the work function of each of the first conductor electrode 103a and the second conductor electrode 103b is  $W_m$ , the work function of the gate 105 is  $W_g$ , and the electron affinity of the semiconductor layer 102 is  $\phi$ , the following conditions are satisfied:  $W_m < \phi + 0.3$  electron volts,  $W_g > \phi + 0.6$  electron volts.

[0046]

As illustrated in FIG. 5B, electrons are injected from the first conductor electrode 103a and the second conductor electrode 103b, and a region 102a having an extremely high electron concentration is formed in the vicinity of the first conductor electrode 103a and the second conductor electrode 103b. In a portion close to the gate 105, a region 102e having an extremely low electron concentration is formed. Between the region 102a and the region 102e, the concentration of electrons is lower in

a portion that is more apart from the first conductor electrode 103a and the second conductor electrode 103b or in a region closer to the gate 105.

[0047]

FIG. 5B shows that the concentration of electrons in a region 102b is lower than that in the region 102a by approximately an order of magnitude, the concentration of electrons in a region 102c is lower than that in the region 102b by approximately an order of magnitude, and the concentration of electrons in a region 102d is lower than that in the region 102c by approximately an order of magnitude. As the concentration of electrons is increased, the conductivity is increased. On the other hand, as the concentration of electrons is decreased, the conductivity is decreased. For example, the semiconductor layer 102 in the region 102e is an insulator.

[0048]

The off-state current of the FET illustrated in FIG. 5B is determined by the region 102e which is formed in a middle area between the first conductor electrode 103a and the second conductor electrode 103b. Meanwhile, it is found that the portion where the first conductor electrode 103a and the gate 105 overlap with each other, the portion where the second conductor electrode 103b and the gate 105 overlap with each other, and a peripheral region of the portions have little influence on the reduction of the off-state current.

[0049]

If the distance between the first conductor electrode 103a and the second conductor electrode 103b is reduced in the FET illustrated in FIG. 5A, the region 102e is narrowed and the region having a higher concentration of electrons than the region 102e is widened. This state is not favorable because the off-state current is increased. Therefore, a certain value of the distance needs to be assured between the first conductor electrode 103a and the second conductor electrode 103b in order to make an off-state current smaller than or equal to a certain value.

[0050]

The present inventor has noticed that the distribution of the concentration of electrons as illustrated in FIG. 5B can also be obtained with a structure other than the structure of FIG. 5A, for example, with a structure as illustrated in FIG. 1A. In the FET having the structure of FIG. 1A, the first conductor electrode 103a and the second

conductor electrode 103b are provided so as not to overlap with the gate 105. In FIG. 1A, an offset region having a width  $d$  is provided between the first conductor electrode 103a and the gate 105.

[0051]

5 The FET illustrated in FIG. 1A may be provided over a substrate of an appropriate material. In such a case, the substrate may be positioned over the gate 105 or below the first conductor electrode 103a in the drawing.

[0052]

10 Normally, such an offset region has the same effect as the case of connecting a resistor in series with an FET. However, according to the consideration of the present inventor, it is found that even when such an offset region is provided, the influence on the operation of the FET is little as long as  $d$  is 100 nm or less, preferably 50 nm or less, and further preferably 20 nm or less.

[0053]

15 This is because electrons flow into the semiconductor layer 102 from the first conductor electrode 103a and the second conductor electrode 103b as described above and thereby a portion having a high concentration of electrons (e.g., the region 102c) is formed even in the offset region. In the case of an n-channel FET, when a positive potential is applied to the gate 105, a portion directly below the offset region in the region 102e and the region 102d in FIG. 1B becomes a region having a high concentration of electrons, and a path connecting the first conductor electrode 103a with the second conductor electrode 103b is formed.

20

[0054]

25 With such a structure, parasitic capacitance between the gate 105 and the first conductor electrode 103a and between the gate 105 and the second conductor electrode 103b can be sufficiently reduced. In order to enjoy this effect, the width  $d$  of the offset region is preferably 10 nm or more. When the width  $d$  of the offset region is less than 10 nm, parasitic capacitance between the gate 105 and the first conductor electrode 103a or between the gate 105 and the second conductor electrode 103b is significantly increased.

30

[0055]

In the FET illustrated in FIG. 1A, the first conductor electrode 103a and the

second conductor electrode 103b are provided on the surface different from the surface provided with the gate 105. An FET in which the first conductor electrode 103a and the second conductor electrode 103b are provided on the same surface that is provided with the gate 105 can also be manufactured.

5 [0056]

FIG. 1C illustrates an FET in which the first conductor electrode 103a, the second conductor electrode 103b, the gate insulating film 104, and the gate 105 are provided on the same surface of the semiconductor layer 102. Offset regions are provided between the gate 105 and the first conductor electrode 103a and between the  
10 gate 105 and the second conductor electrode 103b.

[0057]

The semiconductor layer 102 is in contact with the first conductor electrode 103a and the second conductor electrode 103b, whereby supply of electrons is caused; thus, regions having various concentrations of electrons are formed as illustrated in FIG.  
15 1C. The distribution of the concentration of electrons is slightly different from that of FIG. 1B since the first conductor electrode 103a and the second conductor electrode 103b are provided on the same surface that is provided with the gate 105.

[0058]

In the structure of FIG. 1C, the influence of the first conductor electrode 103a and the second conductor electrode 103b is relatively reduced particularly on the  
20 opposite side from the gate in the semiconductor layer 102; accordingly, the concentration of electrons in that portion is reduced as compared to the structure of FIG. 1B. As a result, the off-state current is further reduced.

[0059]

Since such an FET has a structure similar to that of a conventional silicon MOSFET, there are advantages in that a process such as multilayer wiring can be easily and simply carried out as compared to the structure of FIG. 1A and that higher integration can be achieved. Further, a doping process using ion implantation, which is necessary in the case of a conventional silicon MOSFET, is unnecessary in the  
25 structure of FIG. 1C. That is, a portion provided with the gate is automatically serves as a channel having an extremely low concentration of electrons, and the other portion corresponds to an extension region having moderate concentrations of electrons.  
30

[0060]

Electrons flow into the semiconductor layer 102 from the first conductor electrode 103a and the second conductor electrode 103b and the portion having moderate concentrations of electrons is formed, which means the portion having moderate concentrations of electrons has an intermediate resistance value between the  
5 resistance value of the on-state FET and the resistance value of the off-state FET.

[0061]

Back to FIGS. 5A to 5C, a conceptual distribution of the concentration of carriers in the semiconductor layer 102 in the case where the gate 105 is removed from the FET of FIG. 5A is illustrated in FIG. 5C. In this case, an effect of the gate that  
10 removes electrons cannot be obtained, and a region having a high concentration of electrons, which is wider than that of FIG. 5B, is formed due to electrons injected from the first conductor electrode 103a and the second conductor electrode 103b.

[0062]

In consideration of the fact that the FET in FIG. 5B is in an off state and a region having a higher concentration of electrons is formed in large area in the semiconductor layer 102 due to the gate 105 in an on state of the FET, FIG. 5C illustrates an FET in the intermediate state between the on state and the off state.  
15

[0063]

The resistance value (the resistance value in the region between the first conductor electrode 103a and the second conductor electrode 103b) in this state also has an intermediate value between the resistance value of the on-state FET and the resistance value of the off-state FET. The resistance value is inversely proportional to the carrier concentration. The resistivity of the semiconductor layer in the element  
20 having a structure in which the gate 105 is removed from the FET of FIG. 5A (hereinafter referred to as a resistor element) is lower than the resistivity of the semiconductor layer in the off-state FET including the same-thickness semiconductor layer by three to eight orders of magnitude.  
25

[0064]

It is preferable to use such a resistor element as a resistor in the inverter illustrated in FIG. 6A as described above. In particular, when the distance  $L$  between the first conductor electrode 103a and the second conductor electrode 103b is more than  
30

or equal to 100 nm and less than or equal to 10  $\mu\text{m}$ , the relation,  $R_{\text{ON}} \ll R \ll R_{\text{OFF}}$ , can be satisfied on the assumption of using the FET which has a channel length approximately the same as the distance  $L$  (a channel length more than or equal to 1/2 times of  $L$  and less than or equal to 5 times of  $L$ ) and has the on-state resistance  $R_{\text{ON}}$  and the off-state resistance  $R_{\text{OFF}}$ .

[0065]

At this time, it is preferable that the channel width of the FET is more than or equal to 50 % and less than or equal to 200 % of the width of the resistor element and the thickness of the semiconductor layer of the FET is more than or equal to 50 % and less than or equal to 200 % of the thickness of the semiconductor layer of the resistor element. Needless to say, it is possible to satisfy the above relation under other conditions.

[0066]

The work function of a conductor is discussed in the above description. The work function of a conductor may be a value determined by an interface with a semiconductor in a simplest assumption; however, a complex physical property such as generation of a compound of the semiconductor and the conductor due to chemical reaction or a trap of electric charge or another element is often observed at the interface in reality.

[0067]

In the case where a first conductor layer with an extremely small thickness of less than or equal to several nanometers and a second conductor layer with a relatively large thickness are stacked over a semiconductor layer in this order, for example, the influence of the work function of the first conductor layer is considerably reduced. Therefore, in application of the present invention, the design may be performed so that the work function or the like of each material at a position that is 5 nm away from an interface with the semiconductor layer satisfies favorable conditions of the present invention.

[0068]

The present invention is particularly effective for a semiconductor material in which substantially only one of an electron and a hole can be used as a carrier. In



other words, a favorable result can be obtained in accordance with the present invention, for example, in the case where the mobility of one of the electron and the hole is higher than or equal to  $1 \text{ cm}^2/\text{Vs}$  whereas the mobility of the other is lower than or equal to  $0.01 \text{ cm}^2/\text{Vs}$ , the other of the electron and the hole does not exist as a carrier, or the effective mass of the other of the electron and the hole is 100 times or more as large as that of a free electron.

#### BRIEF DESCRIPTION OF DRAWINGS

[0069]

10 In the accompanying drawings:

FIGS. 1A to 1C illustrate operation principles of field effect transistors of the present invention;

FIGS. 2A to 2C illustrate an example of a semiconductor circuit of the present invention;

15 FIGS. 3A to 3C illustrate an example of a semiconductor circuit of the present invention;

FIGS. 4A to 4D illustrate an example of a manufacturing process of a semiconductor circuit of the present invention;

FIGS. 5A to 5C illustrate principles of the present invention; and

20 FIGS. 6A and 6B are circuit diagrams of conventional inverters.

#### BEST MODE FOR CARRYING OUT THE INVENTION

[0070]

Hereinafter, embodiments will be described with reference to the drawings.

25 Note that the embodiments can be implemented in various modes, and it is easily understood by those skilled in the art that modes and details can be changed in various ways without departing from the spirit and scope of the present invention. Therefore, the present invention is not construed as being limited to the description of the embodiments. Note that in structures described below, the same portions or portions having similar functions are denoted by the same reference numerals in different drawings, and detailed description thereof is not repeated.

[0071]

(Embodiment 1)

In this embodiment, a semiconductor circuit illustrated in FIGS. 2A to 2C will be described. FIG. 2A is a conceptual diagram illustrating a cross section of the semiconductor circuit, and FIG. 2B illustrates the semiconductor circuit of FIG. 2A seen from the bottom side. As illustrated in FIG. 2A, this semiconductor circuit includes a first conductor electrode 103a, a second conductor electrode 103b, and a third conductor electrode 103c which are in contact with one surface of a semiconductor layer 102. The other surface of the semiconductor layer 102 is provided with a gate 105. A gate insulating film 104 is provided between the gate 105 and the semiconductor layer 102.

10 [0072]

A substrate may be provided either below the first conductor electrode 103a, the second conductor electrode 103b, and the third conductor electrode 103c or over the gate 105. The semiconductor layer 102 of this semiconductor circuit is generally rectangular as illustrated in FIG. 2B and provided with the first conductor electrode 103a, the second conductor electrode 103b, and the third conductor electrode 103c. In addition, it is preferable that the semiconductor layer 102 is formed of an i-type semiconductor, and the bandgap of the semiconductor is preferably greater than or equal to 2 electron volts and less than 4 electron volts, further preferably greater than or equal to 2.9 electron volts and less than 3.5 electron volts.

20 [0073]

The gate 105 is provided so as to overlap with a region of the semiconductor layer 102 between the first conductor electrode 103a and the second conductor electrode 103b (the region does not include a portion overlapping with the first conductor electrode 103a and the second conductor electrode 103b) but so as not to overlap with a region of the semiconductor layer 102 between the second conductor electrode 103b and the third conductor electrode 103c (the region does not include a portion overlapping with the second conductor electrode 103b and the third conductor electrode 103c).

[0074]

With such a structure, the first conductor electrode 103a, the second conductor electrode 103b, the gate 105, and a portion of the semiconductor layer 102 which is surrounded by the first conductor electrode 103a, the second conductor electrode 103b, and the gate 105 form an FET. In addition, the second conductor electrode 103b, the

third conductor electrode 103c, and a portion of the semiconductor layer 102 between the second conductor electrode 103b and the third conductor electrode 103c form a resistor.

[0075]

5 In other words, as illustrated in FIG. 2A, the former functions as a transistor portion, and the latter functions as a resistance portion. The distributions of the concentration of electrons in the transistor portion and the resistance portion of the semiconductor layer 102 are almost the same as the distribution illustrated in FIG. 5B and the distribution illustrated in FIG. 5C, respectively. Accordingly, as illustrated in  
10 the circuit diagram of FIG. 2C, an inverter of the type of FIG. 6A is obtained.

[0076]

Further, as illustrated in FIG. 2B, the length of the transistor portion in the channel width direction and the length of the resistance portion in a direction corresponding to the channel width direction are substantially the same. It is obvious  
15 from the following reason that the inverter having the structure of FIGS. 2A to 2C has higher integration than the inverter illustrated in FIG. 6B.

[0077]

For example, in formation of the inverter of the type of FIG. 6B in a similar manner, a gate needs to be provided also between the second conductor electrode 103b  
20 and the third conductor electrode 103c. However, in order to ensure the insulation between the gate 105 and a gate adjacent to the gate 105, a distance more than or equal to the minimal processing line width needs to be set between the adjacent gates. As a result, the width of the second conductor electrode 103b needs to be large.

[0078]

25 In FIGS. 2A and 2B, the minimal processing line width is a width of the first conductor electrode 103a, the second conductor electrode 103b, or the third conductor electrode 103c. Accordingly, in the inverter of the type of FIG. 6B, the width of the second conductor electrode 103b needs to be twice the width of that in FIGS. 2A and 2B. In contrast, in the inverter of the type of FIG. 6A, it is not necessary to provide a gate  
30 between the second conductor electrode 103b and the third conductor electrode 103c; accordingly, the width of the second conductor electrode 103b can be set to a minimal line width.

[0079]

The semiconductor device as illustrated in FIGS. 2A to 2C may be manufactured in the following manner: the first conductor electrode 103a, the second conductor electrode 103b, and the third conductor electrode 103c are formed over a substrate and then the semiconductor layer 102, the gate insulating film 104, and the gate 105 are formed.

[0080]

Alternatively, the following method may be employed: the gate 105 is formed over a substrate and then the gate insulating film 104, the semiconductor layer 102, the first conductor electrode 103a, the second conductor electrode 103b, and the third conductor electrode 103c are formed.

[0081]

Note that although the distance between the first conductor electrode 103a and the second conductor electrode 103b is substantially the same as the distance between the second conductor electrode 103b and the third conductor electrode 103c in FIGS. 2A to 2C, the former distance may be set more than or less than the latter distance.

[0082]

(Embodiment 2)

In this embodiment, a semiconductor circuit illustrated in FIGS. 3A to 3C will be described. FIG. 3A is a conceptual diagram illustrating a cross section of the semiconductor circuit, and FIG. 3B illustrates the semiconductor circuit of FIG. 3A seen from the bottom side. In a manner similar to that of the semiconductor device illustrated in FIGS. 2A to 2C, this semiconductor circuit includes a first conductor electrode 103a, a second conductor electrode 103b, and a third conductor electrode 103c which are in contact with one surface of a semiconductor layer 102, as illustrated in FIG. 3A. The other surface of the semiconductor layer 102 is provided with a gate 105. A gate insulating film 104 is provided between the gate 105 and the semiconductor layer 102. It is preferable that the semiconductor layer 102 is formed of an i-type semiconductor, and the bandgap of the semiconductor is preferably greater than or equal to 2 electron volts and less than 4 electron volts, further preferably greater than or equal to 2.9 electron volts and less than 3.5 electron volts.

[0083]

The gate 105 is provided so as to overlap with at least part of a region *A* of the semiconductor layer 102 between the first conductor electrode 103a and the second conductor electrode 103b (the region *A* does not include a portion overlapping with the first conductor electrode 103a and the second conductor electrode 103b) but so as not to overlap with a region *B* of the semiconductor layer 102 between the second conductor electrode 103b and the third conductor electrode 103c (the region *B* does not include a portion overlapping with the second conductor electrode 103b and the third conductor electrode 103c).

[0084]

10 A point different from that of the semiconductor device illustrated in FIGS. 2A to 2C is that the gate 105 overlaps with neither the first conductor electrode 103a nor the second conductor electrode 103b and offset regions are included. In other words, the offset regions having a length *d* are included between the gate 105 and the first conductor electrode 103 and between the gate 105 and the second conductor electrode 103b.

15 [0085]

The semiconductor layer 102 of this semiconductor circuit has a complicated shape as illustrated in FIG. 3B. The semiconductor layer 102 has a wide width in the left part (in a portion including the region *A*) and a narrow width in the right part (in a portion including the region *B*). In this manner, the resistance in the right part is increased and the resistance ratio of the resistance in the right part with respect to the resistance in the left part is adjusted.

[0086]

25 Also in this semiconductor device, in a manner similar to that of Embodiment 1, the first conductor electrode 103a, the second conductor electrode 103b, the gate 105, and a portion of the semiconductor layer 102 which is surrounded by the first conductor electrode 103a, the second conductor electrode 103b, and the gate 105 form an FET which is similar to that of FIG. 1A. In addition, the second conductor electrode 103b, the third conductor electrode 103c, and a portion of the semiconductor layer 102 between the second conductor electrode 103b and the third conductor electrode 103c form a resistor which is similar to that of FIG. 5C.

30 [0087]

In other words, as illustrated in FIG. 3A, the former functions as a transistor portion, and the latter functions as a resistance portion. The distributions of the concentration of electrons in the transistor portion and the resistance portion of the semiconductor layer 102 are almost the same as the distribution illustrated in FIG. 1B and the distribution illustrated in FIG. 5C, respectively. The circuit diagram is illustrated in FIG. 3C. This semiconductor device can be used as the inverter illustrated in FIG. 6A. The resistance of the resistance portion of this semiconductor device is higher than that of Embodiment 1.

[0088]

10 In the inverter of this embodiment, the resistance can be made high when the input of the transistor is Low; accordingly, power consumption can be reduced. In addition, for the same reason, a breakdown of an element due to a flow-through current can be prevented; accordingly, reliability can be increased.

[0089]

15 By the way, in the case where an inverter of the type of FIG. 6B is manufactured using a FET including an offset region like the one described in this embodiment, the reduction in the degree of integration, which has been pointed out in Embodiment 1, can be overcome. In other words, due to the existence of the offset region, the distance between gates is more than the minimal line width. Accordingly, even in the case of forming the second conductor electrode 103b to have a minimal line width, a gate adjacent to the gate 105 can be provided between the second conductor electrode 103b and the third conductor electrode 103c.

[0090]

25 However, since a contact between the gate and the conductor electrode needs to be obtained as described above, the degree of integration is reduced as compared to the type of FIG. 6A.

[0091]

(Embodiment 3)

30 In this embodiment, a manufacturing method of a semiconductor device will be described with reference to FIGS. 4A to 4D. First, as illustrated in FIG. 4A, a semiconductor layer 102 and a gate insulating film 104 are formed over a substrate 101. A variety of substrates can be given as examples of the substrate 101, but the substrate

101 needs to have such a property as to withstand the subsequent treatment. Further, it is preferable that a surface of the substrate 101 has an insulating property. Accordingly, the substrate 101 is preferably a single insulator; an insulator, metal, or semiconductor whose surface is provided with an insulating layer; or the like.

5 [0092]

In the case of using an insulator for the substrate 101, various kinds of glasses, sapphire, quartz, ceramics, or the like can be used. In the case of using a metal, aluminum, copper, stainless steel, silver, or the like can be used. In the case of using a semiconductor, silicon, germanium, silicon carbide, gallium nitride, or the like can be used. In this embodiment, barium borosilicate glass is used as the substrate 101.

[0093]

As a semiconductor material of the semiconductor layer 102, an oxide semiconductor including indium and zinc is used. Other than the above oxide semiconductor, a variety of oxide semiconductors can be used. In this embodiment, the semiconductor layer 102 is formed in the following manner: an indium zinc oxide film having a thickness of 30 nm is formed by a sputtering method using an oxide target including equal amounts of indium and zinc and then the film is patterned.

[0094]

An insulating film formed by a sputtering method is used as the gate insulating film 104. As a material of the gate insulating film 104, silicon oxide, aluminum oxide, aluminum nitride, hafnium oxide, lanthanum oxide, yttrium oxide, or the like can be used. In this embodiment, aluminum oxide having a thickness of 100 nm is formed by a sputtering method as the gate insulating film 104.

[0095]

Appropriate heat treatment is preferably performed either after formation of the semiconductor layer 102 or after formation of the gate insulating film 104 or at both of the timings. This heat treatment is for reducing the hydrogen concentration or oxygen vacancies in the semiconductor layer 102, and if possible, the heat treatment is preferably performed right after formation of the semiconductor layer 102.

30 [0096]

In the heat treatment, it is preferable that heat treatment in a reducing atmosphere is initially performed and then heat treatment in an oxygen atmosphere is

performed. In the initial heat treatment in a reducing atmosphere, hydrogen is efficiently released together with oxygen. In the next heat treatment in an oxygen atmosphere, oxygen vacancies can be reduced.

[0097]

5 Then, a gate 105 is formed as illustrated in FIG. 4B. A material of the gate 105 can be a metal having a high work function such as platinum, gold, or tungsten. Alternatively, a compound having an electron affinity of 5 electron volts or more, such as indium nitride, may be used. The gate 105 may include a single material of any of the above-described materials or may have a multilayer structure where a portion in  
10 contact with the gate insulating film 104 includes any of the above-described materials. In this embodiment, a 100-nm-thick platinum film and a 100-nm-thick aluminum film are formed by a sputtering method and etched, so that the gate 105 is formed.

[0098]

Further, an interlayer insulator 106 is formed by a sputtering method. The  
15 interlayer insulator 106 is preferably formed using a material having a low dielectric constant. In this embodiment, the interlayer insulator 106 is a silicon oxide film having a thickness of 300 nm formed by a CVD method. As illustrated in FIG. 4C, the interlayer insulator 106 is planarized by a chemical mechanical polishing (CMP) method.

20 [0099]

Then, contact holes reaching the semiconductor layer 102 are formed, and a first conductor electrode 103a, a second conductor electrode 103b, and a third conductor electrode 103c are formed. In this embodiment, a 50-nm-thick titanium nitride film and a 150-nm-thick titanium film are successively formed by a sputtering method and  
25 patterned, so that the first conductor electrode 103a, the second conductor electrode 103b, and the third conductor electrode 103c are formed. In this manner, a semiconductor circuit illustrated in FIG. 4D is formed.

[0100]

A portion on the left side of the semiconductor layer 102 in FIG. 4D, over  
30 which the gate 105 is formed, functions as an active layer of a FET, and a portion on the right side in FIG. 4D, over which the gate 105 is not provided, functions as a resistor. This circuit can be used as the inverter illustrated in FIG. 6A.



[0101]

(Embodiment 4)

The semiconductor devices described in Embodiments 1 to 3 can be used in a variety of electronic devices, for example, in driver circuits for display devices such as liquid crystal displays, EL (electro luminescent) displays, and FE (field emission) displays, driver circuits for image sensors, semiconductor memories, and the like. Further, the semiconductor devices described in Embodiments 1 to 3 can be used in electronic devices including the above-described electronic devices, for example, in television sets, personal computers, communication devices such as mobile phones, electronic notebooks, portable music players, and the like.

This application is based on Japanese Patent Application serial no. 2010-024580 filed with Japan Patent Office on February 5, 2010, the entire contents of which are hereby incorporated by reference.

## CLAIMS

1. A field effect transistor comprising:

a semiconductor layer;

5 a first conductor electrode and a second conductor electrode which are provided in contact with one surface of the semiconductor layer; and

a gate provided on the other surface side of the semiconductor layer,

wherein an offset region is formed in at least one of a region between the first conductor electrode and the gate and a region between the second conductor electrode and the gate, and

10 wherein a bandgap of the semiconductor layer is greater than or equal to 2 electron volts and less than 4 electron volts.

2. A field effect transistor comprising:

a semiconductor layer;

15 a first conductor electrode and a second conductor electrode which are provided in contact with one surface of the semiconductor layer; and

a gate provided on the other surface side of the semiconductor layer,

20 wherein an offset region is formed in at least one of a region between the first conductor electrode and the gate and a region between the second conductor electrode and the gate.

3. A field effect transistor comprising:

a semiconductor layer;

25 a first conductor electrode and a second conductor electrode provided in contact with one surface of the semiconductor layer; and

a gate provided over the same surface,

30 wherein an offset region is formed in at least one of a region between the first conductor electrode and the gate and a region between the second conductor electrode and the gate.

4. A semiconductor device comprising:

a semiconductor layer;

a first conductor electrode, a second conductor electrode, and a third conductor electrode which are provided in contact with one surface of the semiconductor layer; and

a gate provided on the other surface side of the semiconductor layer,

5 wherein the gate overlaps with at least part of a region between the first conductor electrode and the second conductor electrode, and

wherein the gate does not overlap with a region between the second conductor electrode and the third conductor electrode.

10 5. A semiconductor device comprising:

a semiconductor layer;

a first conductor electrode, a second conductor electrode, and a third conductor electrode which are provided in contact with one surface of the semiconductor layer; and

15 a gate provided over the same surface of the semiconductor layer,

wherein the gate overlaps with at least part of a region between the first conductor electrode and the second conductor electrode, and

wherein the gate does not overlap with a region between the second conductor electrode and the third conductor electrode.

20

6. The field effect transistor according to claim 1, wherein a portion of the first conductor electrode and a portion of the second conductor electrode which are in contact with the semiconductor layer have a work function lower than a sum of an electron affinity of the semiconductor layer and 0.3 electron volts.

25

7. The field effect transistor according to claim 2, wherein a portion of the first conductor electrode and a portion of the second conductor electrode which are in contact with the semiconductor layer have a work function lower than a sum of an electron affinity of the semiconductor layer and 0.3 electron volts.

30

8. The field effect transistor according to claim 3, wherein a portion of the first conductor electrode and a portion of the second conductor electrode which are in

contact with the semiconductor layer have a work function lower than a sum of an electron affinity of the semiconductor layer and 0.3 electron volts.

9. The semiconductor device according to claim 4, wherein a portion of the  
5 first conductor electrode and a portion of the second conductor electrode which are in contact with the semiconductor layer have a work function lower than a sum of an electron affinity of the semiconductor layer and 0.3 electron volts.

10. The semiconductor device according to claim 5, wherein a portion of the  
10 first conductor electrode and a portion of the second conductor electrode which are in contact with the semiconductor layer have a work function lower than a sum of an electron affinity of the semiconductor layer and 0.3 electron volts.

11. The field effect transistor according to claim 1, wherein an ohmic junction  
15 is formed between the semiconductor layer and the first conductor electrode and between the semiconductor layer and the second conductor electrode.

12. The field effect transistor according to claim 2, wherein an ohmic junction  
is formed between the semiconductor layer and the first conductor electrode and  
20 between the semiconductor layer and the second conductor electrode.

13. The field effect transistor according to claim 3, wherein an ohmic junction  
is formed between the semiconductor layer and the first conductor electrode and  
between the semiconductor layer and the second conductor electrode.

25

14. The semiconductor device according to claim 4, wherein an ohmic junction  
is formed between the semiconductor layer and the first conductor electrode and  
between the semiconductor layer and the second conductor electrode.

30

15. The semiconductor device according to claim 5, wherein an ohmic junction  
is formed between the semiconductor layer and the first conductor electrode and  
between the semiconductor layer and the second conductor electrode.

16. The field effect transistor according to claim 1, further comprising a gate insulating film between the semiconductor layer and the gate.

5 17. The field effect transistor according to claim 2, further comprising a gate insulating film between the semiconductor layer and the gate.

18. The field effect transistor according to claim 3, further comprising a gate insulating film between the semiconductor layer and the gate.

10

19. The semiconductor device according to claim 4, further comprising a gate insulating film between the semiconductor layer and the gate.

15 20. The semiconductor device according to claim 5, further comprising a gate insulating film between the semiconductor layer and the gate.

21. The field effect transistor according to claim 1, wherein a work function of a portion of the gate which is the closest to the semiconductor layer is higher than a sum of an electron affinity of the semiconductor layer and 0.6 electron volts.

20

22. The field effect transistor according to claim 2, wherein a work function of a portion of the gate which is the closest to the semiconductor layer is higher than a sum of an electron affinity of the semiconductor layer and 0.6 electron volts.

25 23. The field effect transistor according to claim 3, wherein a work function of a portion of the gate which is the closest to the semiconductor layer is higher than a sum of an electron affinity of the semiconductor layer and 0.6 electron volts.

30 24. The semiconductor device according to claim 4, wherein a work function of a portion of the gate which is the closest to the semiconductor layer is higher than a sum of an electron affinity of the semiconductor layer and 0.6 electron volts.

25. The semiconductor device according to claim 5, wherein a work function of a portion of the gate which is the closest to the semiconductor layer is higher than a sum of an electron affinity of the semiconductor layer and 0.6 electron volts.

5           26. The field effect transistor according to claim 1, wherein a width of the offset region is more than or equal to 10 nm and less than or equal to 100 nm.

27. The field effect transistor according to claim 2, wherein a width of the offset region is more than or equal to 10 nm and less than or equal to 100 nm.

10

28. The field effect transistor according to claim 3, wherein a width of the offset region is more than or equal to 10 nm and less than or equal to 100 nm.

29. The semiconductor device according to claim 4, wherein a width of a first  
15 portion of the semiconductor layer between the first conductor electrode and the second conductor electrode is wider than that of a second portion of the semiconductor layer between the second conductor electrode and the third conductor electrode.

30. The semiconductor device according to claim 5, wherein a width of a first  
20 portion of the semiconductor layer between the first conductor electrode and the second conductor electrode is wider than that of a second portion of the semiconductor layer between the second conductor electrode and the third conductor electrode.

31. The field effect transistor according to claim 1, wherein the semiconductor  
25 layer comprises an i-type semiconductor.

32. The field effect transistor according to claim 2, wherein the semiconductor layer comprises an i-type semiconductor.

30           33. The field effect transistor according to claim 3, wherein the semiconductor layer comprises an i-type semiconductor.

34. The semiconductor device according to claim 4, wherein the semiconductor layer comprises an i-type semiconductor.

5 35. The semiconductor device according to claim 5, wherein the semiconductor layer comprises an i-type semiconductor.

10 36. The field effect transistor according to claim 1, wherein the gate comprises a material selected from the group consisting of platinum, gold, tungsten, and indium nitride.

37. The field effect transistor according to claim 2, wherein the gate comprises a material selected from the group consisting of platinum, gold, tungsten, and indium nitride.

15 38. The field effect transistor according to claim 3, wherein the gate comprises a material selected from the group consisting of platinum, gold, tungsten, and indium nitride.

20 39. The semiconductor device according to claim 4, wherein the gate comprises a material selected from the group consisting of platinum, gold, tungsten, and indium nitride.

25 40. The semiconductor device according to claim 5, wherein the gate comprises a material selected from the group consisting of platinum, gold, tungsten, and indium nitride.

41. The semiconductor device according to claim 4, wherein the semiconductor device is an inverter.

30 42. The semiconductor device according to claim 5, wherein the semiconductor device is an inverter.

FIG. 1A

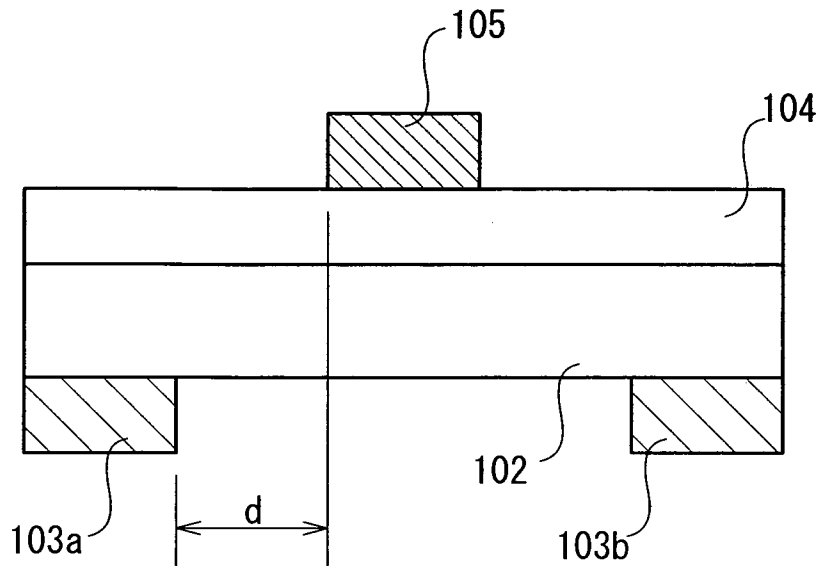


FIG. 1B

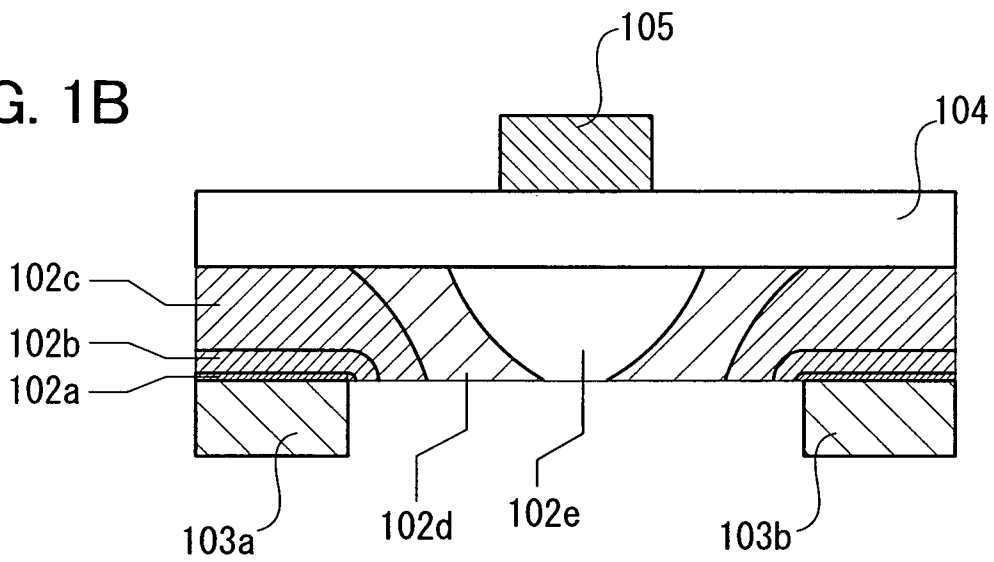


FIG. 1C

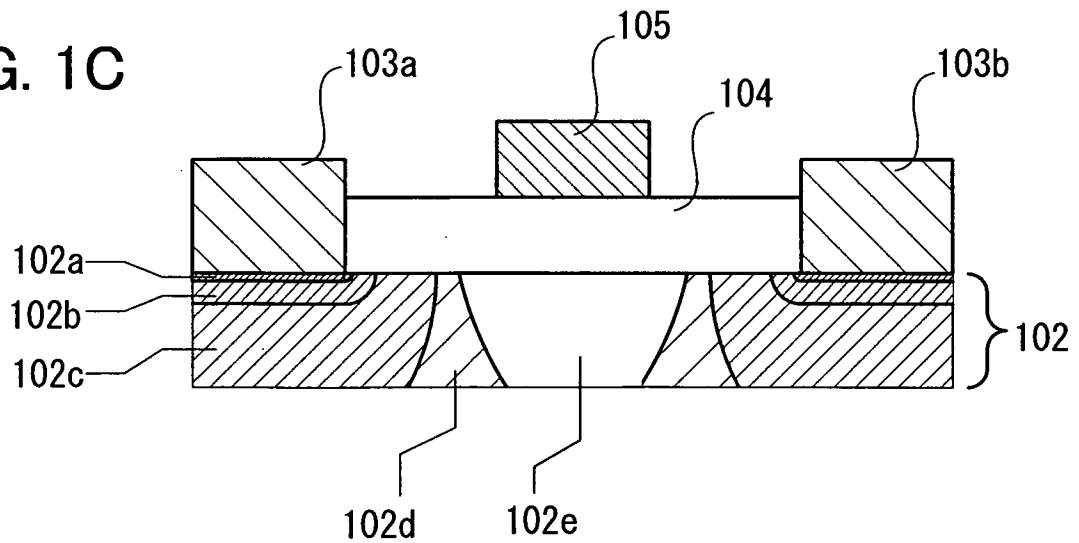




FIG. 2A

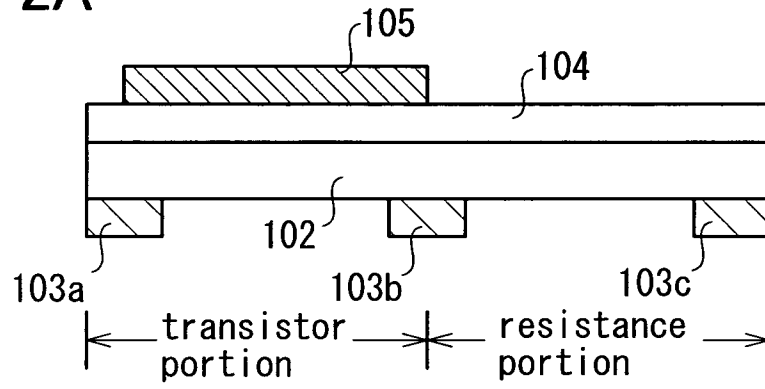


FIG. 2B

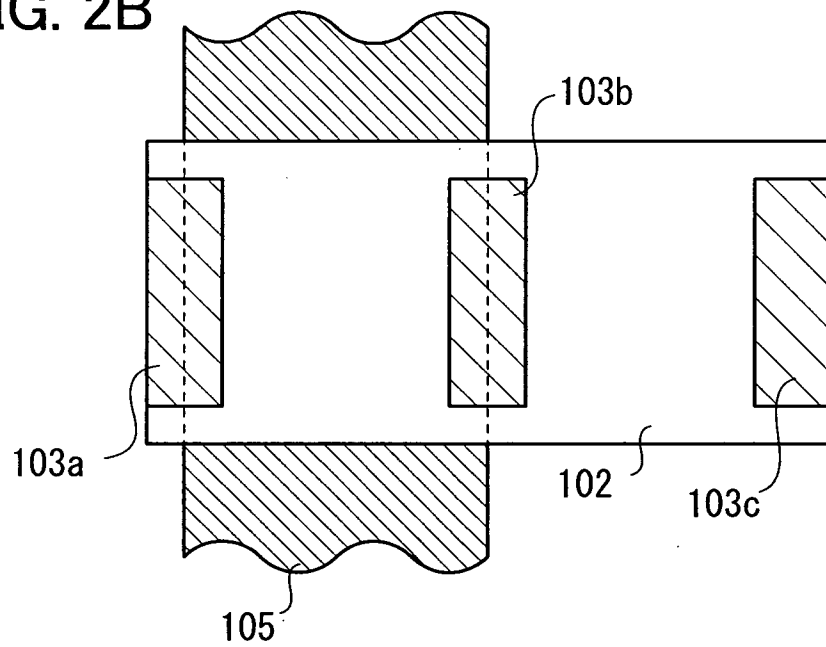


FIG. 2C

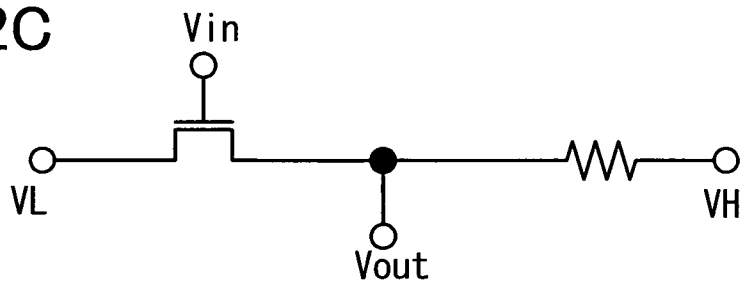


FIG. 3A

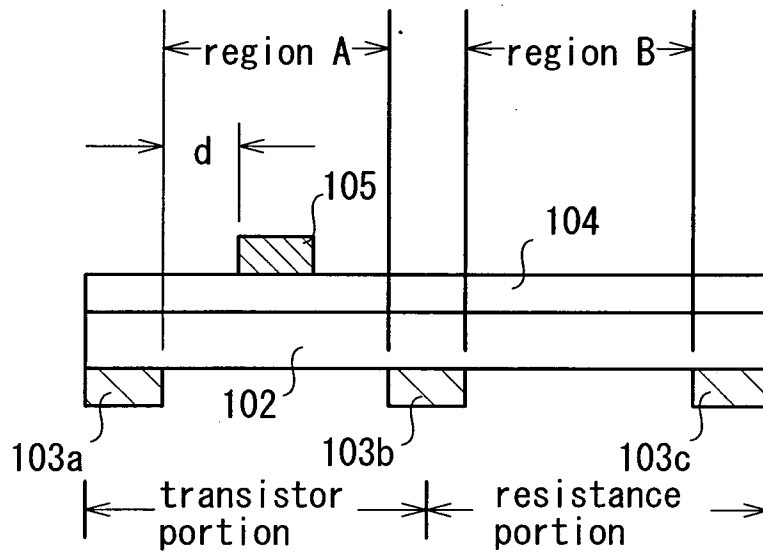


FIG. 3B

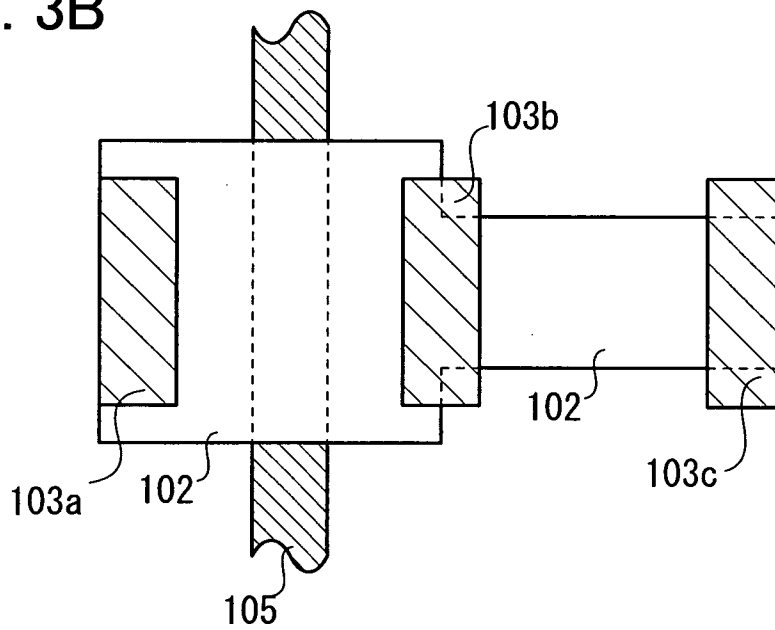


FIG. 3C

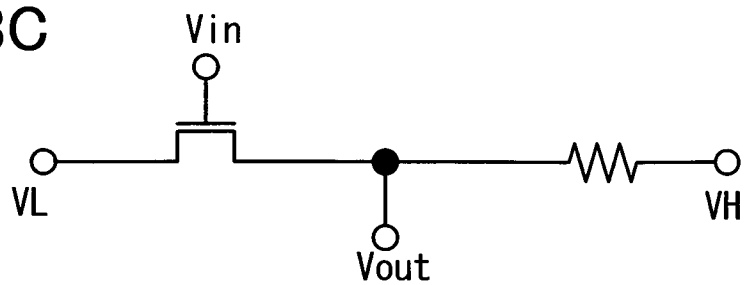


FIG. 4A

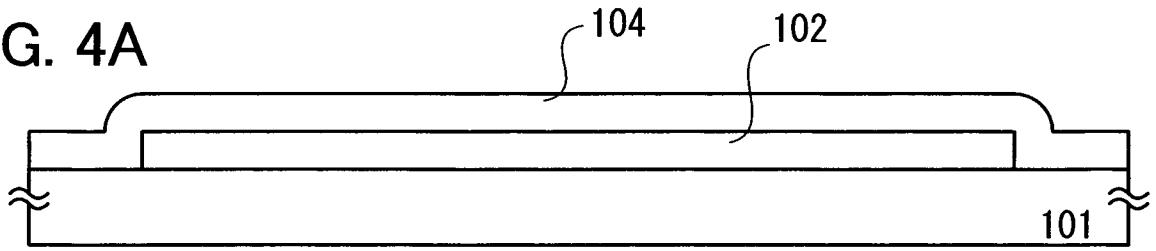


FIG. 4B

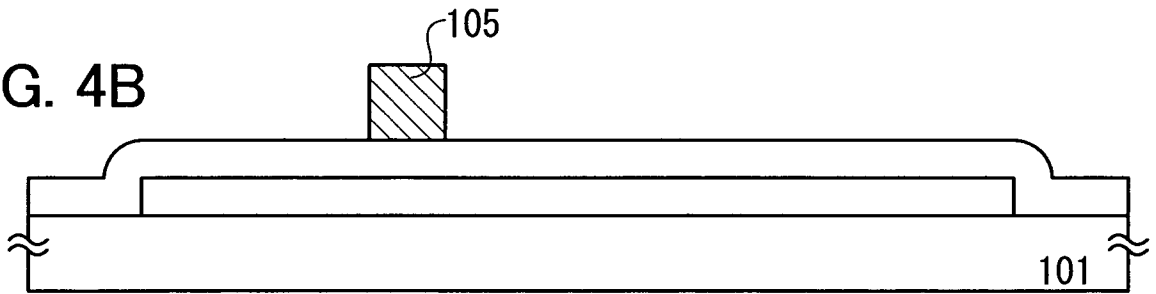


FIG. 4C

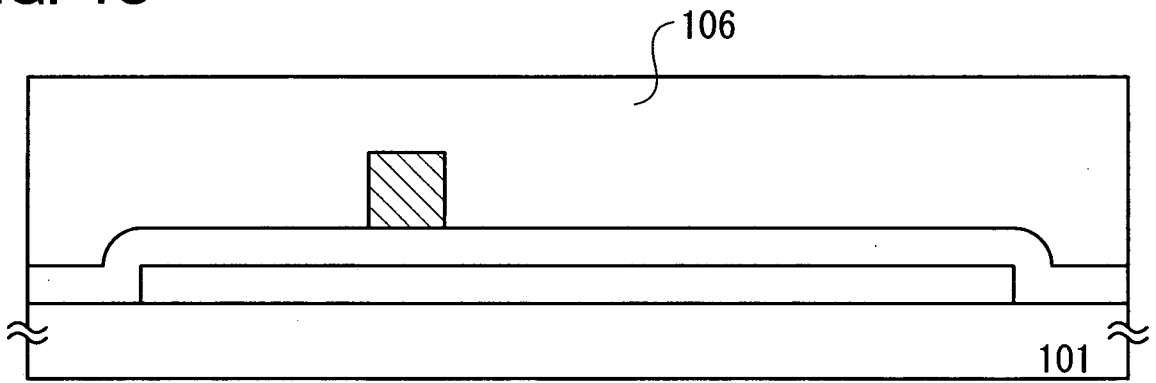
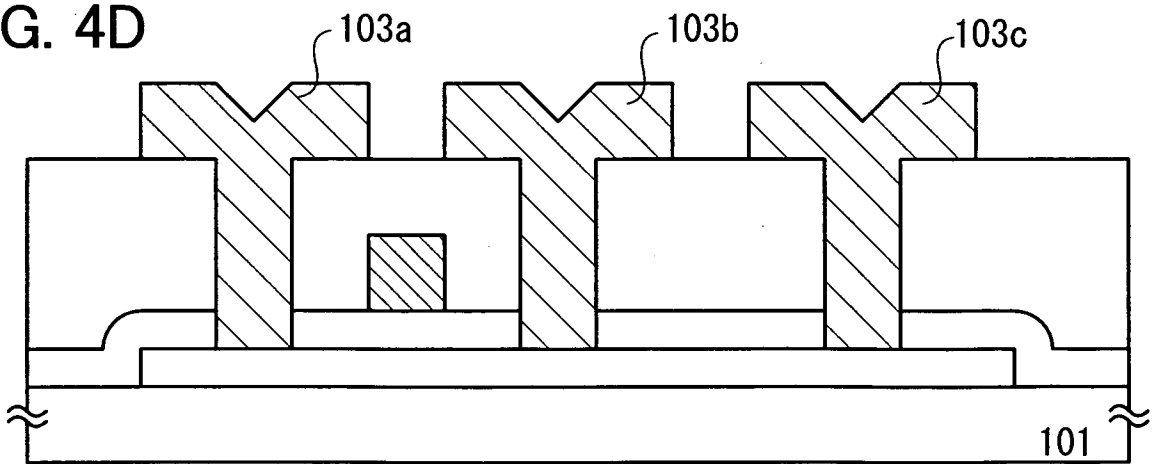


FIG. 4D



← transistor portion →      ← resistance portion →

FIG. 5A

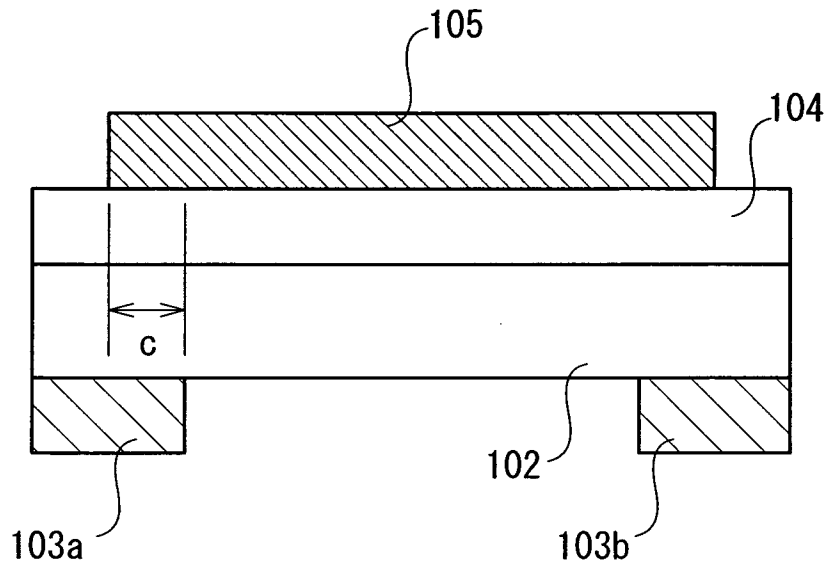


FIG. 5B

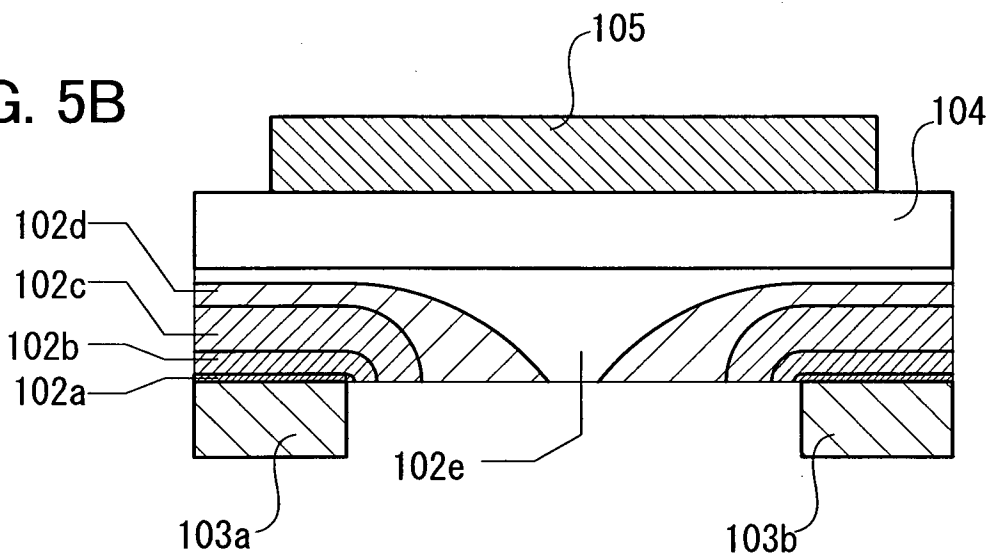


FIG. 5C

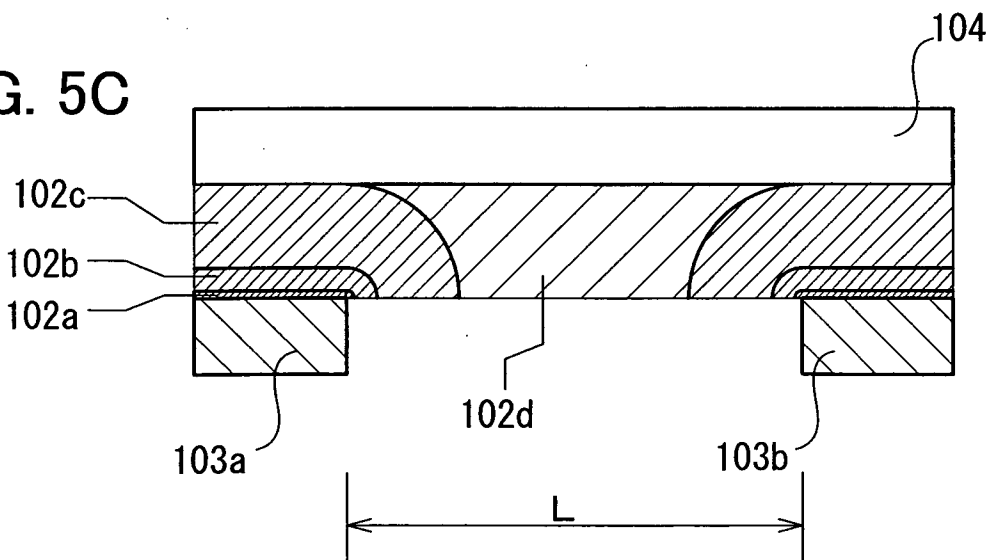


FIG. 6A

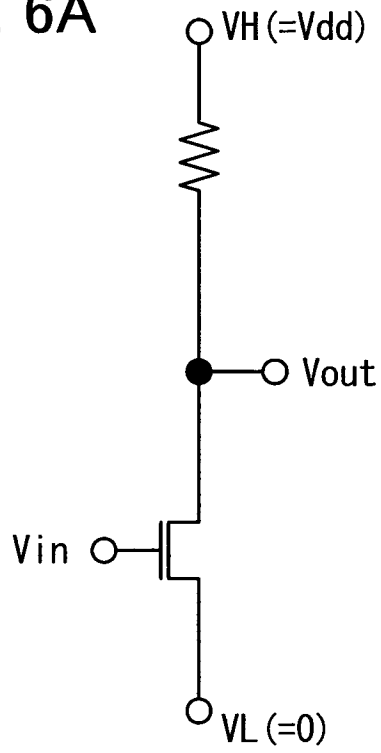
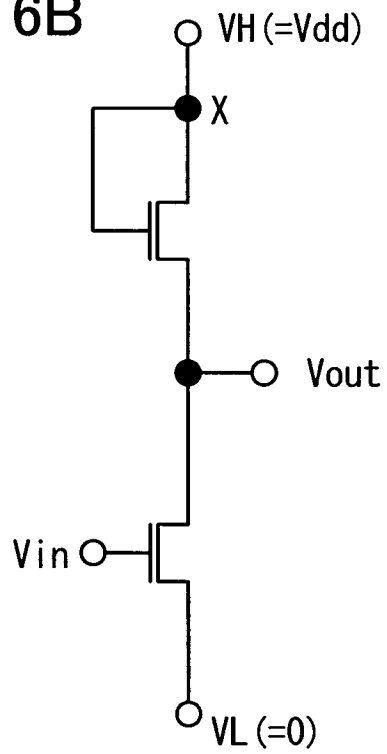


FIG. 6B



EXPLANATION OF REFERENCE

101: substrate, 102: semiconductor layer, 103a: first conductor electrode, 103b: second conductor electrode, 103c: third conductor electrode, 104: gate insulating film, 105: gate, and 106: interlayer insulator.

## INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2011/051143

A. CLASSIFICATION OF SUBJECT MATTER		
Int.Cl. H01L21/336(2006.01) i, H01L21/28(2006.01) i, H01L29/417(2006.01) i, H01L29/423(2006.01) i, H01L29/49(2006.01) i, H01L29/786(2006.01) i		
According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED		
Minimum documentation searched (classification system followed by classification symbols)		
Int.Cl. H01L21/336, H01L21/28, H01L29/417, H01L29/423, H01L29/49, H01L29/786		
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched		
Published examined utility model applications of Japan 1922-1996 Published unexamined utility model applications of Japan 1971-2011 Registered utility model specifications of Japan 1996-2011 Published registered utility model applications of Japan 1994-2011		
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	JP 2007-123861 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2007.05.17, [0047]-[0071], Fig.1,3 & US 2007/0072439 A1 & EP	2, 3, 7, 8, 12, 13, 17, 18, 22, 23, 32 , 33, 37, 38
Y	1770788 A2 & CN 1941299 A	1, 6, 11, 16, 21, 2 6-28, 31, 36
A		4, 5, 9, 10, 14, 15 , 19, 20, 24, 25, 2 9, 30, 34, 35, 39- 42
Y	JP 2010-028021 A (FUJIFILM CORPORATION) 2010.02.04, [0022] (No Family)	1, 6, 11, 16, 21, 2 6, 31, 36
<input checked="" type="checkbox"/> Further documents are listed in the continuation of Box C. <input type="checkbox"/> See patent family annex.		
* Special categories of cited documents: "A" document defining the general state of the art which is not considered to be of particular relevance "E" earlier application or patent but published on or after the international filing date "L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified) "O" document referring to an oral disclosure, use, exhibition or other means "P" document published prior to the international filing date but later than the priority date claimed "T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone "Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art "&" document member of the same patent family		
Date of the actual completion of the international search		Date of mailing of the international search report
15.04.2011		26.04.2011
Name and mailing address of the ISA/JP		Authorized officer
<b>Japan Patent Office</b>		Nobutaka SHIBAYAMA
3-4-3, Kasumigaseki, Chiyoda-ku, Tokyo 100-8915, Japan		4M 4 6 6 5
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## INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2011/051143

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2010-016126 A (FUJIFILM CORPORATION) 2010.01.21, [0058] (No Family)	26-28
A	JP 2007-142041 A (TOSHIBA CORPORATION) 2007.06.07, [0019]-[0021], Fig.7 & US 2007/0108518 A1 & CN 1967875 A	4, 5, 9, 10, 14, 15, 19, 20, 24, 25, 29, 30, 34, 35, 39-42



## INTERNATIONAL SEARCH REPORT

International application No.

PCT/JP2011/051143

**Box No. II Observations where certain claims were found unsearchable (Continuation of item 2 of first sheet)**

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1.  Claims Nos.:  
because they relate to subject matter not required to be searched by this Authority, namely:
  
2.  Claims Nos.:  
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:
  
3.  Claims Nos.:  
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

**Box No. III Observations where unity of invention is lacking (Continuation of item 3 of first sheet)**

This International Searching Authority found multiple inventions in this international application, as follows:

Claim 2,3 lack novelty over JP 2007-123861 A (SEMICONDUCTOR ENERGY LABORATORY CO., LTD.) 2007.05.17, [0047]-[0071], Fig.1,3 & US 2007/0072439 A1 & EP 1770788 A2 & CN 1941299 A, and involve no special technical features.

1.  As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.
2.  As all searchable claims could be searched without effort justifying additional fees, this Authority did not invite payment of additional fees.
3.  As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:
  
4.  No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

**Remark on Protest**

- The additional search fees were accompanied by the applicant's protest and, where applicable, the payment of a protest fee.
- The additional search fees were accompanied by the applicant's protest but the applicable protest fee was not paid within the time limit specified in the invitation.
- No protest accompanied the payment of additional search fees.