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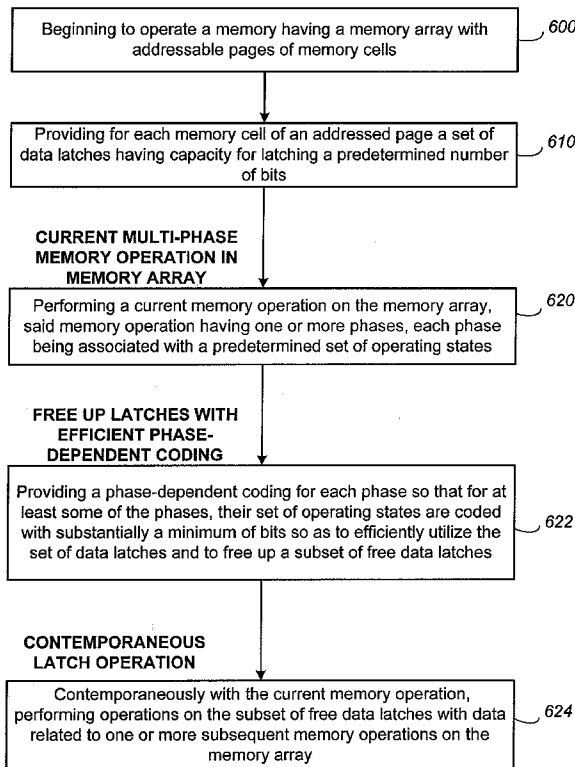
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[Continued on next page]

(54) Title: NON-VOLATILE MEMORY WITH BACKGROUND DATA LATCH CACHING DURING PROGRAM OPERATIONS AND METHODS THEREFOR



LATCH OPERATION CONTEMPORANEOUS WITH CURRENT MULTI-PHASE MEMORY OPERATION

(57) Abstract: Part of the latency from memory read or write operations is for data to be input to or output from the data latches of the memory via an I/O bus. Methods and circuitry are present for improving performance in non-volatile memory devices by allowing the memory to perform some of these data caching and transfer operations in the background while the memory core is busy with a write operation. In the exemplary embodiment, when the multiple phases of a write operation vary as to the number of states to track, a phase-dependent coding enables efficient utilization of the available data latches, thereby allowing a maximum of surplus latches for background cache operations.

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G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

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