(12) UK Patent Application (19) GB (11) 2 141 847 A

(43) Application published 3 Jan 1985

(21) Application No 8411337

(22) Date of filing 3 May 1984

(30) Priority data

(31) 58/079797 (32) 6 May 1983 (33) JP
58/188017 7 Oct 1983

(51) INT CL[3]
G06F 15/347

(52) Domestic classification
G4A MV
U1S 2284 G4A

(56) Documents cited
None

(58) Field of search
G4A

(71) Applicant
Seiko Instruments & Electronics Ltd. (Japan),
31-1 6-chome Kameido, Koto-ku, Tokyo, Japan

(72) Inventors
Takaomi Tatemichi,
Masato Takahashi

(74) Agent and/or Address for Service
J. Miller & Co.,
Lincoln House, 296-302 High Holborn, London WC1V 7JH

(54) Matrix multiplication apparatus for graphic display

(57) A matrix multiplication apparatus comprises memory (10), constituted by random access memories (102-132), for storing elements of image transformation matrices. The memory addresses are each divided into high address and low address parts. The high address parts specify particular matrix elements, and the low address parts access the elements sequentially bit-by-bit, starting from the least significant bit, so as to enable serial reading. A multiplication unit consists of pairs of serial multiplicators (502-532) which are either used in a cascade connection or independently as independent multiplicators, in order to correspond to the data length of a multiplicand.

FIG.4a

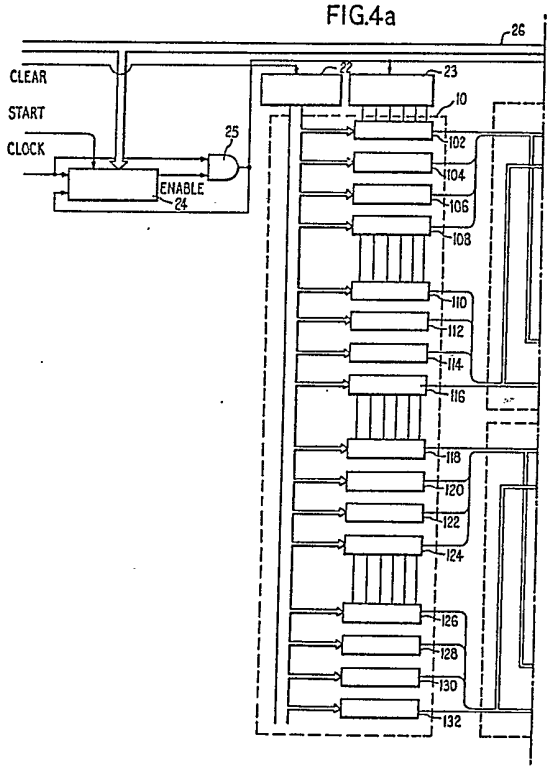
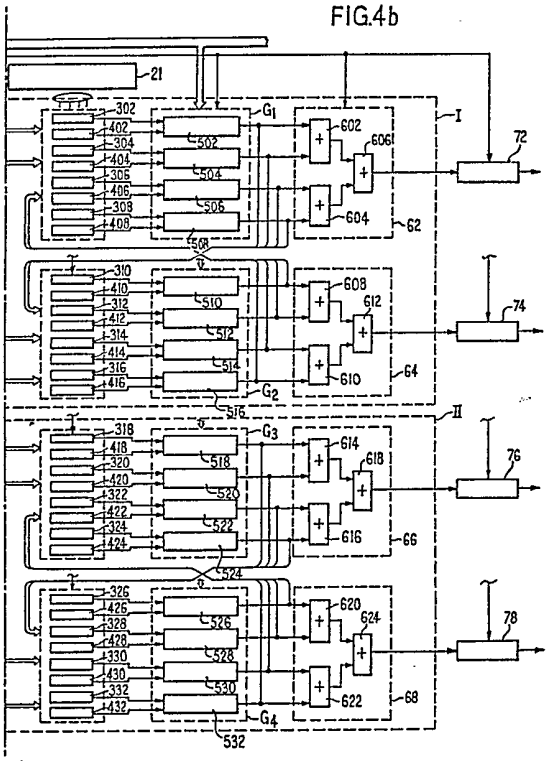


FIG.4b



GB 2 141 847 A

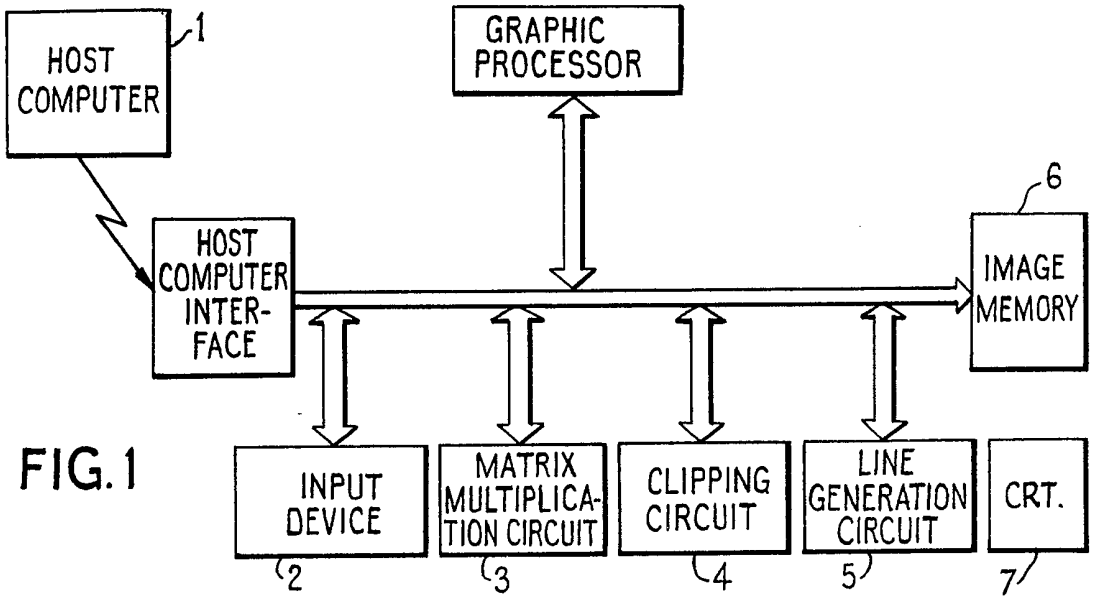


FIG. 1

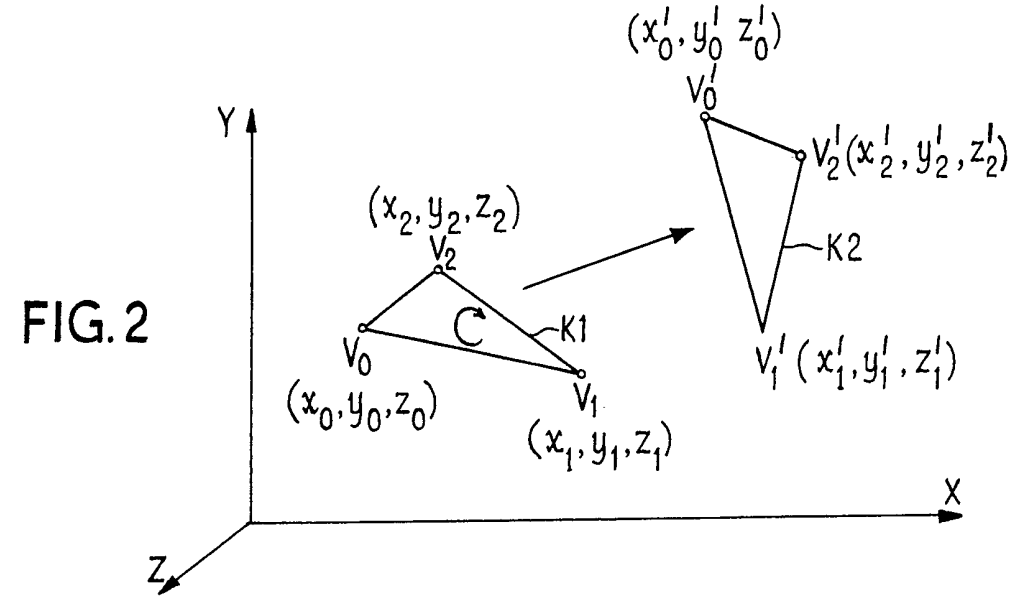


FIG. 2

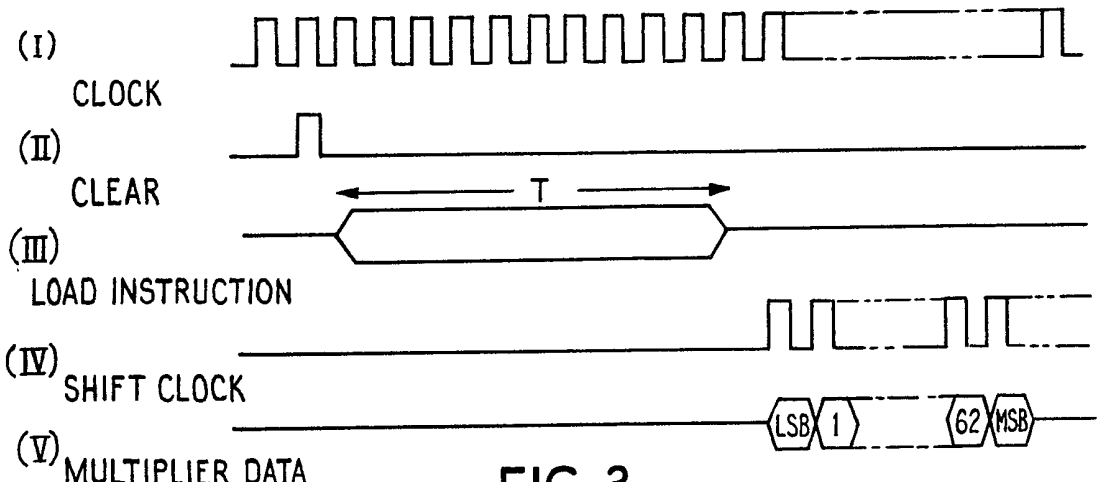


FIG. 3

FIG.4a

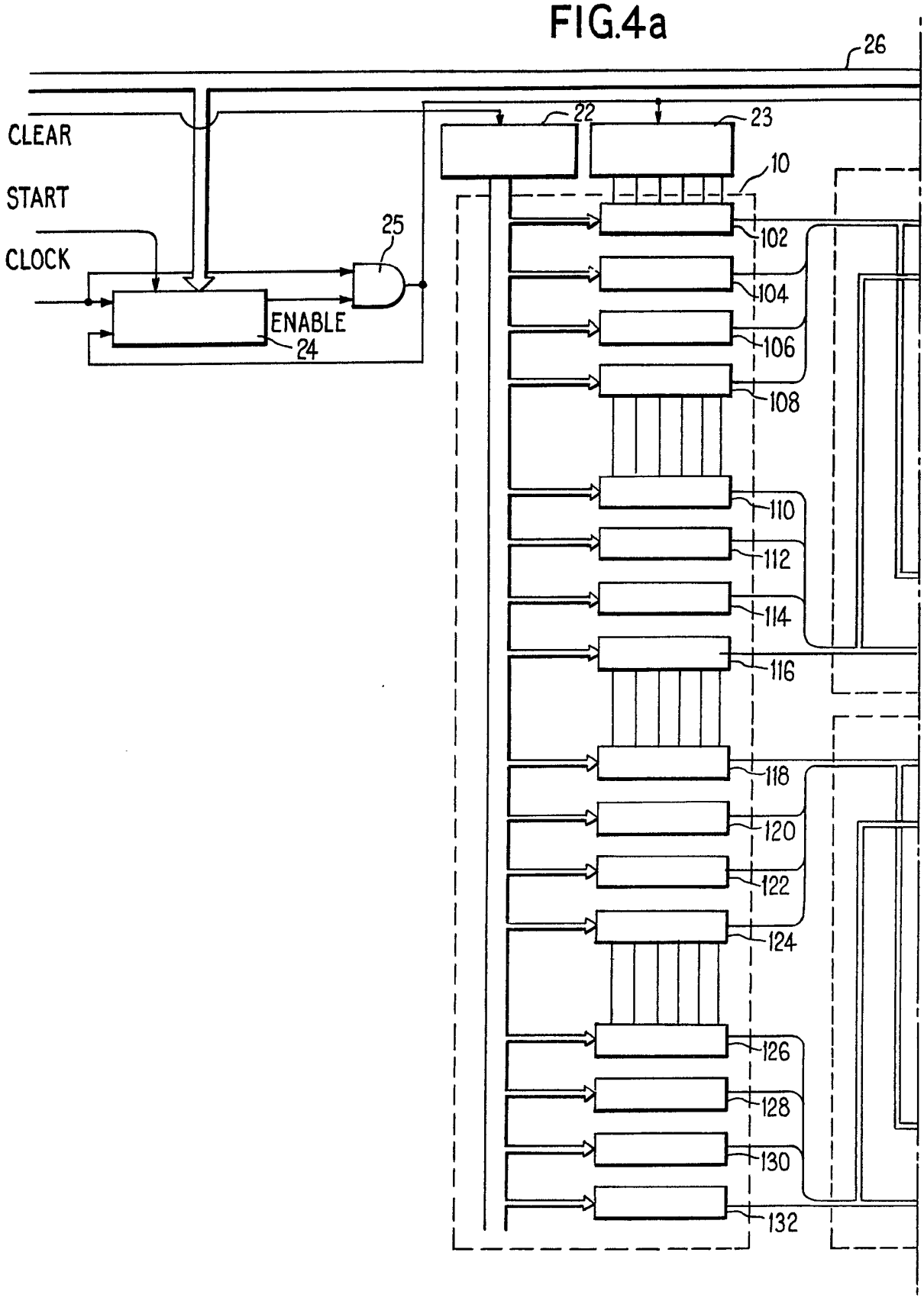
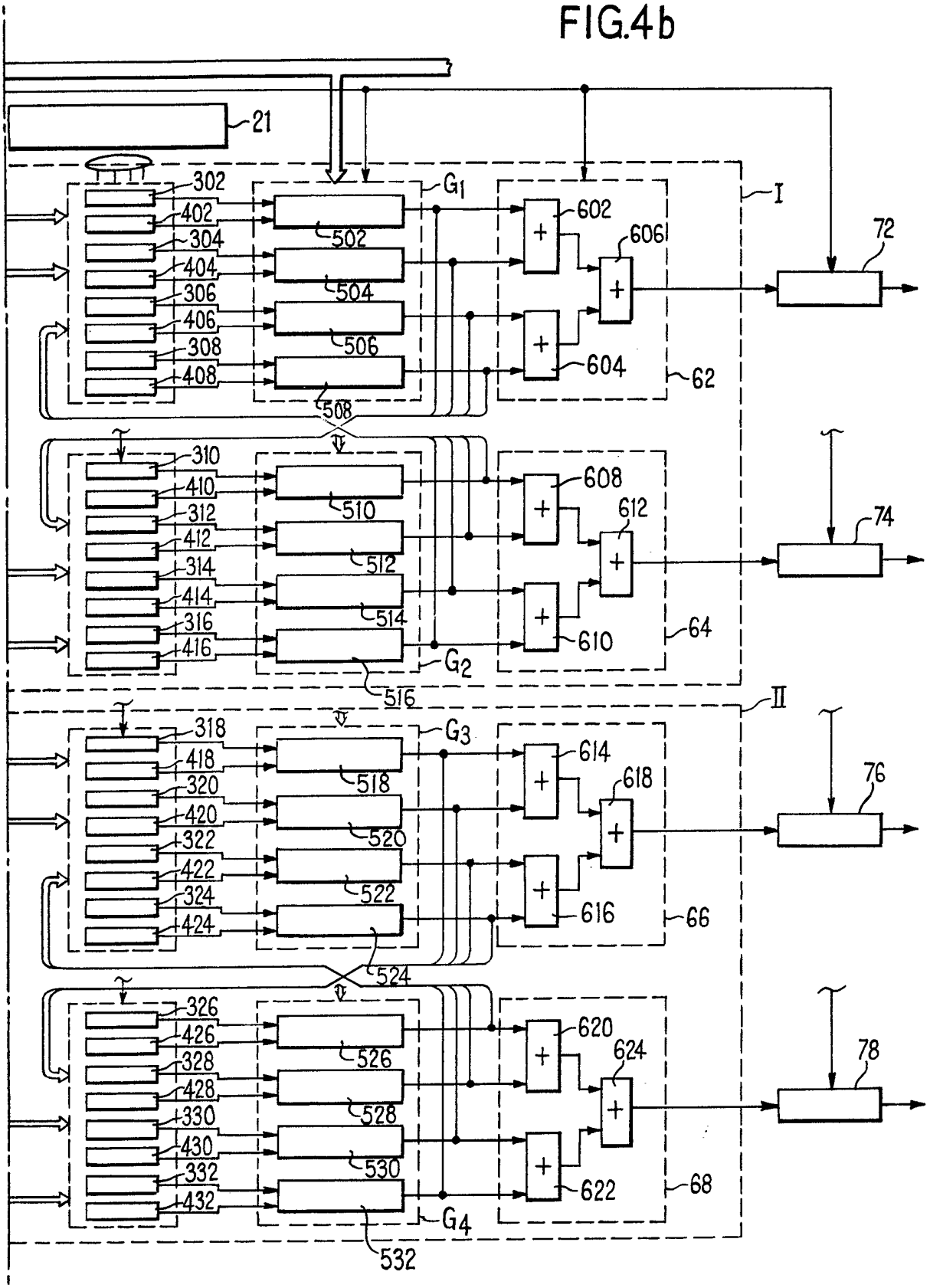

26
CLEAR
START
CLOCK
22
23
10
25
ENABLE
24
102
104
106
108
110
112
114
116
118
120
122
124
126
128
130
132

FIG.4b


21
I
II
G1
G2
G3
G4
62
64
66
68
72
74
76
78
302
402
304
404
306
406
308
408
310
410
312
412
314
414
316
416
318
418
320
420
322
422
324
424
326
426
328
428
330
430
332
432
502
504
506
508
510
512
514
516
518
520
522
524
526
528
530
532
602
604
606
608
610
612
614
616
618
620
622
624

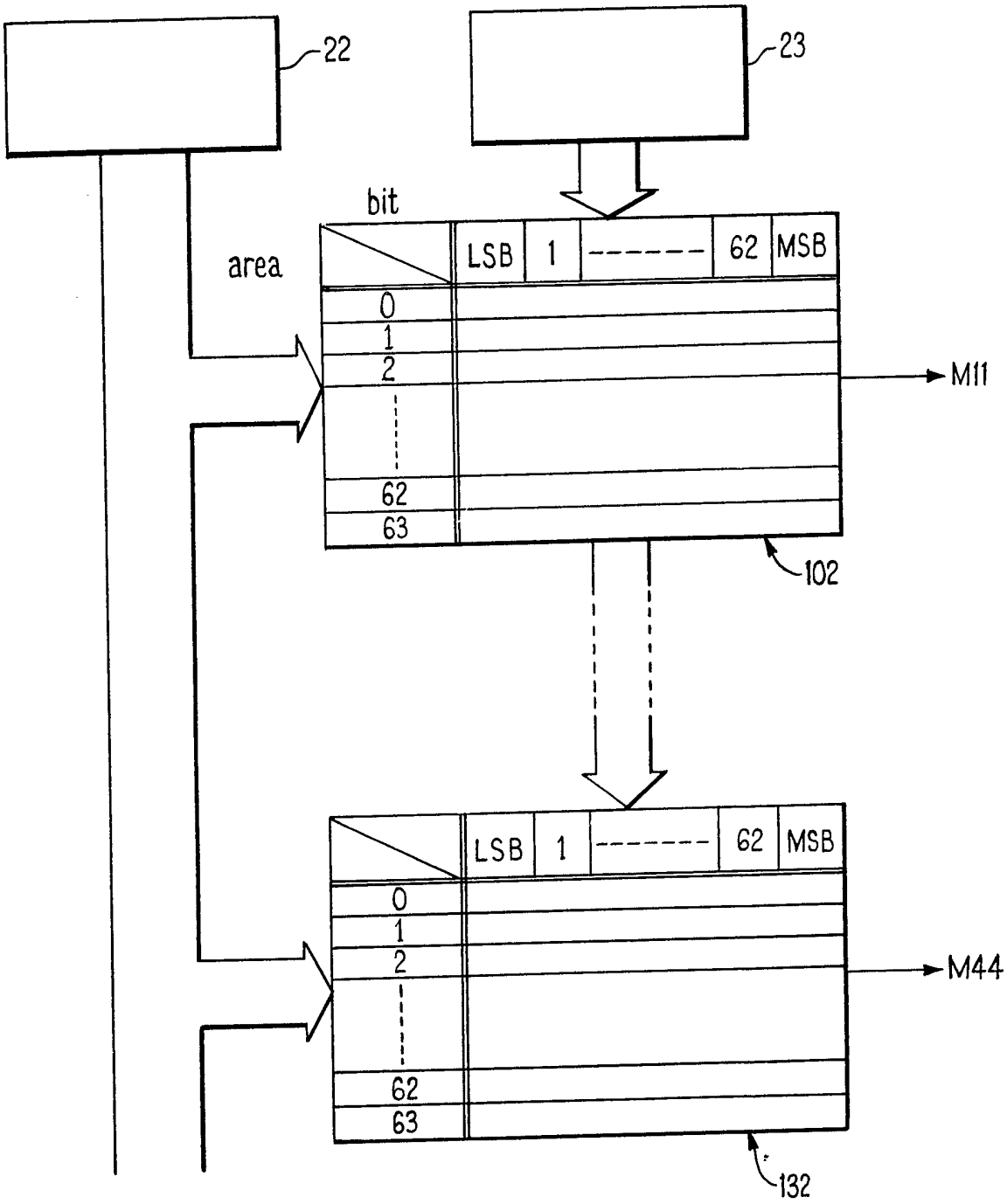

22
23
bit
area
LSB
1
62
MSB
0
1
2
62
63
M11
102
LSB
1
62
MSB
0
1
2
62
63
M44
132

FIG.5

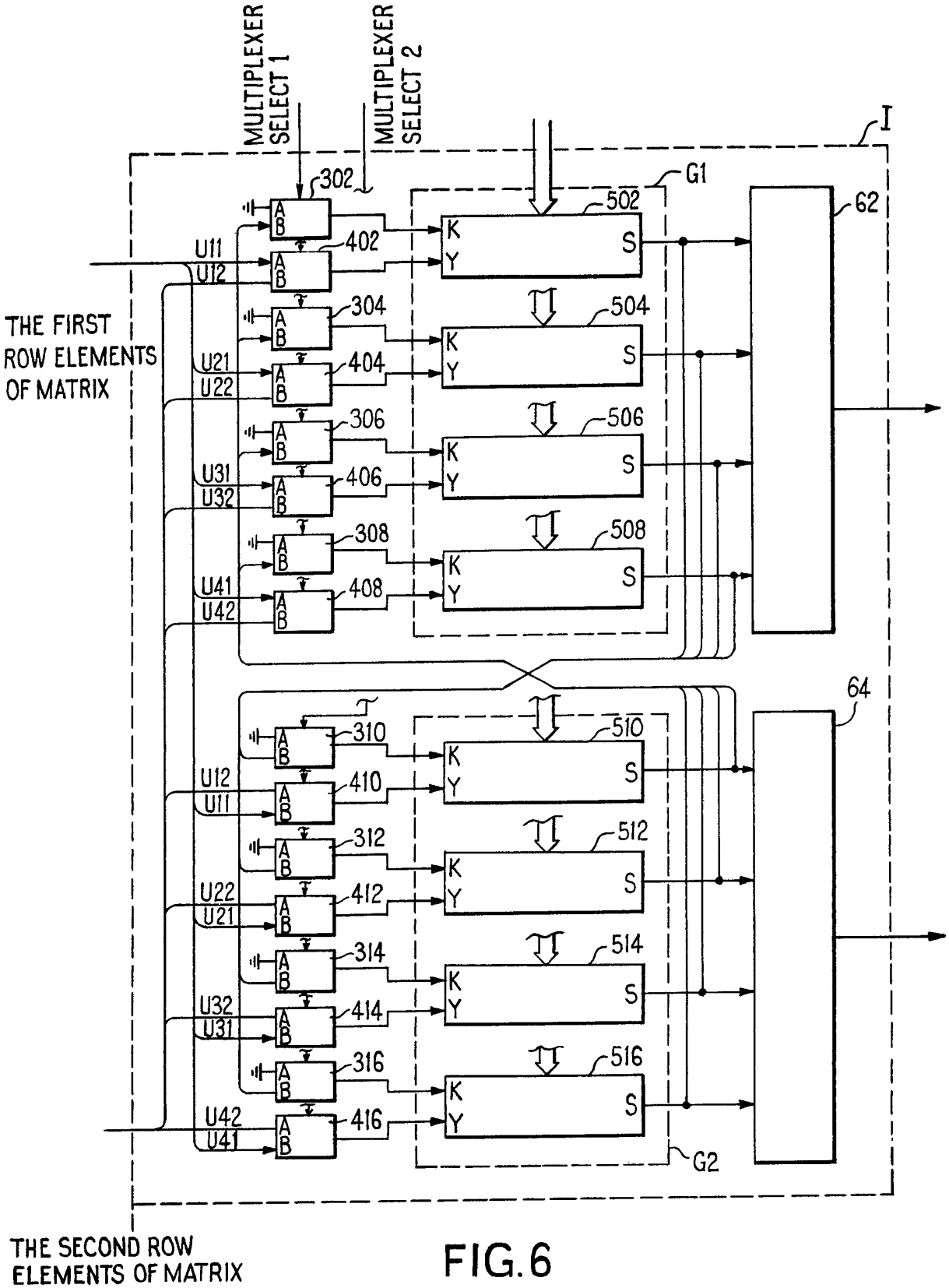

MULTIPLEXER SELECT 1
MULTIPLEXER SELECT 2
I
G1
G2
62
64
302
402
304
404
306
406
308
408
310
410
312
412
314
414
316
416
502
504
506
508
510
512
514
516
U11
U12
U21
U22
U31
U32
U41
U42
K
Y
S
A
B
THE FIRST ROW ELEMENTS OF MATRIX
THE SECOND ROW ELEMENTS OF MATRIX

FIG.6

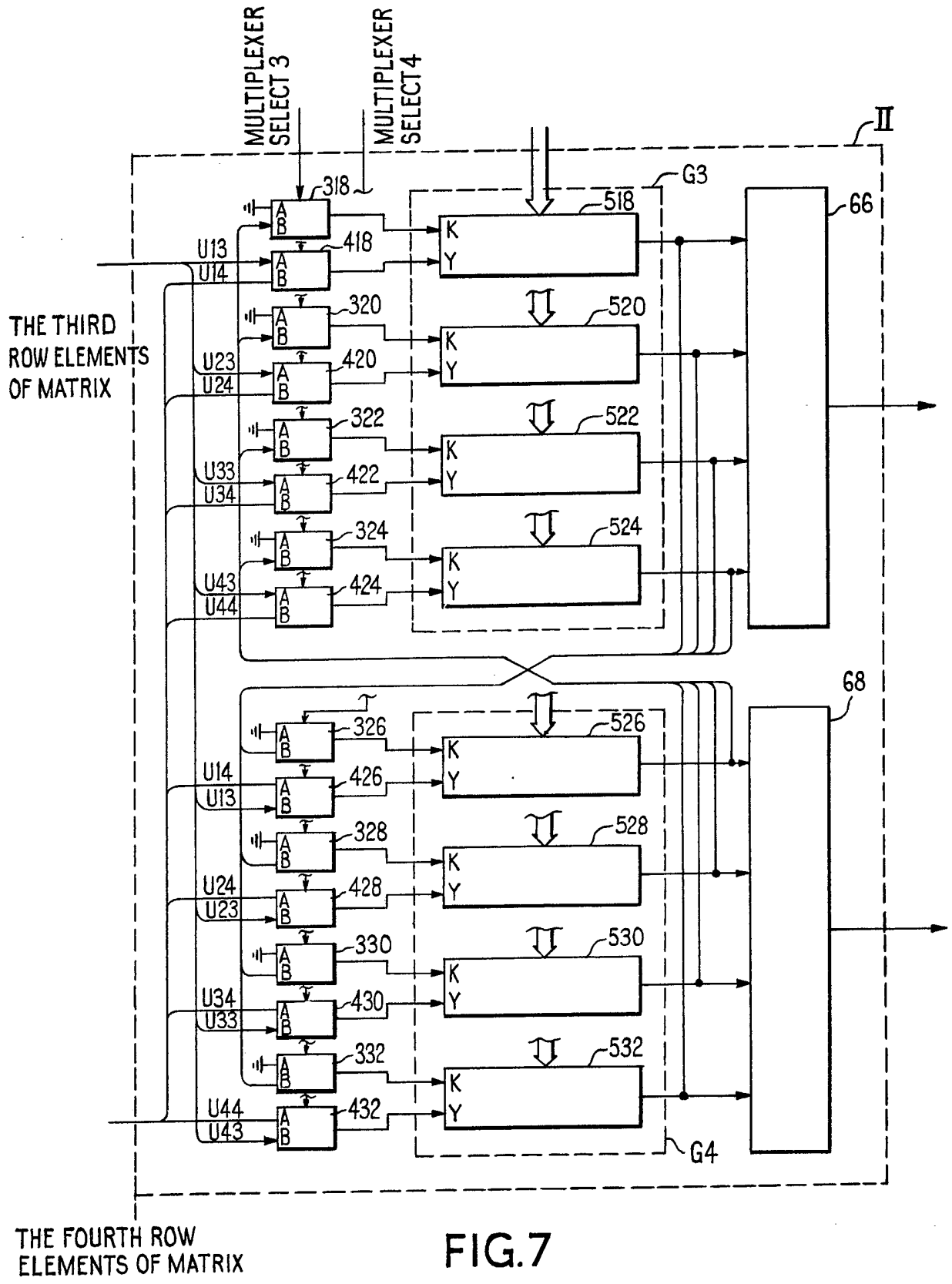

MULTIPLEXER SELECT 3
MULTIPLEXER SELECT 4
II
G3
G4
66
68
THE THIRD ROW ELEMENTS OF MATRIX
THE FOURTH ROW ELEMENTS OF MATRIX
U13
U14
U23
U24
U33
U34
U43
U44
318
418
320
420
322
422
324
424
326
426
328
428
330
430
332
432
518
520
522
524
526
528
530
532
A
B
K
Y

FIG.7

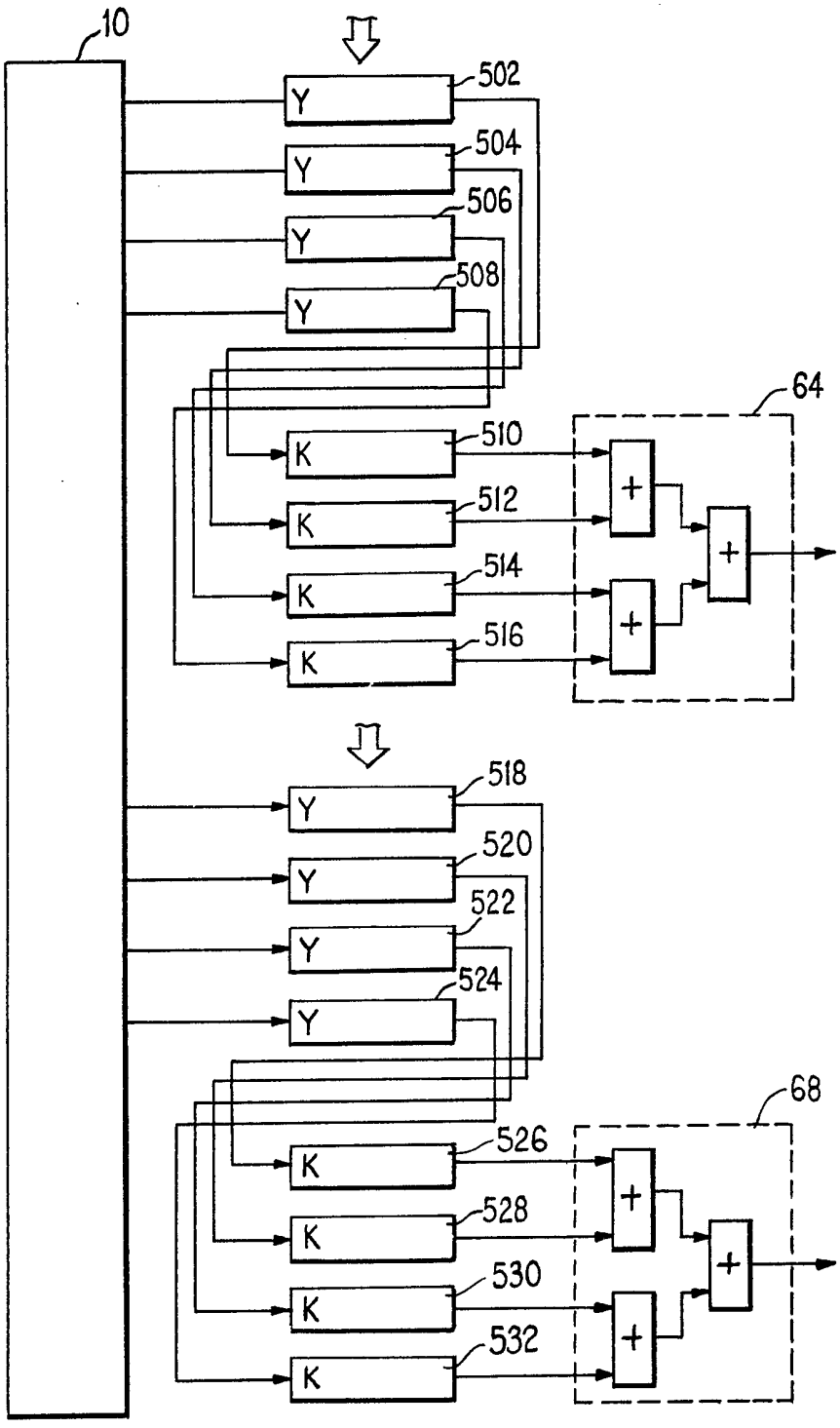

10
Y
502
Y
504
Y
506
Y
508
64
K
510
K
512
K
514
K
516
+
+
+
Y
518
Y
520
Y
522
Y
524
68
K
526
K
528
K
530
K
532
+
+
+

FIG.8

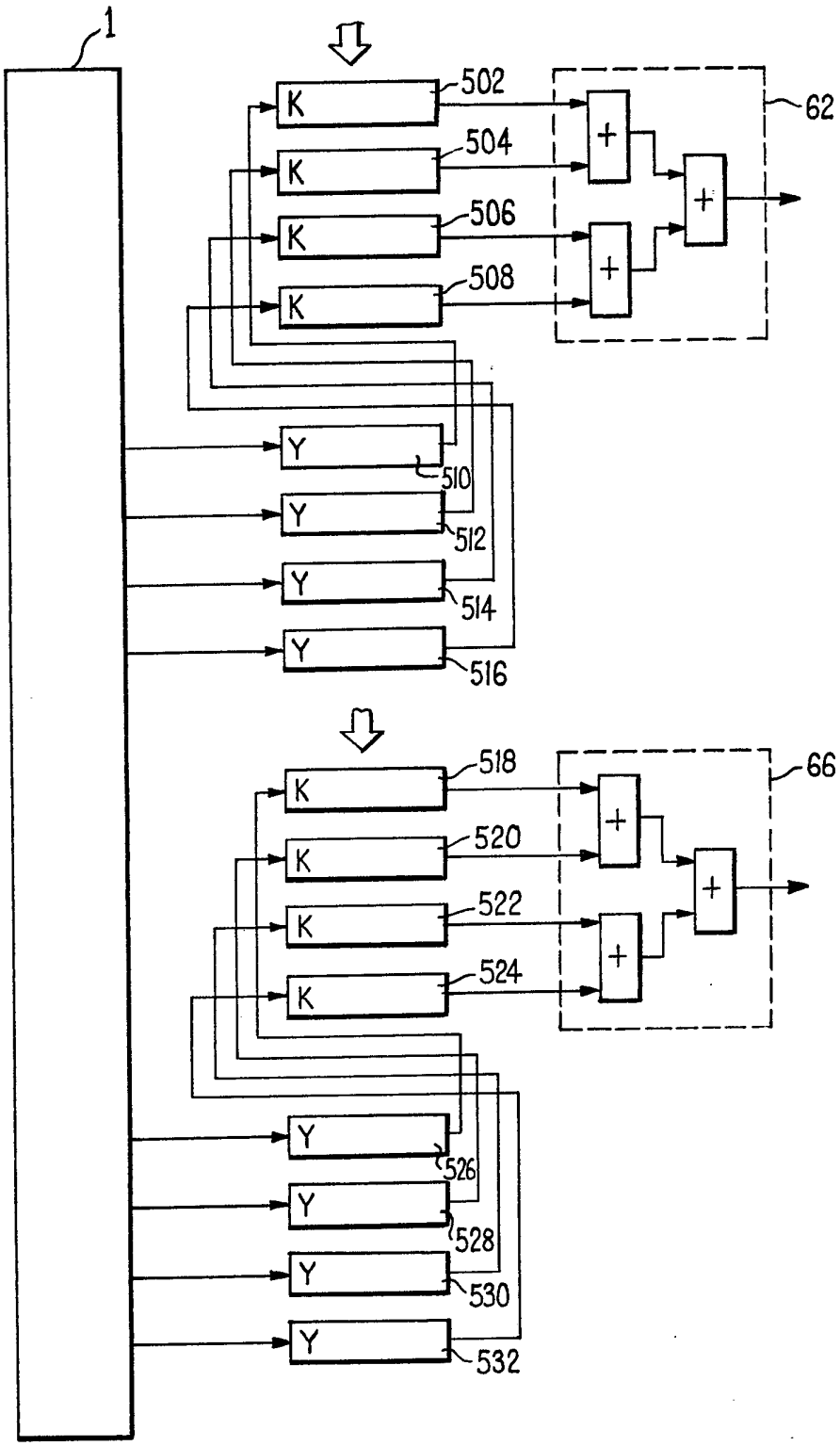

1
K
502
K
504
K
506
K
508
62
+
+
+
Y
510
Y
512
Y
514
Y
516
K
518
K
520
K
522
K
524
66
+
+
+
Y
526
Y
528
Y
530
Y
532

FIG.9

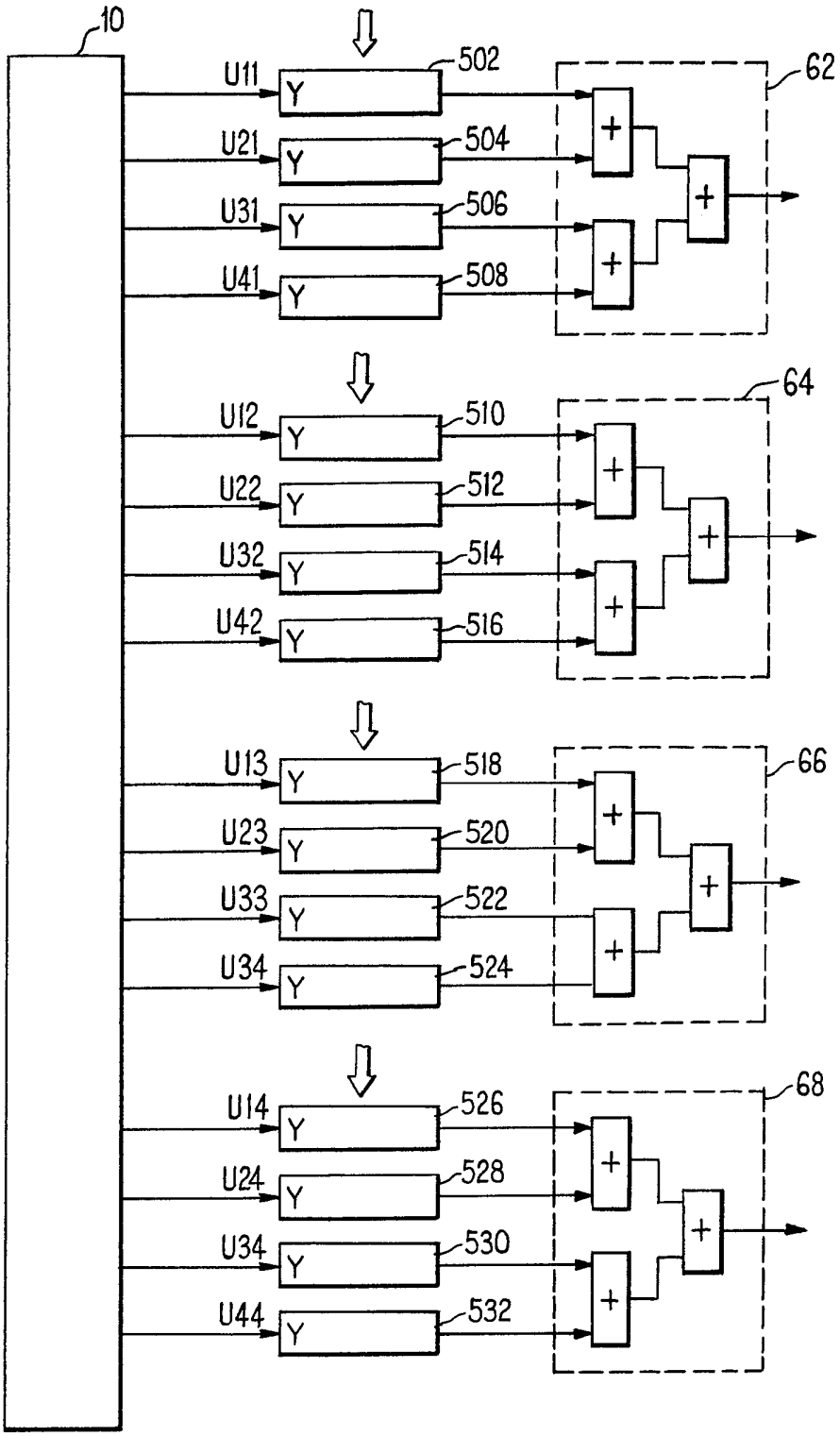

10
U11
U21
U31
U41
U12
U22
U32
U42
U13
U23
U33
U34
U14
U24
U34
U44
Y
502
504
506
508
510
512
514
516
518
520
522
524
526
528
530
532
62
64
66
68
+

FIG. 10

FIG. 11

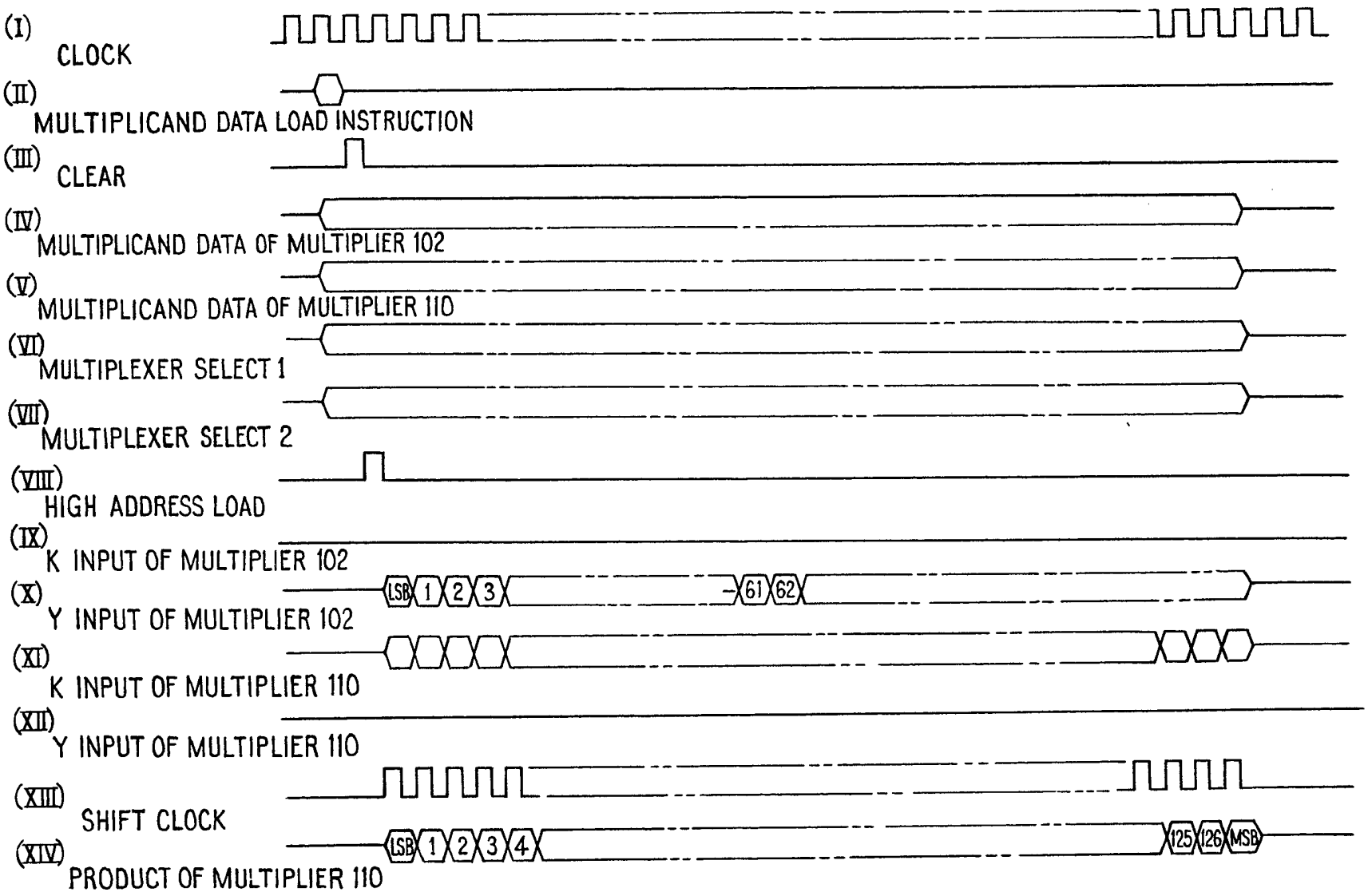
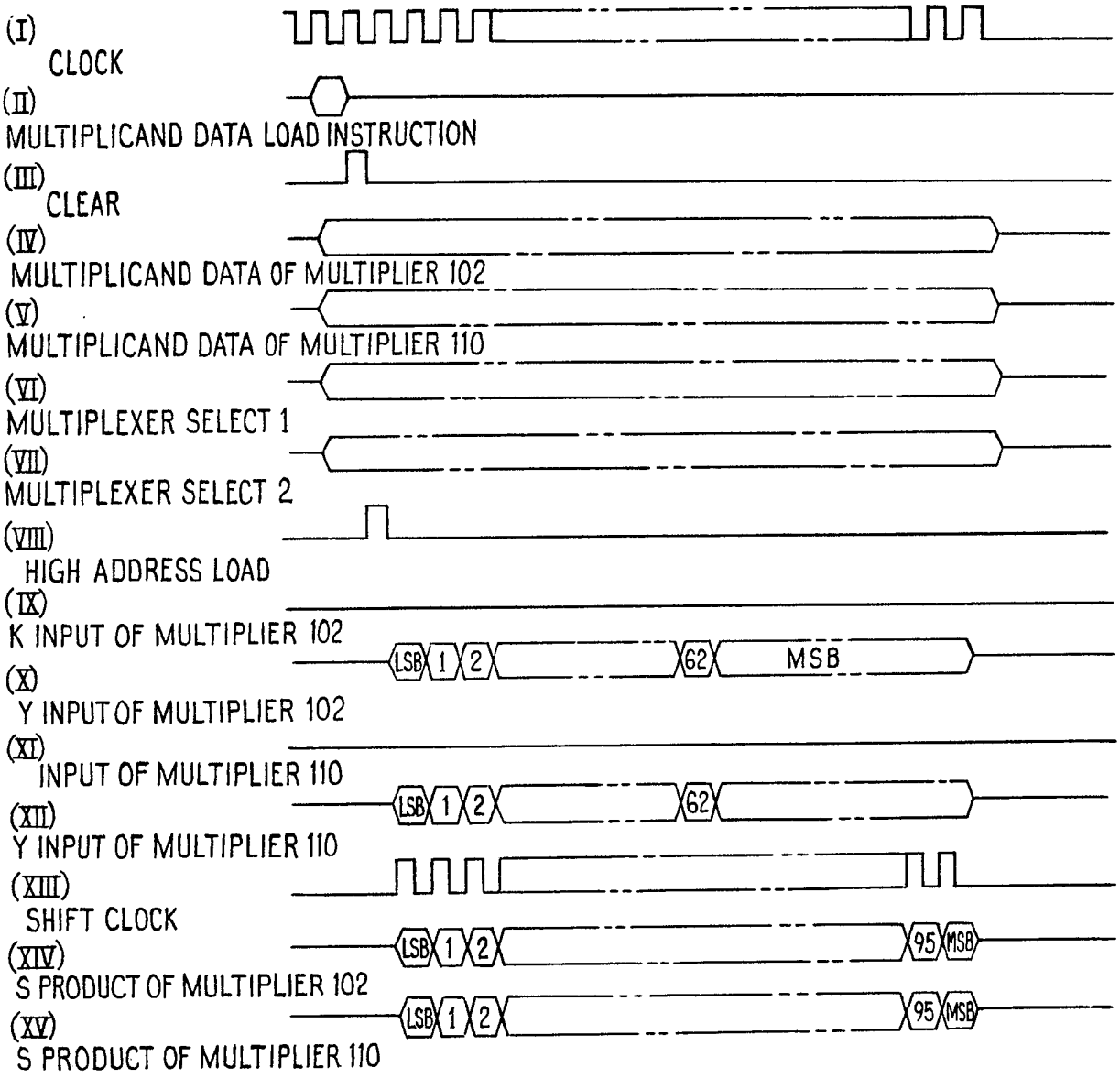

(I)
CLOCK
(II)
MULTIPLICAND DATA LOAD INSTRUCTION
(III)
CLEAR
(IV)
MULTIPLICAND DATA OF MULTIPLIER 102
(V)
MULTIPLICAND DATA OF MULTIPLIER 110
(VI)
MULTIPLEXER SELECT 1
(VII)
MULTIPLEXER SELECT 2
(VIII)
HIGH ADDRESS LOAD
(IX)
K INPUT OF MULTIPLIER 102
(X)
Y INPUT OF MULTIPLIER 102
LSB
1
2
3
61
62
(XI)
K INPUT OF MULTIPLIER 110
(XII)
Y INPUT OF MULTIPLIER 110
(XIII)
SHIFT CLOCK
(XIV)
PRODUCT OF MULTIPLIER 110
LSB
1
2
3
4
125
126
MSB

FIG. 12


(I)
CLOCK
(II)
MULTIPLICAND DATA LOAD INSTRUCTION
(III)
CLEAR
(IV)
MULTIPLICAND DATA OF MULTIPLIER 102
(V)
MULTIPLICAND DATA OF MULTIPLIER 110
(VI)
MULTIPLEXER SELECT 1
(VII)
MULTIPLEXER SELECT 2
(VIII)
HIGH ADDRESS LOAD
(IX)
K INPUT OF MULTIPLIER 102
LSB
1
2
62
MSB
(X)
Y INPUT OF MULTIPLIER 102
(XI)
INPUT OF MULTIPLIER 110
LSB
1
2
62
(XII)
Y INPUT OF MULTIPLIER 110
(XIII)
SHIFT CLOCK
LSB
1
2
95
MSB
(XIV)
S PRODUCT OF MULTIPLIER 102
LSB
1
2
95
MSB
(XV)
S PRODUCT OF MULTIPLIER 110

SPECIFICATION

Matrix multiplication apparatus for graphic display

This invention relates to matrix multiplication apparatus for graphic displays.

The present invention seeks to provide a matrix multiplication apparatus which can reduce the time taken to read data from a matrices elements memory, can form a serial multiplicator in accordance with the data length of a multiplicand, and can multiply a transformation matrix by coordinate data at high speed.

Although the present invention is primarily directed to any novel integer or step, or combination of integers or steps, herein disclosed and/or as shown in the accompanying drawings, nevertheless, according to one aspect of the present invention to which, however, the invention is in no way restricted, there is provided a matrix multiplication apparatus for graphic display which transforms line segment into a dot pattern and displays the corresponding picture, the apparatus comprising: matrix storing means capable of reading out directly and serially elements of matrices acting as multipliers; and multiplication means capable of changing the number of bits input thereto, in accordance with the data length of a multiplicand, and of multiplying said multiplier from said matrix storing means.

Preferably said matrix storing means comprises random access memories provided with a number of blocks corresponding to the number of elements of a matrix, in which each block is divided into at least one area, and which has a memory capacity such that one area can store the elements of a matrix, and which has high address terminals for designating said areas and low address terminals for reading out said matrix elements stored in said area in bit units starting from the least significant bit, high address setting means connected to said high address terminals, and low address setting means connected to said low address terminals.

Preferably said multiplication means comprises one set of multiplicators consisting of two groups, each group in turn consisting of a plurality of serial multiplicators each of a number of bits greater than the shortest data length of said multiplicand, and each being equipped with a direct-connection terminal and a cascade terminal, first change-over means for connecting two serial multiplicators of different groups in a cascade connection to form a pair, or for enabling said serial multiplicators of said pair to operate independently of each other, second change-over means for changing over multipliers input from matrix terminals to the direct-connection terminal of each multiplicator, and addition means for adding the results of multiplications within said groups and output one matrix element.

Said first change-over means may have two input terminals and one output terminal, one of said input terminals being grounded with the other connected to the other of said serial multiplicators forming said pair, and said output terminal is connected to the cascade terminal of each multiplicator.

Said second change-over means may have two input terminals and one output terminal, one of said input terminals being connected to an odd-numbered row element output terminal of said matrix storing means with the other being connected to an even-numbered row element output terminal thereof, and said output terminal is connected to the direct-connection terminal of each multiplicator.

The invention is illustrated, merely by way of example, in the accompanying drawings, in which:-

Figure 1 is a block diagram of a graphic display;

Figure 2 is a schematic view explaining the transformation of a figure in a graphic display;

Figure 3 is a timing chart illustrating the operation of a conventional matrix multiplication apparatus using a stack memory as a matrices elements memory;

Figure 4 is a block diagram of one embodiment of a matrix multiplication apparatus according to the present invention for a graphic display;

Figure 5 is a diagram of the construction of a memory of the matrix multiplication apparatus of Figure 4;

Figures 6 and *7* are block circuit diagrams of details of the matrix multiplication apparatus of Figure 4;

Figures 8 and *9* are schematic illustrations of how multiplication circuit groups are connected when conversion matrices are being multiplied together in the matrix multiplication apparatus of Figure 4;

Figure 10 is a schematic illustration of how the multiplication circuit groups are connected when coordinate data and a transformation matrix are being multiplied together in the matrix multiplication apparatus of Figure 4;

Figure 11 is a timing chart illustrating the operation of the matrix multiplication apparatus of Figure 4 when transformation matrices are being multiplied together; and

Figure 12 is a timing chart illustrating the operation of the matrix multiplication apparatus of Figure 4 when a conversion matrix is being multiplied by coordinate data.

A graphic display is shown in Figure 1 and has a matrix multiplication circuit 3 which calculates line segments transferred thereto from a host computer 1 in accordance with the instructions from an input device 2 such as a keyboard, so as to execute enlargement, reduction, rotation, perspective viewing or translating of a figure. A clipping circuit 4 then determines whether or not the figure after the transformation then remains within a window, the line segment is transformed into coordinate values on display screen coordinates by a window viewport transformation, a line generation circuit 5 generates pixels interpolating between line segments, an image memory 6 temporarily stores dot data, and a display is thereafter produced on a cathode ray tube (CRT) 7.

In order to transform a figure K1 to a figure K2, as shown in Figure 2, a rotational movement and a

translation movement must be carried out. For this reason, the matrix multiplication circuit 3 executes a multiplication of a rotational transformation matrix R for rotational movement, a translation transformation matrix P for translation, and a coordinate data L, that is, an affine transformation according to the following formula, for each of the line segments V_0, V_1, V_2 of the figure K1:

$$L.P.R.=(Xi,Yi,Zi,1)\cdot \begin{matrix} P_{11} & P_{12} & P_{13} & P_{14} \\ P_{21} & P_{22} & P_{23} & P_{24} \\ P_{31} & P_{32} & P_{33} & P_{34} \\ P_{41} & P_{42} & P_{43} & P_{44} \end{matrix} \begin{matrix} R_{11} & R_{12} & R_{13} & R_{14} \\ R_{21} & R_{22} & R_{23} & R_{24} \\ R_{31} & R_{32} & R_{33} & R_{34} \\ R_{41} & R_{42} & R_{43} & R_{44} \end{matrix}$$

This calculation is done in the following way. First, a multiplication of the translation transformation matrix P as the multiplicand by the rotational transformation matrix R is performed to obtain a transformation matrix W, and then all the line segments of the figure are multiplied by the transformation matrix W, using the coordinate matrix (x_i, y_i, z_i, 1) as the multiplicand.

This matrix multiplication is done conventionally as follows. A transformation matrix U necessary for the calculation is temporarily called in a parallel system to a shift register from a stack memory in which are stored element matrices, by a load instruction (III), Figure 3, and while the data is converted into serial data by shift clocks, it is applied to a multiplicator as a multiplier (V) and is then multiplied serially by the multiplicand that is input previously.

Although a stack memory is an extremely convenient memory for calculation processing in which the data stored therein must be frequently updated, it has the problem for serial multiplication that the multipliers are first called by a load instruction before the start of the calculation and are applied bit-by-bit to the multiplicator by the shift clocks, so that an excessive period of time is needed for the execution of the load instruction, and the calculation time for one multiplication is very long.

The coordinate data L usually consists of 32 bits, but the transformation matrices, such as the rotational transformation matrix R or the translation transformation matrix P, have a long data length of 64 bits in order to provide an improved calculation accuracy.

Conventionally, the multiplication of transformation matrices with each other and the multiplication of a transformation matrix by coordinate data are carried out using a serial multiplicator of a 64-bit construction. When the transformation matrix W is multiplied by the coordinate data, therefore, 32 zeros are added to the high-order bits of the coordinate data so as to make it match the data length of the transformation matrix acting as the multiplier, and the multiplication is effected between data each of 64 bits.

Accordingly, 64 + 64 = 128 shift clocks are required for a single calculation, although the multiplication is actually done between data of an effective length of 32 bits and data of an effective length of 64 bits and the total length of data actually handled is only 96 bits. In other words, as many as 32 bits of excess clocks are necessary, and time is wasted during the period of the calculation with the transformation matrix W and the coordinate data that occupies the major proportion of the calculation time in a graphic display.

Referring now to Figure 4 there is shown one embodiment of a matrix multiplication apparatus according to the present invention having a matrices elements memory 10 which is constructed of random access memories (hereinafter referred to "RAMs") 102 - 132 forming 16 blocks and storing matrix elements U11 - U44. Each RAM is divided into 64 areas each consisting of 64 bits, as shown in Figure 5, and the *n*th area of each RAM stores a corresponding matrix element (Uij) of one transformation matrix, so that 64 different matrices can be read therefrom.

The output terminals of the RAMs 102 - 132 of the matrices elements memory 10 are connected to multiplier input terminals of serial multiplicators 502 - 532 by second multiplexers 402 - 432 that are controlled by a multiplexer control circuit 21. The address terminals of each RAM are divided into high address terminals A11 ... A6 for selecting the *n*th area and low address terminals A5 ... A0 for reading out the element data $(Uij)_n$ stored in that area. The high address terminals A11 ... A6 of each RAM are connected in common to the output terminal of a high address counter 22, while the low address terminals A5 ... A0 are connected in common to a low address counter 23, so that the *n*th area can be specified by a high address and thereafter the low addresses are sequentially designated from the least significant address so that the matrix can be read out in bit units.

A shift counter 24 is connected to a clock signal source, and AND gate 25 and a data bus 26, and is constituted so that when shift number signals are input thereto from the data bus after the reception of a start signal, it outputs an enable signal until a predetermined number of clock signals have been inputted to the low address counter 23. The AND gate 25 continues to output the shift clocks to the low address counter 23, the serial multiplicators 502 - 532 and addition circuits 62 - 68 only during the period in which the shift counter 24 outputs the enable signal.

Multiplication is effected by two multiplication circuit groups I and II, each multiplication circuit group being further divided into two groups G1 and G2, G3 and G4 respectively. The multiplication circuit groups also contain first multiplexers 302 - 332 that are controlled by signals from the multiplexer control circuit 21, the serial multiplicators 502 - 532 that can be connected in cascade connections by corresponding first

multiplexers or can be used independently of one another, the addition circuits 62 - 68 that add outputs from these multiplicators, and the second multiplexers 402 - 432.

As shown in Figures 6 and 7, the multiplication circuit groups I and II have serial multiplicators 502 - 516, 518 - 532, respectively, that can multiply 32-bit data in a serial form. Each multiplicator has a cascade terminal K, a direct-connection terminal Y, and a serial output terminal S. The cascade terminals K are connected to the corresponding first multiplexers 302 - 332 which each have two input terminals A and B, a selection signal input terminal and an output terminal. The direct-connection terminals Y are connected to the corresponding second multiplexers 402 - 432 which each have two input terminals, a selection signal input terminal and an output terminal.

One of the input terminals A of each of the first multiplexers 302 - 332 is grounded and the other input terminal B is connected to the output terminal of a multiplicator of the other group so as to form pairs of multiplicators 502 and 510, 504 and 512, 506 and 514, 508 and 516, 518 and 526, 520 and 528, 522 and 530, and 524 and 532. Thus, the multiplicators can be selectively connected so that when they are placed in this cascade connection, they can handle 64-bit multiplicands. In the first multiplication circuit group I, the input terminal A of each of the second multiplexers 402 – 432 is connected to an output terminal of the first row of the matrices elements memory 10, and its input terminal B is connected to an output terminal of the second row thereof, so that each element U11 ... U41 and U12 ... U42 of the first and second rows of the matrices elements memory 10 can be input thereto. In the second multiplication circuit group II, the input terminals A are connected to an output terminal of the third row of the matrices elements memory 10, and the input terminals B are connected to an output terminal of the fourth row, so that each element of the third and fourth rows U13 ... U43 and U14 ... U44 can be input thereto. According to this arrangement, matrix elements of either row can be selected for each multiplication circuit for the multiplication of transformation matrices (Figures 8 and 9), and the transformation matrix elements corresponding to each multiplicator can be selectively output for the multplication of coordinate data by a transformation matrix (Figure 10).

The addition circuits 62 - 68 each consist of two adders 602 and 604, 608 and 610, 614 and 616, 620 and 622, respectively, that are connected to two of these multiplicators to obtain a sum of the outputs thereof, and third adders 606, 612, 618, 624 which obtain a sum of the outputs of these pairs of adders. The addition circuit 62 - 68 each output one of the elements of the matrix obtained by the calculation to corresponding buffer registers 72 - 78 connected thereto.

The operation of the matrix multiplication apparatus of Figure 4 will now be described with reference to the timing charts of Figures 11 and 12.

This example of the operation concerns the case in which line segments input from a host computer, such as the triangular figure K1 of Figure 2, is transformed and moved to figure K2 by instructions from the keyboard.

In this example, a multiplication of the translation transformation matrix P by the rotational transformation matrix R must be done first, as described above, to obtain the transformation matrix W.

First of all, the multiplexer control circuit 21 selects terminals A of the first multiplexers 302 - 308 of the first group G1 of the multiplication circuit group I, and terminals B of the first and second multiplexers 310 - 316 and 410 - 416 of the second group G2 thereof. Similarly, it selects terminals A of the first and second multiplexers 318 - 324 and 418 - 424 of the first group G3 of the second multiplication circuit group II and terminals B of the first and second multiplexers 326 - 332 and 426 - 432 of the second group G4 thereof. As a result, the multiplicators of each group are connected to the corresponding multiplicators of the other group in a cascade arrangement, that is, the multiplicator 502 is connected to the multiplicator 510, the multiplicator 504 is connected to the multiplicator 512, the multiplicator 506 is connected to the multiplicator 514 and the multiplicator 508 is connected to the multiplicator 516 in the multiplication circuit group I and the multiplicator 518 is connected to the multiplicator 526, the multiplicator 520 is connected to the multiplicator 528, the multiplicator 522 is connected to the multiplicator 530 and the multiplicator 524 is connected to the multiplicator 532 in the multiplication circuit group II, thereby forming multiplicators of a 64-bit construction. Thus, 64-bit data can be input as a multiplicand.

After this preparation is completed, the translation transformation matrix acting as the multiplicand is input to the multiplication circuit groups I and II from the data bus 26. Accordingly, as shown in Figure 8, the pairs of multiplicators in the multiplication group I receive the elements of the first column of the translation transformation matrix P, that is, the multiplicators 502 and 510 receive element P_{11} of column 1, row 1, the multiplicators 504 and 512 receive element P_{12} of the column 1, row 2, the multiplicators 506 and 514 receive element P_{13} of column 1, row 3, and the multiplicators 508 and 516 receive element P_{14} of column 1, row 4. The pairs of multiplicators in the multiplication circuit group II similarly receive the elements of the first column of the translation transformation matrix P, that is, the multiplicators 518 and 526 receive element P_{11} of column 1, row 1, the multiplicators 520 and 528 receive element P_{12} of column 1, row 2, the multiplicators 522 and 530 receive element P_{13} of column 1, row 3 and the multiplicators 524 and 532 receive element P_{14} of column 1, row 4. After the input of the multiplicand is thus completed, the area *n* of the matrices elements memory 10 which holds therein the rotational transformation matrix R necessary for moving figure K1 to figure K2 is selected. The high address corresponding to this area is set in the high address counter 22, and at the same time the shift counter 24 outputs shift clocks to the low address counter 25 to read out sequentially the data $(Uij)_n$ in the area n designated by the high address counter 22, at the timing of the shift clocks, starting from the least significant bit LSB.

Accordingly, the multiplicators in the first group G1 of the multiplication circuit group I receive the elements of the first column in synchronism with the shift clocks and start the multiplication, that is, the multiplicator 502 receives and starts a multiplication with element R_{11} of column 1, row 1, the multiplicator 504 does the same with element R_{21} of the column 2, row 1, the multiplicator 506 does the same with element R_{31} of column 3, row 1 and the multiplicator 508 does the same with element R_{41} of column 4, row 1. The multiplicator 510 outputs $R_{11} \times P_{11}$, the multiplicator 512 outputs $R_{12} \times P_{21}$, the multiplicator 514 outputs $R_{13} \times P_{31}$ and the multiplicator 516 outputs $R_{14} \times P_{41}$. The results of these calculations are added by the addition circuit 64 to provide the element $R_{11} \cdot P_{11} + R_{12} \cdot P_{21} + R_{13} \cdot P_{31} + R_{14} \cdot P_{41}$. At the same time, the multiplication circuit group II receives the elements of the third column, that is, the multiplicator 518 receives R_{13}, the multiplicator 520 receives R_{23}, the multiplicator 522 receives R_{33}, and the multiplicator 524 receives R_{43}, starting from the least significant bit, and the results of the calculations therewith are output from the multiplicators 526 - 532. These results are added by the addition circuit 68 to provide the element of column 1, row 3, i.e. $R_{11} \cdot P_{13} + R_{12} \cdot P_{23} + R_{13} \cdot R_{33} + R_{14} \cdot P_{43}$. The elements W_{11} and W_{13} thus calculated are input to shift registers 74,78 connected to the corresponding addition circuits 64,68 and after they are digitially processed, they are ordered in a predetermined bit length, e.g. 64 bits, and are stored in an empty area of the matrices elements memory 10. In the same way, similar calculations are carried out four times with different column elements of the translating transformation matrix acting as the multiplicands, to obtain the transformation matrix elements W_{21}, W_{23}, W_{31}, W_{33}, W_{41}, and W_{43}.

When the calculation of this transformation matrix is completed, the multiplexer control circuit 21 changes over the second multiplexers 402 - 432 and the multiplication circuit group I repeats this calculation process four times using the second row of the rotational transformation matrix R as the multiplier and replacing the column elements of the translation transformation matrix. Similarly, the multiplication circuit group II repeats the calculation process four times using the elements of the fourth line of the rotational transformation matrix as the multiplier. Thus, the elements W_{12}, W_{14}, W_{22}, W_{24}, W_{32}, W_{34}, W_{42}, and W_{44} of the transformation matrix W are calculated.

When all the transformation matrix W is stored in the matrices elements memory 10, the multiplexer control circuit 21 selects all the terminals A of the first and second multiplexers 302 - 332 and 402 - 432 and grounds the cascade terminals K of the multiplicators to form independent 32-bit multiplicators, as shown in Figure 10. The serial input terminal Y of each multiplicator is connected to the output terminal of the matrices elements memory 10 so that the multiplicators 502 - 508 of the first group of the multiplication circuit group I can be connected to elements W_{11} - W_{14} of the first column of the transformation matrix W, the multiplicators of the second group to elements W_{21} - W_{24} of the second column, and the multiplicators of groups G3 and G4 of the multiplication circuit group II to elements W_{31} - W_{34} and W_{41} - W_{44} of the third and fourth columns, respectively, as shown in Figure 10.

After this preparation is completed, the x-coordinate data is input to first multiplicators 502, 510, 518, 526 in each group, the y-coordinate data to second multiplicators 504, 512, 520, 528, the z-coordinate data to third multiplicators 506, 514, 522, 530, and 1 to fourth multiplicators 508, 516, 524, 532. Under this state, the high address of the area holding the transformation matrix W determined in the procedure described above is set in the high address counter 22, and the shift clocks are input to the low address counter 23, so that the multiplicators 502 - 532 receive the elements of the transformation matrix W, that is, the multiplicator 502 receives the element of column 1, row 1 of the transformation matrix, the multiplicator 504 receives the element of column 2, row 1, ..., and the multiplicator 532 receives the element of column 4, row 4, starting from the least significant bit, and they execute the multiplication in a serial system. After 96 clocks corresponding to the bit length have thus been applied to the multiplicators the addition circuit 62 outputs the coordinate data x, the addition circuit 64 outputs the coordinate data y, the addition circuit 66 outputs the coordinate data z, and the addition circuit 68 outputs 1, thereby completing the calculation of the data (x_m', y_m', z_m', 1) for one coordinates point V_m. In this manner, the coordinate data for each point V_0, V_1, ... are sequentially input as multiplicands to the multiplicators 502 - 532 in order to execute the multiplication by the transformation matrix W. When a number of shift clocks corresponding to the data length have been input, the result of the multiplication is output, making it possible to perform an affine transformation without wasting any time in the calculation process.

CLAIMS

1. A matrix multiplication apparatus for graphic display which transforms line segment into a dot pattern and displays the corresponding picture, the apparatus comprising: matrix storing means capable of reading out directly and serially elements of matrices acting as multipliers; and multiplication means capable of changing the number of bits input thereto, in accordance with the data length of a multiplicand, and of multiplying said multiplicand by said multiplier from said matrix storing means.

2. A matrix multiplication apparatus as claimed in claim 1 in which said matrix storing means comprises random access memories provided with a number of blocks corresponding to the number of elements of a matrix, in which each block is divided into at least one area, and which has a memory capacity such that one area can store the elements of a matrix, and which has high address terminals for designating said areas and low address terminals for reading out said matrix elements stored in said area in bit units starting from the least significant bit, high address setting means connected to said high address terminals, and low address

setting means connected to said low address terminals.

3. A matrix multiplication apparatus as claimed in claim 1 or 2 in which said multiplication means comprises one set of multiplicators consisting of two groups, each group in turn consisting of a plurality of serial multiplicators each of a number of bits greater than the shortest data length of said multiplicand, and each being equipped with a direct-connection terminal and a cascade terminal, first change-over means for connecting two serial multiplicators of different groups in a cascade connection to form a pair, or for enabling said serial multiplicators of said pair to operate independently of each other, second change-over means for changing over multipliers input from matrix terminals to the direct-connection terminal of each multiplicator, and addition means for adding the results of multiplications within said groups and output one matrix element.

4. A matrix multiplication apparatus as claimed in claim 3 in which said first change-over means has two input terminals and one output terminal, one of said input terminals being grounded with the other connected to the other of said serial multiplicators forming said pair, and said output terminal is connected to the cascade terminal of each multiplicator.

5. A matrix multiplication apparatus as claimed in claim 3 or 4 in which said second change-over means has two input terminals and one output terminal, one of said input terminals being connected to an odd-numbered row element output terminal of said matrix storing means with the other being connected to an even-numbered row element output terminal thereof, and said output terminal is connected to the direct-connection terminal of each multiplicator.

6. A matrix multiplication apparatus substantially as herein described with reference to and as shown in Figures 4 to 12 of the accompanying drawings.

7. Any novel integer or step, or combination of integers or steps, hereinbefore described, irrespective of whether the present claim is within the scope of, or relates to the same or a different invention from that of, the preceding claims.

Printed in the UK for HMSO, D8818935, 10/84, 7102.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.