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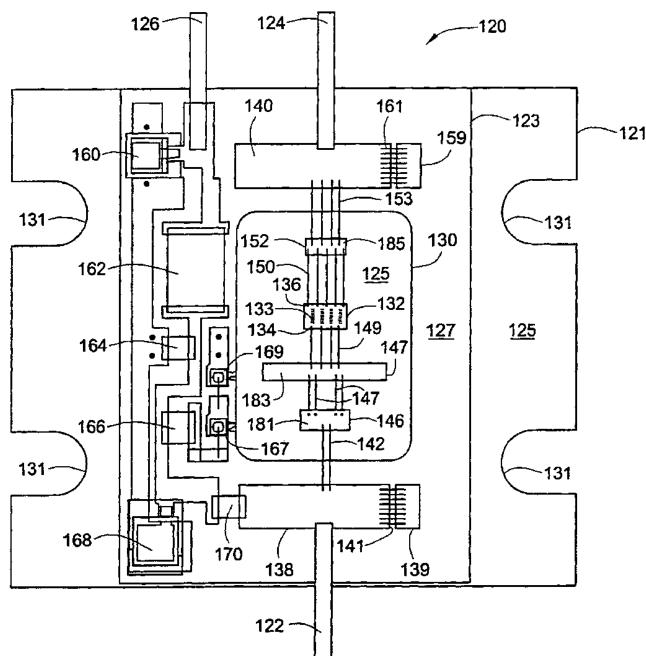
For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: HIGH IMPEDANCE MATCHED RF POWER TRANSISTOR



(57) Abstract: A high frequency LDMOS power transistor device comprises a conductive mounting flange having a dielectric substrate attached thereto, the substrate having a window formed therein, exposing a portion of the mounting flange. A semiconductor die attached to the exposed portion of the mounting flange, the die having a plurality of transistors formed thereon having common electrode input and output terminals. An input lead is attached to the substrate and electrically coupled to the respective electrode input terminals via an input transmission path, the input transmission path including an input impedance matching element disposed on the substrate. An output lead is attached to the substrate and electrically coupled to the respective electrode output terminals via an output transmission path, the output transmission path including an output impedance matching element disposed on the substrate. In a preferred embodiment, the input and output impedance matching elements comprise respective shunt stubs formed on the substrate. DC biasing and temperature compensation circuitry may also be located on the substrate and electrically coupled to the input transmission path.

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SPECIFICATION

HIGH IMPEDANCE MATCHED RF POWER TRANSISTOR

BACKGROUND OF THE INVENTION

5 Field of the Invention

The present invention pertains generally to the field of power transistors and, more particularly, to impedance matching of radio frequency (RF) power transistor devices for use in wireless communication amplifiers.

10 Background

The use of radio frequency (RF) amplifiers in wireless communication networks is well known. With the considerable recent growth in the demand for wireless services, such as personal communication services (PCS), the operating frequency of wireless networks has increased dramatically and is now well into the microwave (i.e., gigahertz)
15 frequencies. At such high frequencies, laterally diffused metal oxide semiconductor ("LDMOS") transistors are preferred over bi-polar transistors for RF power amplification devices for use in antenna base stations.

In a typical deployment, an LDMOS RF power transistor device comprises a plurality of electrodes formed on a silicon die, each electrode comprising a plurality of
20 interdigitated transistors. The individual transistors of each electrode are connected to respective common input (gate) and output (drain) terminals, with the underside of the die comprising a source terminal. The die is attached, e.g., by a known eutectic die attach process, to a metal flange serving as both a heat sink and a common ground (source) reference. Respective input (gate) and output (drain) lead frames are attached to the sides
25 of the flange, electrically isolated from the metal flange, wherein the input and output lead frames are coupled by multiple wires to the respective input and output electrode terminals on the silicon die.

By way of illustration, FIG. 1 shows a simplified circuit schematic of an (unmatched) LDMOS device, having an input (gate) lead 12, an output (drain) lead 14 and
30 a source 16 through an underlying substrate. Transmission inductance through the input path, e.g., a plurality of bond wires connecting the input lead 12 to the common input

terminal of the respective transistor fingers, is represented by inductance 18. Output inductance through the output path, e.g., a plurality of bond wires connecting the common output terminal of the respective transistors to the output lead 14, is represented by inductance 20.

5 Consistent output performance of such high frequency RF power transistors in base station amplifier circuits is traditionally problematic due to natural variables that each device possesses. In particular, RF power transistor devices have natural variances in output gain and signal phase shift, especially over varying input voltages and changes in temperature. Such variances must be compensated for in the amplifier circuits in order to 10 achieve reliable and consistent output performance.

An established technique to address this problem is to match the transistor device input and output to a substantially higher impedance, e.g., approximately fifty ohms, which greatly reduces the possibility of variations in gain or phase caused by individual device fluctuations. DC biasing and temperature compensation circuitry are also 15 traditionally employed at the device input terminal to compensate for inherent differences between individual power transistor devices and for changes in temperature during operation.

A simplified schematic illustration of this approach is shown in FIG. 2. In particular, an RF input signal 22 is matched via input matching circuitry 24 to 20 approximately fifty ohms and input at the gate terminal lead 26 into an LDMOS transistor device 28. The device 28 includes a dc bias voltage input 30, which is coupled to dc bias and temperature compensation circuitry 32. The RF output signal 36 at the drain terminal lead 38 of the device 28 is matched to approximately fifty ohms via output matching circuitry 34.

25 In addition to "external matching" of the input and output signals, "internal matching" of the input and output transistor electrode terminals on the die to the respective input and output lead frames is also highly desirable for proper operation of the amplifier device. Unlike external device matching, however, matching to the respective input and output electrode terminals on the die is done at relatively low impedance levels, e.g., one 30 to three ohms on the input (gate) side and five to eight ohms on the output (drain) side. As will be appreciated by those skilled in the art, the actual impedance at the respective

electrode input and output terminals is a function of operating power and frequency, as well as the number of electrode cells/dies of the particular device.

By way of example, FIG. 3 shows a known (matched) LDMOS power transistor device 40. The device 40 includes an input (gate) lead 42 and an output (drain) lead 44 attached to a mounting flange 45. A first plurality of wires 48 couple the input lead 42 to a first terminal of an input matching capacitor 46. A second terminal of the input matching capacitor 46 is coupled to ground, i.e., flange 45. A second plurality of wires 52 couple the first terminal of matching capacitor 46 to the respective input terminals 49 of a plurality of interdigitated electrodes 51 formed on a semiconductor die 50, with the underside of the die 50 (source) mounted to the flange 45. By proper selection of the matching capacitor 46 and the series inductance of wires 48 and 52, the input impedance between the input lead 42 and electrode input terminals 49 can be effectively matched.

Respective output terminals 53 of the electrodes are coupled to the output lead 44 by a third plurality of wires 54. In order to impedance match the output of the device, a shunt inductance is used. Towards this end, the output lead 44 is coupled to a first terminal of a DC blocking capacitor 58 (i.e., an AC short) by a fourth plurality of wires 60, the blocking capacitor 58 having a substantially higher value than the input matching capacitor 46. FIG. 4 shows a schematic circuit representation of the device of FIG. 3, wherein the transmission inductance through the respective pluralities of wires is designated by the corresponding reference numbers of the wires in FIG. 3. A more preferred output-matched LDMOS topology is disclosed and described in U.S. Patent Application Serial No. 09/204,666, which is hereby fully incorporated by reference.

As will be appreciated by those skilled in the art, different applications and circuit designs incorporating high (i.e., microwave) frequency power transistor devices may require correspondingly different external matching and biasing circuitry designs and layout, which can add significant complexity and cost. Typically, such matching and biasing circuitry comprises a combination of precisely sized inductors, capacitors, resistors and transmission paths, which may require substantial circuit board space adjacent the power transistor device. One particular problem that is encountered relates to the difficulty in attaching the mounting flange of the device in precisely the same location in each amplifier circuit layout.

By way of illustration, FIGS. 5 and 6 show a power transistor device 80 mounted on a heat sink 82 as part of an amplifier circuit 75. In particular, the mounting flange 86 of the device 80 is mounted on the heat sink 82 via a conventional solder weld 84. A single layer printed circuit board 88 is also secured to the heat sink 82, e.g., by screws (not
5 shown). A portion of the printed circuit board 88 is removed to form a mounting area (or "well") 85 for the flange 86 to be attached directly to the heat sink 82. The printed circuit board 88 includes a conductive top surface 90, a layer of dielectric material 92, and a metal bottom surface 94, respectively. The bottom surface 94 and heat sink 82 collectively act as a reference ground with respect to circuit elements (not shown) attached
10 to the top surface 90. Respective leads 96 and 98 extend from opposite sides of the device 80 and are connected via solder welds 100 and 102 to corresponding conductive paths 97 and 99 formed by portions the top surface 90 of the printed board 88.

As will be appreciated by those skilled in the art, in order to allow sufficient room for attaching or removing the device 80 from the heat sink 88, the mounting well 85 must
15 be sized lager than the dimensions of the flange 86. As a result, the exact positioning of the flange 86 within the well 85 can vary, as indicated by the arrows 87. This, in turn causes the exact location of the lead frame solder welds 100 and 102 to vary in different devices, since the leads 96 and 98 are typically of a fixed length. This is problematic, in that even slight variances in the location of the electrical connection between the
20 respective lead frames 96 and 98 and the conductive transmission paths 97 and 99 can cause corresponding variances in device performance due to varying transmission path impedance. Compensating for these differences (e.g., by adjustment or "tuning" of the matching and/or dc biasing circuitry) typically requires significant manual time and cost.

Additionally, leads 96 and 98 are required to be relatively wide in order to connect
25 the device terminals to the conductive paths 97 and 99 at the relatively low impedance levels found on the die, which may cause reliability problems related to the mechanical solder connections 100 and 102.

SUMMARY OF THE INVENTION

The present invention is directed to an RF power transistor device, wherein relatively high input and output impedance matching is provided within the device structure itself and, thus, is not required external to the device, e.g., as part of an amplifier
5 circuit employing the device.

In a preferred embodiment, a high frequency LDMOS RF transistor device comprises a conductive mounting flange with a top surface. A dielectric substrate is attached to the top flange surface, the substrate having a window formed therein, exposing a portion of the top flange surface. A semiconductor die is attached to the exposed portion
10 of the top flange surface, the die having a plurality of transistors formed thereon having common electrode input and output terminals. Respective device input and output leads are attached to the dielectric substrate, wherein the input lead is coupled to the electrode input terminals and the output lead is coupled to the electrode output terminals.

In accordance with a first aspect of the invention, an input signal shunt stub is
15 formed on the dielectric substrate as part of a conductive path between the input lead and the respective electrode input terminals. Similarly, an output shunt stub is formed on the dielectric substrate as part of a conductive path between the output lead and the respective electrode output terminals. The respective input and output signal shunt stubs are preferably sized and configured to be effective capacitors to match the respective input
20 and output leads to a relatively high impedance, e.g., fifty ohms.

One advantage of this aspect of the invention is that the relatively high impedance "seen" by the device input and output leads allows for the use of relatively narrow lead frames extending from the device to respective conductive areas on an adjacent printed circuit board.

25 In accordance with a further aspect of the invention, dc biasing and temperature compensation circuitry is also formed on the dielectric substrate and electrically coupled to the input transmission path.

As will be apparent to those skilled in the art, other and further aspects and advantages of the present invention will appear hereinafter.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the present invention are illustrated by way of example, and not by way of limitation, in the figures of the accompanying drawings, in which like reference numerals refer to like components, and in which:

5 FIG. 1 is a schematic circuit diagram of an unmatched LDMOS power transistor device;

FIG. 2 is a simplified partial schematic, partial block diagram of an LDMOS power transistor device employed in a base station amplifier circuit;

FIG. 3 is a partial top view of an LDMOS RF power transistor device;

10 FIG. 4 is a schematic circuit diagram of the LDMOS device of FIG. 3;

FIG. 5 is a partial cut-away side view of an LDMOS power transistor device attached to a heat sink, in which conductive surface leads located on an adjacent printed circuit board are connected to respective input and output leads extending from the transistor device via solder weld connections;

15 FIG.6 is a top view of the assembly of FIG. 5;

FIG. 7 is a partial plan view of an exemplary preferred LDMOS device configured in accordance with the present invention; and

FIG. 8 is a simplified partial schematic, partial block diagram of the LDMOS device of FIG. 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

FIGS. 7 and 8 illustrate a preferred LD MOS power transistor device 120, which includes a conductive mounting flange 121 configured with a plurality of slots 131 to facilitate securing the flange 121 to a heat sink (not shown) with corresponding mounting
5 screws (not shown). The flange 121 has a top surface 125 upon which a dielectric (e.g., alumina) substrate 123 is attached. The dielectric substrate 123 has a rectangular window 130 formed proximate its center, exposing a portion of the top flange surface 125. Within the window 130, a semiconductor (i.e., silicon) die 132 is attached to the exposed top flange surface 125, the die 132 having a plurality of electrodes 133 formed thereon, each
10 electrode comprising a plurality of interdigitated transistors having respective input and output terminals 134 and 136.

An input lead 122, output lead 124, and bias voltage lead 126 are each attached to a top surface 127 of the substrate 123. In particular, the input lead 122 is attached to a conductive pad or "shunt stub" 138 formed on the top surface 127 of the substrate 123.
15 Notably, the input stub 138 is electrically "floating" with respect to the ground (flange 121). Depending on the operating frequency of the device 120, the input shunt stub 138 will alternately act as a shunt capacitor or an inductor. In a preferred operating frequency range for the device 120, the input shunt stub 138 is sized to act as a shunt capacitor, which effectively matches an input RF signal carried on lead 122 to relatively a high
20 impedance, e.g., approximately fifty ohms.

Notably, the effective capacitance of input shunt stub 138 (i.e., as "seen" at the input lead 122) may be adjusted by increasing or decreasing its size and/or configuration. For example, as shown in FIG. 7, if a relatively high capacitance is desired, a further conductive area 139 may be formed on the substrate surface 127 and coupled to the input
25 shunt stub 138 by a selected number (having a selected length) of bond wires 141.

A plurality of bond wires 142 couple the input shunt stub 138 to a first terminal 181 of a first input matching MOSCAP 146 formed on the top flange surface 125. A second terminal (not shown) of the first input matching MOSCAP 146 is coupled to ground, i.e., the top flange surface 125. The MOSCAP 146 reduces, or steps down, the
30 impedance "seen" on the input wires 142 by a selected factor, e.g., to twelve to fifteen ohms in one preferred embodiment. As will be appreciated by those skilled in the art, the actual step down in impedance depends on many factors, including the selected number of

bond wires 142 (two are used in the LDMOS of FIG. 7), the length of each wire, and the operating parameters of the device 120.

Because the impedance at the input terminals 134 is relatively low (e.g., one to two ohms in one preferred embodiment), a second input matching MOSCAP 148 formed on
5 the top flange surface 125 is also employed in the input transmission path. In particular, a further plurality of bond wires 147 couple the first terminal 181 of the first input matching MOSCAP 146 to a first terminal 183 of the second input matching MOSCAP. A second terminal (not shown) of the second input matching MOSCAP 148 is coupled to the top flange surface 125. The second MOSCAP 148 further steps down the impedance on the
10 input transmission path – i.e., as "seen" on the input wires 147. The first terminal 183 of the second MOSCAP 148 is coupled the low impedance electrode input terminals 134 on the die 132 by a still further plurality of bond wires 149. Again, the actual step down in impedance between the first MOSCAP 146, the second MOSCAP 148 and the electrode input terminals 134 depends on many factors, including the selected number and length of
15 the respective bond wires 147 and 149, and the operating parameters of the device 120.

By proper selection of the input matching values of MOSCAPs 146 and 148, as well as proper selection of the number and length (i.e., to set the transmission inductance) of the bond wires 142, 147 and 149, the input impedance between the input shunt stub 138 and the electrode input terminals 134 can be effectively matched.

20 A still further plurality of bond wires 150 couple the electrode output terminals 136 to a first terminal 185 of an output matching MOSCAP 152 formed on the top flange surface 125. A second terminal (not shown) of the output matching MOSCAP 152 is coupled to ground, i.e., the top flange surface 125. The first terminal 185 of the output matching MOSCAP 152 is coupled to an output stub shunt 140 formed on the top surface
25 127 of the substrate 123. As with the input stub 138, the output stub 138 is electrically "floating" with respect to the ground (flange 121). Depending on the operating frequency of the device 120, the output shunt stub 140 will alternately act as a shunt capacitor or an inductor. In a preferred operating frequency range for the device 120, the output shunt stub 140 is sized to act as a shunt capacitor, which effectively matches an output RF signal
30 carried on the output lead 124 to relatively a high impedance.

Because the impedance at the output electrode terminals 136 is relatively higher than at the input terminals 134, only a single output matching MOSCAP 152 is employed

to "step up" the impedance between the output electrode terminals 136 and the output shunt stub 140. As shown in FIG. 7, for higher capacitance values, a further conductive area 159 may be formed on the substrate surface 127 and coupled to the output shunt stub 140 by a selected number (having a selected length) of bond wires 161. In a preferred embodiment, the impedance seen at the input lead 122 is substantially matched to the impedance seen at the output lead 124, e.g., to approximately fifty ohms

In accordance with a further aspect of the invention, dc bias and temperature compensation circuitry are also formed on the top surface 127 of the dielectric substrate 123. As best seen in FIG. 8, the dc bias voltage (i.e., gate to source voltage) input lead 126 is coupled with a first thin film capacitor 160 to eliminate any RF signals that might be present and then passed through a relatively large voltage divider resistance 162. As seen at node "A" in FIG. 8, a first path from the voltage divider resistance 162 is through a relatively small resistance 170 coupled to the device input transmission path at the input shunt stub 138. A second path from the voltage divider resistance 162 is through a further thin film capacitor 168 to ground. A still further path from the voltage divider resistance 162 is through a further resistance 164 to ground. A final path from the voltage divider resistance 162 is through temperature compensation circuitry, including a resistance 166 in series with a pair of cascading Schottky diodes 167 and 169. In a preferred embodiment, the Schottky diodes 167 and 169 are thermally coupled to (e.g., using a plurality of via holes), but electrically isolated from, the mounting flange 121.

Notably, the relatively high impedance "seen" by the device input and output leads 122 and 124 allows for the use of relatively narrow lead frames extending from the device 120 to respective conductive areas on an adjacent printed circuit board.(not shown), simplifying both construction of the device 120 and its installation in an amplifier circuit.

While preferred embodiments and applications of the present invention have been shown and described, as would be apparent to those skilled in the art, many modifications and applications are possible without departing from the inventive concepts herein. For example, the inventive concepts can also be applied to a bi-polar transistor device, wherein the die is electrically isolated from the flange.

Thus, the scope of the disclosed invention is not to be restricted except in accordance with the appended claims.

CLAIMS

What is claimed is:

1. A power transistor device, comprising:

a conductive mounting flange;

5 a dielectric substrate attached to the mounting flange, the substrate having a window formed therein, exposing a portion of the mounting flange;

a semiconductor die attached to the exposed portion of the mounting flange, the die having a plurality of transistors formed thereon having common electrode input and output terminals;

10 an input lead attached to the substrate and electrically coupled to the respective electrode input terminals via an input transmission path, the input transmission path including an input impedance matching element disposed on the substrate; and

an output lead attached to the substrate and electrically coupled to the respective electrode output terminals via an output transmission path, the output transmission path

15 including an output impedance matching element disposed on the substrate.

2. The power transistor device of claim 1, wherein the input and output impedance matching elements comprise respective shunt stubs formed on the substrate.

20 3. The power transistor device of claim 1, further comprising dc biasing circuitry located on the substrate and electrically coupled to the input transmission path.

4. The power transistor device of claim 1, further comprising temperature compensation circuitry located on the substrate and electrically coupled to the input

25 transmission path.

5. The power transistor device of claim 4, wherein the temperature compensation circuitry is thermally coupled to the mounting flange.

30 6. The power transistor device of claim 1, wherein the respective input and output leads are substantially impedance matched.

7. The power transistor device of claim 6, wherein the respective input and output leads are matched to approximately fifty ohms.

8. The power transistor device of claim 1, comprising further input and output
5 impedance matching elements located on the mounting flange.

9. A power transistor device, comprising:

a conductive mounting flange;

a dielectric substrate attached to the mounting flange, the substrate having a
10 window formed therein, exposing a portion of the mounting flange;

a semiconductor die attached to the exposed portion of the mounting flange, the die having a plurality of transistors formed thereon having common electrode input and output terminals;

an input lead attached to the substrate and electrically coupled to the respective
15 electrode input terminals via an input transmission path, the input transmission path including an input impedance matching element disposed on the substrate;

an output lead attached to the substrate and electrically coupled to the respective electrode output terminals via an output transmission path, the output transmission path including an output impedance matching element disposed on the substrate;

20 dc biasing circuitry located on the substrate and electrically coupled to the input transmission path; and

temperature compensation circuitry located on the substrate and electrically coupled to the input transmission path.

25 10. The power transistor device of claim 9, wherein the input and output impedance matching elements comprise respective shunt stubs formed on the substrate.

11. The power transistor device of claim 9, wherein the temperature compensation circuitry is thermally coupled to the mounting flange.

30

12. The power transistor device of claim 9, wherein the respective input and output leads are substantially impedance matched.

13. The power transistor device of claim 12, wherein the respective input and output leads are matched to approximately fifty ohms.

5 14. The power transistor device of claim 9, comprising further input and output impedance matching elements located on the mounting flange.

15. A power transistor device, comprising:

a conductive mounting flange;

10 a dielectric substrate attached to the mounting flange, the substrate having a window formed therein, exposing a portion of the mounting flange;

a semiconductor die attached to the exposed portion of the mounting flange, the die having a plurality of transistors formed thereon having common electrode input and output terminals;

15 an input lead attached to the substrate and electrically coupled to the respective electrode input terminals via an input transmission path, the input transmission path including a first shunt stub formed on the substrate and an input matching MOSCAP formed on the flange; and

an output lead attached to the substrate and electrically coupled to the respective 20 electrode output terminals via an output transmission path, the output transmission path including a second shunt stub formed on the substrate and an output matching MOSCAP formed on the flange.

16. The power transistor device of claim 15, further comprising dc biasing circuitry 25 located on the substrate and electrically coupled to the input transmission path.

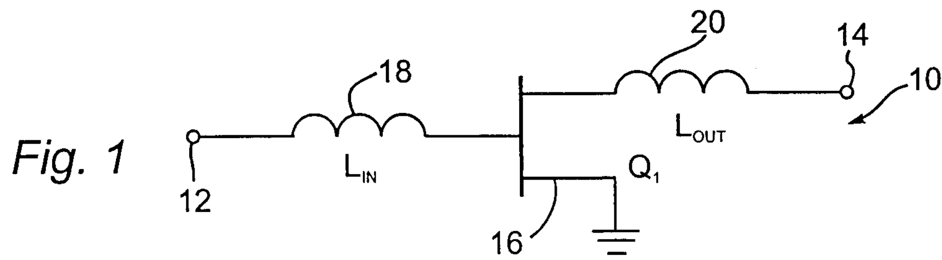
17. The power transistor device of claim 9, further comprising temperature compensation circuitry located on the substrate, the temperature compensation circuitry being electrically coupled to the input transmission path and thermally coupled to the flange.

5

18. The power transistor device of claim 15, wherein the respective input and output leads are substantially impedance matched.

19. The power transistor device of claim 18, wherein the respective input and output

10 leads are matched to approximately fifty ohms.



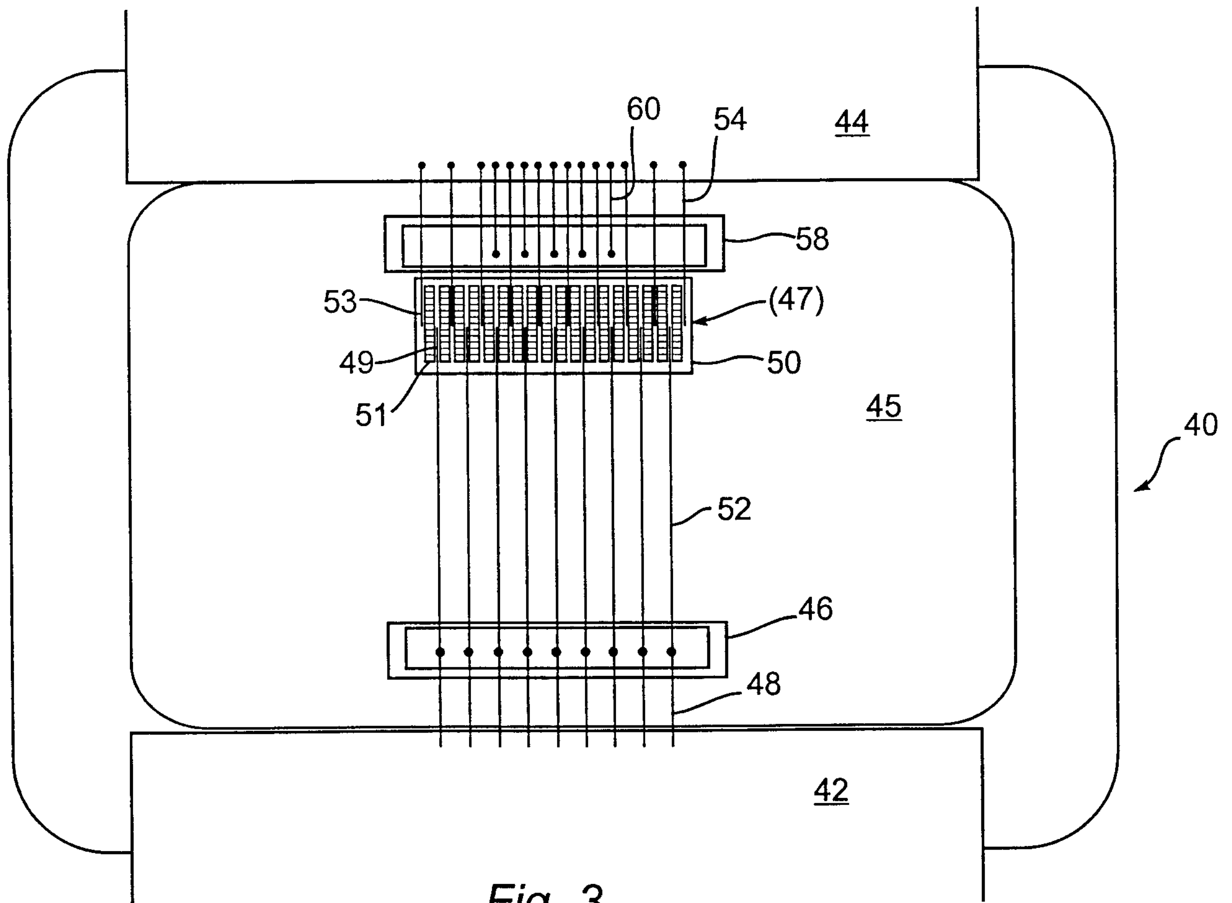


Fig. 3

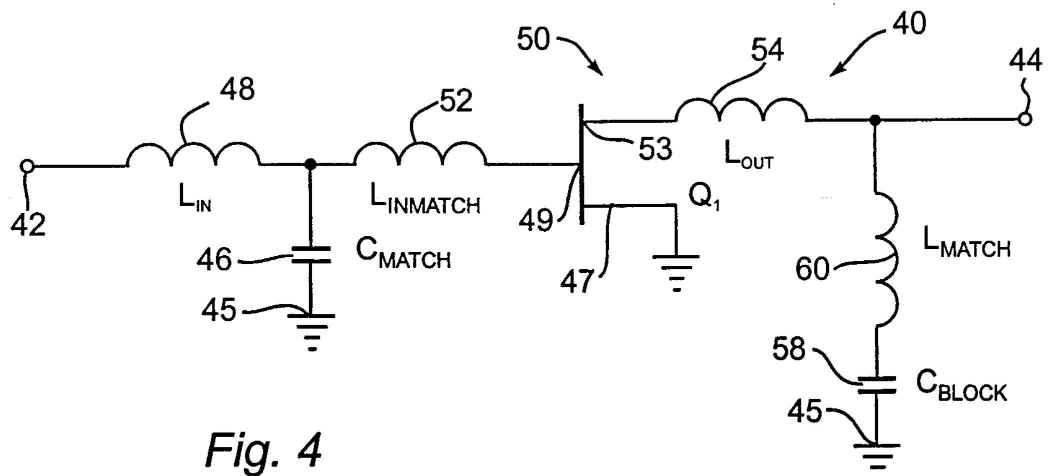


Fig. 4

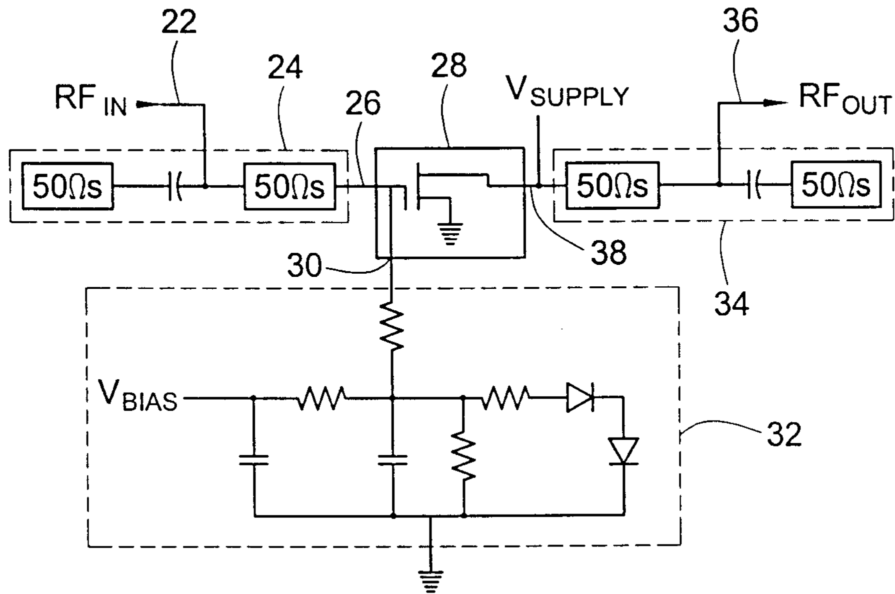


Fig. 2

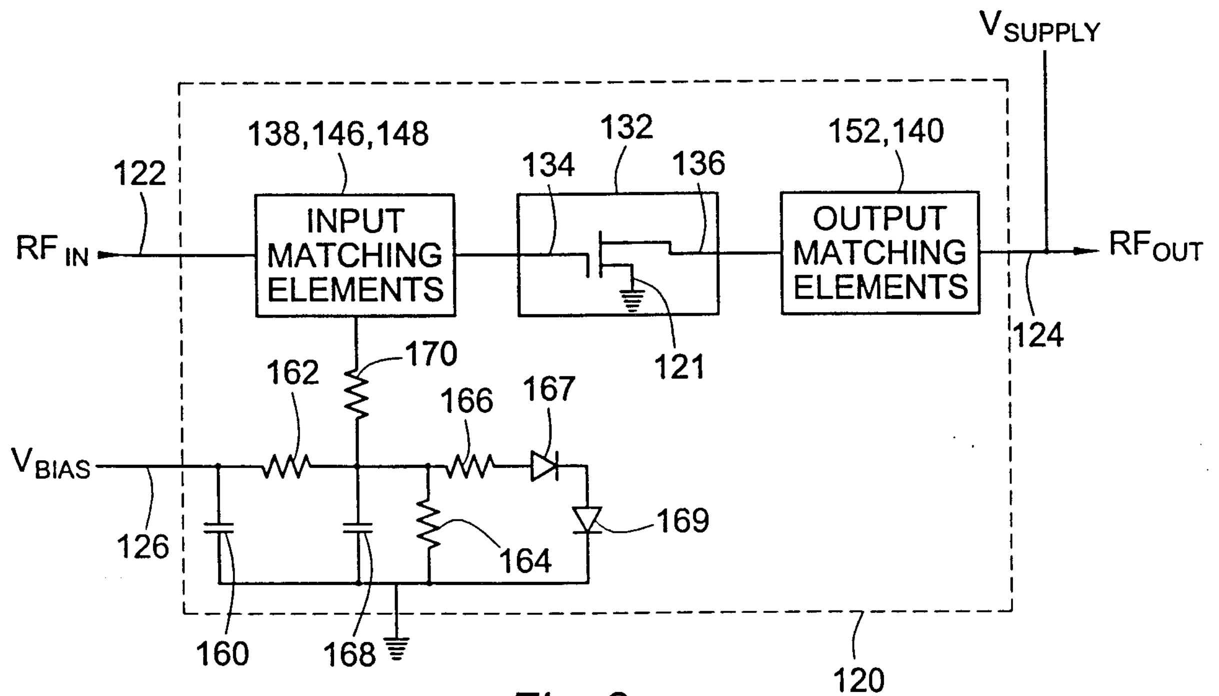


Fig. 8

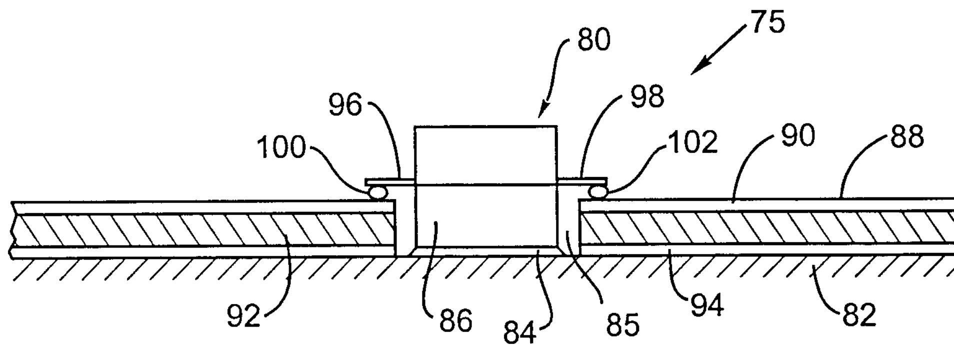


Fig. 5

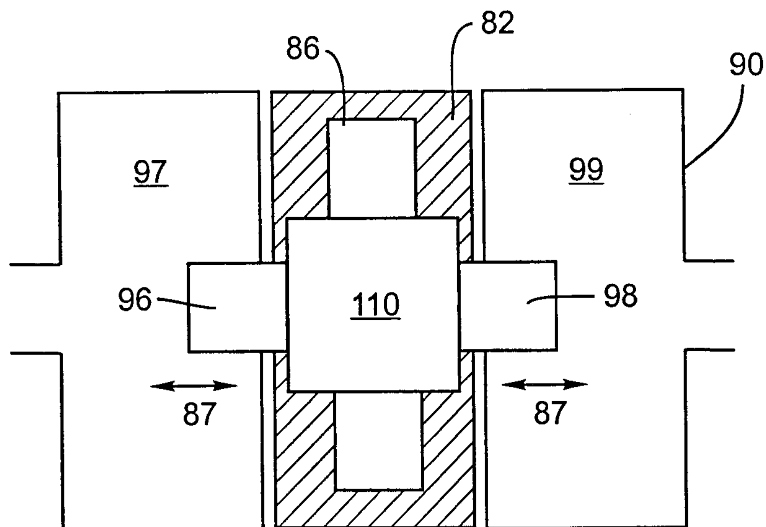


Fig. 6

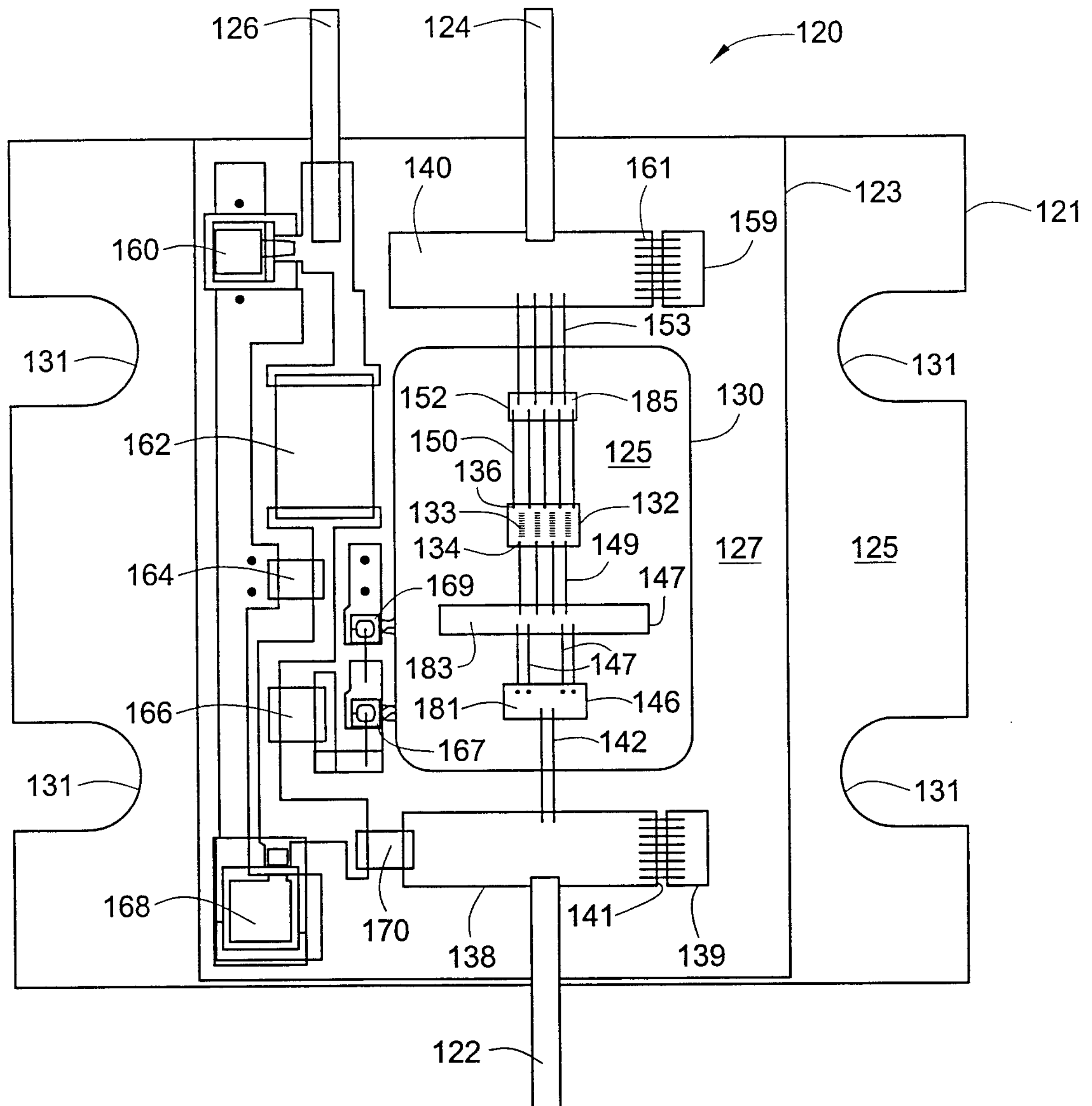


Fig. 7

INTERNATIONAL SEARCH REPORT

Interr. ›al Application No
PCT/US 00/14848

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L23/66

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 901 042 A (MAEDA MASAHIRO ET AL) 4 May 1999 (1999-05-04) column 1, line 44 -column 2, line 8; figure 4A	1,2,6,8, 15
X	LIANG T ET AL: "EQUIVALENT-CIRCUIT MODELING AND VERIFICATION OF METAL-CERAMIC PACKAGES FOR RF AND MICROWAVE POWER TRANSISTORS" IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES,US,IEEE INC. NEW YORK, vol. 47, no. 6, PART 01, June 1999 (1999-06), pages 709-713, XP000830155 ISSN: 0018-9480 the whole document	1,2,6-8

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

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Date of the actual completion of the international search	Date of mailing of the international search report
28 August 2000	11/09/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Ahlstedt, M

1

Form PCT/ISA/210 (second sheet) (July 1992)

Intern. nal Application No
PCT/US 00/14848

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 967 258 A (FITHIAN MICHAEL J ET AL) 30 October 1990 (1990-10-30) column 1, line 61 - line 66 ---	1-19
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