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H01L 27/108

(52) UK CL (Edition N)
H1K KGAMS K1DE K11B4 K11C1B K11D K11D1 K4C11 K9B9 K9E

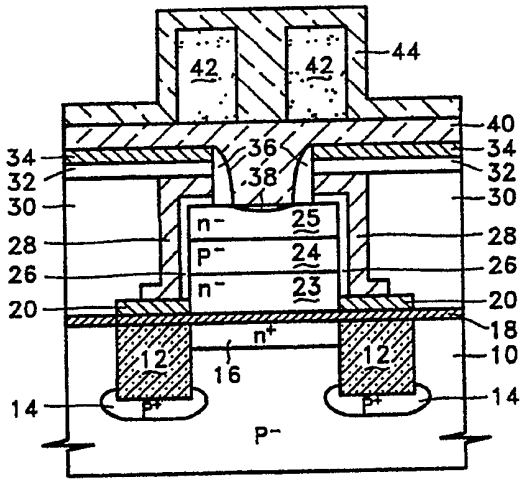
(56) Documents Cited
US 5192704 A US 5136534 A

(58) Field of Search
UK CL (Edition M) H1K KGAMS KGAMX
INT CL[5] H01L
Online database: WPI

(54) Dram memory cell utilising surrounding gate transistor and method of manufacture

(57) A highly integrated DRAM and method of manufacture are disclosed. A trench isolation region (12) is formed in order to define an active region in a semiconductor substrate (10), and a bit line (18) is formed on the semiconductor substrate (10) wherein the trench isolation region (12) is formed. A silicon pillar (23, 24, 25) is formed on the bit line (18), and drain (23), channel (24), and source (25) regions of a transistor are sequentially formed from a lower portion of the silicon pillar to an upper portion thereof. A gate insulating film (26) and a gate line (28) are sequentially formed so as to surround the silicon pillar, and a planarizing layer (30) is formed between the adjacent gate lines (28). An insulating layer is formed on the gate lines (28), having a contact hole for exposing the source region (25) of the transistor. A capacitor storage node (46) is formed on an insulating layer, and is connected to the source region (25) of the transistor through the contact hole. A buried bit line structure and a vertical gate structure surrounding a silicon pillar are formed, and thus, the maximum effective active area can be utilized.

FIG. 8B



GB 2 288 276 A

FIG. 1A

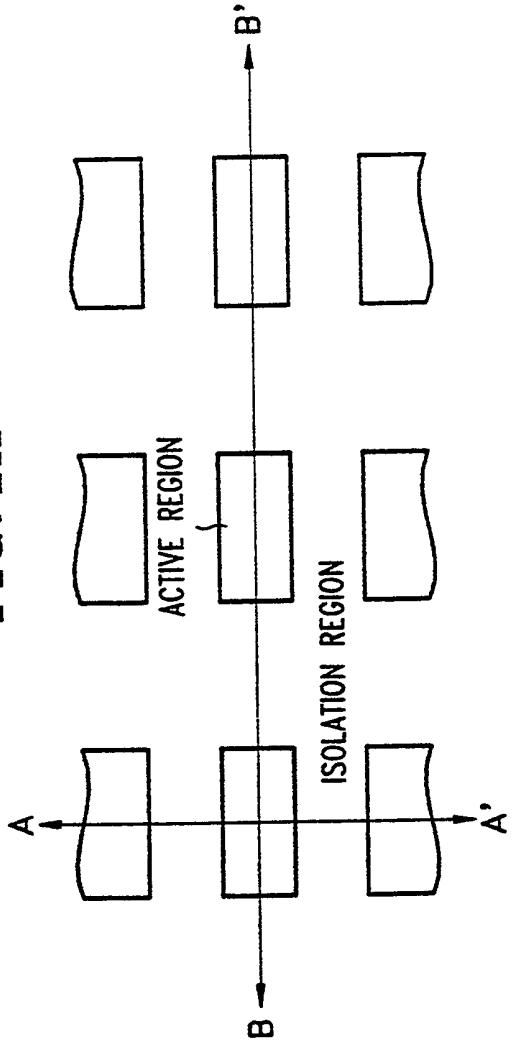


FIG. 1C

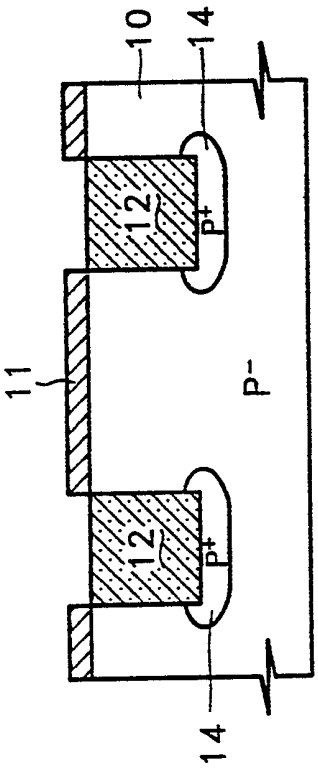


FIG. 1B

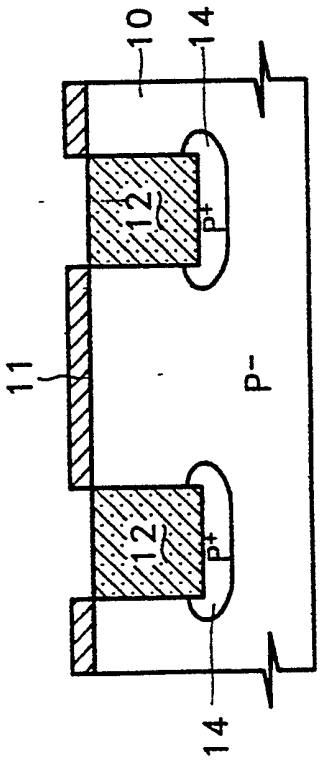


FIG. 2A

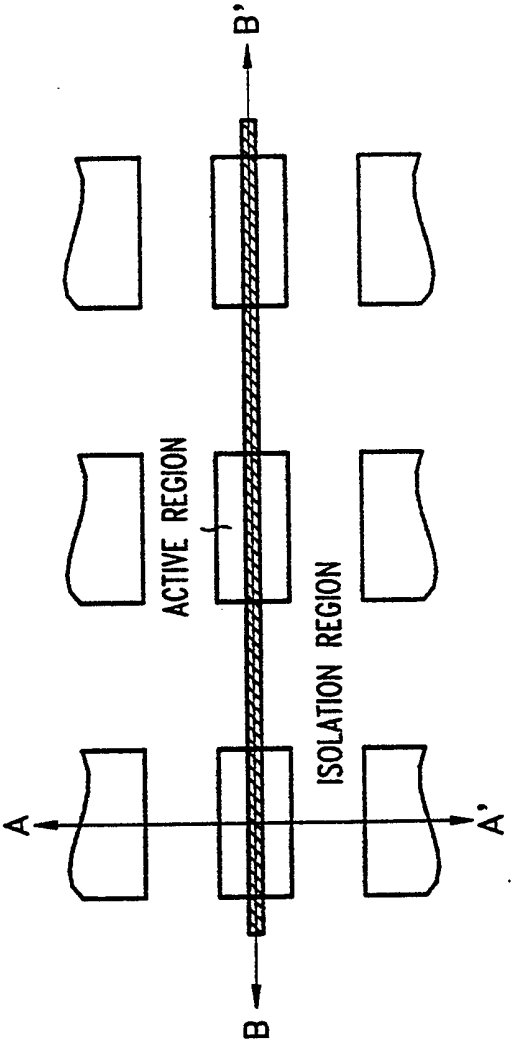


FIG. 2C

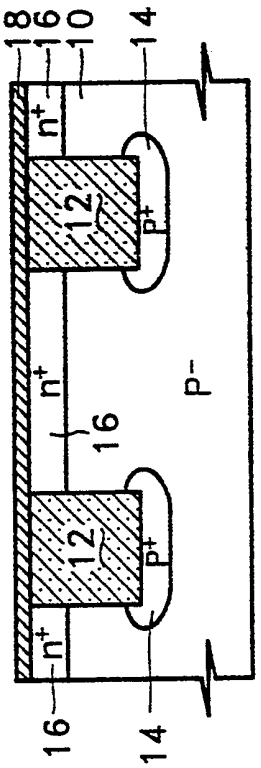


FIG. 2B

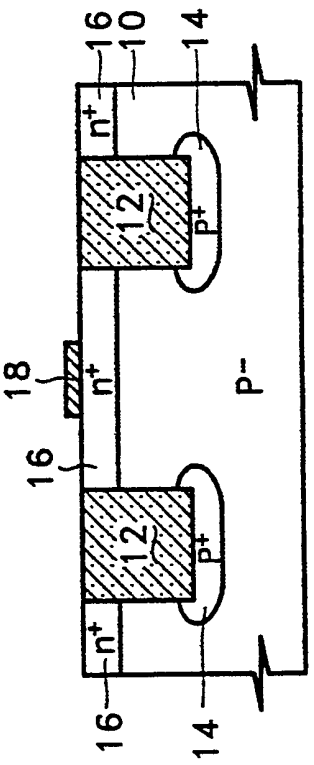


FIG. 3B

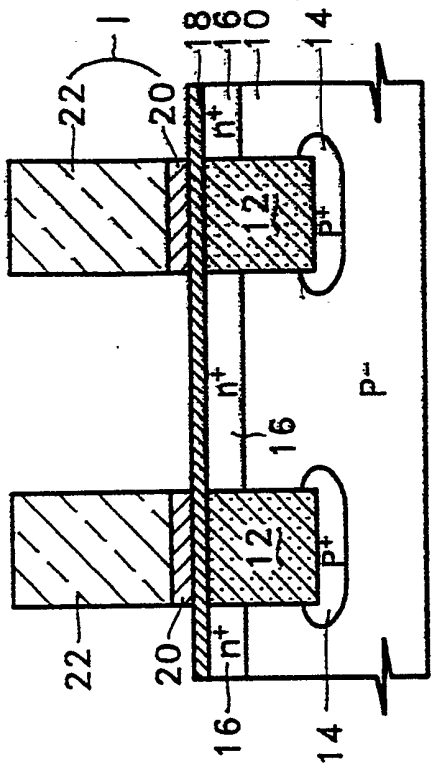
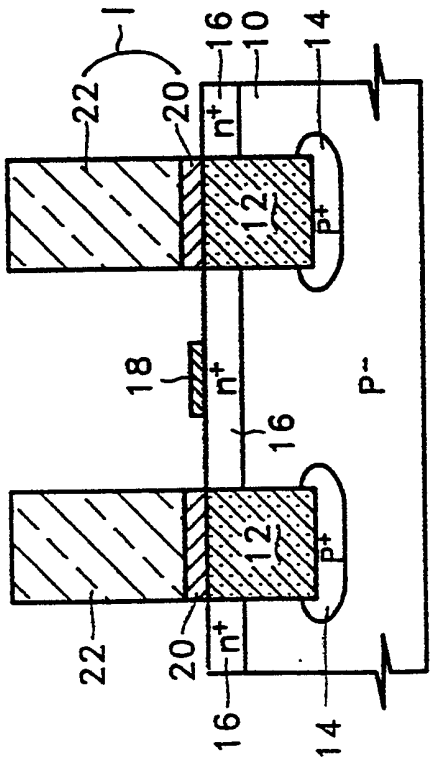

1
18
16
10
14
22
20
n+
12
P+
P--
16
22
20
n+
16
14

FIG. 3A


1
16
10
14
22
20
n+
12
P+
18
n+
P--
16
22
20
n+
16
14

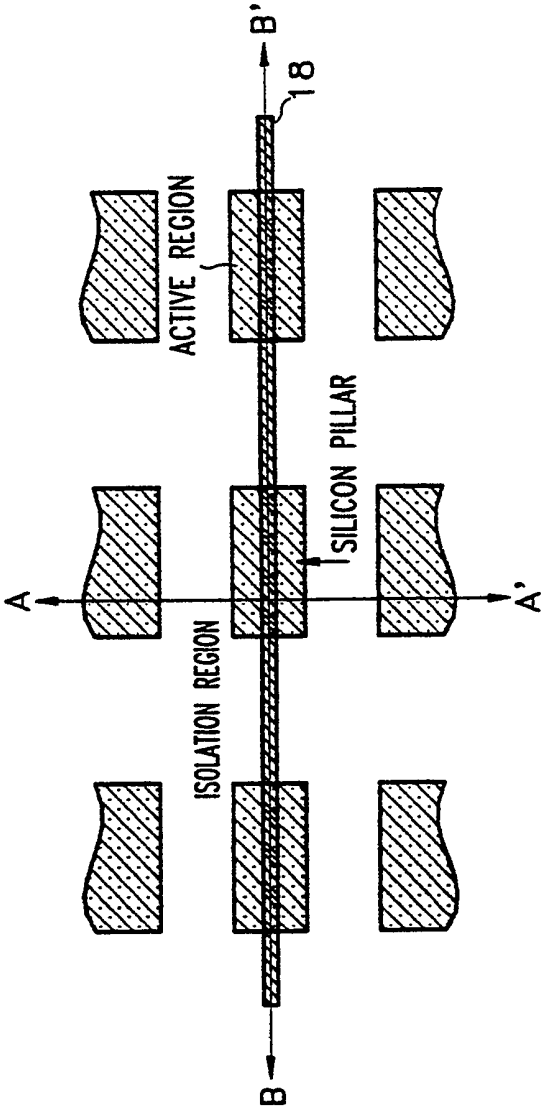


FIG. 4A

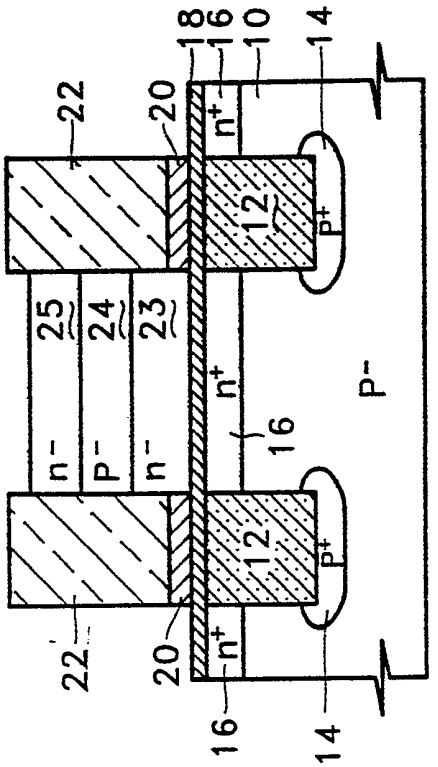


FIG. 4C

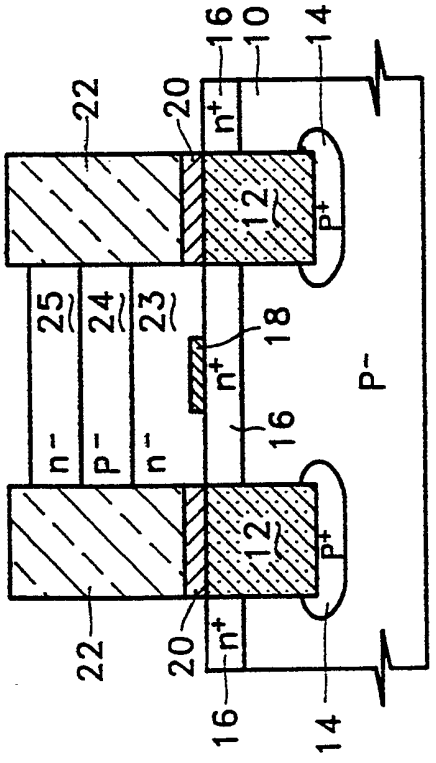
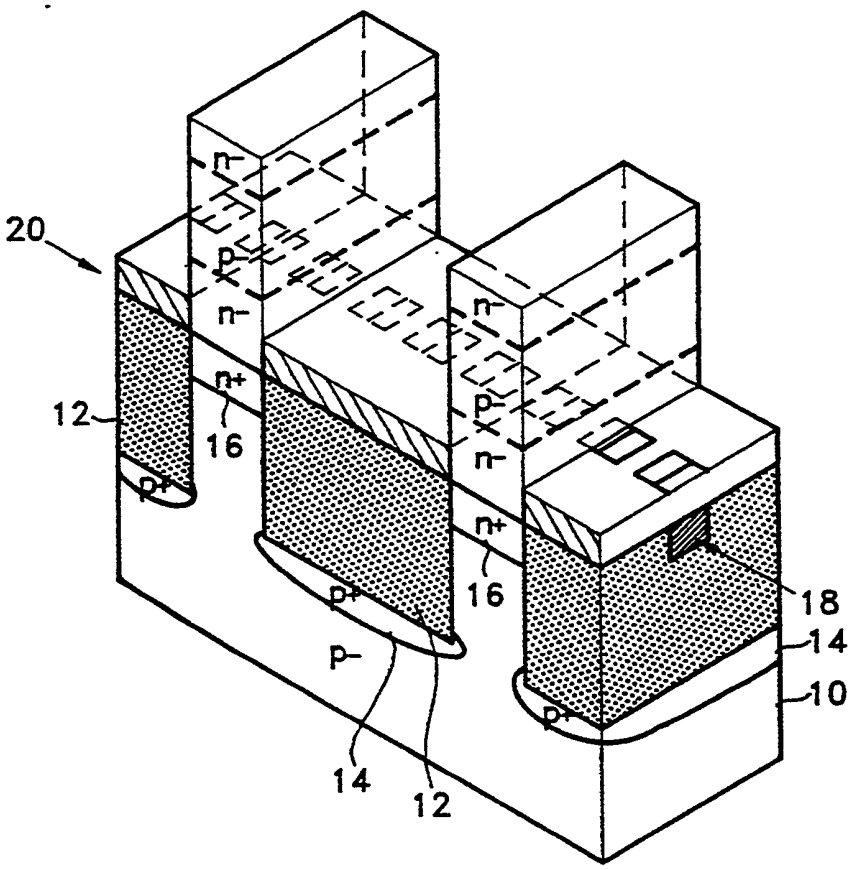


FIG. 4B

FIG. 4D



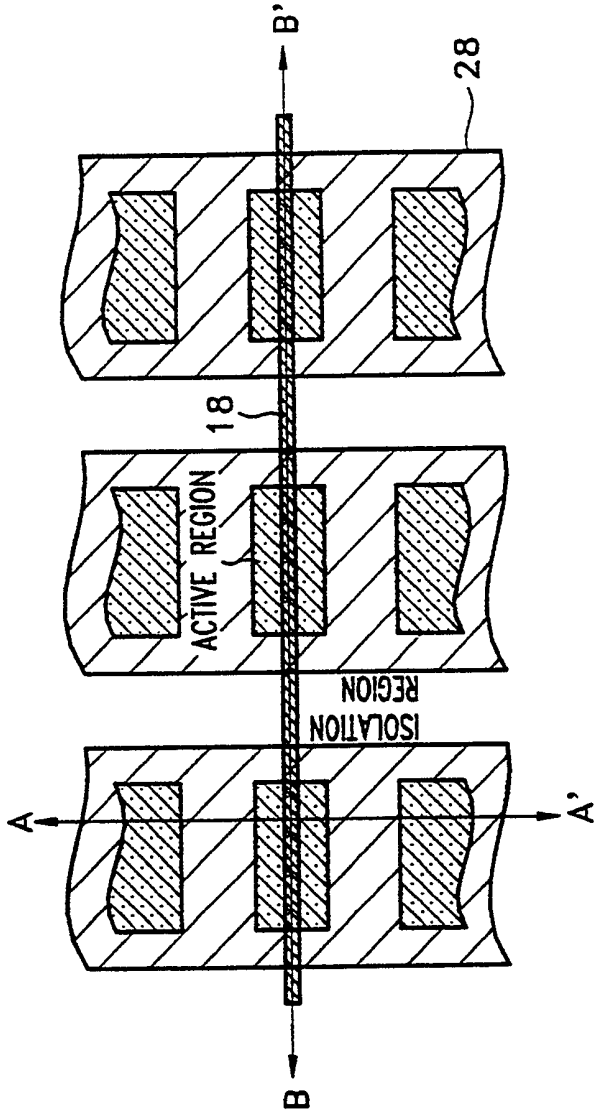


FIG. 5A

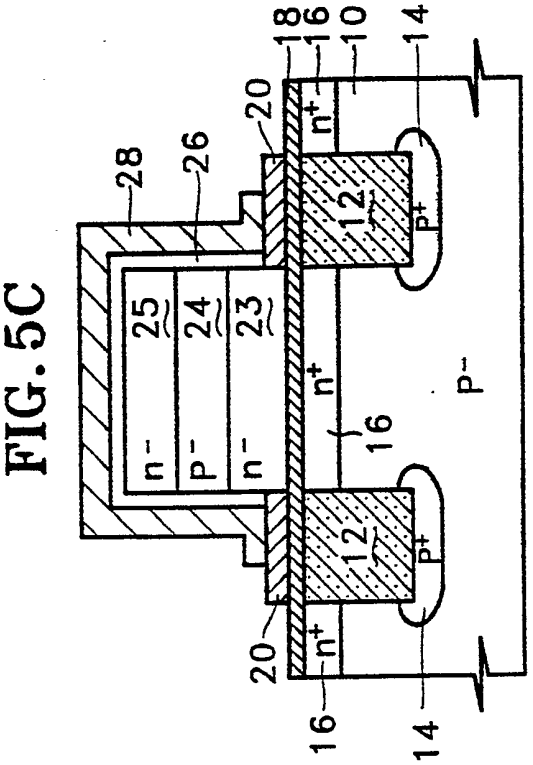


FIG. 5C

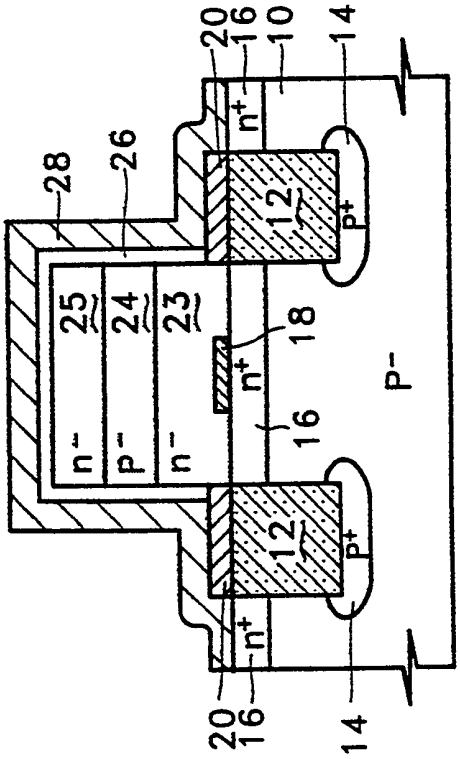


FIG. 5B

FIG. 6B

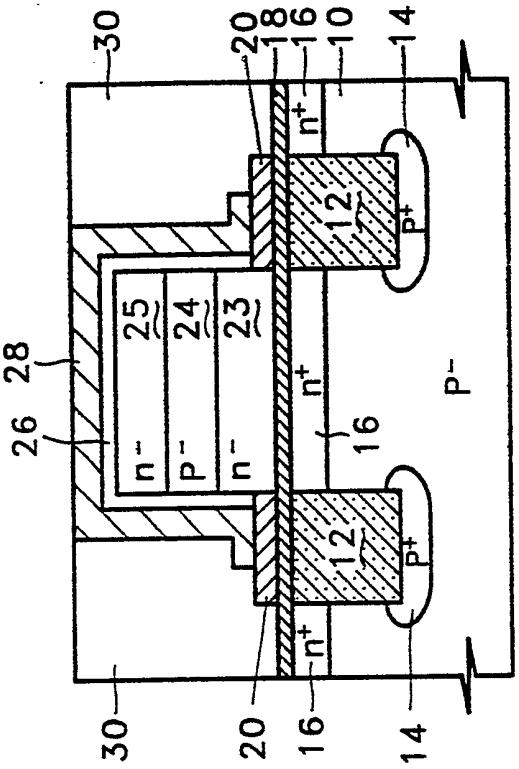

30
20
18
16
10
14
n+
12
P+
25
24
23
28
26
n−
P−
n−
16
P−
n+
12
P+
n+
30
20
16
14

FIG. 6A

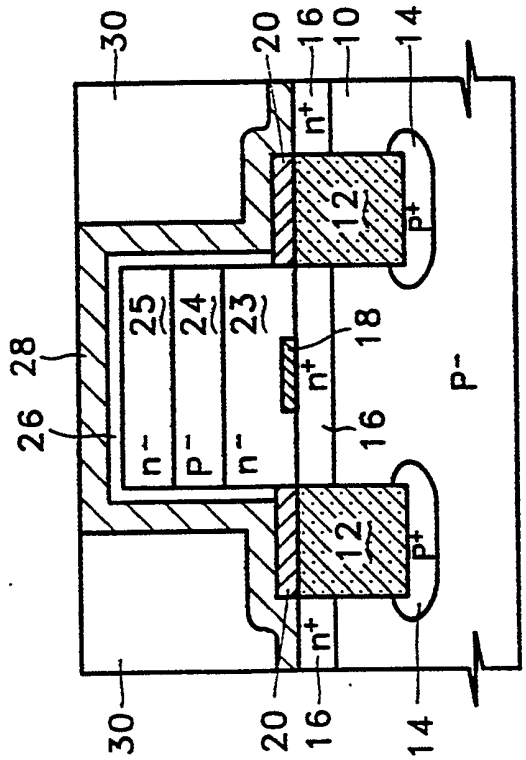

30
20
16
10
14
n+
12
P+
25
24
23
28
18
26
n−
P−
n−
16
P−
n+
12
P+
n+
30
20
16
14

FIG. 7B

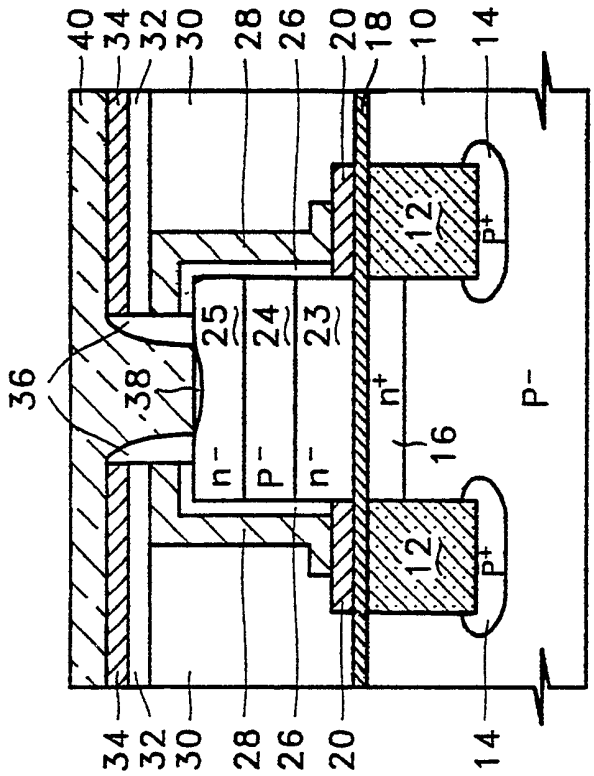

40
34
32
30
28
26
20
18
10
14
12
P+
25
24
23
36
38
n−
P−
n−
n+
16
P−

FIG. 7A

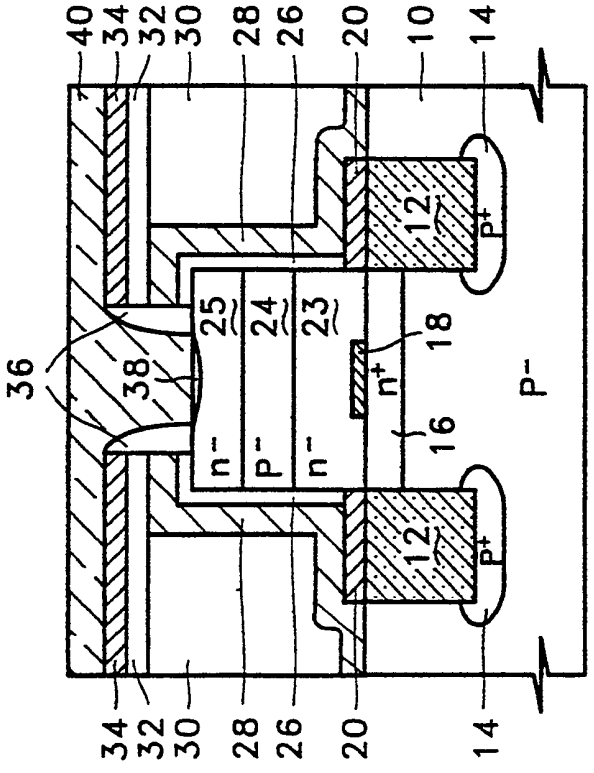
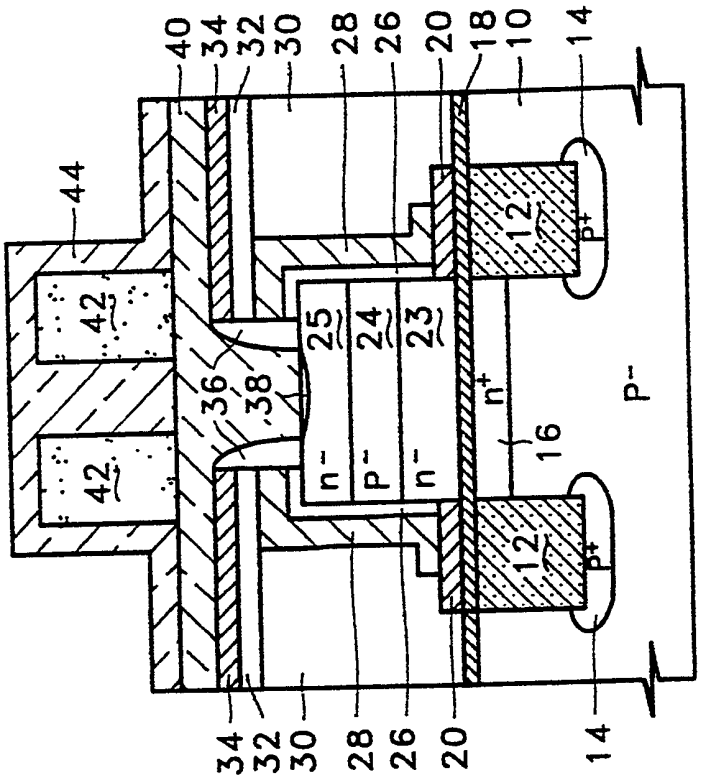

40
34
32
30
28
26
20
10
14
12
P+
25
24
23
18
36
38
n−
P−
n−
n+
16
P−

FIG. 8B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34
32
30
28
26
20
18
10
14
44
42
42
36
38
25
24
23
n⁻
P⁻
n⁻
n⁺
16
12
12
P⁺
P⁺
P⁻
34
32
30
28
26
20
14

FIG. 8A

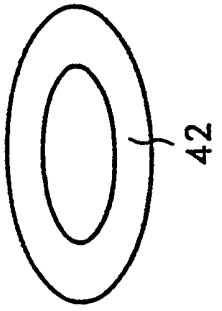
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FIG. 10

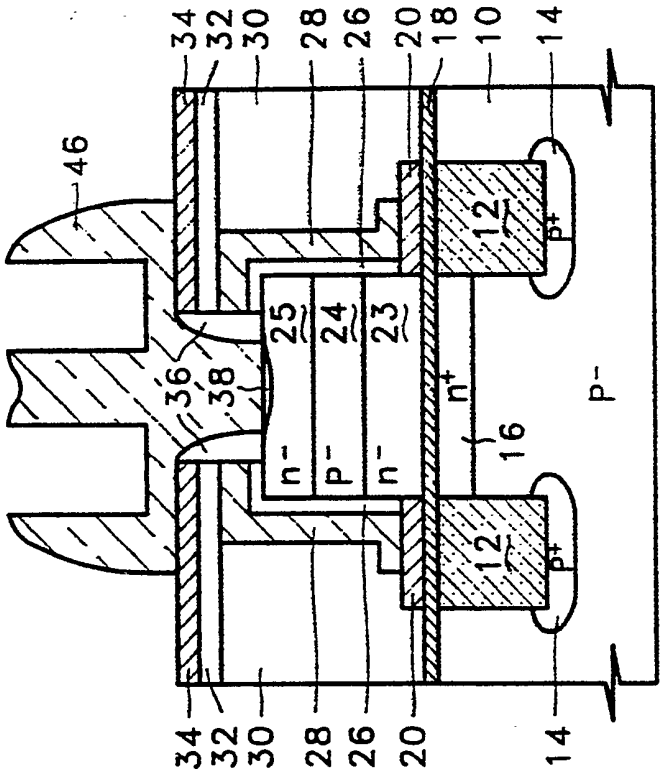

34
32
30
28
26
20
18
10
14
46
12
P+
25
24
23
36
38
n+
16
n-
P-
n-
P-

FIG. 9

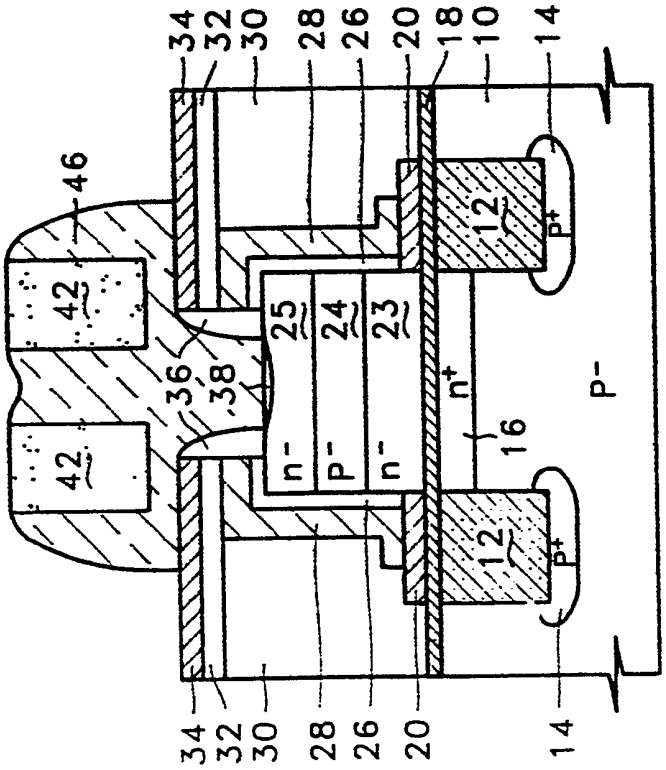

34
32
30
28
26
20
18
10
14
46
42
42
12
P+
25
24
23
36
38
n+
16
n-
P-
n-
P-

FIG. 11

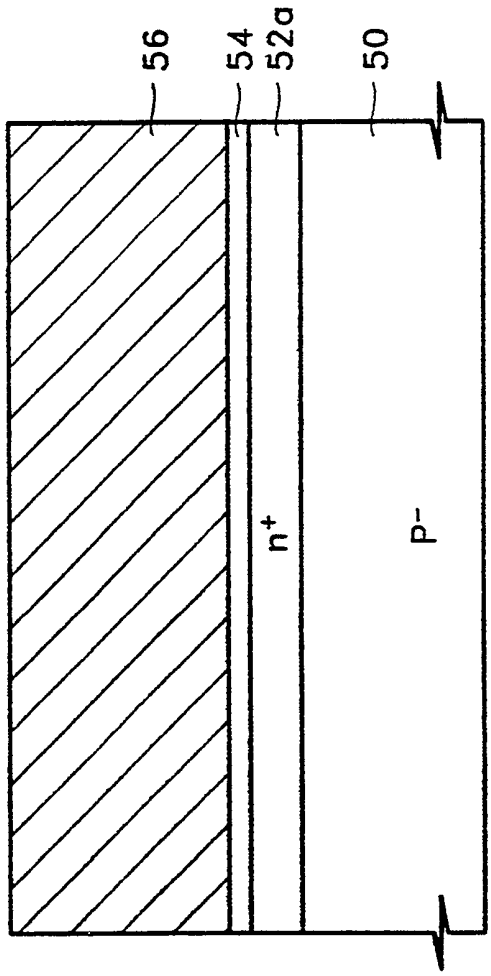


FIG. 12A

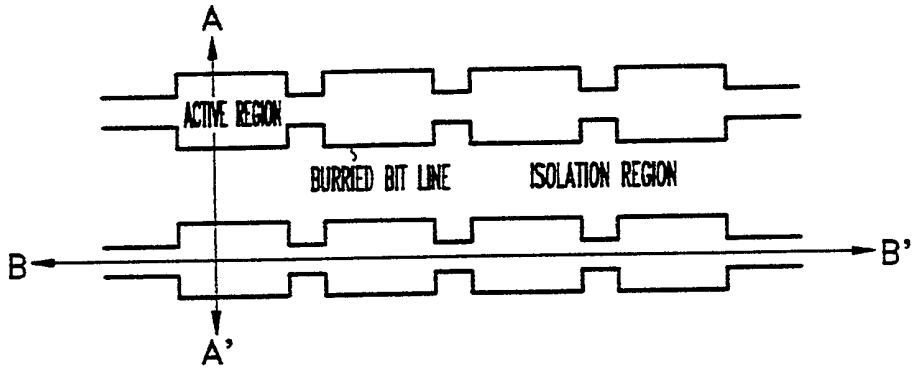


FIG. 12B

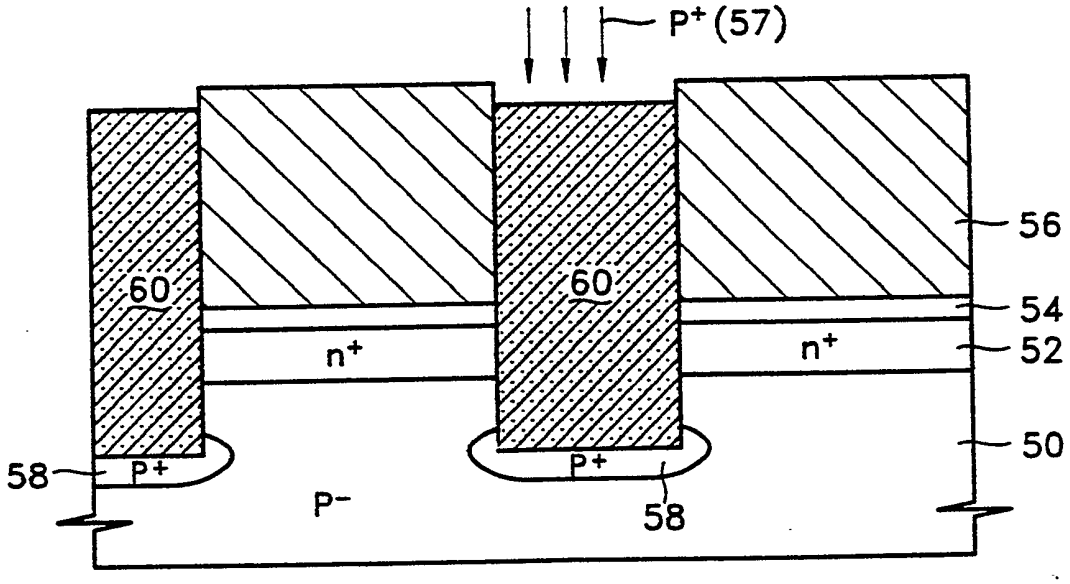


FIG. 13

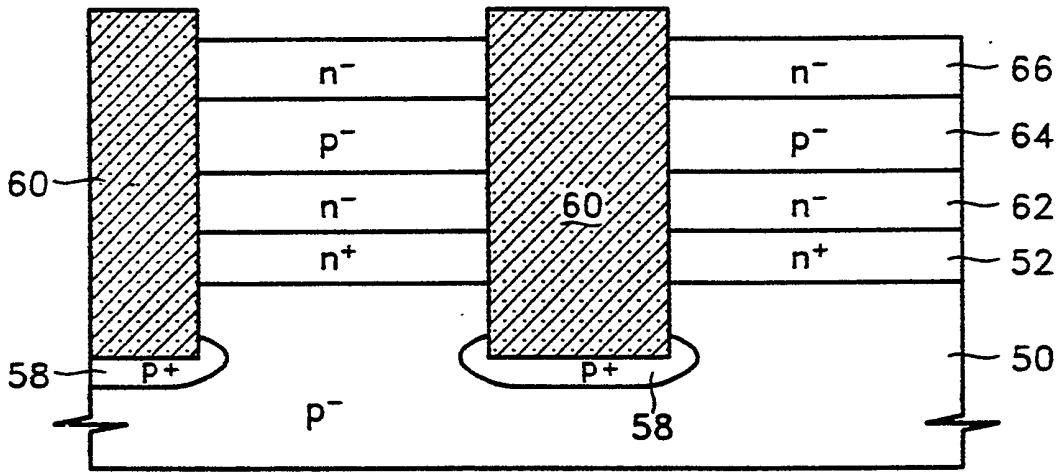

n⁻
p⁻
n⁻
n⁺
60
60
58
P+
P+
p⁻
58
66
64
62
52
50

FIG. 14

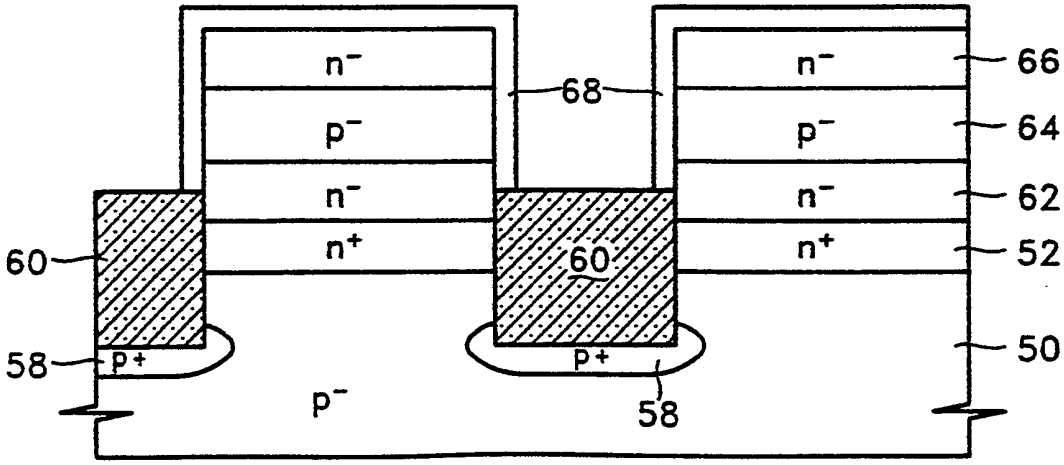

n⁻
p⁻
n⁻
n⁺
68
60
60
58
P+
P+
p⁻
58
66
64
62
52
50

FIG. 15A

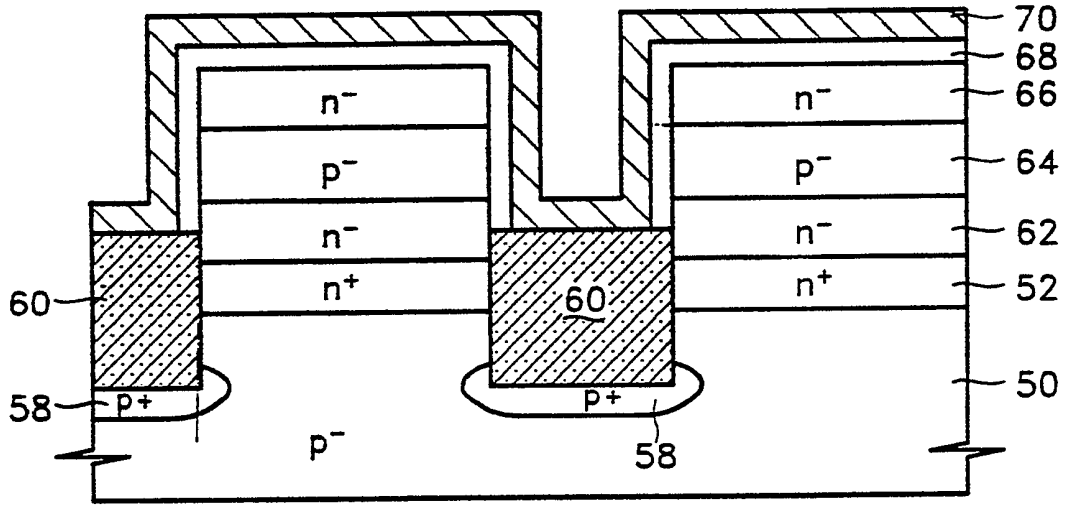


FIG. 15B

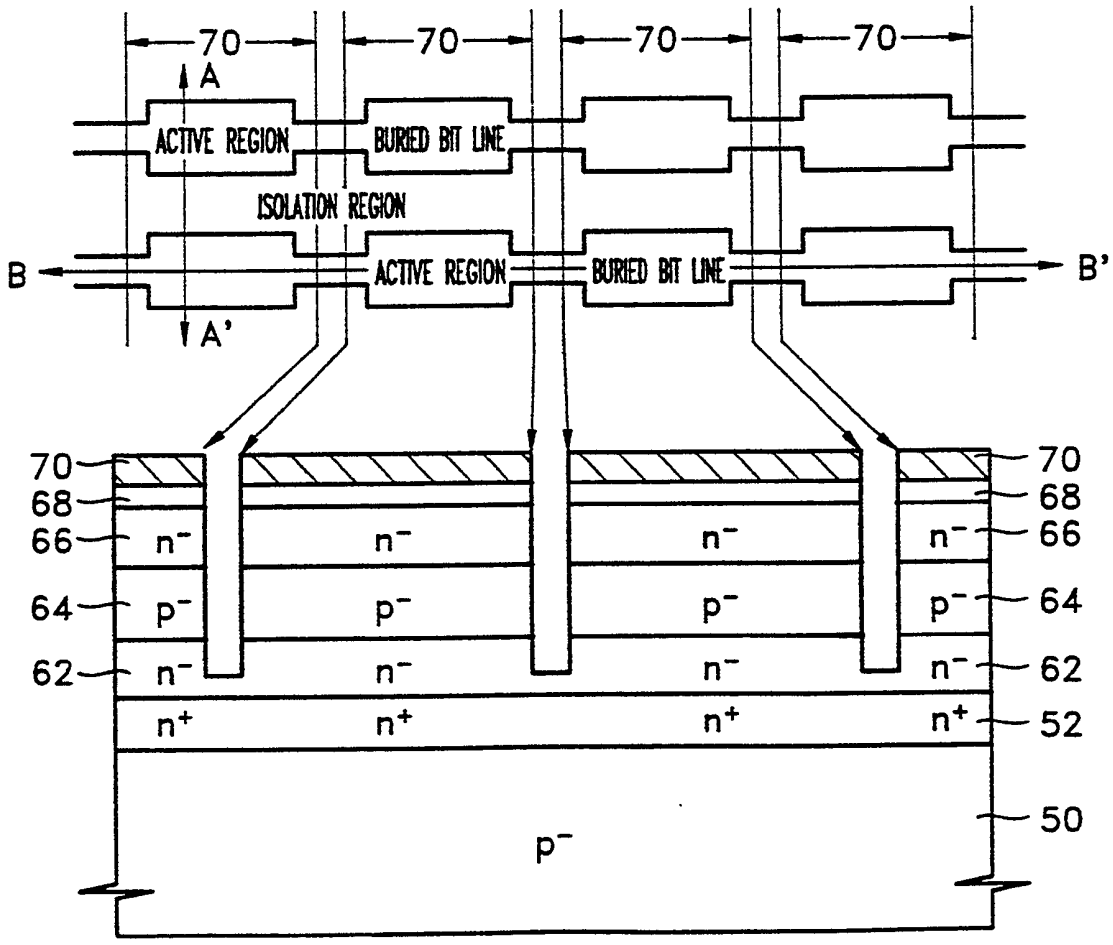


FIG. 16

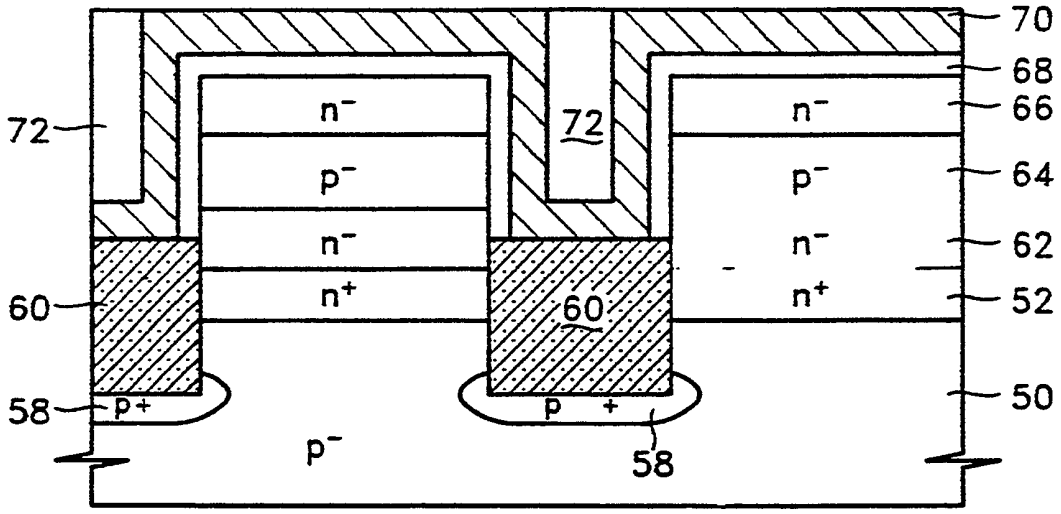

70
68
66
64
62
52
50
72
72
n⁻
n⁻
p⁻
p⁻
n⁻
n⁻
n⁺
n⁺
60
60
58
p+
p+
p⁻
58

FIG. 17

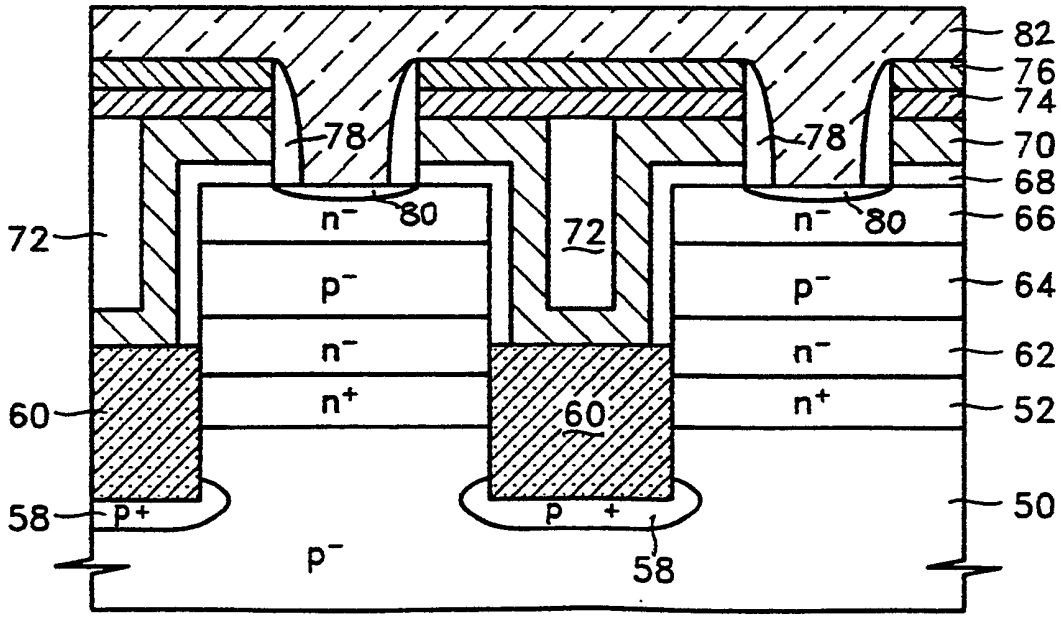

82
76
74
70
68
66
64
62
52
50
78
78
72
72
n⁻
n⁻
80
80
p⁻
p⁻
n⁻
n⁻
n⁺
n⁺
60
60
58
p+
p+
p⁻
58

FIG. 18

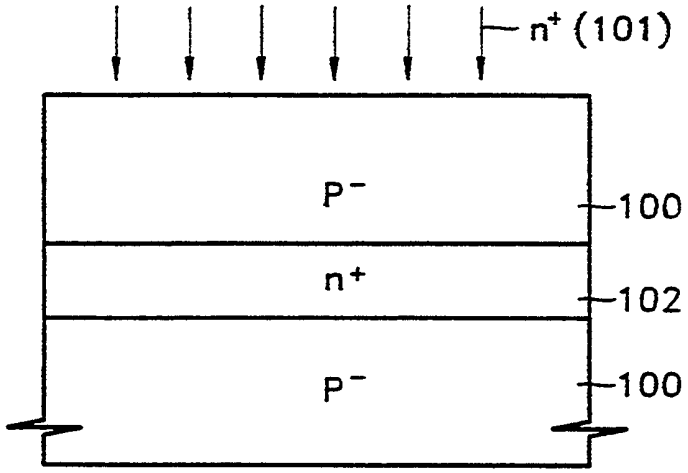


FIG. 19

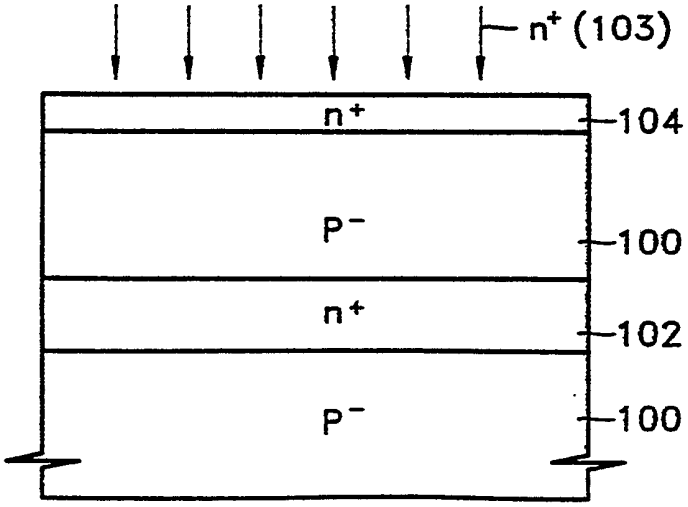


FIG. 20A

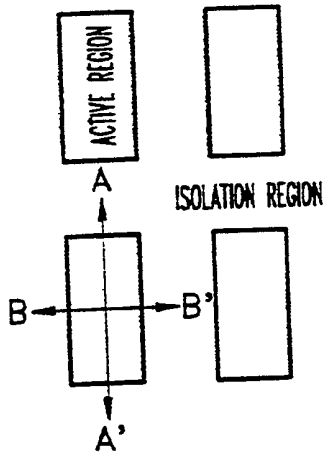


FIG. 20B

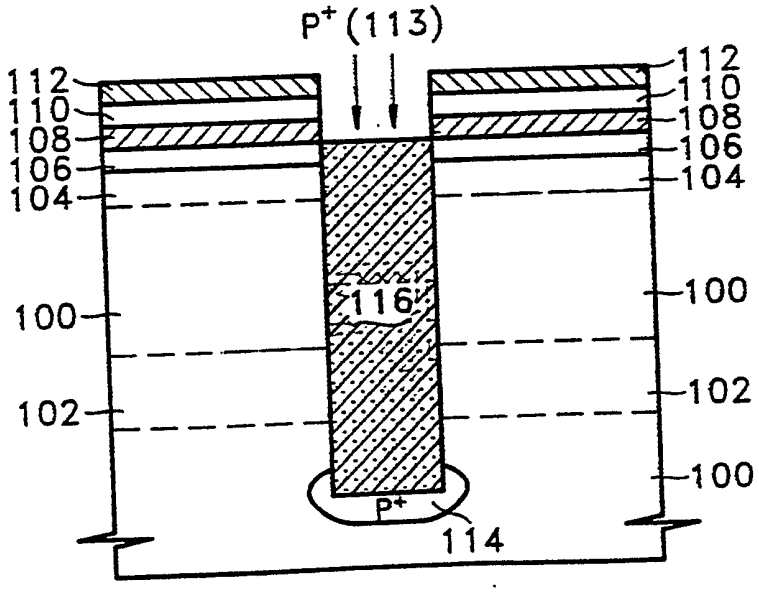


FIG. 21A

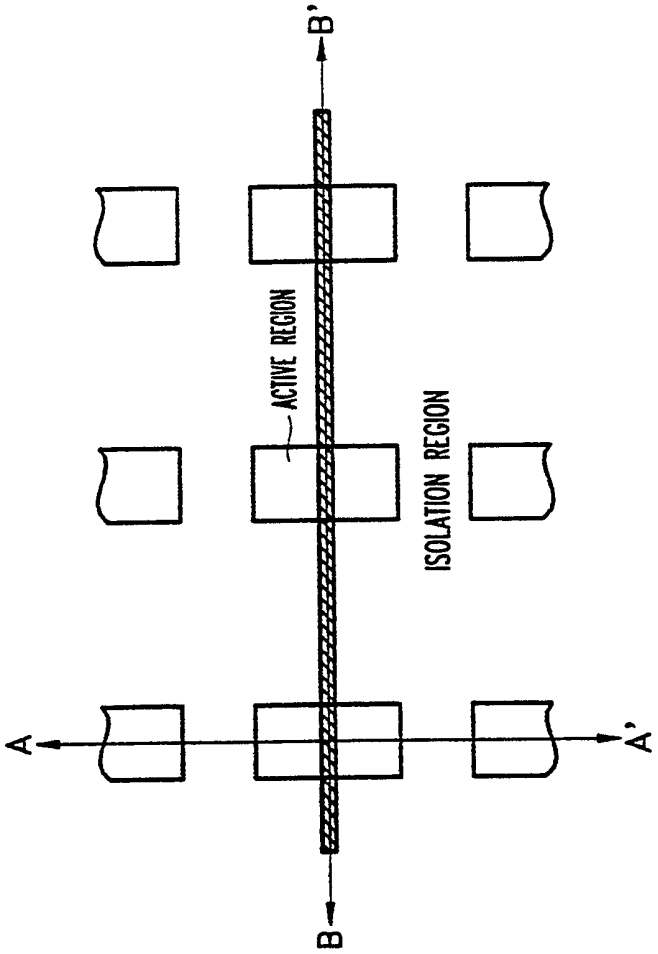


FIG. 21B

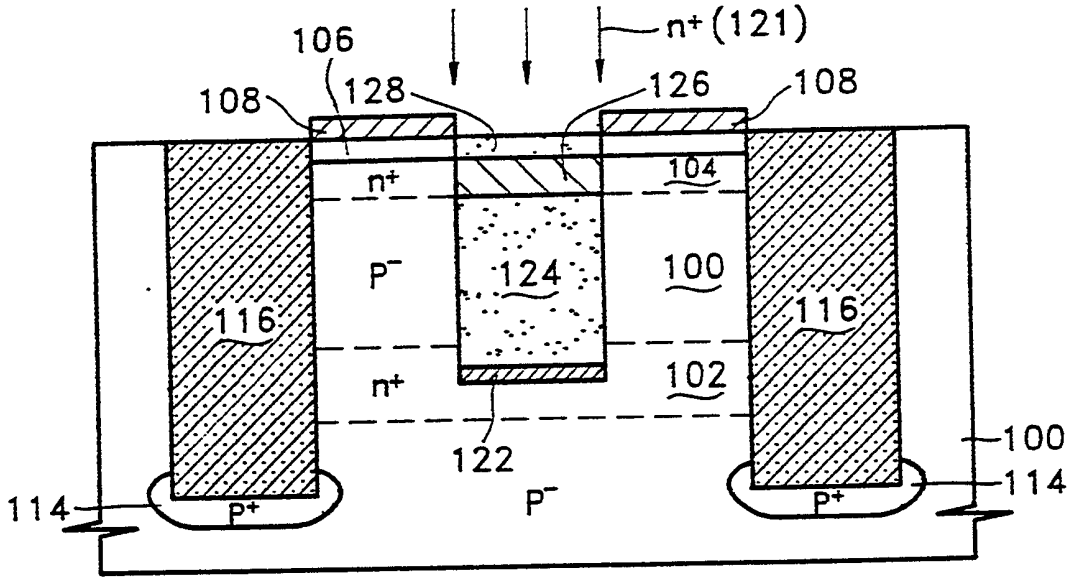


FIG. 21C

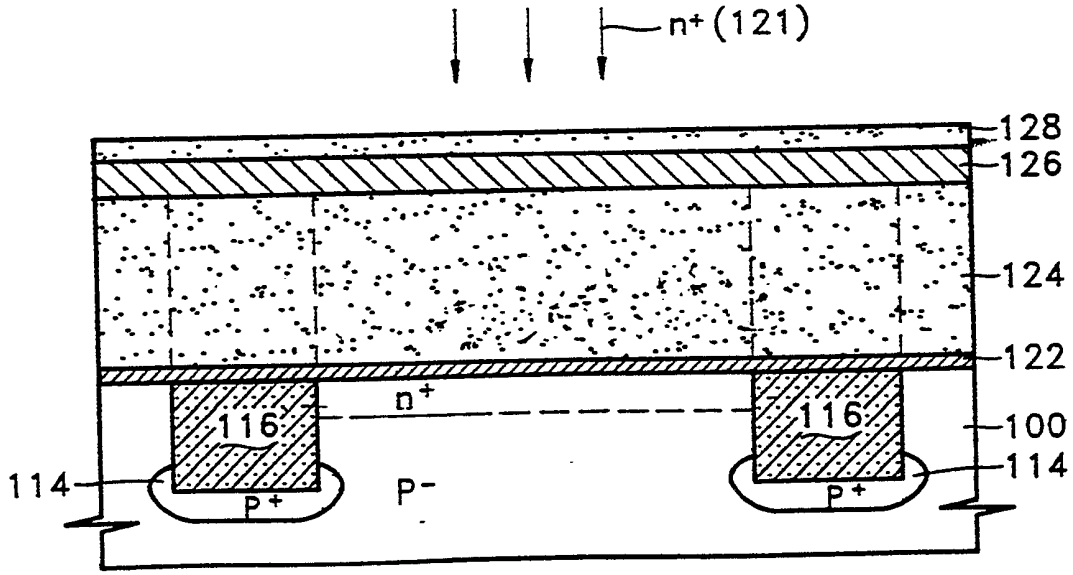


FIG. 22A

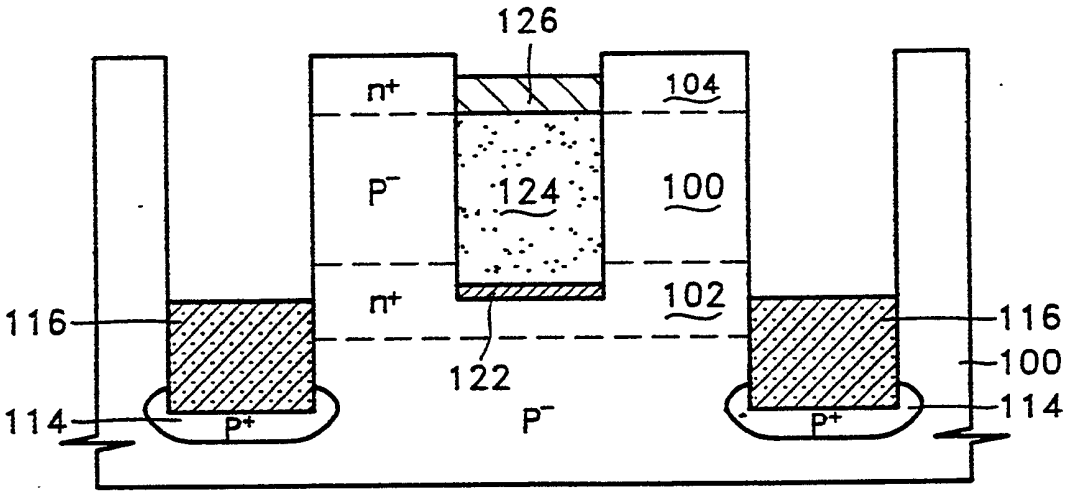


FIG. 22B

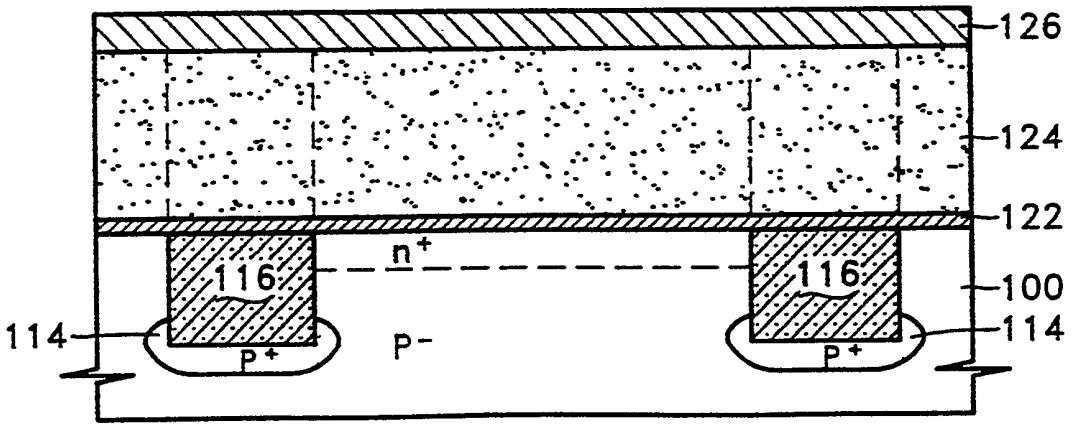


FIG. 23A

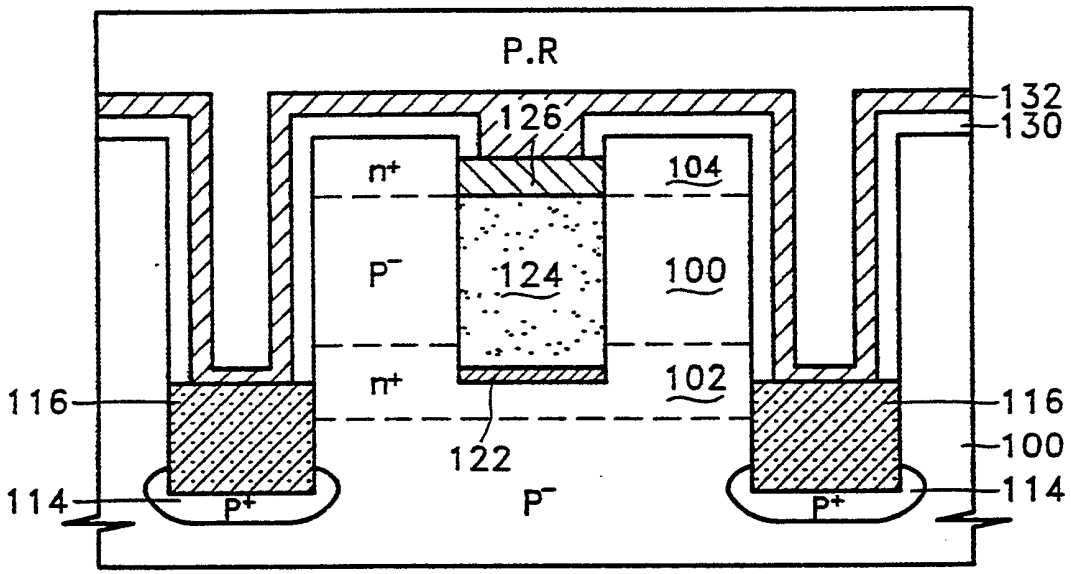


FIG. 23B

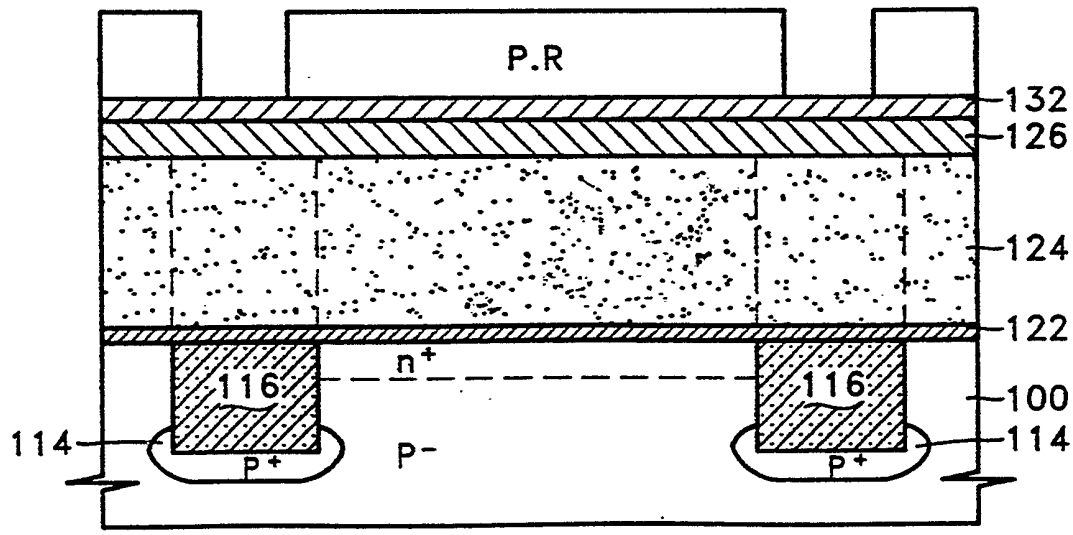


FIG. 24

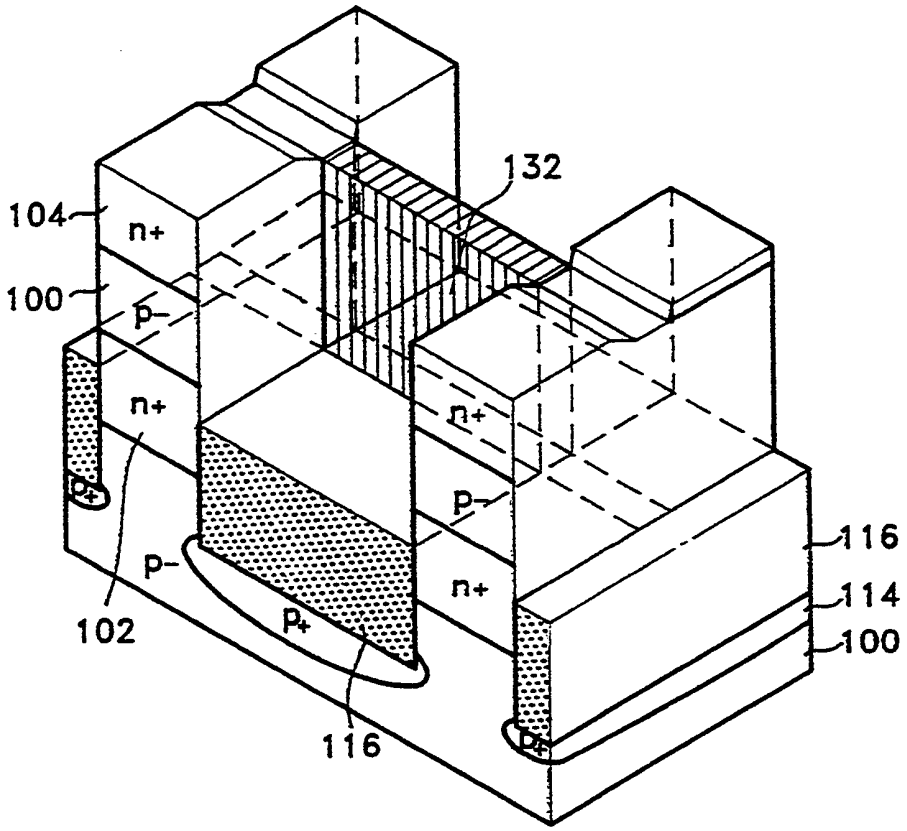


FIG. 25

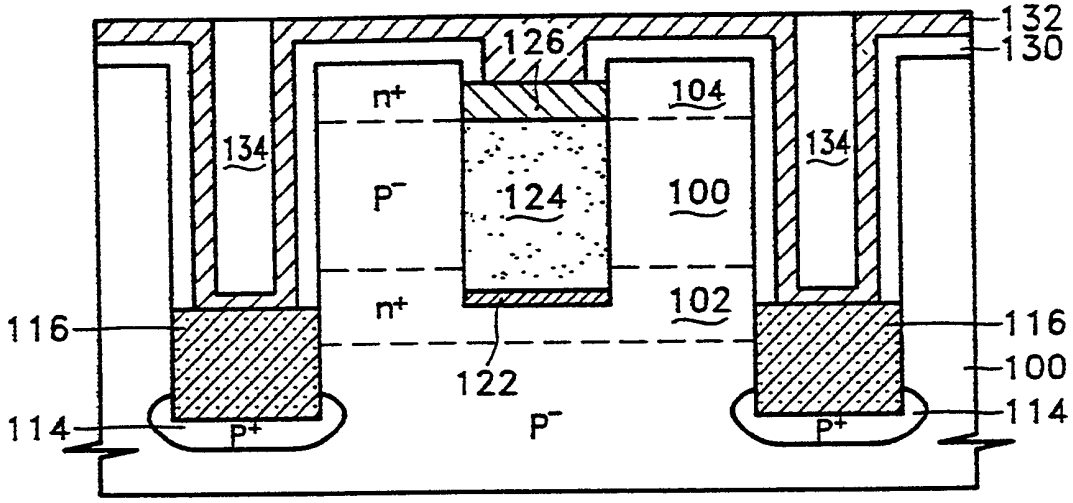
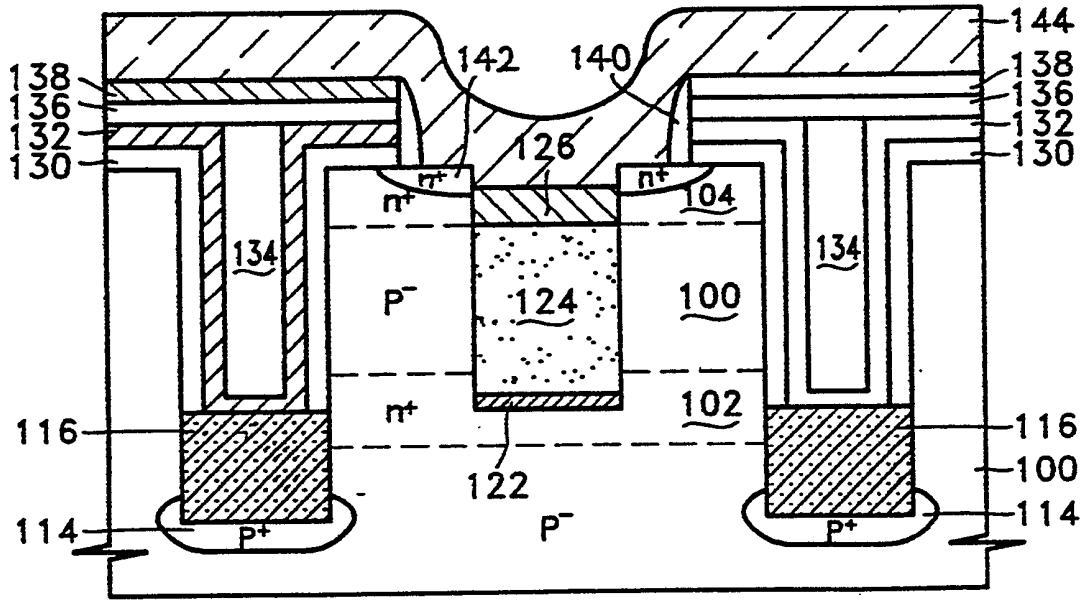

132
130
126
n+
104
134
134
P⁻
124
100
n+
102
116
116
122
100
114
114
P+
P⁻
P+

FIG. 26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138
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136
136
132
132
130
130
126
n+
n+
n+
104
134
134
P⁻
124
100
n+
102
116
116
122
100
114
114
P+
P⁻
P+

SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

The present invention relates to a semiconductor device and a method for manufacturing the same, and more particularly, to a semiconductor device having a buried bit line and a cylindrical gate cell and a method for manufacturing the same.

Integrating the maximum number of devices in the minimum cell area is important for increasing the integration of a semiconductor memory cell, and particularly, of a dynamic random access memory (DRAM) cell.

The memory cell of a one giga bit DRAM cell which is a next generation occupies less than $0.3\mu m^2$ area and is composed of one transistor and one capacitor. This is the same area as previously needed for just the contact hole for interconnection in a one mega bit DRAM cell. Forming one transistor, one capacitor, and one contact hole for interconnection all together in such a small area for constituting a unit cell, is practically impossible.

In most memory cells hitherto incorporated in chips, a transistor, a capacitor and a contact hole are formed laterally on a planar layout, and the total area thereof acts as an element for determining the area of the memory cell. Accordingly, since a transistor, a capacitor, and a contact hole for connection of the source and drain regions are formed in less than a $0.3\mu m^2$ area for constituting a one giga bit memory cell, a three-dimensional cell structure is needed to

overcome area limitations and the cell structure must be altered from a lateral layout into a vertical layout structure.

Also, it is necessary to utilize a maximum effective active area by maximizing the active area by reducing the distance between isolation regions, and by forming the contact hole without the loss of additional active area.

K. Sunouchi et al. suggest a SGT cell wherein all devices for the unit memory cell are formed in one silicon pillar isolated by a matrix-like trench (see IEDM '89, "A Surrounding Gate Transistor (SGT) cell for 64/256Mbit DRAMs").

However, the SGT cell has the following problems.

First, the process of forming the silicon pillar and a capacitor are complex. Secondly, the isolation characteristics are poor. Thirdly, there is a large possibility that a short between a capacitor plate node and a gate electrode occurs during a process for forming the gate electrode.

Accordingly, it is an object of the present invention to provide a highly integrated semiconductor device which enables solution of the problems of the conventional method described above.

It is another object of the present invention to provide a method for manufacturing a highly integrated semiconductor device especially suitable for manufacturing the above semiconductor device.

According to the present invention there is provided a semiconductor device comprising:

a semiconductor substrate;

a trench isolation region formed in order to define an active region in the semiconductor substrate;

a bit line formed on the semiconductor substrate wherein the trench isolation region is formed;

a silicon pillar formed on the bit line, and having a drain, a channel, and a source region of a transistor which are sequentially formed from a lower potion of the silicon pillar to an upper portion thereof;

a gate insulating film and a gate line formed sequentially so as to surround the silicon pillar;

a planarizing layer formed between the adjacent gate lines;

an insulating layer formed on the gate lines, having a contact hole for exposing the source region of the transistor; and

a storage node of a capacitor formed on the insulating layer, being connected to the source region of the transistor through the contact hole.

According to another aspect of the invention there is provided a method for manufacturing a highly integrated semiconductor device comprising the steps of:

forming a trench isolation region in order to define an active region in a semiconductor substrate of a first conductivity type;

forming a bit line on the semiconductor substrate wherein the trench isolation region is formed;

forming an insulating film pillar, composed of a first insulating layer and a second insulating layer stacked on the

first insulating layer, only on the trench isolation region;

forming a silicon pillar wherein a drain, a channel, and a source region of a transistor are formed sequentially from a lower portion of the silicon pillar to an upper porion thereof, on the semiconductor substrate exposed by the insulating film pillar;

removing the second insulating film;

forming a gate insulating film and a gate line sequentially so as to surround the silicon pillar;

depositing an insulating material on the resultant structure wherein the gate line is formed, and etching back the insulating material to thereby form a planarizing layer;

forming an insulating layer on the resultant structure wherein the planarizing layer is formed;

etching the insulating layer partially to thereby form a contact hole to expose the source region in the silicon pillar; and

forming a storage node of a capacitor, being connected to the source region through the contact hole, on the resultant structure wherein the contact hole is formed.

According to the present invention, a buried bit line structure and a vertical gate structure surrounding a silicon pillar are used, and thus, the maximum effective active area can be utilized.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings in which:

FIGs.1A to 10 illustrate a method for manufacturing a

semiconductor device according to an embodiment of the present invention;

FIGs.11 to 17 illustrate a method for manufacturing a semiconductor device according to another embodiment of the present invention, and

FIGs.18 to 26 illustrate a method for manufacturing a semiconductor device according to a further embodiment of the present invention.

FIGs.1A to 1C show steps for forming a trench isolation region 12, wherein FIGs.1B and 1C are cross-sectional views taken along line AA′ and BB′ in FIG.1A, respectively. A nitride is deposited on a first conductivity type, e.g., a p^- type semiconductor substrate 10 and is patterned by a lithographic process, thereby to form a nitride pattern 11 on the region where an active region of semiconductor substrate 10 will be formed. Then, after etching substrate 10 to a predetermined depth using nitride pattern 11 as an etch-mask to thereby form a trench (not shown), p^+ type impurity ions are implanted for strengthening the electrical characteristics between devices, thereby forming a p^+ impurity layer 14 under the bottom region of the trench. Then, an insulating material, e.g., an oxide, is deposited on the entire surface of the substrate 10 wherein the trench is formed and is etched back, so as to fill the interior of the trench with the insulating material, thereby forming trench isolation region 12.

FIGs.2A to 2C show the steps of forming a bit line 18, wherein FIGs.2B and 2C are cross-sectional views taken along line AA′ and BB′ in FIG.2A, respectively. After removing

nitride pattern 11 on the active region, second conductivity type, e.g., n^+ type impurity ions are implanted on the entire surface of the semiconductor substrate 10, thereby to form an n^+ impurity region 16 in the surface of substrate 10. The n^+ impurity region 16 is provided for decreasing contact resistance between a bit line and a drain region of a transistor, which will be formed in a subsequent process. Thereafter, a conductive material, e.g., an impurity-doped polysilicon, is deposited on the substrate 10 wherein n^+ impurity region 16 is formed and is patterned by a lithographic process, thereby to form bit line 18.

FIGs.3A and 3B show the steps of forming an insulating film pillar (I), wherein FIGs.3A and 3B are cross-sectional views taken along line AA′ and BB′ of FIG.2A, respectively. For example, a nitride and an oxide are sequentially deposited on the entire surface of the resultant structure wherein bit line 18 is formed, thereby to form a first insulating film 20 and a second insulating film 22. Then, second insulating film 22 and first insulating film 20 are patterned by a lithographic process, to form insulating film pillar (I).

FIGs.4A to 4D show the steps of forming a drain 23, a channel 24 and a source region 25 of a transistor, wherein FIGs.4B and 4C are cross-sectional views taken along line AA′ and BB′ in FIG.4A, respectively, and FIG.4D is a perspective view taken along the above line BB′. An n^- type first epitaxial semiconductor layer 23 is grown using the semiconductor substrate exposed by insulating film pillar (I) as a seed. Then, a p^- type second epitaxial semiconductor layer 24 and an

n^- type third epitaxial semiconductor layer 25 are sequentially grown on n^- type first epitaxial semiconductor layer 23, to thereby form a silicon pillar. The n^- type first epitaxial semiconductor layer 23 is used as the drain of the nMOS transistor, and p^- type second epitaxial semiconductor layer 24 and n^- type third epitaxial semiconductor layer 25 are used as the channel and the source of the nMOS transistor, respectively. Here, n^- type first epitaxial semiconductor layer 23 serving as the drain region is connected with bit line 18.

A p^- type epitaxial semiconductor layer which will be used as the channel of the nMOS transistor may be grown to the upper portion of the insulating layer pillar (I), using the substrate exposed by insulating layer pillar (I) as a seed. After that, n^- type impurity ions are twice implanted, that is, with a high energy and a low energy, respectively, thereby to form drain 23 and source region 25 on the lower portion and the upper portion of the p^- type epitaxial semiconductor layer, respectively.

Thereafter, second insulating film 22 constituting the insulating film pillar (I) is removed, and the resultant structure is shown in FIG.4D.

FIGs.5A to 5C show the steps of forming a gate insulating film 26 and a gate line 28, wherein FIGs.5B and 5C are cross-sectional view taken along line AA′ and BB′ in FIG.5A, respectively. A thermal oxidation process is performed on the resultant structure wherein the silicon pillar used as drain 23, channel 24, and source 25 of the transistor is formed, thereby to form gate insulating film 26 on the surface of the

silicon pillar. Then, after depositing a conductive layer, e.g., an impurity-doped polysilicon, on the resultant structure wherein gate insulating film 26 is formed, the conductive layer is patterned by a lithographic process, to form gate line 28 surrounding the silicon pillar. At this time, bit line 18 on trench isolation region 12 and gate line 28 are mutually insulated by first insulating film 20.

FIGs.6A and 6B show the steps of forming a planarizing layer 30. After depositing an insulating material on the resultant structure wherein gate line 28 is formed, the insulating material layer is etched back until the top surface of gate line 28 is exposed, thereby to form planarizing layer 30 for control a step-difference due to the silicon pillar.

FIGs.7A and 7B show the steps of forming a contact hole and a first conductive layer 40. Insulating materials, e.g., a high temperature oxide (HTO) and a nitride, are sequentially deposited on the resultant structure wherein planarizing layer 30 is formed, thereby to form a first insulating layer 32 and a second insulating layer 34. At this time, a third insulating layer, e.g., composed of a high temperature oxide, may be formed on second insulating layer 34. Thereafter, second insulating layer 34, first insulating layer 32, gate line 28, and gate insulating film 26 which are stacked on source region 25 of the transistor, are etched by a lithographic process, to thereby form a contact hole (not shown) for exposing source region 25. Then, an insulating material, e.g., a high temperature oxide, is deposited on the resultant structure wherein the contact hole is formed, and is etched thereby to

form an insulating spacer 36 on the side of the contact hole. Here, insulating spacer 36 is provided for preventing an electrical short between gate line 28 and a capacitor storage node which will be formed in a subsequent process. Thereafter, n^+ type impurity ions are implanted on the resultant structure wherein insulating spacer 36, to form an n^+ type plug layer 38 in the upper surface of source region 25. The n^+ type plug layer 38 is provided for decreasing a contact resistance between source region 25 and a storage node which will be formed in subsequent process. Then, a conductive material, e.g., an impurity-doped polysilicon, is deposited on the resultant structure wherein n^+ type plug layer 38 is formed, thereby to form first conductive layer 40.

FIGs.8A and 8B show the steps of forming a material pattern 42 and a second conductive layer 44, wherein FIG.8A is a plan view of the material pattern shown in FIG.8B. A material which has a different etch rate from that of the material constituting first conductive layer 40 with respect to any anisotropic etching process, e.g., a high temperature oxide is deposited to form a material layer (not shown) on the resultant structure wherein first conductive layer 40. Then, the material layer is patterned by a lithographic process, to form material pattern 42. Thereafter, a conductive material, which has a different etch rate from that of the material constituting material pattern 42 and which has the same or a similar etch rate as that of the material constituting first conductive layer 40, e.g., an impurity-doped polysilicon is deposited on the resultant structure wherein material pattern

42 is formed, thereby to form second conductive layer 44.

FIGs.9 and 10 show the steps of forming a storage node 46 of a capacitor. First and second conducting layers 40 and 44 are etched back using material pattern 42 as an etch-mask, thereby to form double cylindrical storage node 46 which is connected to source region 25 of the transistor. Then, material pattern 42 is removed.

FIGs.11 to 17 are plan views and cross-sectional views for illustrating a method for manufacturing a semiconductor device according to another embodiment of the present invention.

FIG.11 shows the steps of forming an n^+ type epitaxial semiconductor layer 52a, and a first and a second material layers 54 and 56. An n^+ type epitaxial semiconductor layer 52a is grown on a p^- type semiconductor substrate 50, using the substrate as a seed. Here, it is obvious that n^+ type epitaxial semiconductor layer 52a may be formed by an ion-implantation process. Then, for example, an oxide and a nitride are sequentially deposited on the resultant structure wherein n^+ type epitaxial semiconductor layer 52a, thereby to form first material layer 54 and second material layer 56. At this time, second material layer 56 must be formed so sufficiently high as the height where the transistor will be formed.

FIGs.12A and 12B show the step of forming a bit line 52 and a trench isolation layer 60. FIG.12B being a cross-sectional view taken along line AA' in FIG.12A. After etching the portion of second and first material layers 56 and 54 where an isolation layer will be formed by a lithographic

process, n^+ type epitaxial semiconductor layer 52a is etched using the remainder second and first material layers 56 and 54 as a mask. Next, substrate 50 is etched to a predetermined depth, thereby forming a trench (not shown). At this time, n^+ type epitaxial semiconductor layer 52a is patterned by the above etching process thereby to form a buried bit line 52, and simultaneously, a trench which will be used as an isolation region is formed. Therefore, an active region and buried bit line 52 are same formed. The active regions in bit line direction (BB′ direction in FIG.12A) are connected without the isolation region.

Thereafter, for strengthening the electrical insulation between the devices, p^+ type impurity ions 57 are implanted on the resultant structure wherein bit line 52 and the trench are formed, thereby to form a p^+ impurity layer 58 under the bottom region of the trench. Then, an insulating material, e.g., an oxide, is deposited on the entire surface of the substrate 50, and is etched back, so as to fill the interior of the trench with the insulating material, thereby forming trench isolation region 60. At this time, the insulating material layer filling trench isolation region 60 is somewhat heightened due to sufficiently high second material layer 56.

FIG.13 shows the steps of forming a drain 62, a channel 64 and a source region 66 of a transistor. After removing first and second material layers 54 and 56, an n^- type first epitaxial semiconductor layer 62 is grown on the semiconductor substrate except trench isolation region 60, using the substrate as a seed. Next, a p^- type second epitaxial

semiconductor layer 64 and an n^- type third epitaxial semiconductor layer 66 are sequentially grown on n^- type first epitaxial semiconductor layer 62, to thereby form a silicon pillar. The n^- type first epitaxial semiconductor layer 62 is used as the drain of the nMOS transistor, and p^- type second epitaxial semiconductor layer 64 and n^- type third epitaxial semiconductor layer 66 are used as the channel and the source of the nMOS transistor, respectively. Here, n^- type first epitaxial semiconductor layer 62 serving as the drain region is connected to n^+ type epitaxial semiconductor layer serving as bit line 52.

Also, a p^- type epitaxial semiconductor layer which will be used as the channel of the nMOS transistor may be grown to the upper portion of the trench isolation region 60, using the substrate except trench isolation region 60 as a seed. After that, n^- type impurity ions are twice implanted, that is, with a high energy and a low energy, respectively, thereby to form drain 62 and source region 66 on the lower portion and the upper portion of the p^- type epitaxial semiconductor layer, respectively.

FIG.14 shows the steps of forming a gate insulating film 68. For exposing the silicon pillar used as drain 62, channel 64, and source 66 of the transistor, the insulating material layer within trench isolation region 60 is etched to drain region 62. Thereafter, a thermal oxidation process is performed on the resultant structure, thereby to form gate insulating film 68 on the surface of the silicon pillar.

FIGs.15A and 15B show the steps of forming a gate line

70, FIG.15A is a cross-sectional view taken along line AA′ of a plan view shown in FIG.15B, and a cross-sectional view shown in FIG.15B is a cross-sectional view taken along line BB′ of the above plan view. After depositing a conductive layer, e.g., an impurity-doped polysilicon, on the resultant structure wherein gate insulating film 68 is formed, the conductive layer, gate insulating film 68 and the silicon pillar are etched by a lithographic process, thereby to form gate line 70 surrounding the silicon pillar. At this time, for insulating each transistors in bit line direction (BB′ direction), the above etching process for forming gate line 70 is progressed to drain region 62 in the silicon pillar.

FIG.16 show the steps of forming a planarizing layer 72. After depositing an insulating material on the resultant structure wherein gate line 70 is formed, the insulating material layer is etched back until the top surface of gate line 70 is exposed, thereby to form planarizing layer 72 for control a step-difference due to the silicon pillar. At this time, planarizing layer 72 completely fills the hole, which was formed during the above etching process for forming gate line.

FIG.17 show the steps of forming a contact hole and a first conductive layer 82. Insulating materials, e.g., a high temperature oxide and a nitride, are sequentially deposited on the resultant structure wherein planarizing layer 72 is formed, thereby to form a first insulating layer 74 and a second insulating layer 76. Thereafter, second insulating layer 76, first insulating layer 74, gate line 70, and gate

insulating film 68 which are stacked on source region 66 of the transistor, are etched by a lithographic process, thereby to form a contact hole (not shown) for exposing source region 66. Then, an insulating material, e.g., a high temperature oxide, is deposited on the resultant structure wherein the contact hole is formed, and is etched to thereby form an insulating spacer 78 on the side of the contact hole. Thereafter, n^+ type impurity ions are implanted on the resultant structure wherein insulating spacer 78 is formed, thereby to form an n^+ type plug layer 80 in the upper surface of source region 66. Then, a conductive material, e.g., an impurity-doped polysilicon, is deposited on the resultant structure wherein n^+ type plug layer 80 is formed, thereby to form first conductive layer 82. Thereafter, though not shown, a process for manufacturing a storage node of a capacitor is completed by the method described with reference to the first embodiment described in connection with Figs. 1A to 10.

According to this embodiment of the present invention, the epitaxial semiconductor layer doped with high concentration is simultaneously used as the active region and the bit line, and the trench isolation region and the silicon pillar can be formed by a single lithographic process, and thus, two lithographic processes are omitted. (According to the first embodiment, after forming the trench isolation region, a lithographic process of forming the insulating film pillar for forming the bit line and the silicon pillar is needed.)

FIGs.18 to 26 are plan views and cross-sectional views

for illustrating a method for manufacturing a semiconductor device according to a further embodiment of the present invention.

FIG.18 shows the steps of forming an n^+ type buried impurity layer 102. An n^+ type first impurity ion 101 is implanted at a high energy on the entire surface of a p^- type semiconductor substrate 100, thereby to form n^+ type buried impurity layer 102 at a predetermined depth of substrate 100. At this time, n^+ type buried impurity layer 102 may be formed by an epitaxial process, and in this case, buried impurity layer 102 is formed on substrate 100.

FIG.19 shows the step of forming an n^+ type surface impurity layer 104. An n^+ type second impurity ion 103 is implanted on the entire surface of substrate 100 wherein n_+ type buried impurity layer 102 is formed, to thereby form n^+ type surface impurity layer 104 in the surface of substrate 100. The n^+ type surface impurity layer 104 is used as a source region of an nMOS transistor, n^+ type buried impurity layer 102 is used as a drain region, and p^- type substrate 100 imposed therebetween is used as a channel region.

Here, in the case where n^+ type buried impurity layer 102 is formed by a epitaxial process as described in connection with FIG.18, a p^- type epitaxial semiconductor layer is grown on n^+ type buried impurity layer 102, and then, an n^+ type epitaxial semiconductor layer is grown thereon, thereby to form n^+ type surface impurity layer 104. Also, n^+ type surface impurity layer 104 may be formed by depositing an n^+ type impurity-doped polysilicon on substrate 100.

FIGs.20A and 20B show the step of forming a trench isolation layer 116. On the resultant structure wherein drain 102, channel 100, and source region 104 are formed, a first oxide film 106, polysilicon film 108, a second oxide film 110, and a nitride film 112 are sequentially formed as a mask layer for forming a trench isolation layer. Thereafter, the mask layer is etched by a lithographic process and substrate 100 is more deeply etched than the drain region 102 using the remainder mask layer as an etch-mask, thereby to form a first trench (not shown). Then, for strengthening the electrical insulation between the devices, p^+ type impurity ions 113 are implanted on the resultant structure wherein the first trench are formed, to thereby form a p^+ impurity layer 114 under the bottom region of the first trench. Thereafter, an insulating material, e.g., an oxide is deposited on the entire surface of the resultant structure, and is etched back to fill the interior of the first trench with the insulating material, thereby forming trench isolation region 116. At this time, the insulating material layer is etched back to first oxide film 106.

FIGs.21A to 21C show the steps of forming a buried bit line 122, and FIGs.21B and 21C are cross-sectional views taken along line AA′ and BB′ in FIG.21A. A predetermined portion of an active region defined by trench isolation region 116 is etched to drain region 102 by a lithographic process, thereby to form a second trench (not shown) for forming a buried bit line. At this time, during the process of etching the second trench, an etch selectivity of a silicon and an oxide filling

trench isolation region 116 must be maintained at 1:1 for preventing an occurrence of a stepped portion in a buried bit line.

Then, n^+ type impurity ions 121 are implanted on the entire surface of the resultant structure wherein the second trench is formed, thereby to form an n^+ type impurity layer (not shown) under the bottom region of the second trench. Thereafter, a conductive material, e.g., an impurity-doped polysilicon is deposited on the resultant structure wherein the second trench is formed, and is etched back to bury bit line 122. Then, an oxide is deposited on the resultant structure wherein bit line 122 is formed, and is etched back to form a first insulating film 124. A nitride is deposited on first insulating film 124 and is etched back to form a second insulating film 126. At this time, nitride film 112 used as the mask layer is removed. Thereafter, an oxide is deposited on the resultant structure and is etched back to form a third insulating film 128. At this time, second oxide film 110 used as the mask layer is removed. Here, the location of second insulating layer 126 composed of a nitride determines thicknesses of bit line 122 and first insulating film 124 during a subsequent process of forming a silicon pillar, and prevents the generation of a gate stringer during a subsequent process of etching a gate line.

FIGs.22A and 22B show the steps of forming a silicon pillar, and FIGs.22A and 22B are cross-sectional views taken along line AA′ and BB′ in FIG.21A. The insulating material layer within trench isolation region 116 is etched to drain

region 102, to thereby form the silicon pillar composed of drain 102, channel 100, and a source 104. At this time, second insulating film 128 is also removed during the above etching process, and polysilicon film 108 used as the mask layer for forming trench isolation region 116 prevents an etching of the substrate region wherein the silicon pillar will be formed. Thereafter, polysilicon film 108 and first oxide film 106 are all removed by a wet etching process.

FIGs.23A and 23B show the steps of forming a gate insulating film 130 and a gate line 132. A thermal oxidation process is performed on the resultant structure wherein the silicon pillar is formed, thereby to form gate insulating film 130 on the surface of the silicon pillar. Then, after depositing a conductive layer, e.g., an impurity-doped polysilicon on the resultant structure wherein gate insulating film 130 is formed, the conductive layer is etched by a lithographic process, thereby to form gate line 132 surrounding the silicon pillar.

FIG.24 is a perspective view showing the resultant structure wherein gate line 132 is formed.

FIG.25 shows the steps of forming a planarizing layer 134. After depositing an insulating material on the resultant structure wherein gate line 132 is formed, the insulating material layer is etched back until the top surface of gate line 132 is exposed, thereby to form planarizing layer 134 for control a step-difference due to the silicon pillar.

FIG.26 show the steps of forming a contact hole and a first conductive layer 144. Insulating materials, e.g., a high

temperature oxide and a nitride, are sequentially deposited on the resultant structure wherein planarizing layer 134 is formed, to thereby form a first insulating layer 136 and a second insulating layer 138. Thereafter, second insulating layer 138, first insulating layer 136, gate line 132, and gate insulating film 130 which are stacked on source region 104 of the transistor, are etched to form a contact hole (not shown) for exposing source region 104. Then, an insulating material, e.g., a high temperature oxide, is deposited on the resultant structure wherein the contact hole is formed, and is etched thereby to form an insulating spacer 140 on the side of the contact hole. Thereafter, n^+ type impurity ions are implanted on the resultant structure wherein insulating spacer 140, thereby to form an n^+ type plug layer 142 in the upper surface of source region 104. Then, a conductive material, e.g., an impurity-doped polysilicon, is deposited on the resultant structure wherein n^+ type plug layer 142 is formed, thereby to form first conductive layer 144. Thereafter, though not shown, a process for manufacturing a storage node of a capacitor is completed by the method described with reference to the first embodiment of Figures 1A to 10.

According to this embodiment of the present invention, the buried bit line and the silicon pillar can be formed without selectively growing an epitaxial semiconductor layer. Also, the contact hole area is reduced due to the buried bit line region located in a center portion of the silicon pillar.

Therefore, according to the present invention described above, a buried bit line structure and a vertical gate

structure surrounding a silicon pillar are formed, and thus, the maximum effective active area can be utilized.

It will be understood by those skilled in the art from the foregoing description of preferred embodiments of the disclosed device that various changes and modifications may be made in the invention without departing from the scope thereof.

CLAIMS:

1. A semiconductor device comprising:

a semiconductor substrate;

a trench isolation region for defining an active region in said semiconductor substrate;

a bit line on said semiconductor substrate wherein said trench isolation region is formed;

a silicon pillar on said bit line, said silicon pillar having drain, channel, and source regions of a transistor sequentially formed from a lower portion of said silicon pillar to an upper portion thereof;

a gate insulating film and a gate line formed sequentially so as to surround said silicon pillar;

a planarizing layer between adjacent gate lines;

an insulating layer on said gate lines, having a contact hole for exposing said source region of the transistor, and

a storage node of a capacitor formed on said insulating layer, being connected to said source region of said transistor through said contact hole.

2. A semiconductor device as claimed in claim 1, wherein said bit line is composed of an epitaxial semiconductor layer.

3. A semiconductor device as claimed in claim 1 or 2, wherein said bit line is formed by the same pattern as that of said active region.

4. A semiconductor device as claimed in any preceding claim, wherein said silicon pillar is composed of an epitaxial semiconductor layer.

5. A semiconductor device comprising:

a semiconductor substrate;

a plurality of first trench isolation regions for defining an active region in said semiconductor substrate;

a silicon pillar between said first trench isolation regions, which is composed of a source, a channel, and a drain of a transistor, sequentially formed from a surface portion of said semiconductor substrate to a bulk thereof;

a second trench formed to said drain region of said silicon pillar so as to connect a side of said silicon pillar;

a bit line formed in a lower portion of said second trench;

an insulating film formed so as to fill the interior of said second trench;

a gate insulating film and a gate line formed sequentially so as to surround another side of said silicon pillar;

a planarizing layer formed between adjacent gate lines;

an insulating layer formed on said gate lines, having a contact hole for exposing said source region of the transistor; and

a storage node of a capacitor formed on said insulating layer, being connected to said source region of said

transistor through said contact hole.

6. A method for manufacturing a semiconductor device comprising the steps of:

forming a trench isolation region in order to define an active region in a semiconductor substrate of a first conductivity type;

forming a bit line on said semiconductor substrate wherein said trench isolation region is formed;

forming an insulating film pillar, composed of a first insulating layer and a second insulating layer stacked on said first insulating layer, only on said trench isolation region;

forming a silicon pillar wherein drain, channel, and source regions of a transistor are formed sequentially from a lower portion of said silicon pillar to an upper porion thereof, on said semiconductor substrate exposed by said insulating film pillar;

removing said second insulating film;

forming a gate insulating film and a gate line sequentially so as to surround said silicon pillar;

depositing an insulating material on the resultant structure wherein said gate line is formed, and etching back said insulating material thereby to form a planarizing layer;

forming an insulating layer on the resultant structure wherein said planarizing layer is formed;

etching said insulating layer partially thereby to form a contact hole for exposing said source region in said silicon pillar; and

forming a storage node of a capacitor, connected to said source region through said contact hole, on the resultant structure wherein said contact hole is formed.

7. A method for manufacturing a semiconductor device as claimed in claim 6, wherein said bit line is composed of an impurity-doped polysilicon layer.

8. A method for manufacturing a semiconductor device as claimed in claim 6, wherein said step of forming said silicon pillar comprising the steps of:

forming a first epitaxial semiconductor layer of a second conductivity type on said semiconductor substrate exposed by said insulating film pillar, which is used as a drain region of a transistor;

forming a second epitaxial semiconductor layer of said first conductivity type on said first epitaxial semiconductor layer, which is used as a channel region of the transistor; and

forming a third epitaxial semiconductor layer of said second conductivity type on said second epitaxial semiconductor layer, which is used as a source region of the transistor.

9. A method for manufacturing a semiconductor device as claimed in claim 6. wherein said step of forming said silicon pillar comprising the steps of:

forming an epitaxial semiconductor layer of said first

conductivity type on said semiconductor substrate exposed by said insulating film pillar;

implanting a first impurity ion of a second conductivity type at a first energy on the resultant structure wherein said epitaxial semiconductor layer is formed, to thereby form a drain region of a transistor in a lower portion of said epitaxial semiconductor layer; and

implanting a second impurity ion of a second conductivity type at a second energy which is lower than said first energy on the resultant structure wherein said drain region is formed, thereby to form a source region of the transistor in an upper portion of said epitaxial semiconductor layer.

10. A method for manufacturing a semiconductor device as claimed in any of claims 6 to 9, wherein said step of forming said storage node of said capacitor comprising the steps of:

forming a first conductive layer on the resultant structure wherein said contact hole is formed;

forming a material pattern on said first conductive layer;

forming a second conductive layer on the resultant structure wherein said material pattern is formed;

etching back said second and first conductive layers; and

removing said material pattern.

11. A method for manufacturing a semiconductor device comprising the steps of:

forming a conductive layer and a material layer

sequentially on a semiconductor substrate of a first conductivity type;

etching said material layer, said conductive layer, and said semiconductor substrate thereby to form a bit line and a trench, simultaneously;

filling the interior of said trench with an insulating material, to form a trench isolation region;

removing said material layer;

forming a silicon pillar wherein drain, channel, and source regions of a transistor are formed sequentially from a lower portion of said silicon pillar to an upper porion thereof, on said semiconductor substrate except said trench isolation region;

etching said insulating material layer within said trench isolation region to said drain region in said silicon pillar;

forming a gate insulating film and a gate line sequentially so as to surround said silicon pillar;

depositing an insulating material on the resultant structure wherein said gate line is formed, and etching back said insulating material to thereby form a planarizing layer;

forming an insulating layer on the resultant structure wherein said planarizing layer is formed;

etching said insulating layer partially to form a contact hole for exposing said source region in said silicon pillar; and

forming a storage node of a capacitor, being connected to said source region through said contact hole, on the resultant structure wherein said contact hole is formed.

12. A method for manufacturing a semiconductor device as claimed in claim 11, wherein said bit line is formed by an epitaxial process.

13. A method for manufacturing a semiconductor device as claimed in claim 11, wherein said step of forming said gate insulating film and said gate line comprises the steps of:

forming a gate insulating film on a surface of said silicon pillar;

forming a conductive layer on the resultant structure wherein said gate insulating film is formed; and

etching said conductive layer, said gate insulating film, and said silicon pillar to said drain region, to form a gate line surrounding said silicon pillar.

14. A method for manufacturing a semiconductor device comprising the steps of:

forming a buried impurity layer of a second conductivity type in a semiconductor substrate of a first conductivity type;

forming a surface impurity layer of said second conductivity type in a surface of said semiconductor substrate wherein said buried impurity layer is formed;

forming a first trench isolation region in order to define an active region in said semiconductor substrate wherein said surface impurity layer is formed;

etching said semiconductor substrate of said active region portion more deeply than said buried impurity layer, to

form a second trench;

forming a bit line in a lower portion of said second trench;

filling the interior of said second trench wherein said bit line is formed, with an insulating material;

etching said first trench isolation region to said buried impurity layer, to form a silicon pillar composed of said buried impurity layer of said second conductivity type, said semiconductor substrate of said first conductivity type, and said surface impurity layer of said second conductivity type;

forming a gate insulating film and a gate line sequentially so as to surround said silicon pillar;

depositing an insulating material on the resultant structure wherein said gate line is formed, and etching back said insulating material to form a planarizing layer;

forming an insulating layer on the resultant structure wherein said planarizing layer is formed;

etching said insulating layer partially to form a contact hole for exposing said surface impurity layer in said silicon pillar; and

forming a storage node of a capacitor, being connected to said surface impurity layer through said contact hole, on the resultant structure wherein said contact hole is formed.

15. A method for manufacturing a semiconductor device as claimed in claim 14, wherein said buried impurity layer and said surface impurity layer of said second conductivity type are formed by an epitaxial process.

16. A method for manufacturing a semiconductor device as claimed in claim 14, wherein said buried impurity layer of said second conductivity type is formed by implanting a first impurity ion of said second conductivity type at a first energy on said semiconductor substrate, and said surface impurity layer of said second conductivity type is formed by implanting a second impurity ion of said second conductivity type at a second energy which is lower than said first energy on said semiconductor substrate.

17. A semiconductor device substantially as herein described with reference to Figs 1A to 10, 11 to 17 and/or 18 to 26 of the accompanying drawings.

18. A method for manufacturing a semiconductor device substantially as herein described with reference to Figs 1A to 10, 11 to 17 and/or 18 to 26 of the accompanying drawings.

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Examiner's report to the Comptroller under Section 17
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Databases (see below)
(i) UK Patent Office collections of GB, EP, WO and US patent specifications.

(ii) ONLINE DATABASE: WPI

Documents considered relevant following a search in respect of Claims :-
1-16

Categories of documents

X: Document indicating lack of novelty or of inventive step.

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A: Document indicating technological background and/or state of the art.

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&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
A	US 5192704	(TEXAS INSTRUMENTS) see whole document	
A	US 5136534	(TEXAS INSTRUMENTS) see whole document	

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