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(56) Documents Cited:
US 20110139961 A1
KR1020160053548
KR1020130056485
KR1020120124559

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Other: **WPI, EPODOC, Patent Fulltext, XPAIP, XPESP, XPIEE, XPI3E, INSPEC, XPIOP, OAC, SPRINGER**

(54) Title of the Invention: **Semiconductor device for light detection**
Abstract Title: **A resistor formed from an anti-reflective coating and overlapping an optical active region of a photodiode**

(57) A semiconductor device 10 for light detection, such as a single photon avalanche diode (SPAD) of a silicon photomultiplier (SiPM), has an anti-reflective coating 30 overlapping an optical active region of a photodiode (such as a doped silicon layer 26). The anti-reflective coating 30 also forms a resistor which is connected to the photodiode (for a passive quenching circuit). Overlapping the resistor with the optical active region may increase the device fill factor. The resistor may be a patterned polysilicon layer with holes 24 filled with silicon oxide (SiO2), having an effective refractive index between that of the polysilicon and silicon oxide. The polysilicon layer may be patterned using a POLY mask of a CMOS process, and the semiconductor device 10 may have a contact stop layer 36 (silicon nitride (Si3N4) or silicon oxynitride (SION)) on the resistor, and a silicon oxide layer 38 on the contact stop layer.

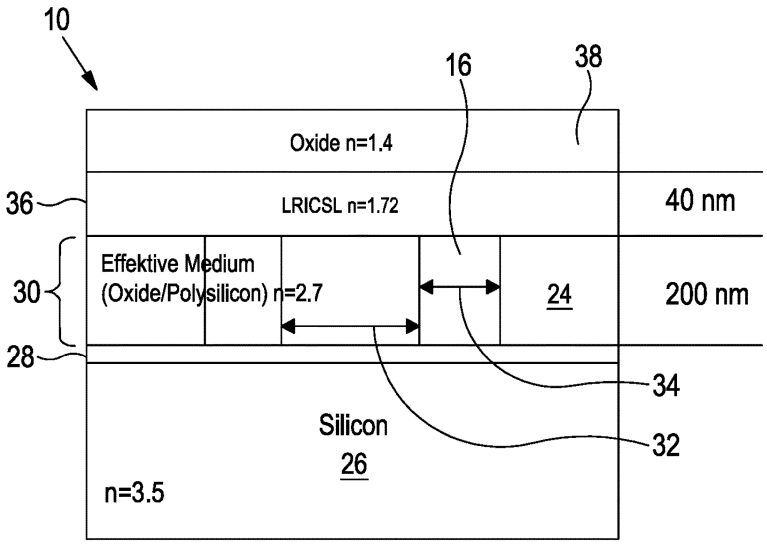

Figure 3

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At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

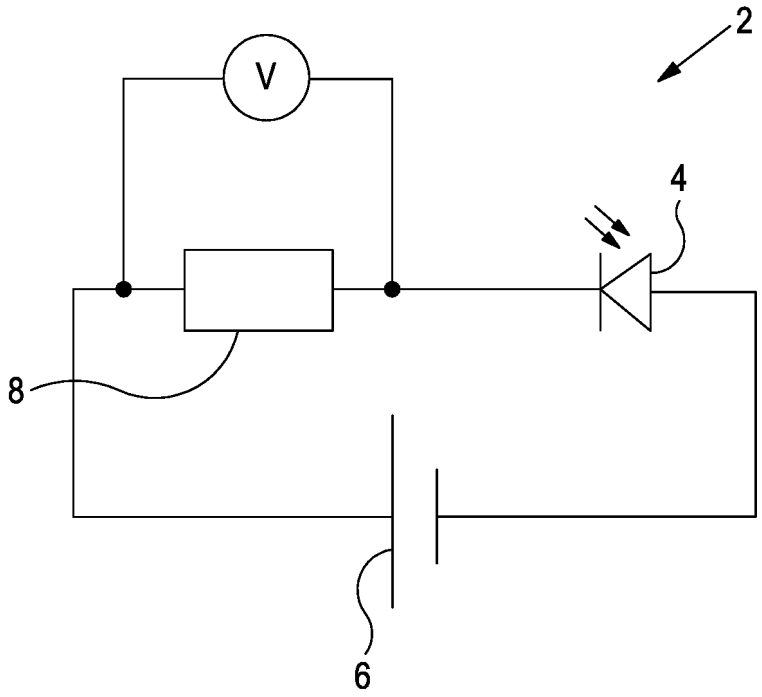

Figure 1

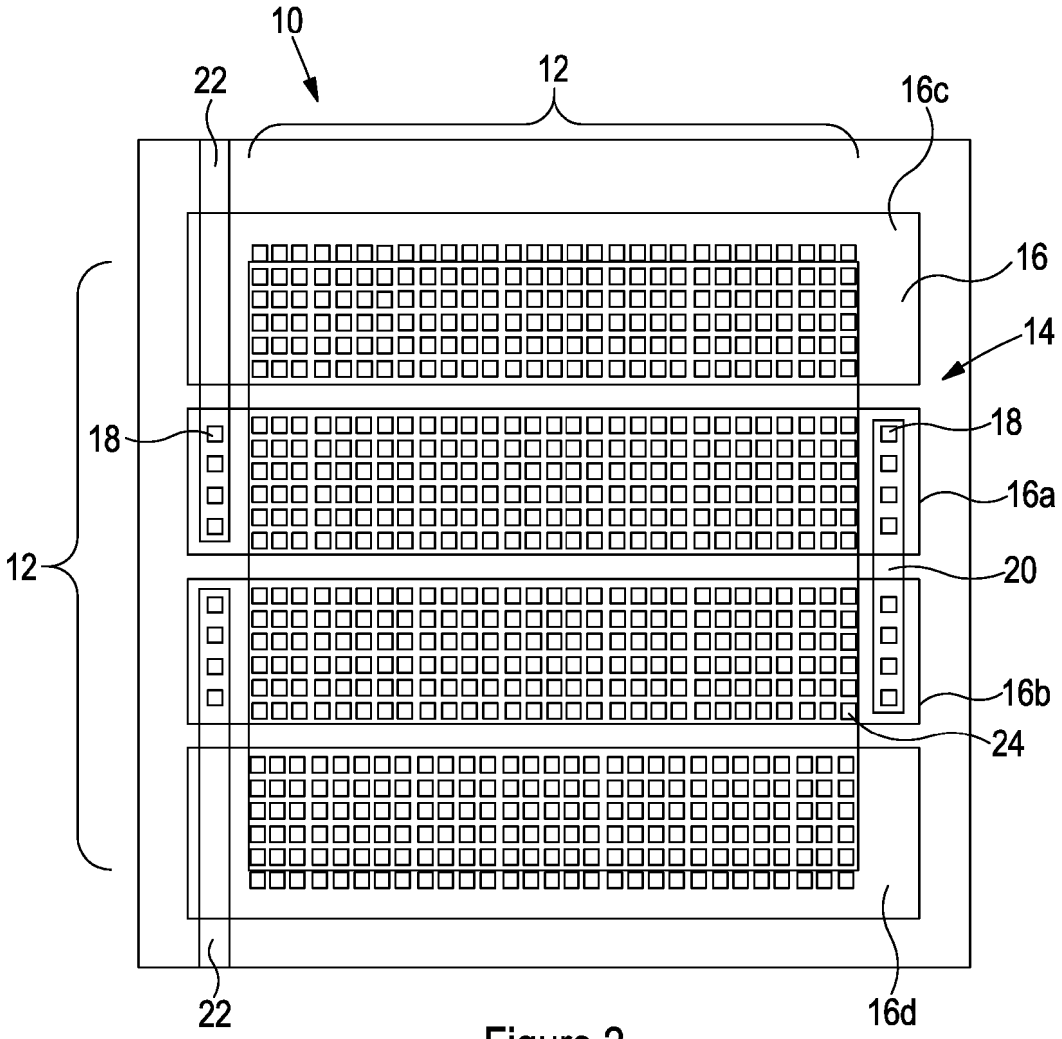

Figure 2

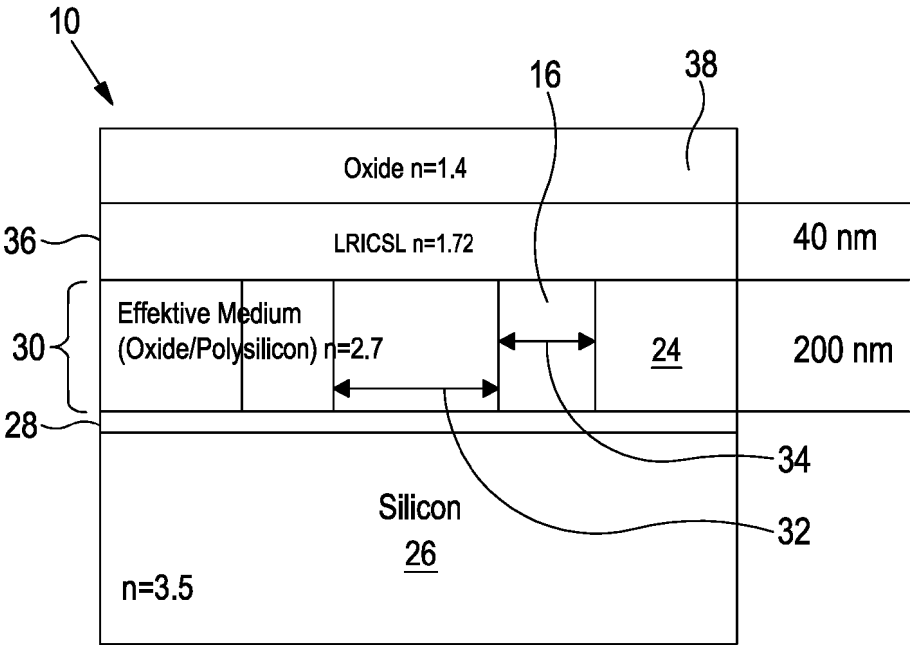

Figure 3

30 08 19

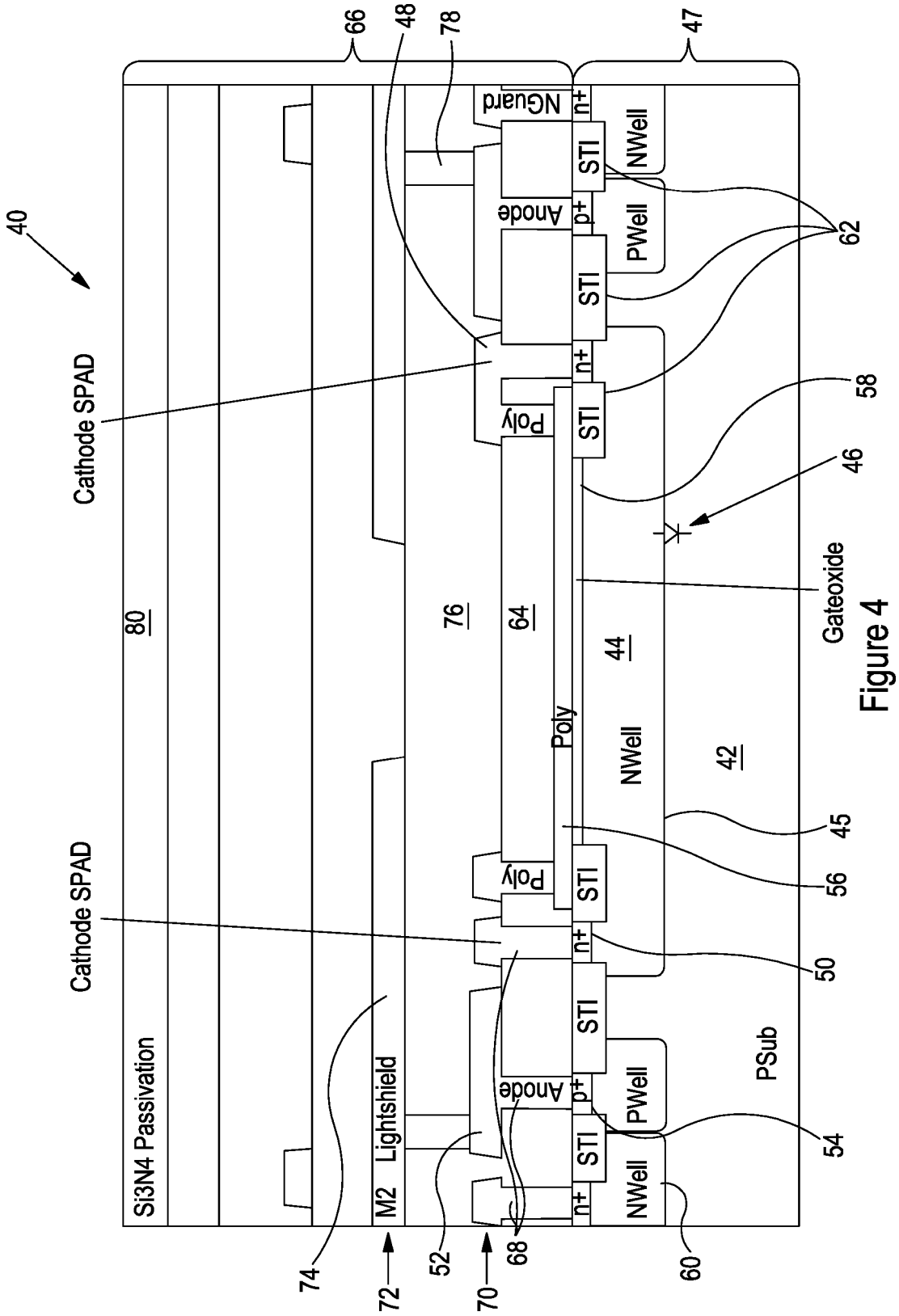

Figure 4

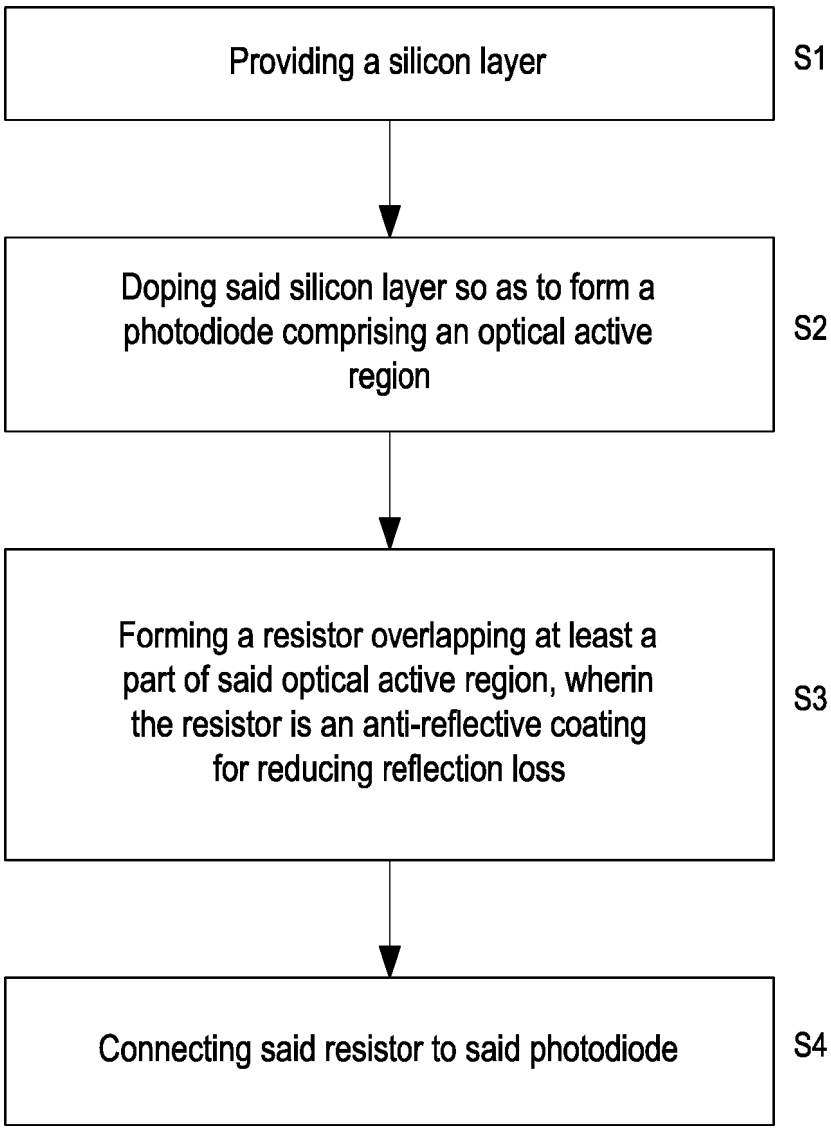

Figure 5

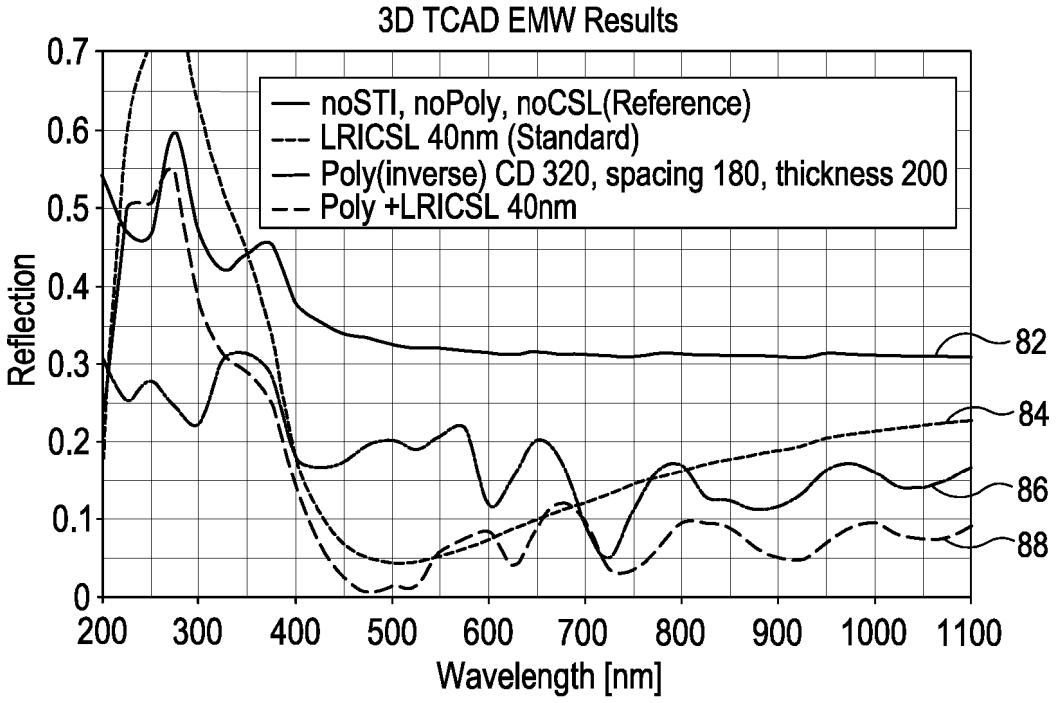

Figure 6

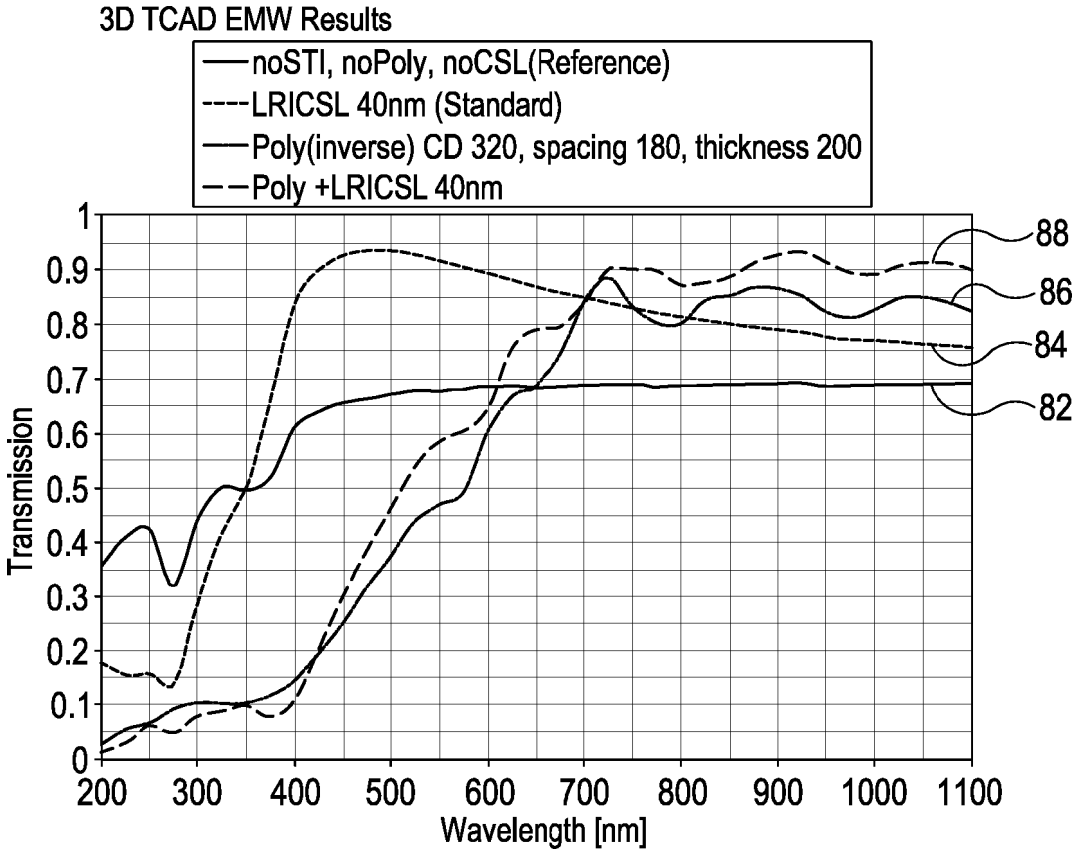

Figure 7

Semiconductor Device for Light Detection

Technical field

The invention concerns a semiconductor device for light detection.

Background

Semiconductor light detectors based on the photodiode are in common use. For example, a Silicon Photomultiplier (SiPM) is used to detect light and comprises an array of individual pixels on a common substrate. Each pixel comprises a photodiode such as Single Photon Avalanche Diode (SPAD).

A SPAD operates by applying a reverse bias that is greater than the breakdown voltage of the diode. A single charge carrier in the depletion region can thereby cause a self-sustaining avalanche through impact ionization, which enables the detection of a single photon.

After the SPAD has been triggered a current will continue to flow until the bias voltage is reduced to the breakdown voltage or below. To reduce the bias voltage, and thereby reset the SPAD, the diode can be loaded with a resistor over which the voltage drops. This is referred to as a Passive Quenching Circuit (PQC). Figure 1 shows a circuit diagram of a passively quenched SPAD device 2 having a photodiode 4, a reverse bias voltage supply 6 and a quenching resistor 8. The voltage drop V across the quenching resistor 8 is measured. The voltage pulse is used as information that an avalanche event has happened. Without an event, the voltage of the source 6 drops nearly completely across the diode 4 (in reverse bias). Passively quenched SPADs require high ohmic resistors, which occupy a significant area and thus lower the fill factor and reduce the sensitivity of such devices. Alternatively, an active quenching circuit can be used, which actively reduces the bias voltage after the SPAD has been triggered.

In a SPAD or other photodiode device, an anti-reflective coating (ARC) may be used over the optical active region to reduce reflection losses, which occur because of the difference in refractive index at the silicon interface. An ARC layer can thus improve the light sensitivity of the device.

European Patent Publication 2040308 describes a photodiode array comprising a plurality of SPADs with passive quenching circuits.

Summary of the invention

Aspects of the present invention provide semiconductor devices for light detection, and methods of forming such, as set out in the accompanying claims.

Preferred embodiments of the invention are described below with reference to the accompanying drawings.

Brief description of the drawings

Figure 1 shows a circuit diagram of a single photon avalanche diode;

Figure 2 shows a schematic diagram of a plan view of a semiconductor device according to an embodiment;

Figure 3 shows a cross section of a semiconductor device according to an embodiment;

Figure 4 shows a cross section of a single photon avalanche diode according to an embodiment;

Figure 5 is a flow diagram illustrating the steps of a method of forming a semiconductor device according to an embodiment;

Figure 6 is a graph showing simulated reflection plotted against wavelength; and

Figure 7 is a graph showing simulated transmission plotted against wavelength.

Detailed description

Embodiments of the invention provide a semiconductor device for light detection having a resistor which is also an anti-reflective coating (ARC). This allows the resistor to overlap the optical active region of the device, without decreasing the light sensitivity of the device. The resistor can have a refractive index between that of silicon and silicon

oxide, so that the refractive index is gradually increased along the path of incident light, thereby reducing the reflection loss at the silicon interface. Because the resistor is located on the optical active region, the "inactive" area around and between such semiconductor devices can be reduced and the fill factor accordingly increased. For example, by positioning the resistor over the optical active region of a SPAD the density of SPADs in an SiPM can be increased.

Figure 2 shows a semiconductor device 10 (e.g. a SPAD) according to an embodiment. The device 10 has an optical active region 12 for absorbing incident photons. The optical active region 12 is the region around the pn-junction (not shown) in the device, within which absorbed photons can excite charge carriers to the conduction band to generate a photocurrent. A resistor 14, having a resistance in the range of 30 kΩ to 150 kΩ, is located on and overlaps the optical active region 12, forming part of an ARC layer. The resistor 14 comprises two strips 16a and 16b of a layer of patterned polysilicon 16 with metal contacts 18. A conductor 20 (typically a metal strip) connects the two strips 16a and 16b of polysilicon layer 16 together. Further conductors 22 can connect the resistor 14 to other devices or to an electrode (not shown). The polysilicon layer 16 comprises a plurality of square holes 24 filled with a dielectric material, typically silicon oxide (SiO_2). The combination of polysilicon and the dielectric material creates an effective medium with a refractive index in between that of the refractive index of the dielectric material and that of polysilicon. For example, silicon oxide has a refractive index of $n = 1.4$ (for light in the visible spectrum, i.e. $300\ nm < \lambda < 750\ nm$) and polysilicon has a refractive index of $n = 3.5$ (for light in the visible spectrum), and the effective medium can be designed to have a refractive index in between these two values ($1.4 < n < 3.5$). The target value of the refractive index will depend on the device application and in particular upon the materials of any other layers in the device. The semiconductor device of Figure 2 comprises further strips 16c and 16d of patterned polysilicon 16, which are a part of the ARC layer, but which are not part of the resistor 14. By using such "dummy elements" along the edges of the optical active region 12 more consistent device behaviour can be achieved.

The polysilicon layer 16 is designed both to provide a desired resistance and a desired refractive index. The density of holes 24 can be increased to increase the ratio of silicon oxide in the layer, which thereby decreases the refractive index of the effective medium. Increasing the amount of oxide will also increase the resistance of the

resistor 14. In this embodiment, the patterned polysilicon layer is used as the resistor 14, so that optical and electrical aspects are used at the same time and at the same location. No extra area is required to position the resistor 14, which would otherwise reduce the fill factor in a pixelated structure.

Preferably, the device 10 is formed in a standard Complementary Metal Oxide Semiconductor (CMOS) process, instead of requiring a dedicated (new) manufacturing process. In a standard CMOS process the polysilicon layer 16 is patterned using the "POLY" mask. In the preferred embodiment, no dedicated process steps have to be introduced to form the resistor 14 and ARC layer. This can make device manufacturing more efficient and significantly reduce those costs normally associated with developing and manufacturing a new device. Embodiments thereby solve the task of coupling light effectively into silicon without the usage of any processing step that is not already part of standard CMOS processing (<= 0.18 µm node). Patterning of fine enough structures to produce an effective medium for wavelengths down to UV is feasible with 0.18 CMOS technology. POLY (inverse): CD 250 nm, spacing 180 nm.

If the semiconductor device 10 is a CMOS device, then the minimum dimensions of the holes 24 in the patterned polysilicon layer 16 are limited by the CMOS process. For example, forming the holes 24 using the "POLY" mask with 0.18 µm CMOS technology, the width of the squares is limited to a minimum of about 250 nm (the Critical Dimension, CD) and the spacing between neighbouring squares is limited to a minimum of about 180 nm. Similarly, for 90 nm CMOS technology, a hole spacing of 90 nm can be achieved. As a consequence, light having a wavelength comparable or smaller to the dimensions of the pattern will not see an effective medium, but will instead see individual regions of dielectric material and polysilicon respectively. Using a dedicated, non-CMOS process, to form the device can remove this disadvantage and provide more design freedom. However, it has been discovered that even for incident light having a wavelength close to or less than the CD, the patterned polysilicon layer can significantly reduce reflection. Although generally smaller holes 24 with smaller spacing is preferable to reduce the granularity of the effective medium, for IR applications holes 24 having a width of up to 700 nm and a spacing of up to 300 nm may be used.

Although Figure 2 shows a polysilicon layer having square holes 24, hexagonal or round shapes are preferable in some applications. For example, having hexagonal holes may allow a greater packing ratio and thereby a greater ratio of silicon oxide, if the application requires a lower refractive index. Computer modelling and simulations may preferably be used to determine the optimal design of the polysilicon layer for a particular application. Hence, the thickness of the polysilicon layer and the shape and size of the holes can be chosen so as to form a resistor with a target resistance and a target refractive index.

In some CMOS processes there may be a Contact Stop Layer (CSL). This layer is a silicon nitride (Si_3N_4) or silicon oxynitride (SION) layer, which has a higher refractive index than silicon oxide. The CSL is needed for the contact etch to stop before reaching the silicon (or more precisely the silicide) and then to change the etching process for a soft landing. As a side effect the higher refractive index of this layer, reduces the difference towards the underlying silicon (Si_3N_4 n = 2 to Si n = 3.8 -> 1.8, vs. SiO_2 n = 1.4 to Si n = 3.8 -> 2.4). With such a layer the reflection at the silicon interface can be significantly reduced. With an appropriate thickness of the CSL the reflection at a certain wavelength can be reduced to values below 5% even without an ARC layer.

Figure 3 shows a cross-section of a semiconductor device 10 according to an embodiment. For ease of understanding, features similar to those of the semiconductor device of Figure 2 have been given the same reference numerals in Figure 3. The device 10 comprises a silicon layer 26, which is doped so as to form a photodiode with a pn-junction (not shown). A patterned polysilicon layer 16, having a thickness of 200 nm, is located on the silicon layer 26, with a gate oxide layer 28 in between. The polysilicon layer 16 forms part of a resistor, such as the resistor 14 of the device 10 in Figure 2. The holes 24 in the polysilicon layer 16 extend through the whole thickness of the polysilicon layer 16, and are filled with silicon oxide. The polysilicon and the oxide filled holes 24 from an effective medium 30 having a refractive index n = 2.7. The holes 24 have a width 32 (e.g. 250 nm) and a spacing 34 (e.g. 180 nm) between adjacent holes 24, to produce the desired refractive index. A 40 nm thick CSL 36 is formed on the patterned polysilicon layer 16. The CSL 36 has a refractive index of n = 1.72, which further reduces the difference in refractive index between adjacent layers in the light path. On top of the CSL 36 is an oxide layer 38

(having a refractive index of 1.4, as discussed above), which may be one of the normal oxide isolation layers formed in a CMOS backend process. The finished device 10 may comprise a number of metal layers (not shown) as well as further oxide layers (not shown).

Embodiments described herein may be particularly advantageous for use in the infrared (IR) wavelength spectrum (typically 700 nm < λ < 1 mm). For IR light there is little to no absorption in the polysilicon layer, so a patterned resistor can be placed directly on top of the optical active region and does not require any additional space. In a passively quenched SPAD, this means that the resistor does not limit the fill factor and would thereby improve the light coupling into the SPAD.

The resistor and ARC layer is separated from the doped silicon by a gate oxide layer (as seen in Figure 3). The voltage swing between the SPAD doping underneath the resistor and the resistor should be smaller than the gate oxide breakdown voltage (e.g. 3.3 V). The resistor is tied with one end to the SPAD device and must quench the avalanche current. This is done by causing a voltage drop across the resistor, which is big enough to reduce the voltage in the SPAD below breakdown. Hence, there is a potential difference between the doped Silicon (anode or cathode) of the SPAD and the quenching resistor. Both are isolated from each other by the gate oxide. This gate oxide has a limit in its voltage capabilities. For example, if the “POLY” of a CMOS process with a 3.3 V gate oxide is used, then the polysilicon resistor voltage difference to the voltage at the uppermost doping of the SPAD, must be smaller than the 3.3. V breakdown limit of the gate oxide. Otherwise there would be a leakage path from the resistor through the gate oxide into the SPAD and the device would not function properly.

Figure 4 shows a cross-section of a lateral SPAD device 40 according to an embodiment. The device 40 is a CMOS device and comprises a p-substrate 42 and an n-well 44 forming a pn-junction 45 and photodiode 46 in the silicon layer 47. A metal contact 48 connects to a heavily doped n+ region 50 in the n-well 44. Another metal contact 52 connects to a heavily doped p+ region 54. In use, a reverse bias voltage is applied to the photodiode 46 by connecting the metal contacts 48 and 52 so that the first metal contact 48 becomes the cathode and the other metal contact 52 becomes the anode of the device 40. The cathode 48 is also connected to a patterned polysilicon resistor 56 overlapping the pn-junction 45 between the p-substrate 42 and

the n-well 44. The resistor 56 is an anti-reflective coating (ARC) layer, which overlaps the optical active region of the photodiode 46 defined by the pn-junction 45. A gate oxide layer 58 isolates the resistor 56 from the n-well 44. An n-well guard ring 60 is used to isolate the SPAD device 40 from other CMOS components (not shown) such as adjacent SPADs in a SiPM. Shallow trench isolation (STI) trenches 62 isolate heavily doped regions in the silicon layer 47 from each other to improve breakdown performance. A first oxide isolation layer 64 of the CMOS backend stack 66 is located on the silicon layer 47 and on the patterned polysilicon resistor 56. Vias 68 connect the doped regions of the silicon layer 47 to the first metal layer 70 of the backend stack 66. The backend stack 66 comprises a second metal layer 72 with a light shield 74. The first and second metal layers 70 and 72 are separated by a second oxide isolation layer 76 and connected by vias 78. The backend stack 66 comprises a silicon nitride (Si_3N_4) passivation layer 80 on top, which protects the underlying layers.

Figure 5 is a flow diagram illustrating the steps of a method of forming a semiconductor device, such as the SPAD device 40 shown in Figure 4. The method comprises providing a silicon layer (step S1), doping said silicon layer to form a photodiode having an optical active region (step S2), forming a resistor overlapping at least a part of said optical active region, wherein the resistor is an anti-reflective coating for reducing reflection loss (step S3), and connecting said resistor to said photodiode (step S4). In one embodiment, the step of forming the resistor (step S4) comprises depositing a polysilicon layer, patterning said polysilicon layer to form a plurality of holes extending through said polysilicon layer, and filling said holes with dielectric material (e.g. SiO_2) so that the resistor comprises an effective medium having a refractive index between 1.4 and 3.5 (for light in the visible spectrum). Preferably, the method is performed as part of a standard CMOS process, and the polysilicon layer is patterned using the "POLY" mask of the CMOS process.

Figure 6 shows the simulated reflection coefficient plotted against wavelength for different semiconductor structures 82, 84, 86 and 88. 3D simulation with Synopsys EMW (Electromagnetic Wave Solver) was used. The reflection coefficient for the case of no matching layers 82 and for a 40 nm CSL 84 are plotted for comparison. The CSL 84 already acts quite well as an ARC layer, but is strongly wavelength dependent and not optimal for IR. In the case of a patterned polysilicon layer 86, the reflection is reduced very well across the whole wavelength range, especially in the red/IR

wavelength region. In the blue/UV range the absorption in polysilicon reduces the positive effect, but still allows use of the patterned polysilicon resistor in the optical path. The light is not completely blocked by the patterned polysilicon resistor, which it would have been by a conventional, continuous, polysilicon resistor. In the case of a patterned polysilicon layer combined with a CSL 88, the device performs very well in the red/IR region, but the reflection coefficient is greater than that of patterned polysilicon without CSL 86 for wavelengths below 330 nm.

Figure 7 shows the simulated transmission coefficient plotted against wavelength for different semiconductor structures 82, 84, 86 and 88. The transmission coefficient for the case of no matching layers 82 and for a 40 nm CSL 84 are plotted for comparison. In general, for both patterned polysilicon 86 and for patterned polysilicon combined with a CSL 88 the transmission performance at low wavelengths is reduced due to absorption, but good performance is achieved for IR. The transmission into silicon proves that a gain of 15 % should be achievable and without requiring modification of the CSL. There is still one oxide to air interface in both structures 86 and 88, which causes 3.5 % reflection, so the reflection at the silicon interface is actually as low as 4 %.

While specific embodiments of the invention have been described above, it will be appreciated that the invention may be practiced otherwise than as described. The descriptions above are intended to be illustrative, not limiting. It will be apparent to one skilled in the art that modifications may be made to the invention as described without departing from the scope of the claims set out below.

Each feature disclosed or illustrated in the present specification may be incorporated in the invention, whether alone or in any appropriate combination with any other feature disclosed or illustrated herein.

CLAIMS:

1. A semiconductor device for light detection comprising:

a photodiode comprising an optical active region; and

a resistor connected to said photodiode and overlapping at least a part of said optical active region, wherein the resistor is formed from an anti-reflective coating for reducing reflection loss.

2. A semiconductor device according to claim 1, wherein said resistor comprises an effective medium having a refractive index between 1.4 and 3.5 for light in the visible spectrum.

3. A semiconductor device according to claim 1 or 2, wherein said resistor has a resistance in the range of 30 kΩ to 150 kΩ.

4. A semiconductor device according to claim 1, 2 or 3, wherein said resistor comprises a patterned polysilicon layer comprising a plurality of holes.

5. A semiconductor device according to claim 4, wherein said holes have a width in the range of 200 nm to 700 nm, and wherein a spacing between neighbouring holes is in the range of 90 nm and 300 nm.

6. A semiconductor layer according to claim 4 or 5, wherein said polysilicon layer has a thickness in the range of 100 nm and 350 nm.

7. A semiconductor device according to claim 4, 5 or 6, wherein said holes are filled with silicon oxide (SiO_2).

8. A semiconductor device according to any one of claims 4 to 7, wherein said holes are one of square, round and hexagonal.

9. A semiconductor device according to any preceding claim, further comprising a contact stop layer comprising silicon nitride (Si_3N_4) or silicon oxynitride (SION) located on said resistor, and a silicon oxide layer located on said contact stop layer.

10. A semiconductor device according to any preceding claim, wherein said semiconductor device is a Single Photon Avalanche Diode (SPAD).

11. A semiconductor device according to claim 10, wherein said resistor is configured to quench an avalanche current in the photodiode when in use.

12. A silicon photomultiplier (SiPM) comprising an array of a plurality of the semiconductor device of any of claims 1 to 11.

13. A method of forming a semiconductor device for light detection, the method comprising:

providing a silicon layer;

doping said silicon layer so as to form a photodiode comprising an optical active region;

forming a resistor overlapping at least a part of said optical active region, wherein the resistor is formed from an anti-reflective coating for reducing reflection loss; and

connecting said resistor to said photodiode.

14. A method according to claim 13, wherein said step of forming said resistor comprises:

depositing a polysilicon layer;

patterning said polysilicon layer to form a plurality of holes extending through said polysilicon layer; and

filling said holes with silicon oxide (SiO_2) so that the resistor comprises an effective medium having a refractive index between 1.4 and 3.5 for light in the visible spectrum.

15. A method according to claim 14, wherein said method is performed as part of a standard Complementary Metal Oxide Semiconductor (CMOS) process, and wherein said step of patterning said polysilicon layer comprises using the “POLY” mask of the CMOS process.

16. A method according to claim 13, 14 or 15, further comprising designing said resistor to have a target resistance and a target refractive index.

Amendments to the pages have been filed as follows:

CLAIMS:

1. A semiconductor device for light detection comprising:
a photodiode comprising an optical active region; and
a resistor connected to said photodiode and overlapping at least a part of said optical active region, wherein the resistor comprises an anti-reflective coating for reducing reflection loss.

2. A semiconductor device according to claim 1, wherein said resistor comprises an effective medium having a refractive index between 1.4 and 3.5 for light in the visible spectrum.

3. A semiconductor device according to claim 1 or 2, wherein said resistor has a resistance in the range of 30 kΩ to 150 kΩ.

4. A semiconductor device according to claim 1, 2 or 3, wherein said resistor comprises a patterned polysilicon layer comprising a plurality of holes.

5. A semiconductor device according to claim 4, wherein said holes have a width in the range of 200 nm to 700 nm, and wherein a spacing between neighbouring holes is in the range of 90 nm and 300 nm.

6. A semiconductor layer according to claim 4 or 5, wherein said polysilicon layer has a thickness in the range of 100 nm and 350 nm.

7. A semiconductor device according to claim 4, 5 or 6, wherein said holes are filled with silicon oxide (SiO_2).

8. A semiconductor device according to any one of claims 4 to 7, wherein said holes are one of square, round and hexagonal.

9. A semiconductor device according to any preceding claim, further comprising a contact stop layer comprising silicon nitride (Si_3N_4) or silicon oxynitride (SION) located on said resistor, and a silicon oxide layer located on said contact stop layer.

10. A semiconductor device according to any preceding claim, wherein said semiconductor device is a Single Photon Avalanche Diode (SPAD).

11. A semiconductor device according to claim 10, wherein said resistor is configured to quench an avalanche current in the photodiode when in use.

12. A silicon photomultiplier (SiPM) comprising an array of a plurality of the semiconductor device of any of claims 1 to 11.

13. A method of forming a semiconductor device for light detection, the method comprising:

providing a silicon layer;

doping said silicon layer so as to form a photodiode comprising an optical active region;

forming a resistor overlapping at least a part of said optical active region, wherein the resistor is formed from an anti-reflective coating for reducing reflection loss; and

connecting said resistor to said photodiode.

14. A method according to claim 13, wherein said step of forming said resistor comprises:

depositing a polysilicon layer;

patterning said polysilicon layer to form a plurality of holes extending through said polysilicon layer; and

filling said holes with silicon oxide (SiO_2) so that the resistor comprises an effective medium having a refractive index between 1.4 and 3.5 for light in the visible spectrum.

15. A method according to claim 14, wherein said method is performed as part of a standard Complementary Metal Oxide Semiconductor (CMOS) process, and wherein said step of patterning said polysilicon layer comprises using the “POLY” mask of the CMOS process.

16. A method according to claim 13, 14 or 15, further comprising designing said resistor to have a target resistance and a target refractive index.

Intellectual Property Office

Application No:	GB1905789.2	**Examiner:**	Dr Gareth W John
Claims searched:	1-16	**Date of search:**	7 October 2019

Patents Act 1977: Search Report under Section 17

Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
A	-	US2011/0139961 A1 (An et al.) See figure 3 and paragraphs 0047-0049.
A	-	KR1020160053548 A (UNIV SUNGKYUNKWAN) See paragraphs 0029 and 0052.
A	-	KR1020120124559 A (KOREA ADV INST SCI&TECHNOLOGY) See figure 3 and paragraphs 0026-0029.
A	-	KR1020130056485 A (LG INNOTEK) See the anti-reflection pattern 500 in figures 2 and 3.

Categories:

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
&	Member of the same patent family	E	Patent document published on or after, but with priority date earlier than, the filing date of this application.

Field of Search:

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Worldwide search of patent documents classified in the following areas of the IPC

H01L

The following online and other databases have been used in the preparation of this search report

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Intellectual Property Office

International Classification:

Subclass	Subgroup	Valid From
H01L	0027/146	01/01/2006
H01L	0031/0216	01/01/2014
H01L	0027/146	01/01/2006
H01L	0031/107	01/01/2006