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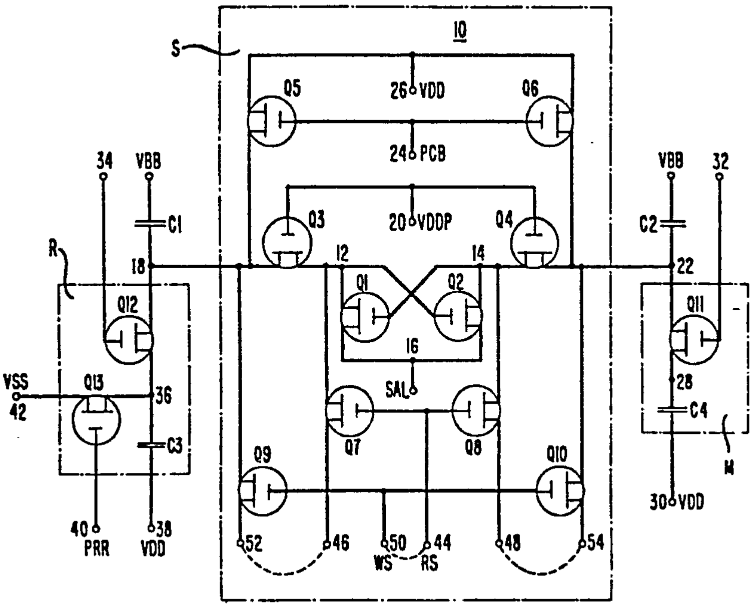

(57) Abstract

An improved field effect transistor sense amplifier uses a cross-coupled pair of first transistors (Q1, Q2) with separate third and fourth transistors (Q3, Q4) connected by the sources to each of one of cross-coupled terminals (12, 14) of the cross-coupled pair (Q1, Q2). Read circuitry (Q7, Q8) is connected directly to the cross-coupled terminals (12, 14) of the cross-coupled pair. Write circuitry (Q9, Q10) is connected to the drains (18, 22) of the third and fourth transistors (Q3, Q4). The improved digital sense amplifier circuit reduces memory access and cycle times and reduces the magnitude of current spikes.

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SENSE AMPLIFIER

Background of the Invention

This invention relates to memory circuitry and, in particular, to improved latching-type sense amplifiers suitable for use with random access memory (RAM) systems.

Latching-type sense amplifiers have been used in dynamic semiconductor memories such as are described in articles entitled "VMOS Technology Applied to Dynamic RAM's" by Kurt Hoffmann and Reinhard Losehand (Fig. 2), and "An 8 mm^2, 5 V 16K Dynamic RAM Using a New Memory Cell" by Gunther Meusburger, Karlheinrich Horninger, and Gerold Lindert (Fig. 2(a)), which appear in the IEEE Journal of Solid-State Circuits, Volume SC-13, No. 5, October 1978, at pages 617-622 and 708-711, respectively. These sense amplifiers consist essentially of first and second cross-coupled transistors and of third and fourth transistors whose drain-source output circuitry couples the cross-coupled pair of transistors to bit lines of the memory. The third and fourth transistors act as buffers between the bit lines, which have relatively heavy capacitance associated therewith, and the cross-coupled pair of transistors. Read/write circuits, which are also denoted as input/output (I/O) circuits, are connected directly to the bit lines or directly to the cross-coupled pair. The third and fourth transistors are either biased so as to make them continuously on during all cycles of the memory or are biased on during only selected portions of the memory cycle. The sense amplifiers described hereinabove tend to provide either slower memory access or cycle time than is desirable and they may incur high current spikes that can cause inaccuracies or reductions in memory operating margins.

It would be desirable to have a sense amplifier that facilitates relatively fast semiconductor memory access and cycle times and which reduces the magnitude of current spikes.

Summary of the Invention

A solution to the above-described problems is achieved with digital sense circuitry comprising a cross-coupled circuit (Q1, Q2) having first (12) and second (14) terminals, read/write circuits (Q7, Q8, Q9, Q10), and first (Q3) and second (Q4) switching-type devices which each have a control terminal and first and second output terminals. The first terminal (12) of the cross-coupled circuit (Q1, Q2) is connected to the first output terminal of the first switching-type device (Q3). The second terminal (14) of the cross-coupled circuit is connected to the first output terminal of the second switching-type device (Q4). The circuitry is characterized in that the read/write circuits (Q7, Q8, Q9, Q10) comprise separate first (Q7) and second (Q8) read circuits and separate first (Q9) and second (Q10) write circuits. The circuitry is further characterized in that the first (Q7) and second (Q8) read circuits are connected to the first (12) and second (14) terminals, respectively, of the cross-coupled circuit (Q1, Q2) and in that the first (Q9) and second (Q10) write circuits are connected to the second output terminal (18) of the first device (Q3) and to the second output terminal (22) of the second device (Q4), respectively.

In one illustrative embodiment of the present circuitry the cross-coupled circuit comprises two n-channel field effect transistors with the gate of each connected to the drain of the other and to one of the first and second terminals of the cross-coupled circuit. The first and second switching-type devices, which may be denoted as buffer devices or transistors, are also n-channel field effect transistors. Each of the read and write circuits comprises a separate n-channel field effect transistor. The drain of the first read transistor is connected to the first terminal of the cross-coupled circuit and the drain of the second read transistor is connected to the second terminal of the cross-coupled circuit. The source of the first write transistor is connected to the drain of the first transistor and the source of the second write transistor is coupled to the drain of the second transistor. It is to be noted that the direction of current flow through a field effect transistor determines which output terminal is denoted as the source or the drain. As the current flow reverses, this designation also reverses.

In one typical application separate bit lines of a memory system are connected directly to the drains (18, 22) of the first and second buffer transistors of the above-described circuitry. Each bit line has at least one memory cell and/or a reference memory cell connected thereto. The first and second buffer transistors (Q3, Q4) are biased so as to be in the conductive state. They are designed to have relatively high impedance such that the capacitance associated with each bit line is buffered from the first and second terminals of the cross-coupled circuitry. The direct connection of the read circuits to the first and second terminals (12, 14) of the cross-coupled circuit facilitates a relatively rapid read operation because read out can occur as soon as the cross-coupled circuit has latched to the proper state. Thus the read out operation need not wait until the potentials of the bit lines change as they will after an appropriate delay which is a function of the resistance of the first and second transistors and the capacitance associated with the respective bit lines. The direct connection of the write circuits to the same terminals (18, 22) as are connected to the bit lines facilitates a rapid write operation. The use of relatively high impedance first and second transistors, as well as their operation in the conductive state during the entire cycle, tends to decrease the magnitude of current spikes. This tends to increase operating noise margins of the memory system and reduce inaccuracies.

Brief Description of the Drawing

FIG. 1 illustrates a sense amplifier in accordance with an embodiment of the invention; and

FIG. 2 illustrates circuitry which can be used in conjunction with the sense amplifier of FIG. 1.

Detailed Description

Referring now to FIG. 1, there is illustrated within dashed line rectangle S a sense amplifier 10 which comprises field effect transistors Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, and Q10. Connected to one side of sense amplifier 10 at a first outer terminal 22 is a switched capacitor memory cell (illustrated within dashed line rectangle M) which comprises a field effect transistor Q11 and a capacitor C4. Connected to the other side at a second outer terminal 18 is a reference memory cell (illustrated within dashed line rectangle R) which comprises field effect transistors Q12 and Q13 and capacitor C3. Memory cell M is connected by the source of Q11 to terminal 22 which has a capacitor C2 connected thereto. Reference memory cell R is connected by the source of Q12 to terminal 18 which has a capacitor C1 connected thereto. Gate terminal 32 is typically coupled to a word line of a semiconductor memory and terminal 22 is coupled to a bit line of the game memory. C1 and C2 represent the parasitic capacitances of all devices and lines connected to terminals 18 and 22, respectively. C1 and C2 are illustrated connected to a potential VBB which represents the potential of a semiconductor body (substrate) in which sense amplifier 10 and memory cell M and reference memory cell R are fabricated.

Sense amplifier 10 senses the logic information stored in memory cell M, provides refresh, and facilitates a rapid reading out and writing in of information while avoiding large current peaks.

The gate of Q2 is connected to the drain of Q1, the source of Q3, the drain of Q7, and to a first inner terminal 12. The gate of Q1 is connected to the drain of Q2, the source of Q4, the drain of Q8, and to a second inner terminal 14. The combination of Q1 and Q2 is known in the art as a cross-coupled pair, a cross-coupled circuit, or a flip-flop. The sources of Q1 and Q2 are connected together to a terminal 16 and to a voltage pulse generator denoted as SAL. One embodiment of SAL is illustrated in FIG. 2 as circuit 58. Q7 and Q8 facilitate the rapid read out of information appearing on inner or readout terminals 12 and 14, respectively. They may be denoted as read circuits or read circuitry. The gates of Q7 and Q8 are connected together to a terminal 44 and to a voltage pulse generator RS. The sources of Q7 and Q8 are connected to terminals 46 and 48, respectively. Terminals 46 and 48 serve as complementary read output terminals.

The drain of Q3 is connected to terminal 18, the source of Q9, and to the source of Q5. The drain of Q4 is connected to terminal 22, the source of Q6, and to the source of Q10. Q9 and Q10 facilitate the rapid writing in of information (data) into memory cells connected to the outer or write in terminals 18 and 22, respectively. They may be denoted as write circuits or write circuitry. The gates of Q9 and Q10 are coupled together to a terminal 50 and to a voltage pulse generator WS. The drains of Q9 and Q10 are connected to terminals 52 and 54, respectively. Terminals 52 and 54 serve as complementary data input (write) terminals. The coupling together of terminals 44 and 50 by a dashed line indicates that these terminals can be connected together. Likewise, the dashed lines connecting terminals 46 and 52 and terminals 48 and 54 indicate that these terminals can be connected together as illustrated.

The drains of Q5 and Q6 are connected together to a terminal 26 and to a power supply VDD. The gates of Q5 and Q6 are connected together to a terminal 24 and to a voltage pulse source PCB. Q5 and Q6 serve as precharge circuitry which is used to selectively set the potentials of terminals 18 and 12 and 22 and 14, respectively, to essentially equal voltages. Q3 and Q4 may be denoted as buffer transistors. The gates of Q3 and Q4 are connected together to a terminal 20 and to a potential source VDDP.

An MOS transistor will be described as "enabled" if the potential of the gate with respect to the source is of sufficient amplitude and polarity to allow conduction between the source and drain thereof. Conversely, a "disabled" MOS transistor is one in which the potential of the gate is insufficient or of the wrong polarity to allow conduction between the source and drain thereof.

The memory cell illustrated within dashed line rectangle M and its mode of operation are well known. The drain of Q11 is connected to one terminal of C4 and to a terminal 28. The second terminal of C4 is connected to a terminal 30 and to potential VDD. The gate of Q11 is connected to a terminal 32. A "1" stored in the memory cell results in terminal 28 being charged to a potential of approximately VDD minus the threshold voltage (Vth) of Q11. Typical values for VDD and Vth are +8 volts and approximately 1 volt, respectively. A "0" stored in the memory cell results in the potential of terminal 28 being charged to a level of approximately VSS. A typical value for VSS is zero volts. A "1" is written into memory cell M by enabling Q11 (by applying the VDD potential to terminal 32) and by applying a potential of VDD minus one threshold voltage, or a more positive voltage, to the source of Q11 (terminal 22). This sets the potential of terminal 28 to VDD-Vth, a stored "1". A "0" is written into the memory cell by enabling Q11 and setting the potential of terminal 22 to VSS. This causes terminal 28 to be set to VSS, a stored "0".

Logic information stored in memory cell M is read out by enabling Q11 and allowing the potential previously stored on terminal 28 to modify the potential of terminal 22. Gate terminal 32 is typically coupled to a word line of a semiconductor memory and terminal 22 is coupled to a bit line of the same memory.

In reference memory cell R the drain of Q13 is connected to one terminal of capacitor C3, to the drain of Q12, and to a terminal 36. A second terminal of C3 is connected to a terminal 38 and to VDD. The gate of Q12 is connected to a terminal 34. The source of Q13 is connected to a terminal 42 and to a power supply VSS. The gate of Q13 is connected to a terminal 40 and a voltage pulse source PRR. C3 is selected to have approximately one-half of the capacitance of C4. The ratio of C3 to C4 affects the relative potential levels of terminals 18 and 22.

Sense amplifier 10 operates essentially as follows: PCB is initially held at a high potential level that is at least a threshold voltage above the potential of power supply VDD. VDDP is also at a potential level which is at least one threshold voltage above the potential of power supply VDD. SAL is at a potential level of VDD and terminals 32, 34, 44, and 50 are all set in potential to VSS. Circuitry 58, which can be used to provide the output waveform of SAL, is illustrated in FIG. 2. PRR is at a potential level of approximately VDD minus one threshold voltage. These conditions enable Q3, Q4, Q5, Q6, and Q13 and disable Q1, Q2, Q7, Q8, Q9, Q10, Q11, and Q12. This causes terminals 18 and 22, as well as 12 and 14, to be set and held at a potential level of VDD. In addition, terminal 36 is set to a potential level of VSS.

Shortly after the beginning of a cycle of operation, PCB and PRR are both reduced in potential to VSS. This causes terminals 12, 14, 18, 22, and 36 to electrically float in potential at the previously set levels. After this occurs, terminals 32 and 34 are increased in potential from VSS to VDD. This enables Q11 and Q12 and thus couples terminal 36 to terminal 18 through Q12 and couples terminal 28 to terminal 22 through Q11. This causes the potentials of terminals 18 and 22 to be modified as a function of the potentials of terminals 36 and 22, respectively, and as a function of the relative capacitances of C3 and C1 and of C4 and C2, respectively. There are parasitic capacitances associated with terminals 12 and 14, but these capacitances (which are not illustrated) are considerably smaller than those of C1 and C2. There is also a parasitic capacitance (not illustrated) associated with terminal 16.

If a "0" is stored in memory cell M, then terminal 28 is initially at VSS (typically zero volts). The enabling of Q11 causes terminal 22 to discharge from the initially set potential level of VDD by an amount ΔV such that it reaches a potential of VDD-ΔV. The simultaneous enabling of Q12 causes terminal 18 to discharge in potential to a value of VDD-.5ΔV. These potentials are achieved because the ratio of C3 to C4 is approximately one to two.

Q3 and Q4 are always enabled and, accordingly, the potential changes at terminals 18 and 22 propagate through Q3 and Q4, respectively, and change the potentials at terminals 12 and 14 such that the potentials of these terminals correspond to the potential of terminals 18 and 22, respectively.

At this point in time terminal 16 is pulsed from the initial potential level of VDD towards potential of VSS. The slope of the edge of the voltage pulse is initially gradual and then increases rapidly. The potential of the gate of Q2 is more positive than the gate of Q1. Accordingly, as terminal 16 drops in potential, Q1 remains disabled and Q2 becomes enabled and begins to conduct and thus discharges terminal 14. The potential difference between terminals 12 and 14 thus increases. Terminal 12 stays essentially at the potential level of VDD-.5ΔV at this time. As soon as the potential difference between terminals 12 and 14 has increased to typically the magnitude of a threshold voltage (1 volt in a typical case), the slope of the voltage waveform applied to terminal 16 (SAL) rapidly increases such that the potentials of terminals 14 and 16 then thereafter rapidly move towards VSS. Terminal 12 stays near the potential of VDD-.5ΔV during the entire time terminal 16 is pulsed from VDD to VSS.

As terminal 16 reaches VSS in potential, terminal 44 (RS) is pulsed in potential from VSS to VDD. Typically terminals 46 and 48 are electrically set in potential to VDD by voltage precharge circuitry (not illustrated) and then allowed to float in potential just prior to the time at which terminal 44 is brought from VSS to VDD. In the case of a stored "0" in memory cell M, Q8 becomes enabled and thus the potential of terminal 14 is transferred to terminal 48. Thus terminal 48 is lowered in potential towards VSS. This represents the read out of a "0" from memory cell M. Q7 remains disabled since the gate, drain, and source thereof are all at or near potential VDD. Thus terminal 46 remains at VDD while terminal 48 drops to a potential level below VDD. Thus the differential voltage between terminals 12 and 14 has been transferred to terminals 46 and 48.

In a typical memory system terminals 46 and 48 will be connected to another sense amplifier (not illustrated) which is especially suited to driving relatively high capacitive loads.

As read out is occurring, memory cell M begins to be refreshed. Terminal 14 discharges rapidly to VSS. Terminal 22 discharges much more slowly because of the resistance of Q4 and the capacitance of C2. Q3 and Q4 are designed in known fashion to have relatively high resistance between drain and source when enabled. Thus the current spike which results from the discharge of C2 has a lower peak magnitude and a longer time duration than would be the case if Q4 had relatively low resistance. It is to be noted that the read out operation can start as soon as the cross-coupled pair is latched up by the negative going voltage pulse applied to terminal 16. There is no need to wait until terminal 22 reaches the same potential as terminal 14. Thus the read out of information from sense amplifier 10 to terminals 46 and 48 can proceed without waiting for refresh to be completed.

As terminal 22 drops to the VSS potential level, terminal 28 likewise drops in potential because Q11 is still enabled. Thus memory cell M has been refreshed such that it now again stores a logic "0". At this point in time terminal 18 is still close in potential to VDD and terminal 36 is charged to a potential of approximately VDD minus the threshold voltage of Q12 because Q12 is enabled at this time.

Now the cycle of operation of sense amlifier 10 can be ended and terminals 32, 34, and 44 are returned to VSS and terminals 16, 24, and 40 are returned to their initial positive potentials. In addition, terminals 46 and 48 are again set in potential to +VDD. This enables Q13 and causes terminal 36 to discharge to VSS. All other previously discussed terminals are set to the initial potential levels discussed earlier.

If memory cell M contains a stored "1" instead of a "0", then during the time when Q11 is initially enabled, terminal 14 remains at the initially set value of VDD. The potential of terminal 12 still drops from VDD to a potential of VDD-.5ΔV. These conditions result in terminal 12 being discharged to VSS when terminal 16 is pulsed to VSS, terminal 48 remaining at +VDD, and terminal 46 dropping towards VSS as terminal 44 (RS) is pulsed to +VDD. This is indicative of the read out of a stored "1" from the memory cell. Memory cell M is refreshed to a full "1" potential level of VDD-Vth as soon as Q11 becomes enabled. Terminal 28 of memory cell M stays at a potential of VDD minus the threshold voltage of Q11 during this cycle of operation. This represents a stored "1" in memory cell M. As terminal 16 is pulled to VSS, terminal 12 is pulled down to VSS because it is at a lower potential than terminal 14. Terminal 18 is likewise pulled down in potential to VSS. Accordingly, terminal 36 is also pulled down in potential to VSS since Q12 is enabled.

Logic signal information (data) can be written into the memory cell through Q10. It is to be noted that the memory cell M can be connected to terminal 18 and the reference memory cell R can be connected to terminal 22. In such case data is written into the memory cell through Q9. During a write cycle of operation the same procedures are used as during a read operation except that terminal 50 (WS) is pulsed in potential from VSS to VDD and terminal 44 is held in potential at VSS. The data to be written into the memory cell M is applied to terminal 54 and the complement thereof is applied to terminal 52. This causes terminals 22 and 18 to be forced to essentially the potentials of terminal 54 and 52, respectively. Thus the desired logic information is transferred into memory cell M since Q11 is enabled at this time.

A read-modified write operation is also possible. After the normal read operation is over, Q7 and Q8 are disabled and Q9 and Q10 are enabled. This allows new information (data) applied to terminal 54 to be written into memory cell M after the previously stored information has been read out.

Memory cell M can be refreshed during a read, a write, or a read-modified write operation. In addition, it can be refreshed even if none of the above operations are carried out. If it is desired only to refresh the information stored in memory cell M, then terminals 44 and 50 are held at VSS during the entire cycle of operation of sense amplifier 10. A memory cell containing a "1", which may or may not have discharged from the full "1" potential level of VDD-Vth, is recharged to or maintained at the full "1" potential level as Q11 becomes enabled. A memory cell containing a "0" is initially charged up to a potential between zero volts and VDD-Vth. The pulsing of terminal 16 thereafter to VSS causes terminal 22 to discharge to VSS and thereby discharges the memory cell such that it again stores a "0".

The number of read and write terminals for sense amplifier 10 can be consolidated from six terminals to three terminals by connecting terminals 46 and 52 together, by connecting terminals 48 and 54 together, and by connecting terminals 44 and 50 together. Even when so configured, the paths including Q7 and Q8 are the primary read paths since they will handle essentially all of the read currents, while for writing Q9 and Q10 provide the primary write paths since they will handle essentially all the write current.

Now referring to FIG. 2, there is illustrated circuitry 58 which can be used as the voltage generator circuit SAL of FIG. 1. Circuitry 58 comprises field effect transistors Q14, Q15, Q16, and Q17 and delay circuits 1 and 2. The output voltage waveform at terminal 16 is designed to be initially at +VDD and then to drop to +VDD-Vth. It then is designed to drop in potential with a gradual slope towards VSS. After a preselected time it is designed to drop in potential at a much more rapid rate and to then reach VSS in potential.

The drains of Q14, Q15, and Q16 and the source of Q17 are all connected to terminal 16. The sources of Q14, Q15, and Q16 are all connected together to power supply VSS. The drain of Q17 is connected to power supply +VDD. The gate of Q14 is connected to an input terminal 60, to a voltage pulse generator CR, and to an input of delay circuit 1. An output terminal of delay circuit 1 is connected to the gate of Q15, an input terminal of delay circuit 2, and to a terminal 62. An output terminal of delay circuit 2 is connected to the gate of Q16, and to a terminal 64. The gate of Q17 is connected to terminal 24 (PCB).

At the beginning of a cycle of operation terminal 24 (PCB) is at a potential at least as positive as +VDD plus a threshold voltage and terminal 60 (CR) is at VSS. This enables Q17 and disables Q14, Q15, and Q16.

This causes terminal 16 to be held at +VDD. Terminal 24 (PCB) is then pulsed to VSS and terminal 16 remains floating in potential at +VDD. Terminal 60 (CR) is then pulsed in potential from VSS to +VDD. Concurrently terminals 32 and 34 (of FIG. 1) are pulsed from VSS to +VDD. This enables Q14 and thus pulls terminal 16 down towards +VSS. The initial rate of fall of the potential of terminal 16 is determined by the impedance of Q14 and the capacitance (not illustrated) on terminal 16 to cause terminal 16 to reach a potential of approximately VDD-Vth at the time terminals 12 and 14 have had their potentials modified as a function of the potential levels stored in the reference memory cell R and memory cell M. This leaves Q1 and Q2 just on the verge of being enabled. The time period of delay of delay circuit 1 is chosen to allow sufficient time for the information stored in memory cell M and in reference cell R to be transferred to terminals 14 and 12, respectively.

After the delay time introduced by delay circuit 1, the gate of Q15 becomes enabled and starts to pull terminal 16 further towards VSS. The impedance of Q 15 is designed to be significantly lower than that of Q14 and somewhat higher than that of Q1 and Q2 or the parallel combination of Q1 and Q2 such that terminal 16 is gradually pulled further down in potential towards VSS as Q15 is enabled. The impedance of Q15 is also selected to limit the rate of all of the potential of terminal 16 so as to allow terminal 12 or 14, whichever is the least positive potential at the time, to closely follow terminal 16 down in potential. This amplifies the differential voltage between terminals 14 and 12 while insuring that the more positive of the two terminals remains at the potential level previously established and essentially does not discharge from that potential level. The delay time associated with delay circuit 2 allows for the differential voltage between terminals 14 and 12 to reach a potential of somewhat greater than a threshold voltage before Q16 becomes enabled. Q16 is of relatively low impedance and is therefore capable of pulling terminal 16 to VSS relatively quickly.

Sense amplifier 10 has been fabricated as part of a 64K (65,536 bits) Random Access Memory that utilizes n-channel insulated gate field effect transistors and memory cells and reference memory cells of a type described herein. Q3 and Q4 each had resistance between drain and source of approximately 50,000 ohms. It has been tested and found to be functional. The memory cells are divided into four 16K arrays. Each 16K array has 256 bit lines associated therewith. A group of 256 sense amplifiers, each of the type disclosed in FIG. 1, is connected to the bit lines in each pair of 16K arrays. A separate SAL voltage generator circuit is connected to each group of 256 sense amplifiers. The impedances of Q14, Q15, and Q16 of the SAL generator circuits are designed to reflect that the impedances of 256 cross-coupled pairs of transistors Q1 and Q2 are being used and not just one cross-coupled pair. The SAL-type voltage generators fabricated have the basic structure illustrated in FIG. 2; however, they have been adapted to allow the complete latching of one of the two groups of sense amplifiers before the other. This serves to limit the number of current spikes occurring simultaneously and to spread current dissipation of the memory more evenly over an entire cycle of operation.

It is to be understood that the embodiments described are merely illustrative of the general principles of the invention. Various modifications are possible within the scope of the invention. For example, p-channel field effect transistors could be substituted for the n-channel field effect transistors provided the polarities of the power supply potentials and voltage pulses are appropriately changed. Still further, a variety of different types of resistors or depletion type field effect transistors could be substituted for transistors Q3 and Q4. Still further the cross-coupled circuitry can be more complex than just two transistors. Another transistor could be added to the illustrated precharge circuitry with the gate of the added transistor connected to the gates of Q5 and Q6 and the drain and source thereof connected to the source of Q5 and the source of Q6, respectively, or to the drains of Q1 and Q2. The sources of Q5 and Q6 could be connected to terminals 12 and 14, respectively, instead of to terminals 18 and 22, respectively. Still further, voltage pulse generator circuit 58 (SAL) could easily be modified or replaced with circuitry which provides the same voltage characteristics. Still further the read and write circuitry can be more complex than just a single transistor for each circuit. Still further, gate terminals 20 of transistors Q3 and Q4 need not be enabled at all times. They can be connected to a voltage pulse generator and appropriately enabled and disabled during a cycle of operation. Still further, gate terminals 20 of Q3 and Q4 could be connected to a voltage pulse generator and appropriate potential levels could be generated to cause Q3 and Q4 to be of lower resistance during the time the information stored in the memory cell M and the reference memory cell R is transferred to terminals 14 and 12, respectively, than at all other times during a cycle of operation.

Claims

1. Digital sense circuitry comprising a cross-coupled circuit (Q1, Q2) having first (12) and second (14) terminals and first (Q3) and second (Q4) switching-type devices which each have a control terminal (20) and a first (12, 14) and a second (18, 22) output terminal, the first output terminals of the first (Q3) and second (Q4) devices are connected to the first (12) and second (14) terminals, respectively, of the cross-coupled circuit (Q1, Q2), read and write circuits (Q7, Q8, Q9, Q10),

CHARACTERIZED IN THAT:

the read and write circuits comprise separate first (Q7) and second (Q8) read circuits and separate first (Q9) and second (Q10) write circuits;

the first and second read circuits are connected to the first (12) and second (14) terminals of the cross-coupled circuit, respectively, and the first write circuit is connected to the second terminal (18) of the first device (Q3), and the second write circuit is connected to the second terminal (22) of the second device (Q4).

2. The circuitry of claim 1 further

CHARACTERIZED IN THAT:

the cross-coupled circuit (Q1, Q2) comprises third (Q1) and fourth (Q2) switching devices which each have a control terminal and first and second output terminals;

the control terminal of the fourth switching device (Q2) is connected to the first output terminal of the third switching device (Q1) and to the first terminal (12) of the cross-coupled circuit (Q1, Q2); and

the control terminal of the third switching device (Q2) is connected to the first output terminal of the fourth switching device (Q2) and to the second terminal (14) of the cross-coupled circuit (Q1, Q2).

3. The circuitry of claim 2 further CHARACTERIZED IN THAT:

the first read circuit (Q7) comprises a fifth switching device (Q7) and the second read circuit (Q8) comprises a sixth switching device (Q8);

the first write circuit (Q9) comprises a seventh switching device (Q9) and the second write circuit (Q10) comprises an eighth switching device (Q10);

each of the fifth (Q7), sixth (Q8), seventh (Q9), and eighth (Q10) switching devices has a control terminal and first and second output terminals;

the first output terminal of the fifth switching device (Q7) is connected to the first terminal (12) of the cross-coupled circuit (Q1, Q2), and the first output terminal of the sixth switching device (Q8) is connected to the second terminal (14) of the cross-coupled circuit (Q1, Q2); and

the first output terminal of the seventh switching device (Q9) is connected to the second output terminal (18) of the first switching device (Q3), and the first output terminal of the eighth switching device (Q10) is connected to the second terminal (22) of the second switching device (Q4).

4. The circuitry of claim 3 further CHARACTERIZED BY

precharge circuitry (Q5, Q6) connected to the second output terminals (18, 22) of the first (Q3) and second (Q4) switching devices.

5. The circuitry of claim 4 further CHARACTERIZED IN THAT:

precharge circuitry (Q5, Q6) comprises ninth (Q5) and tenth (Q6) switching devices which each have a control terminal and first and second output terminals;

the control terminals of the ninth (Q5) and tenth (Q6) switching devices are connected together;

the second output terminal of the ninth switching device (Q5) is connected to the second output terminal (18) of the first switching device (Q3); and

the second output terminal of the tenth switching device (Q6) is connected to the second output terminal (22) of the second switching device (Q4)

6. The circuitry of claim 5 further CHARACTERIZED IN THAT:

the second output terminals (16) of the third (Q1) and fourth (Q2) switching devices are connected together;

voltage pulse generator circuitry (Q14, Q15, Q16, and Q17 and delay circuits 1 and 2) which comprises eleventh (Q14), twelfth (Q15), thirteenth (Q16), and fourteenth (Q17) switching devices which each have a control terminal and first and second output terminals and which further comprises first (1) and second (2) delay circuits;

the first (Q3), second (Q4), third (Q1), fourth (Q2), fifth (Q7), sixth (Q8), seventh (Q9), eighth (Q10), ninth (Q5), tenth (Q6), eleventh (Q14), twelfth (Q15), thirteenth (Q16), and fourteenth (Q17) switching devices all are field effect transistors;

the sources of the eleventh (Q14), twelfth (Q15), and thirteenth (Q16) transistors are connected together;

the drains of the eleventh (Q14), twelfth (Q15), and thirteenth (Q16) transistors and the source of the fourteenth (Q17) transistor are connected to the sources (16) of the third (Q1) and fourth (Q2) transistors;

the gate of the eleventh (Q14) transistor is connected to an input terminal (60) and is connected to a first input terminal of the first delay circuit (1);

an output terminal (62) of the first delay circuit (1) is connected to the gate of the twelfth (Q15) transistor and to an input terminal of the second delay circuit (2); and

an output terminal (64) of the second delay circuit is connected to the gate of the thirteenth (Q16) transistor.

7. The circuitry of claim 8 further CHARACTERIZED IN THAT

all of the field effect transistors (Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, and Q10) are enhancement mode n-channel field effect transistors.

FIG. 1

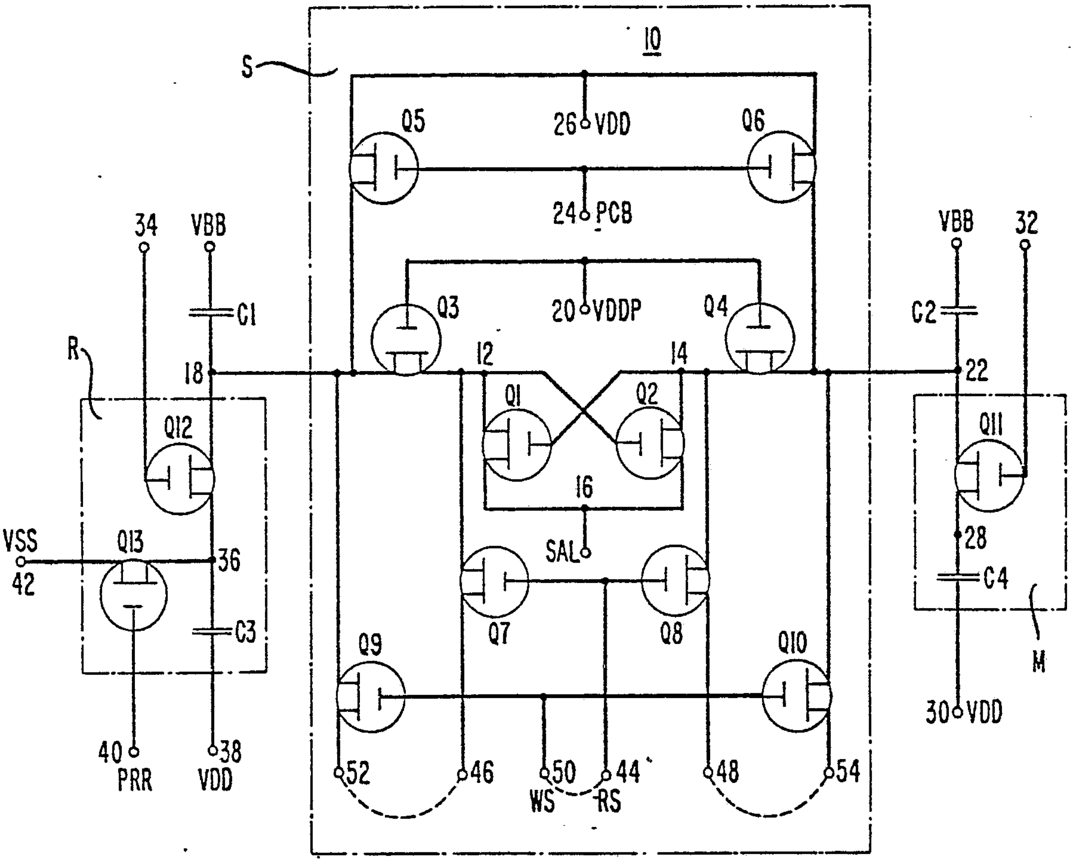
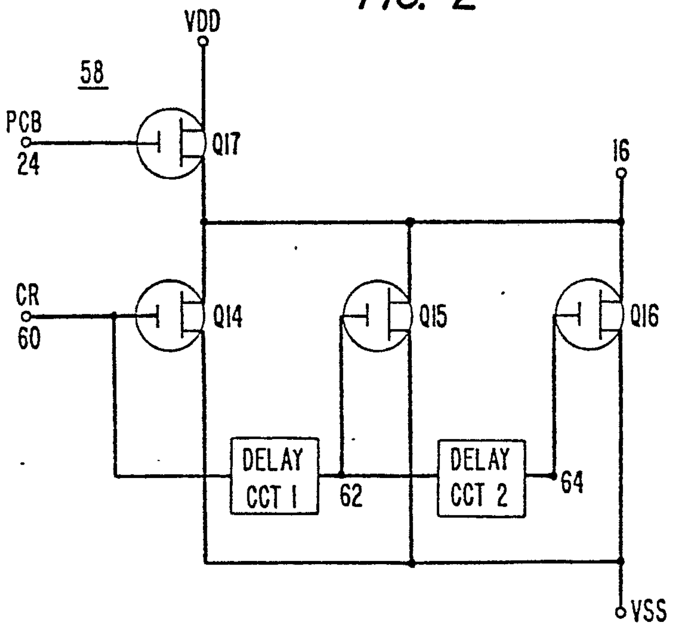

10
S
Q5
26 VDD
Q6
24 PCB
34
VBB
VBB
32
Q3
20 VDDP
Q4
C1
C2
R
18
12
14
22
Q1
Q2
Q12
Q11
16
28
VSS
42
Q13
36
SAL
C4
Q7
Q8
C3
M
Q9
Q10
30 VDD
40
PRR
38
VDD
52
46
50
WS
44
RS
48
54

FIG. 2


VDD
58
PCB
24
Q17
16
CR
60
Q14
Q15
Q16
DELAY CCT 1
62
DELAY CCT 2
64
VSS

INTERNATIONAL SEARCH REPORT

International Application No PCT/US80/00075

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [8]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int. Cl^3 G11C7/00

U. S. Cl. 307/355;365/190

WO80/01730

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	307/279,291,355,356,362,Digest 3 365/190,196,202,203,205,207,208

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
X	US,A, 4,007,381 Published 8 February 1977, See in Fig. 2 elements M5, M6, through which information is written, and M11, M15 through which information to be read-out passes, Mohsen.	1-3
A	US,A, 4,085,457 published 18 April 1978, see Fig. 2, Itoh.	
A	US,A, 4,069,474 published 17 January 1978, see Fig. 2, Boettcher et al.	
A	US,A, 4,061,999 published 6 December 1977, see Fig. 1, Proebsting et al.	
A	US,A, 4,021,682 published 3 May 1977, see Fig. 3, Elmer et al.	

* Special categories of cited documents: [15]

"A" document defining the general state of the art

"E" earlier document but published on or after the international filing date

"L" document cited for special reason other than those referred to in the other categories

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but on or after the priority date claimed

"T" later document published on or after the international filing date or priority date and not in conflict with the application, but cited to understand the principle or theory underlying the invention

"X" document of particular relevance

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2] 12 June 1980	Date of Mailing of this International Search Report [2] 18 JUN 1980
International Searching Authority [1] ISA/US	Signature of Authorized Officer [20] Larry N. Anagnos Larry N. Anagnos

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

A	US,A, 4,053,873, Published 11 October 1977, see Fig. 1, Freeman et al.	
A	US,A, 4,119,871 Published 10 October 1978, see Fig. 1-2, Zibert.	
A	US,A, 3,838,295, Published 24 September 1974, see Fig. 1, Lindell.	
A	US,A, 4,070,590, Published 24 January 1978, Ieda et al.	
A	US,N, IBM Technical Disclosure Bulletin, Published January 1976, Vol. 18 No. 8, Page 2450-1, Arzubi.	

V.☐ **OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE** [10]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1.☐ Claim numbers ...., because they relate to subject matter [12] not required to be searched by this Authority, namely:

2.☐ Claim numbers ...., because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

VI.☐ **OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING** [11]

This International Searching Authority found multiple inventions in this international application as follows:

1.☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2.☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3.☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.