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(56) Documents Cited
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INT CL^6 **H01L 21/3205 21/70 21/8242 27/108**
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(54) Abstract Title

Method of forming a tantalum oxide containing capacitor

(57) A method of forming a tantalum oxide containing capacitor which improves the Ta_2O_5 film's properties, and includes providing a plasma silicon nitride film having a thickness of 20~100 angstroms, sufficient to prevent oxidation of a lower capacitor electrode, by a plasma nitridation process using a reactant gas during the step of preprocessing the surface of the lower capacitor electrode. The plasma silicon nitride film is formed by nitrifying a surface portion of the lower capacitor electrode by means of excitation of a reactant gas with a plasma. The plasma nitridation process is effective to form a sufficiently thick silicon nitride film on the lower capacitor electrode and anneal the resulting substrate in the same process chamber. Also, the method is applicable to a more simplified annealing mechanism, providing cost savings in the manufacture of DRAM devices, in the form of an ozone annealing process using thermal energy of more than about 400°C. In the ozone annealing process, the thermal energy is generated by heating a susceptor where wafers are placed.

Fig. 3

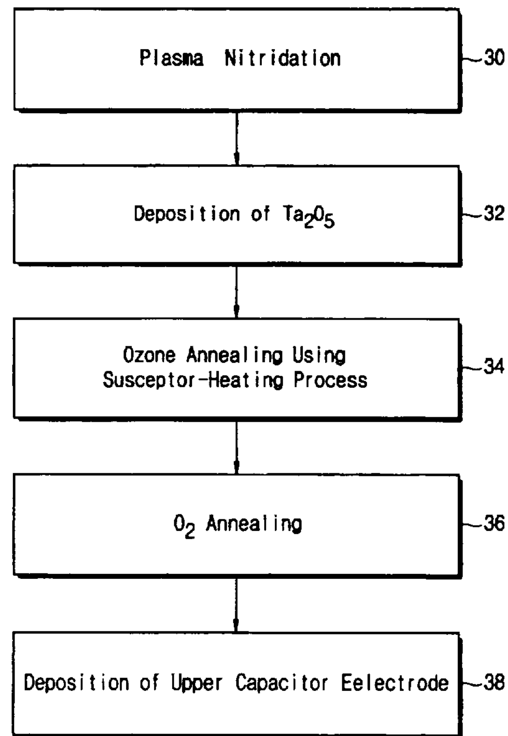

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Fig. 1

(Prior Art)

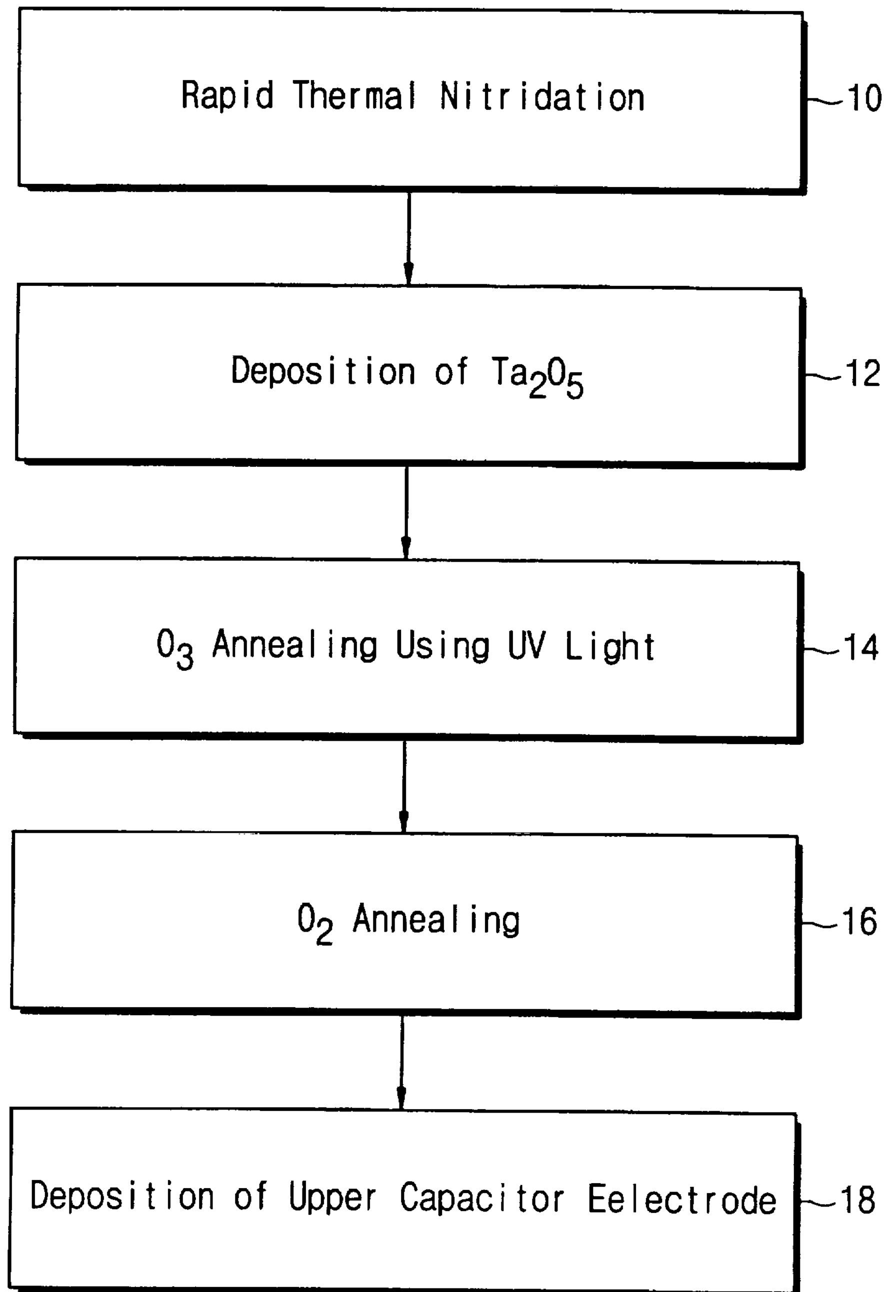


Fig. 2

(Prior Art)

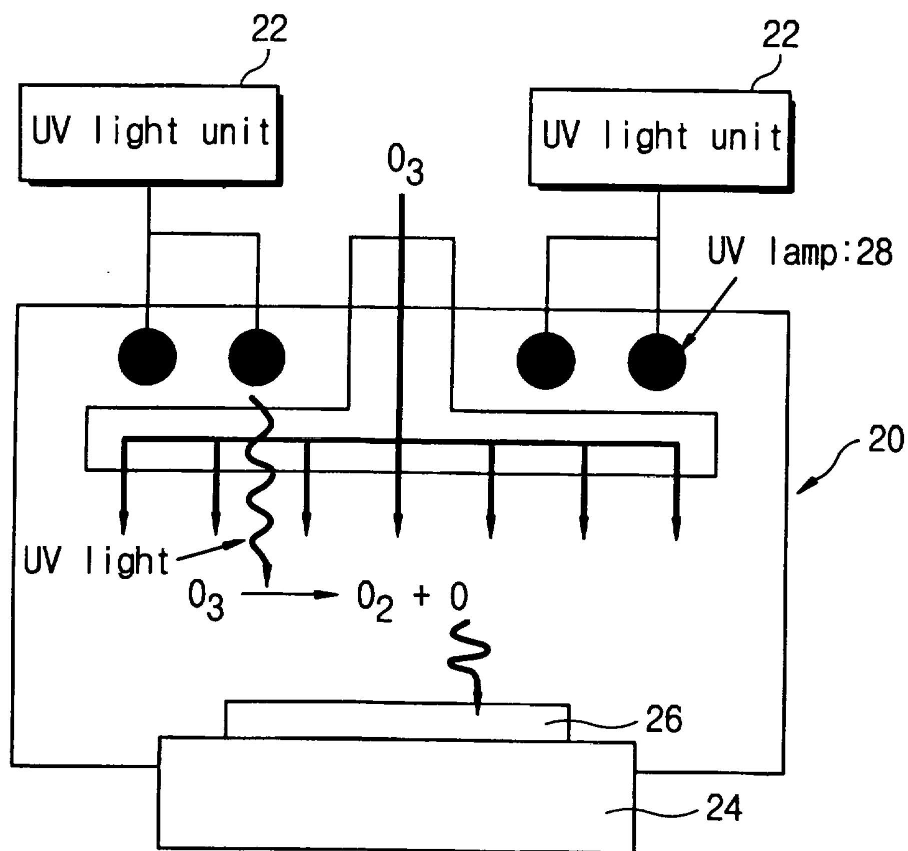


Fig. 3

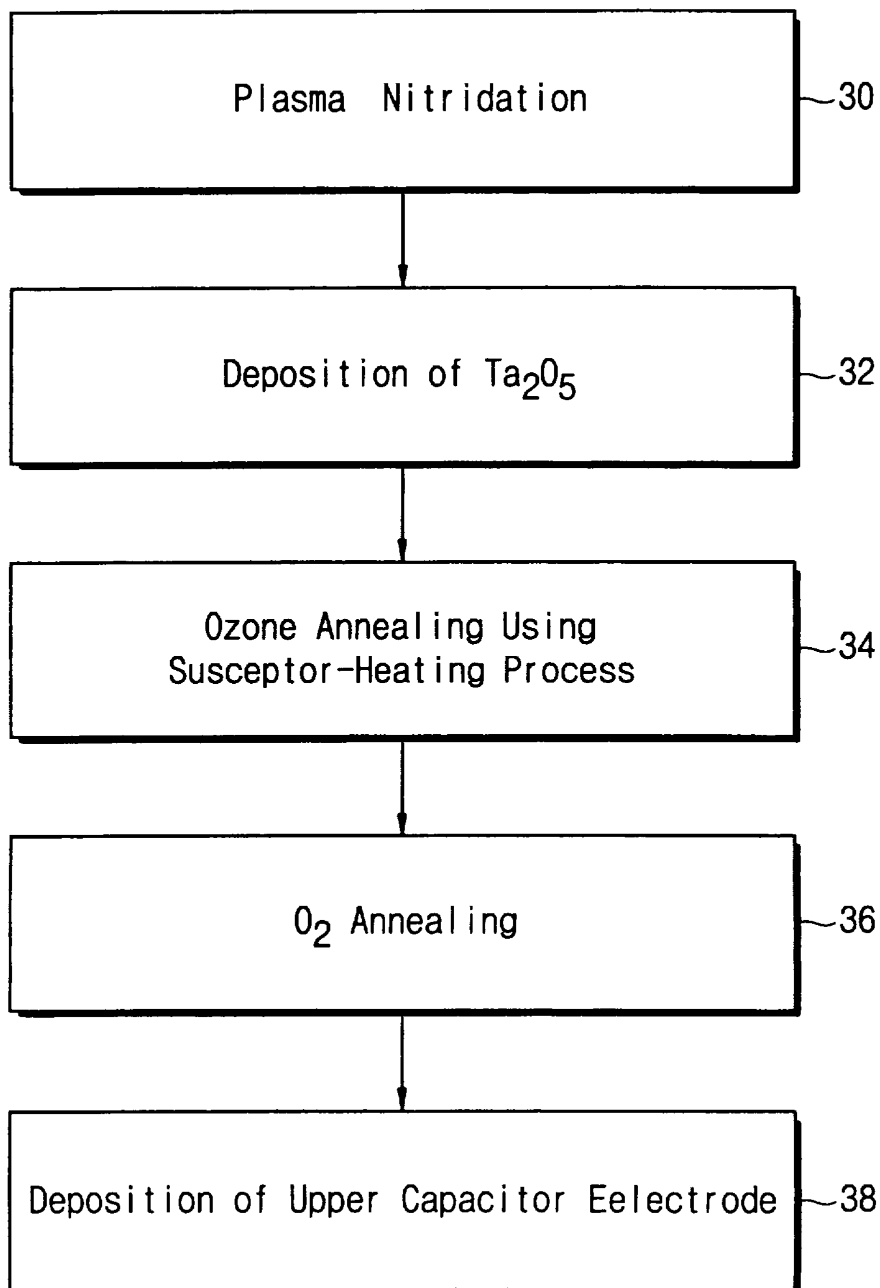


Fig. 4A

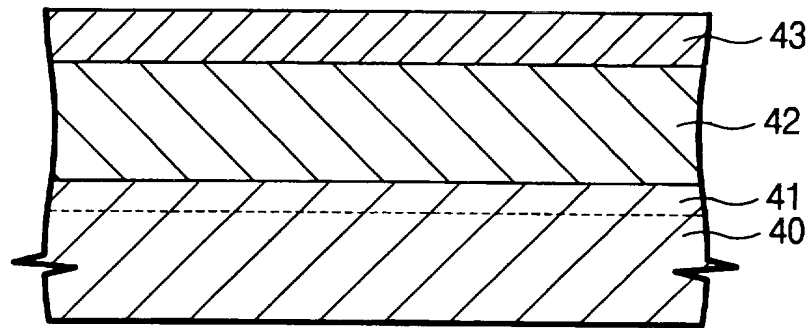


Fig. 4B

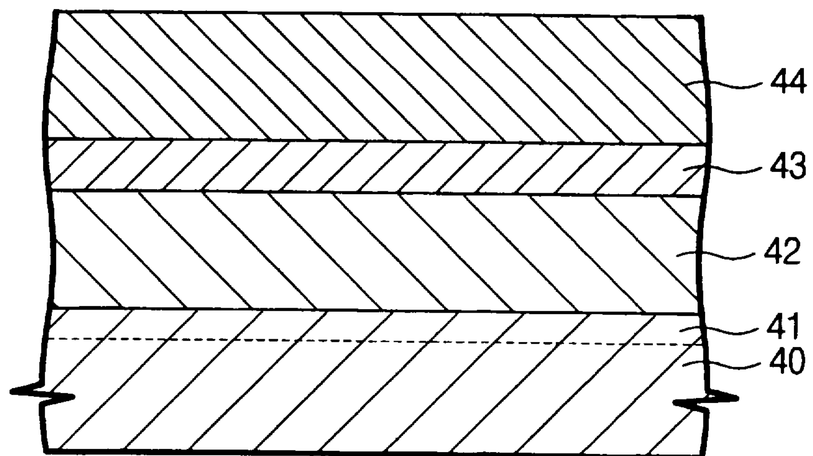


Fig. 4C

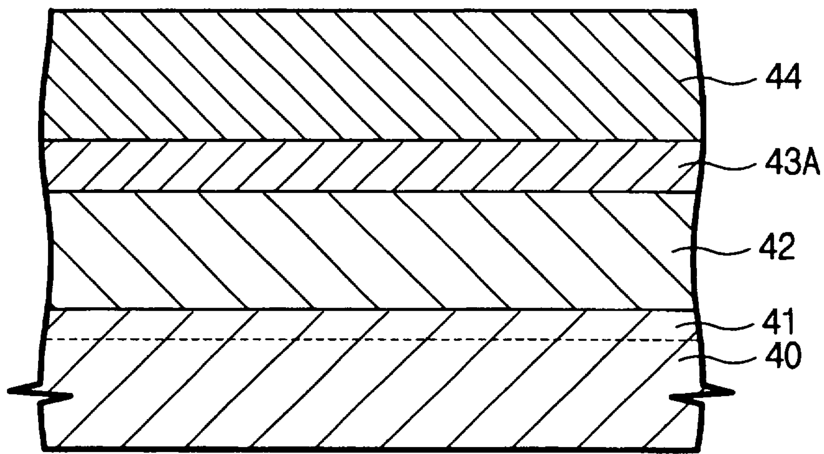


Fig. 4D

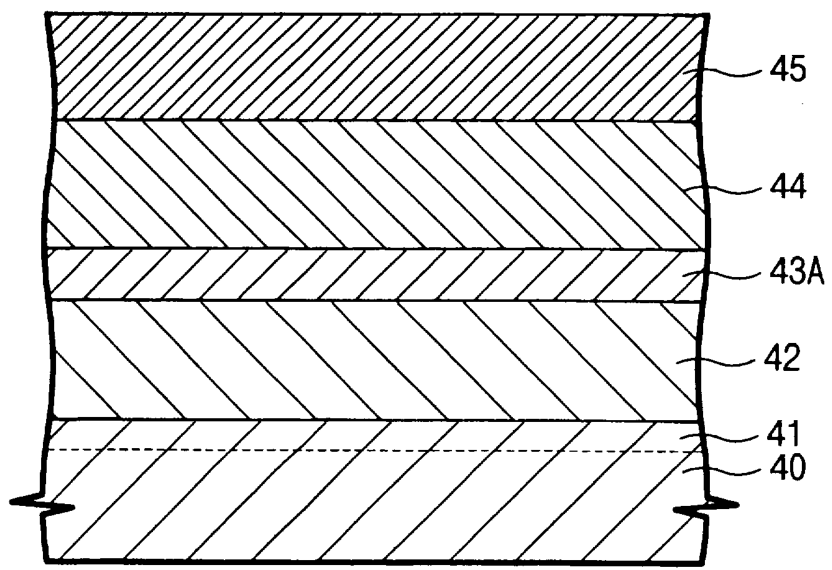


Fig. 5

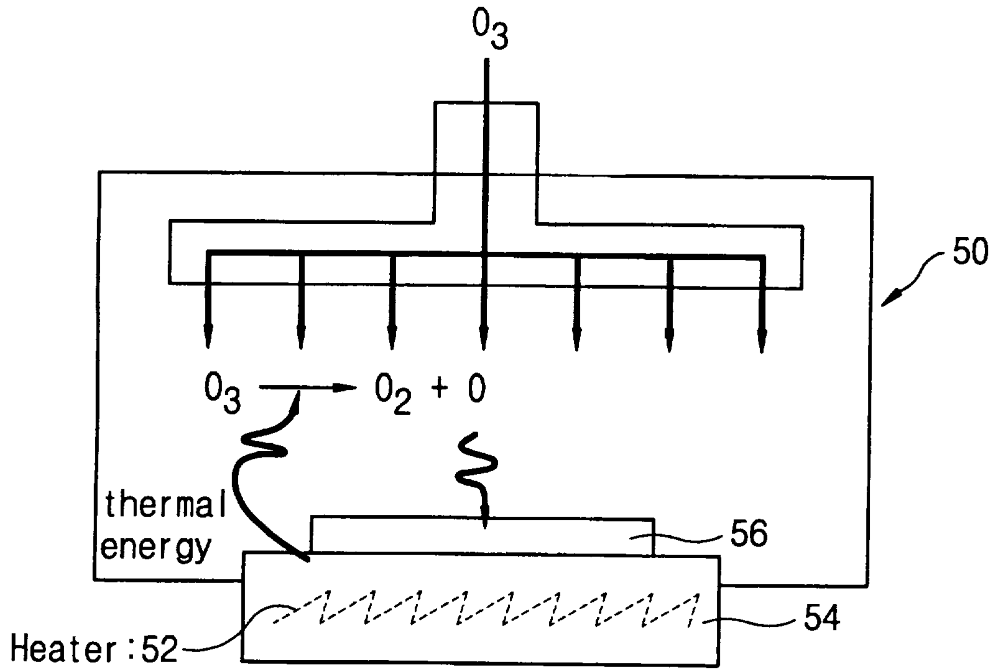
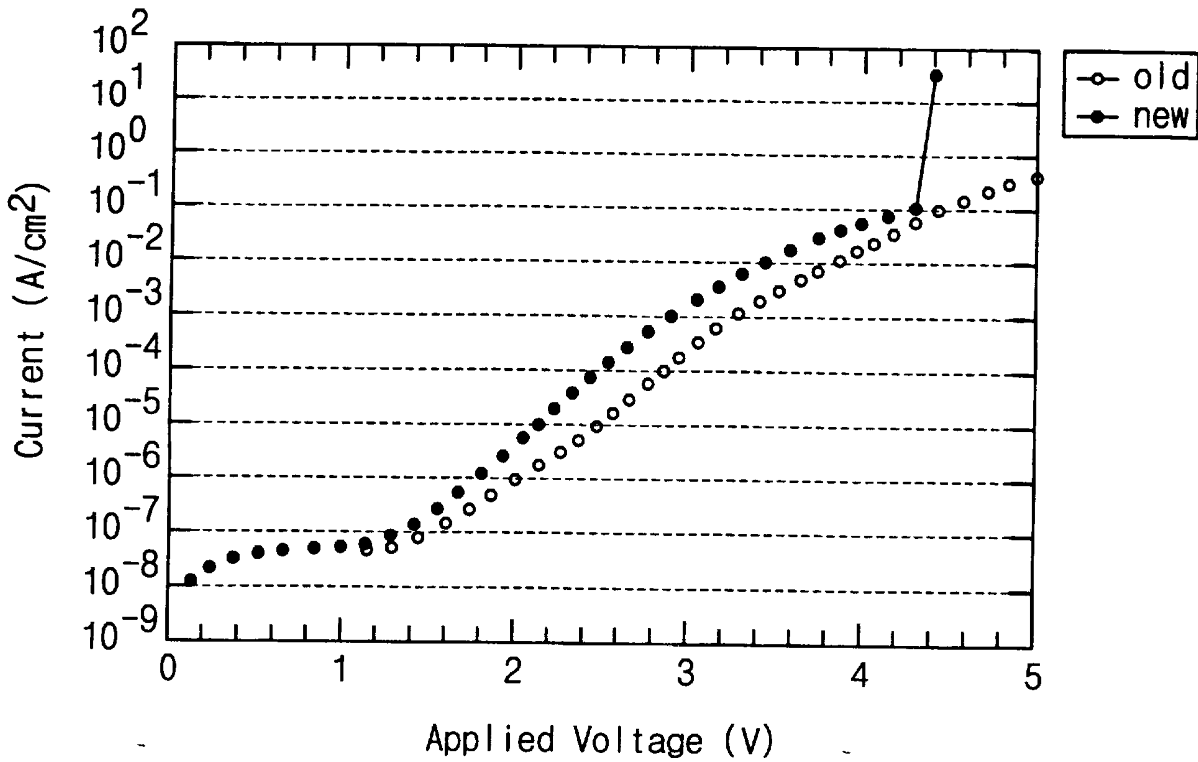


Fig. 6



METHOD OF FORMING A TANTALUM OXIDE CONTAINING CAPACITOR

Field of the Invention

The present invention relates to a method of forming dynamic random access memory (DRAM) cell capacitor having high dielectric constant material, and more particularly to a
5 method of forming a tantalum oxide (Ta_2O_5) containing capacitor.

Background of the Invention

As DRAMs increase in memory cell density, there is a continuing challenge to maintain sufficiently high storage capacitance despite decreasing cell area. Additionally, there is a continuing goal to further decrease cell area. one principal way of increasing cell
10 capacitance is through cell structure techniques. Such techniques include three-dimensional cell capacitors. Such as trenched or stacked capacitors. Yet as feature size continues to become smaller and smaller, development of improved materials for cell dielectrics as well as the cell structure are important. The feature size of 256 Mb DRAMs will be on the order of 0.25 micron, and conventional dielectrics such as SiO_2 and Si_3N_4 might not be suitable
15 because of small dielectric constants.

Highly integrated memory devices, such as 256 Mbit DRAMs, are expected to require a very thin dielectric film for the 3-dimensional capacitor of cylindrically stacked or trench structures. To meet this requirement, the capacitor dielectric film thickness will be below 2.5 nm of SiO_2 equivalent thickness. Chemical vapor deposited (CVD) Ta_2O_5 films are
20 considered to be very promising cell dielectric films for this purpose, as the dielectric constant of Ta_2O_5 is approximately three times that of conventional Si_3N_4 capacitor dielectric films. However, one drawback associated with Ta_2O_5 dielectric films is undesired leakage current characteristics. Accordingly, although Ta_2O_5 material has inherently higher dielectric properties, as-deposited Ta_2O_5 typically produces unacceptable results due to leakage

current.

One prior art technique disclosed includes exposing the polysilicon film to rapid thermal nitridation prior to subsequent deposition of the Ta_2O_5 film. Such rapid thermal nitridation includes exposing the subjected polysilicon film to temperatures of from about
5 800°C. to 1100°C. for sixty seconds in an ammonia atmosphere at atmospheric pressure to form a silicon nitride film. The silicon nitride film formed thus acts as a barrier film to oxidation during Ta_2O_5 deposition and subsequent high temperature densification processes to prevent surface oxidation of the lower polysilicon electrode. Typical method of forming a Ta_2O_5 containing capacitor using the prior art process concepts is shown by a flow chart
10 of Fig. 1.

Referring to Fig. 1, a lower capacitor electrode made from conductively doped polysilicon connects to a diffusion film which is formed in a silicon substrate. The polysilicon electrode is subjected to a rapid thermal processing step (in this case rapid thermal nitridation (RTN)) which converts a top surface of the polysilicon electrode into a
15 silicon nitride film in step 10 of Fig. 1. Since the silicon nitride film formed thus is formed extremely thin, for example, about 5~10 angstroms thick due to inherent RTN process property, it can not prevent oxidation of the polysilicon electrode during subsequent oxidation annealing steps. In detail, oxygen atoms in a tantalum oxide film formed by subsequent step trend to be diffused penetrating the extremely thin silicon nitride film into
20 the polysilicon electrode during subsequent oxidation annealing steps. Herein, if the silicon nitride film does not have a sufficient thickness, the oxygen atoms react with silicon of the polysilicon electrode to thereby form SiO_2 film on the electrode. As a result, a SiO_2 equivalent thickness T_{oxeq} is increased due to the RTN process and thereby capacitance of finally fabricated DRAM cell capacitor is lowered. Next, a capacitor cell dielectric material,
25 tantalum oxide, is formed over the RTN film in step 12. The tantalum oxide film formed thus has the primary disadvantage as compared to insulators (for example, SiO_2 or Si_3N_4) with lower dielectric constants in that it has its fairly high conductivity with substantial current leakage due to deviation from stoichiometric composition of Ta:O, particularly,

oxygen vacancies due to deficiency of oxygen in the tantalum oxide film. Therefore, the tantalum oxide film requires substantially a higher temperature annealing cycle to improve the film's electrical properties, particularly, to fill up the oxygen vacancies of the tantalum oxide film with oxygen atoms. One method is, as illustrated in step 14 of Fig. 1, an ozone (O_3) annealing process which generates oxygen atoms by exposing the resulting substrate to ultraviolet (UV) light under ozone ambient and fills up them into the oxygen vacancies. However, the use of the ozone annealing process leads to increase in the production cost of DRAM devices. This is because a UV light unit (shown by reference numeral 22 in Fig.2) for exposing UV light through UV lamps 28 is very costly as compared with a heater unit (not shown in Fig. 2) for heating a susceptor 24 in a process chamber 20 where substrates 26 are placed. Next, an O_2 annealing process is in step 16 carried out at a high temperature, for example, at about 750°C.~800°C. so as to eliminate carbon or hydrogen carbon compound containing in the tantalum oxide film. Finally, a titanium nitride (TiN) film is formed over the tantalum oxide film to form an upper capacitor electrode in step 18 of Fig. 1.

Furthermore, since in the prior art method the process steps of forming the Ta_2O_5 and Si_3N_4 films are performed separately in different process chambers, throughput of process steps is more longer.

Summary of the Invention

The present invention is intended to solve the problems, and it is an object of the invention to provide a method of forming a tantalum oxide containing capacitor in which a silicon nitride film serving as a barrier film has a thickness sufficient to prevent surface oxidation of a lower capacitor electrode during subsequent annealing process steps.

It is a further object of the present invention to provide a method of forming a tantalum oxide containing capacitor in which during an ozone annealing process for filling up oxygen vacancies in the tantalum oxide film with oxygen atoms generation of the oxygen atoms is accomplished by heating a wafer-placed susceptor.

It is another object of the present invention to provide a method of forming a tantalum oxide containing capacitor in which process steps of forming the tantalum oxide and silicon nitride films are performed in the same process chamber.

According to one aspect of the present invention, a method of forming a capacitor on a substrate having a conductive diffusion film therein comprises the step of, after forming a lower capacitor electrode on the substrate to connect electrically to the conductive diffusion film, forming a plasma silicon nitride film on the lower capacitor electrode. With this method, the plasma silicon nitride film serves as a reaction prevention film having a thickness sufficient to prevent oxidation of the lower capacitor electrode during subsequent oxidation annealing processes. The method further comprises the steps of forming a high dielectric constant film of tantalum oxide on the plasma silicon nitride film, performing an ozone annealing process to fill up oxygen vacancies in the tantalum oxide film with oxygen atoms, performing an O_2 annealing process to densify the tantalum oxide film, and forming an upper capacitor electrode on the plasma silicon nitride film, wherein the steps of forming the plasma silicon nitride film and performing the ozone annealing process are carried out in same process chamber.

In this method, the lower capacitor electrode is made of a conductively doped polysilicon.

In this method, the step of forming the plasma silicon nitride film comprises converting a surface portion of the lower capacitor electrode into a silicon nitride film by exciting a reactant gas with a plasma. The reactant gas is one selected from a group consisting of NH_3, N_2 and N_2O.

In this method, the thickness of the plasma silicon nitride film is in the range of 20~100 angstroms.

In this method, the oxygen atoms of the ozone annealing process are generated in the process chamber under ozone ambient by heating a susceptor where the substrate is placed.

In this method, the ozone annealing process is performed at a temperature of 300°C. to 600°C., preferably at 450°C., at a pressure of 1 mTorr to 50 Torr.

In this method, the plasma silicon nitride film after the O_2 annealing process is converted into a silicon nitride composition which is composed of Si_3N_4 and SiO_2 or SiON.

In this method, the O_2 annealing process is performed at a temperature of 750°C.~800°C.

5 ## Brief Description of the Drawings

This invention may be understood and its objects will become apparent to those skilled in the art by reference to the accompanying drawings as follows:

Fig. 1 is a flow chart illustrating a prior art method of forming a tantalum oxide containing capacitor for DRAM applications;

10 Fig. 2 is a schematic view of an ozone annealing chamber used for generating oxygen atoms by exposing ultraviolet light under ozone ambient in accordance with the prior art method of Fig. 1;

Fig. 3 is a flow chart illustrating a novel method of forming a tantalum oxide containing capacitor for DRAM applications according to an embodiment of the present
15 invention;

Figs. 4A through 4D are cross-sectional views showing the process steps of the novel method of forming a tantalum oxide containing capacitor for DRAM applications according to the embodiment of the present invention;

Fig. 5 is a schematic view of an ozone annealing chamber used for generating oxygen
20 atoms by heating a wafer-placed susceptor under ozone ambient in accordance with the present invention; and

Fig. 6 is a graph depicting the measured results of the tantalum oxide containing capacitors fabricated according to the novel method of the present invention and the prior art method.

25 ## Detailed Description of Preferred Embodiments

The process of the present invention improves the Ta_2O_5 film's properties, providing

a silicon nitride film having a thickness (for example, 20 ~ 100 angstroms) enough to prevent oxidation of the lower capacitor electrode, by a plasma nitridation process using a reactant gas (for example, NH_3 gas) during the step of pre-processing the surface of the lower capacitor electrode. Herein, the plasma nitridation process means that a plasma silicon
5 nitride film is formed by nitrifying a surface portion of the lower capacitor electrode by means of excitation of a reactant gas with a plasma. The plasma nitridation process is more effective not only to form the sufficiently thick silicon nitride film on the lower capacitor electrode but also to anneal the resulting substrate in the same process chamber. Furthermore, the process of the present invention is applicable to the more simplified
10 annealing mechanism, thereby providing cost saving of DRAM devices, by ozone annealing process using a susceptor-heating process for producing thermal energy of more than about 400°C. This is due to the more effective mechanism by the susceptor-heating ozone annealing as compared with regular UV ozone annealing. In the susceptor-heating ozone annealing process, the thermal energy is generated by heating a susceptor where wafers is
15 placed. This makes the heater used ozone annealing process superior to UV ozone annealing in the light of cost saving of DRAM devices.

Fig. 3 is a flow chart illustrating processing steps according to a preferred embodiment of the invention, and Figs. 4A through 4D show by cross-sectional representation the process steps (substantially, corresponding to those of Fig. 3) according
20 to the preferred embodiment of the invention.

Referring now to Fig. 3 and Fig. 4A, a supporting substrate 40 has been first prepared by prior fabrication steps of a conventional or non-conventional process. For example, the supporting substrate 40 may be comprised of a silicon wafer or simply a material that has been previously processed over a silicon (or germanium) substrate. Regardless of the nature
25 of substrate, the general concept of the present invention will focus on the subsequent nitridation of capacitor plate electrode, particularly, lower capacitor electrode.

Referring again to Figs. 3, and 4A, a conductive diffusion film 41 has been formed in the substrate 40. A lower capacitor electrode 42 is formed which connects to the diffusion

film 41. The electrode 42 need not connect directly to the diffusion film 41 as there may also be a connecting conductor, such as a conductive plug (through not shown), formed between the diffusion film 41 and the electrode 42. Through not required, it is preferred that the electrode 42 is conductively doped polysilicon. Assuming the electrode 42 is polysilicon,
5 it is now subjected to a pre-processing step shown in step 30 of Fig. 3, a plasma nitridation step using a reactant gas which converts a top surface of the polysilicon 42 into a plasma silicon nitride film (for example, Si_3N_4 film) 43 of about 20~100 angstroms in thickness. The reactant gas is selected from a group consisting of NH_3, N_2 and N_2O. The plasma silicon nitride film 43 serves as a reaction prevention film to prevent surface oxidation of the
10 electrode 42 during subsequent oxidation annealing steps. Herein, it is one of two key points of the present invention that the silicon nitride film 43 is formed having a thickness sufficient to prevent surface oxidation of the lower capacitor electrode 42 during subsequent oxidation annealing steps. If the comparatively thin silicon nitride film is formed on the top surface of the lower capacitor electrode 42 as in RTN (rapid thermal nitridation) of the prior
15 art, it can not withstand against surface oxidation of the electrode 42 during subsequent oxidation annealing steps. This is because oxygen atoms trend to be diffused penetrating the thin silicon nitride film into the electrode 42 during subsequent oxidation annealing steps. Thus, if the silicon nitride film having a sufficient thickness is not formed on the lower capacitor electrode 42, the oxygen atoms in a tantalum oxide film to be formed by
20 subsequent step react with silicon of the polysilicon electrode 42 to thereby form SiO_2 film on the electrode 42. As a result, a SiO_2 equivalent thickness T_{oxeq} is increased and thereby capacitance of finally fabricated DRAM cell capacitor is lowered. However, with the present invention, since the plasma silicon nitride film 43 can be formed having a thickness sufficient to prevent surface oxidation of the electrode 42, formation of SiO_2 film on the
25 electrode can be suppressed, although subsequent oxidation annealing steps are carried out at high temperature.

Next, as shown in Fig. 4B and in step 32 of Fig. 3, a capacitor dielectric film 44 of preferably amorphous tantalum oxide (Ta_2O_5) is formed over the plasma silicon nitride film

43. The amorphous Ta_2O_5 film 44 is formed by, for an example, low pressure chemical vapor deposition (LPCVD) using $Ta(OC_2H_5)_5$ with oxygen gas.

Subsequently, as shown in steps 34 and 36 of Fig. 3 and in Fig. 4C, the resulting substrate after formation of the capacitor dielectric film 44 is subjected to two continuous
5 annealing process steps, ozone (O_3) annealing and O_2 annealing. The ozone annealing process is carried out to fill up oxygen vacancies in the Ta_2O_5 film 44 with oxygen atoms in step 34 of Fig. 3. In this ozone annealing process, as shown in Fig. 5, oxygen atoms to be filled up into oxygen vacancies of the Ta_2O_5 film 44 are generated by heating by means of a heater 53 a susceptor 54 where wafers are placed. The ozone annealing process is
10 performed at a temperature of 300°C. to 600°C., preferably at about 450°C., at a pressure of 1 mTorr to 50 Torr. Herein, it is the other key point of the present invention that for the ozone annealing process generation of oxygen atoms for filling up oxygen vacancies of the Ta_2O_5 film 44 can be accomplished by heating the wafer-placed susceptor 54 preferably to about 450°C. Use of susceptor heating process to generate oxygen atoms is more effective
15 in simplification of ozone annealing mechanism as compared with regular UV ozone annealing process of the prior art. Also, during the ozone annealing process the silicon nitride film 43 may be converted into a film 43A which is composed of a composition of Si_3N_4 and SiO_2 or SiON. If the silicon nitride film 43 is formed having a very sufficient thickness, an extremely thin SiO_2 (or SiON) film (not shown) enough to exert no influence
20 on the DRAM cell capacitor may be formed on the silicon nitride film 43.

Of the two continuous annealing processes, the O_2 annealing process is in step 36 carried out at a high temperature, for example, at about 750°C.~800°C. to eliminate carbon or hydrogen carbon compound (C_xH_y) containing in the amorphous Ta_2O_5 film 44 and to allow densification of the amorphous Ta_2O_5 film 44. Since such carbon and/or hydrogen
25 carbon compound containing in the Ta_2O_5 film 44 serves as leakage current sources in DRAM cell capacitors, those sources must be eliminated to improve undesired leakage characteristics of the Ta_2O_5 film 44. The dielectric constant of the amorphous Ta_2O_5 film 44 is less than approximately twenty, but that of the Ta_2O_5 film 44 densified by the O_2 annealing

process is changed to twenty four. Thus, the dielectric constant of the Ta_2O_5 film 44 densified thus is approximately six times that of SiO_2. Furthermore, the initial thickness of the silicon nitride film 43 formed by the plasma nitrization was about 20~100 angstroms, and the resulting thickness after the O_2 annealing process was about 25~105 angstroms. In
5 addition to prevention of oxidation of the lower capacitor electrode, the resulting silicon nitride film 43A may serve as a leakage prevention barrier film so as to improve leakage of the Ta_2O_5 film 44. This is because the Ta_2O_5 film 44 has inherently high leakage current characteristics.

Next, as shown in step S38 of Fig. 3 and in Fig. 4D, a double-film structure electrode
10 of low resistance which is comprised of a chemical vapor deposited TiN and conductively doped polysilicon is formed to thereby form an upper capacitor electrode 45. The process then continues by conventional methods to complete the DRAM device.

Fig. 6 shows the measured results of the tantalum oxide containing capacitors fabricated according to the novel method of the present invention and the prior art method,
15 using MOS I-V measurement. As can be seen, since the silicon nitride film of the tantalum oxide containing capacitor which is fabricated by RTN process of the prior art is very extremely thin, the leakage was much worse, as shown by a curve line 60 of Fig. 6. This is because the silicon nitride film formed by RTN process does not have a thickness enough to prevent surface oxidation of the lower capacitor electrode, thus degrading the dielectric
20 properties. But, as shown by a curve line 62 of Fig. 6, it can be seen that the dielectric properties of the tantalum oxide containing capacitor formed according to the present invention is improved.

While this invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various
25 changes in form and details may be made without departing from the sprit and scope of this invention.

WHAT IS CLAIMED IS:

1. A method of forming a capacitor on a substrate having a conductive diffusion film therein, comprising the steps of:

forming a lower capacitor electrode on the substrate to connect electrically to the
5 conductive diffusion film;

forming a plasma silicon nitride film on the lower capacitor electrode, the plasma silicon nitride film serving as a reaction prevention film having a thickness sufficient to prevent oxidation of the lower capacitor electrode during subsequent oxidation annealing processes;

10 forming a high dielectric constant film of tantalum oxide on the plasma silicon nitride film;

performing an ozone annealing process to fill up oxygen vacancies in the tantalum oxide film with oxygen atoms;

performing an O_2 annealing process to densify the tantalum oxide film; and

15 forming an upper capacitor electrode on the plasma silicon nitride film,

wherein the steps of forming the plasma silicon nitride film and performing the ozone annealing process are carried out in same process chamber.

2. The method according to claim 1, wherein the lower capacitor electrode is made of a conductively doped polysilicon.

20 3. The method according to claim 1, wherein the step of forming the plasma silicon nitride film comprises converting a surface portion of the lower capacitor electrode into a silicon nitride film by exciting a reactant gas with a plasma.

4. The method according to claim 3, wherein the reactant gas is one selected from a group consisting of NH_3, N_2 and N_2O.

5. The method according to claim 1, wherein the thickness of the plasma silicon nitride film is in the range of 20~100 angstroms.

6. The method according to claim 1, wherein the oxygen atoms of the ozone annealing process are generated in the process chamber under ozone ambient by heating a
5 susceptor where the substrate is placed.

7. The method according to claim 1, wherein the ozone annealing process is performed at a temperature of 300°C. to 600°C., preferably at 450°C., at a pressure of 1 mTorr to 50 Torr.

8. The method according to claim 1, wherein the plasma silicon nitride film after the
10 O_2 annealing process is converted into a silicon nitride composition which is composed of Si_3N_4 and SiO_2 or SiON.

9. The method according to claim 1, wherein the O_2 annealing process is performed at a temperature of 750°C.~800°C.

The Patent Office

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Claims searched: 1-9

Examiner: Miss E.L.Rendle
Date of search: 4 March 1999

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Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): H1K (KFLS, KFLX)

Int Cl (Ed.6): H01L 21/3205, 21/70, 21/8242, 27/108

Other: EPOQUE: WPI, EPODOC, PAJ

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
Y	EP 0 046 868 A2	(IBM) see whole document, especially figure 4 and page 8 lines 1-26.	1, 2, 5, 7
Y	US 5 468 687	(IBM) see whole document.	1, 2, 5, 7
Y	Patent Abstracts of Japan abstract of JP07211791 & JP07211791, see abstract.		1
Y	Patent Abstracts of Japan abstract of JP5984570 & JP5984570, see abstract.		1

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