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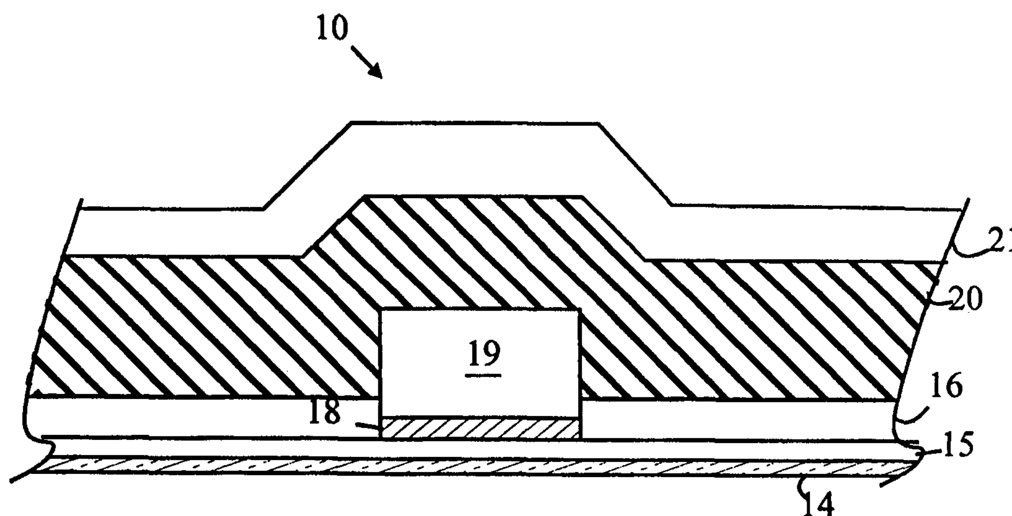
(54) Title: LEAD TITANATE ISOLATION LAYERS FOR USE IN FABRICATING PZT–BASED CAPACITORS AND SIMILAR STRUCTURES



(57) Abstract

A method for constructing a device (10) having a bottom electrode (18 and 19) in contact with a layer of a ferroelectric dielectric material (20). In the method of the present invention, a layer of a field ferroelectric material (16) is deposited on a substrate and etched to form a trench in which the bottom electrode (18 and 19) is constructed. The bottom electrode (18 and 19) is then deposited and a layer of the ferroelectric dielectric material (20) is deposited over the bottom electrode and at least a portion of the field ferroelectric material (16). The ferroelectric layers (16 and 20) are deposited in a perovskite state. These layers (16 and 20) are etched back to the substrate in those areas that are outside of the device (10).

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Lead Titanate Isolation Layers for Use in Fabricating PZT-Based Capacitors and Similar Structures

Field of the Invention

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The present invention relates to integrated circuits, and more particularly, to methods of constructing PZT containing structures on integrated circuits.

Background of the Invention

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Ferroelectric based capacitors are increasing in demand as integrated circuit elements. Capacitors having lead titanium zirconate (PZT) family of dielectrics offer large dielectric constants which, in turn, make the construction of small capacitors with relatively large capacitances possible. A ferroelectric capacitor consists of a PZT layer sandwiched between 15 two planar electrodes. Capacitors utilizing platinum electrodes are particularly advantageous, since such capacitors exhibit excellent crystallinity compared to capacitors utilizing other electrode materials.

Ferroelectric based field-effect transistors are also known to the art. These transistors 20 have a structure which may be viewed as a capacitor in which the top electrode has been replaced by a semi-conductor layer having two separated contacts corresponding to the source and drain of the transistor. The bottom electrode and ferroelectric layer are constructed in essentially the same manner as the bottom electrode and ferroelectric layer of a ferroelectric capacitor.

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An integrated circuit utilizing ferroelectric capacitor-like structures is typically constructed in two phases. First, the conventional CMOS circuits which connect to the ferroelectric devices are constructed in the silicon substrate. A protective layer of SiO_2 is then placed over the CMOS devices and the ferroelectric devices constructed on the 30 protective layer or on a second protective layer deposited over the SiO_2 layer. The ferroelectric devices are connected to the underlying CMOS devices by etching vias in the protective layer.

The bottom electrode and ferroelectric layer of a ferroelectric structure are typically constructed by depositing a patterned bottom electrode on the protective layer and then covering the surface with the ferroelectric layer. The top electrodes are then deposited and the electrode/ferroelectric layer is stack etched back to the protective layer.

For example, U.S. Patent 5, 242,534 describes a construction method in which a titanium oxide layer is formed over the SiO_2 layer. A layer of titanium is then deposited, and the layer is masked and etched in those regions that are to become the bottom electrode leaving a trench in the titanium layer. The bottom electrode, typically platinum or a titanium/platinum stack, is then deposited in the trench. The mask is then removed and the exposed titanium is oxidized. This leaves the regions between the bottom electrodes covered with titanium oxide and the bottom electrode recessed in the titanium oxide layer. The PZT dielectric layer is then deposited over the wafer. The top electrodes are typically deposited as a uniform layer. The top electrodes and dielectric layer are then stack etched back to the titanium oxide layer in the regions between the capacitor-like structures.

For the purposes of the present discussion, the regions between the capacitors will be referred to as the "field". The above described process requires the PZT dielectric layer to crystallize both over the platinum electrodes and in the field. The PZT compositions typically utilized for the dielectric layer can form two types of crystals, perovskite and pyrochlore. The PZT compositions and deposition conditions are chosen such that the portion of the layer that crystallizes over the platinum electrode is all perovskite. Unfortunately, these compositions and conditions do not lead to a pure perovskite layer over the titanium oxide in the field. Typically, the field contains a mixture of perovskite and pyrochlore.

The respective etch rates for perovskite and pyrochlore structures differ significantly, with pyrochlore structures etching at a much slower rate than perovskite structures. As a result, the stack etch leaves pyrochlore islands in the field. These structures make it difficult to etch the vias used to connect the ferroelectric structures to the underlying CMOS circuits in the field.

Broadly, it is the object of the present invention to provide an improved method for constructing ferroelectric based devices.

5 It is a further object of the present invention to provide a method for constructing ferroelectric based devices that do not lead to pyrochlore islands in the field region.

These and other objects of the present invention will become apparent to those skilled in the art from the following detailed description of the invention and the accompanying 10 drawings.

Summary of the Invention

The present invention is a method for constructing a device having a bottom electrode 15 in contact with a layer of a ferroelectric dielectric material. In the method of the present invention, a layer of a field ferroelectric material is deposited on a substrate. The bottom electrode is then deposited and a layer of the ferroelectric dielectric material is deposited over the bottom electrode and at least a portion of the field ferroelectric material. The dielectric ferroelectric layer that crystallizes over the field ferroelectric material is substantially all in 20 the same crystalline state which is preferably the perovskite state. These layers are etched back to the substrate in those areas that are outside of the device.

Brief Description of the Drawings

25 Figures 1-4 are cross-sectional views of the construction of a capacitor at various stages in a construction process according to the present invention.

Detailed Description of the Invention

30 The problems discussed above would be eliminated if the ferroelectric layer used for the dielectric crystallized completely as either a pyrochlore or perovskite. As long as the material is all of one type, the dielectric layer in the field can be etched back to the protective

layer without leaving the islands of pyrochlore discussed above. In the preferred embodiment of the present invention, the dielectric layer in the field is perovskite, since this form is easier to etch.

5 The preferred embodiment of the present invention is based on the observation that certain doped lead titanate compositions (PLT or PLZT) crystallize so quickly that these compositions do not require a nucleation source on the underlying surface to fully crystallize in the perovskite phase. Unfortunately, these compositions do not provide optimal electrical properties; hence, they cannot be used for the dielectric layer in the ferroelectric device. In
10 the present invention, lanthanum doped lead titanate is used in the field region on top of the titanium oxide.

Refer now to Figures 1-4 which are cross-sectional views of the construction of a capacitor 10 at various stages in the construction process. Referring to Figure 1, capacitor 10
15 is constructed on a substrate 12 which is presumed to have the circuitry to which capacitor 10 is to be connected. A protective layer of SiO_2 14 is assumed to cover substrate 12. However, other protective layers may be utilized.

A layer 15 of titanium oxide is first deposited over layer 14. This layer is preferably
20 formed by depositing a layer of metallic titanium, typically 200 Å thick, and then oxidizing this layer by heating in an oxygen environment. Next, a layer 16 of PLT or PLZT, typically 400 Å thick is deposited on layer 15. A photoresist mask 17 is then deposited and patterned to leave layer 16 exposed in the region 38 to be occupied by the bottom electrode of the capacitor. The mask must be of sufficient thickness to accommodate the bottom electrode
25 after the etching step discussed below.

PLT layer 16 is then etched back to titanium oxide layer 15 to create a trench in which the bottom electrode is to be deposited. A wet etch utilizing 1:1:3 HCL/BOE(6:1)/H_2O may be used for this step. It should be noted that a portion of the titanium oxide layer 15 may also
30 be etched away if a suitable etchant is utilized.

The bottom electrode is next deposited through the photoresist mask 17. In the preferred embodiment of the present invention, the bottom electrode consists of a layer of titanium 18 and a layer of platinum 19. The preferred thicknesses for these layers are 50 Å and 1500 Å, respectively. The titanium layer improves the adhesion of the bottom
5 electrode. After the deposition of the platinum layer, the photoresist mask is removed leaving the bottom electrode in a trench in the PLT layer as shown in Figure 2. The bottom electrode is then annealed in an oxygen environment to harden the electrode prior to the deposition of the ferroelectric dielectric layer.

10 Refer now to Figure 3. After the construction of the bottom electrode, a dielectric layer 20 comprising the electrical PZT, PLZT, or PNZT material is deposited over the bottom electrode and sintered. A platinum layer 21 is then deposited over dielectric layer 20. The platinum layer will become the top electrode of capacitor 10. The various layers are then etched. The portion of the dielectric layer in the field region is etched back to the titanium
15 oxide layer 15 leaving capacitor 10 as shown in Figure 4.

The top electrode may be formed by stack etching the dielectric and platinum layers. Alternatively, the top electrode may be patterned separately using a lift off process.

20 It should be noted that the both layer 20 and layer 16 are perovskite. Hence, the problems encountered when the field area contained pyrochlore regions have been eliminated and the etch will proceed cleanly to the underlying titanium oxide layer.

The etch rates of the ferroelectric layers depend on the dopant concentrations utilized
25 in each layer. Accordingly, in the preferred embodiment of the present invention, the compositions of the field ferroelectric material is chosen to follow that of the dielectric material. For example, if 4/20/80 PNZT is used for the dielectric layer 20, 15/0/100 PLZT is used for the field dielectric layer 16.

30 The above described embodiments of the present invention utilized a procedure in which the field ferroelectric material is deposited and sintered prior to etching the trench for the bottom electrode. However, embodiments in which the field ferroelectric material is

patterned and etched to form the trench prior to sintering may also be utilized. Since it is easier to etch the ferroelectric material prior to sintering, this embodiment of the present invention can provide better control of the dimensions of the bottom electrode. It does, however, require a second masking step for depositing the bottom electrode.

5

As noted above, the present invention may also utilize embodiments in which the dielectric material in the field region crystallizes as pyrochlore. While this material is more difficult to etch, the layer can still be etched back at a uniform rate, thereby leaving the top surface of the protective layer free of islands that might interfere with subsequent deposition

10 steps.

While the above embodiments have been described in terms of particular combinations of PNZT and PLZT layers, other combinations of material may also be utilized. For example, the field layer may also be constructed from PLT or PNZT provided the

15 concentrations of the components provides a surface in which the crystallization of the subsequently deposited dielectric layer results in a single crystalline phase. Dielectric layers may be constructed from PZT, PLZT, PNZT or other materials currently used for dielectric layers in ferroelectric-based capacitors.

20 Various modifications to the present invention will become apparent to those skilled in the art from the foregoing description and accompanying drawings. Accordingly, the present invention is to be limited solely by the scope of the following claims.

WHAT IS CLAIMED IS:

1. A method for constructing a device having a bottom electrode in contact with a layer of a ferroelectric dielectric material, said method comprising the steps of:

5

depositing a layer of a field ferroelectric material on a substrate;

depositing said bottom electrode;

10 depositing a layer of said ferroelectric dielectric material over said bottom electrode and at least a portion of said layer of said field ferroelectric material; and

etching said layer of said ferroelectric dielectric material and said field dielectric material in regions not occupied by said device, wherein said field ferroelectric material and
15 said ferroelectric dielectric material are chosen such that said layer of dielectric material that crystallizes over said field ferroelectric material is substantially all in the same crystalline state at the time of said etching.

2. The method of Claim 1 wherein said field material and said dielectric material are
20 chosen such that the portion of said dielectric layer over said field ferroelectric material is perovskite.

3. The method of Claim 1 wherein said ferroelectric dielectric material and said field ferroelectric material have substantially the same etch rates.

25

4. The method of Claim 1 wherein said ferroelectric dielectric material is chosen from the group consisting of PZT, PNZT, and PLZT.

5. The method of Claim 1 wherein said field ferroelectric dielectric material is chosen
30 from the group consisting of PLT, PLZT, and PNZT.

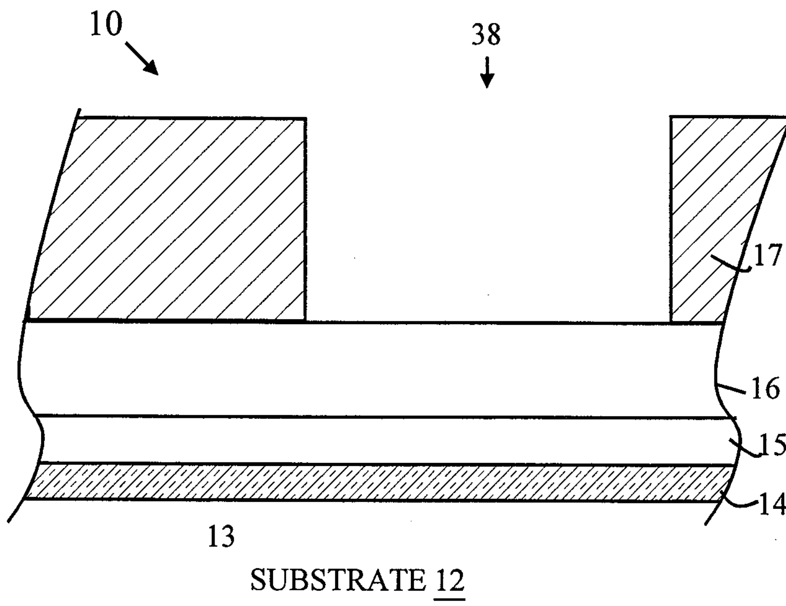

FIGURE 1

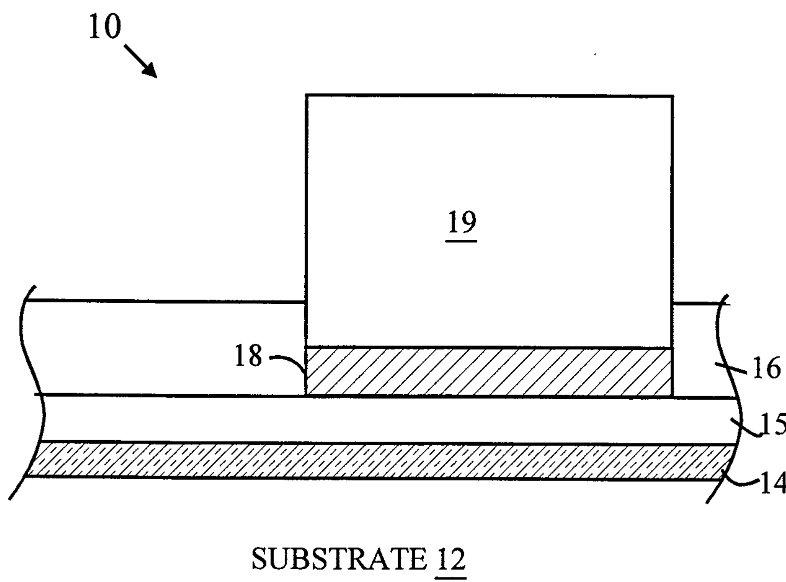

FIGURE 2

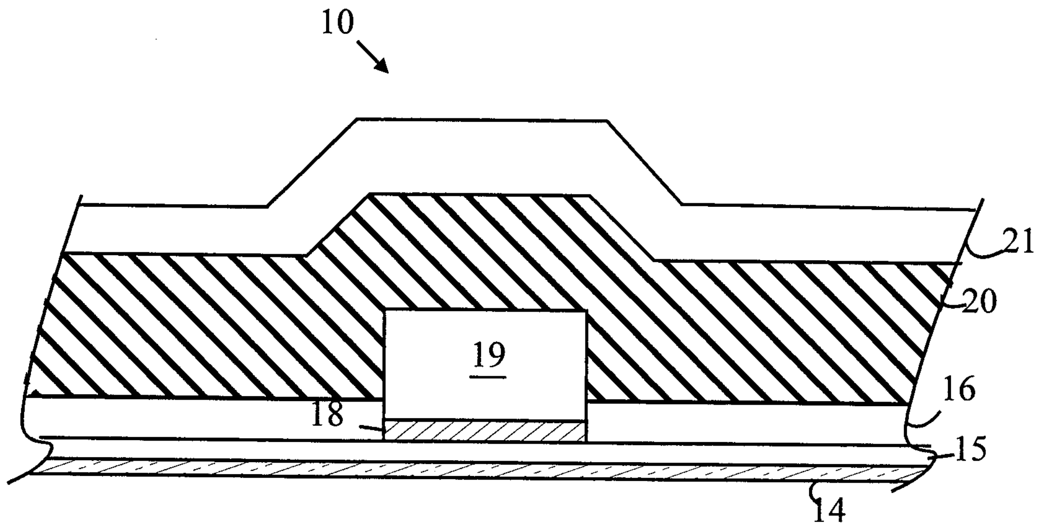

FIGURE 3

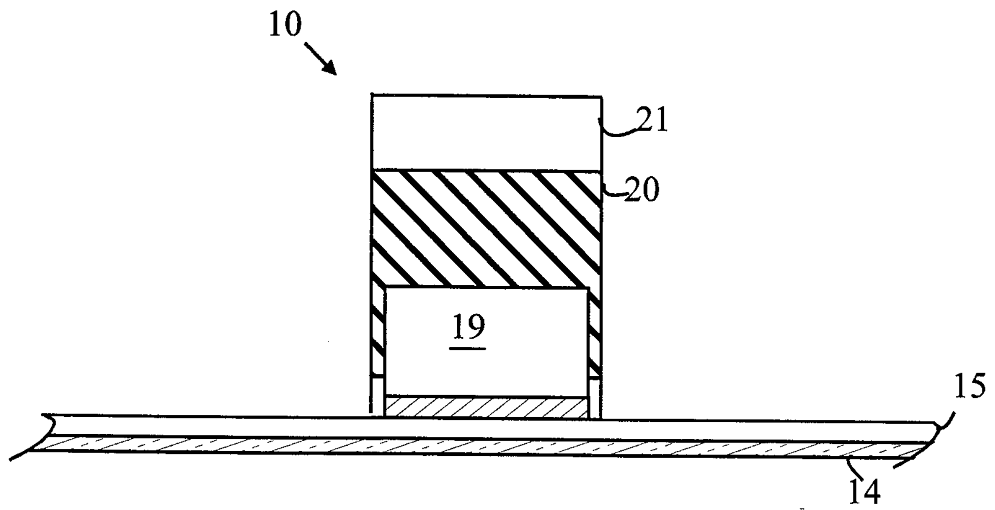

FIGURE 4

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/27928

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :Please See Extra Sheet.
US CL :438/240, 3, 396, 393

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : Please See Extra Sheet.

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,393,352 A (SUMMERFELT) 28 February 1995 (28/02/95), Figures 1, 2, and 3.	1
Y	US 5,326,721 A (SUMMERFELT) 05 July 1994 (05/07/94), Figures 1, 2, 3, and 4.	1
Y	US 5,242,534 A (BULLINGTON et al) 07 September 1993 (07/09/93), Figure 5.	1
Y	US 5,851,896 A (SUMMERFELT) 22 December 1998 (22/12/98), Figure 17.	1
Y	US 5,650,362 A (NASHIMOTO) 22 July 1997 (22/07/97), Figure 2.	1
Y	US 5,426,075 A (PERINO et al) 20 June 1995 (20/06/95), Figure 9.	1

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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International application No.
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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,731,220 A (TSU et al) 24 March 1998 (24/03/98), Figure 2.	1
A	US 5,736,449 A (MIKI et al) 07 April 1998 (07/04/98), see entire document.	1-5

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US98/27928

A. CLASSIFICATION OF SUBJECT MATTER:
IPC (6):

HO1L 21/8242, HO1L 21/70, HO1L 21/20, HO1L 29/12

B. FIELDS SEARCHED
Minimum documentation searched
Classification System: U.S.

438/240, 3, 396, 393, 239, 241, 242, 243, 244, 245, 246, 247, 248, 249, 250, 251, 252, 253, 254, 255, 256, 386, 387, 388, 389, 390, 391, 392, 394, 395, 397, 398, 399

B. FIELDS SEARCHED
Electronic data bases consulted (Name of data base and where practicable terms used):

U.S. PTO APS (USPAT file) and IEEE
serch terms: capacitor, ferroelectric?, PZT?, PNZT?, PLZT?, PLT?, lead titanate, lead zirconate, lithium niobate, lithium tantalate, perovskite, pyrochlore, lead zironate titanate, lanthanum?, neodymium?, piezoelectric?