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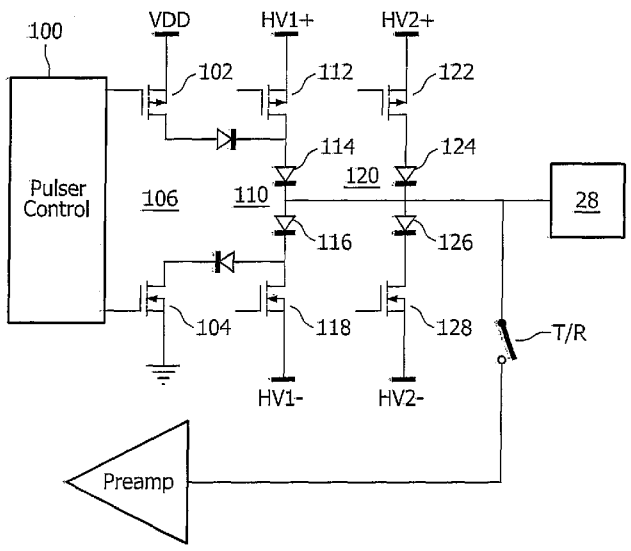

FIG. 3

(57) Abstract: An ultrasonic diagnostic imaging system transmitter produces transducer drive pulses of two or more bipolar pulse levels. The transmitter includes a first pair of drive transistors coupled between a first pair of bipolar high voltage levels and having an output coupled to an output terminal. A second pair of drive transistors is coupled between a second pair of bipolar high voltage levels and has an output coupled to the output terminal. Control logic is responsive to control bits for selecting one of the pairs of drive transistors and the polarity of the output pulse. Level translation circuitry translates control signals from the control logic to drive signals for the high voltage drive transistors, A active pull-to-ground circuit is operable to pull the output level to ground following an output pulse to control ring-down of the ultrasound transducer driven by the transmitter, and to present a high output impedance at the output when the transmitter is not enabled.

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DUAL PULSER FOR AN ULTRASONIC TRANSMITTER

This invention relates to medical diagnostic ultrasound systems and, in particular, to a transmitter for an array of ultrasound transducer elements which includes a dual level pulser.

In pulse-echo ultrasound imaging, an ultrasonic wave is transmitted into the body of a patient by the elements of a transducer array. By controlling the times at which individual elements are actuated the transmitted ultrasound can be steered in a desired direction and focused at a desired depth in the body. The energy of the transmitted waves is reflected by tissue and cells in the body and the resultant echo signals are received by the same transducer elements. The echo signals received by the individual elements are delayed by delay amounts necessary to bring the echo signals from a desired location into coherence. The properly delayed signals are combined to produce a coherent echo signal. By repeating this process for many directions and depths, echo data is acquired which enables an image to be formed of a two or three dimensional region of the body.

One way to control the ultrasound is to transmit beams in different directions over an image region which thoroughly scans the region to be imaged. For optimal resolution it is desirable to focus each beam as tightly as possible so that echo signals are predominately produced along each beam direction. However transmitted ultrasound beams have main lobes and sidelobes, much in the same way as an antenna. Echoes received from off-axis sidelobes can contribute noise and artifact signals to the desired signals from the main beam, resulting in noisy or

unclear images. One way to control sidelobe production is by the technique known as apodization. Transmit apodization weights the signals applied to different transducer elements differently so that the pattern of transmitted signals from the different transducer elements will exhibit a more favorable lobe pattern which contributes less noise and artifact signals to the ultrasound image. Different apodization patterns can be used for imaging at different depths so that the most favorable lobe pattern is developed for the desired focal depth of imaging. It is thus desirable to provide control of the transmit characteristics of each transducer element independently of the others, and it is further desirable to afford flexibility in the degree of control afforded, so that those who program the beamformer have as much control as possible over transmit apodization.

One way to provide a high level of control for transmit apodization is to drive each transducer element of the array with a controllable linear amplifier. This will enable a maximal degree of control over apodization, since the precise waveform transmitted by each transducer element can be precisely controlled. Such control is desirable for premium ultrasound systems, where the highest degree of image resolution is necessary, as are applications such as Doppler and harmonic imaging, where considerable control over transmit frequencies is needed. But for less expensive ultrasound systems, lower performing transmitters provide acceptable performance. A less expensive system can use pulse transmitters, where the signal applied to each transducer element is either on or off. The restriction to a simple on or off transmit signal

greatly reduces the degree of control that the beamformer designer has over apodization, however. Thus it is desirable to provide a greater degree of control for a pulser type of transmitter so that greater control over apodization is afforded.

In accordance with the principles of the present invention, a diagnostic ultrasound system is provided in which the elements of the ultrasound transducer are driven by a dual level pulser. The dual level pulser provides twice as many transmit levels as the standard pulser, or more, depending upon the implementation. The additional transmit levels afford double or more of the levels of control for transmit apodization than the conventional transmit pulser. A constructed embodiment of the present invention additionally provides an active pulldown drive for ringdown control and low power utilization for power-sensitive applications such as battery-powered ultrasound systems.

In the drawings:

FIGURE 1 illustrates in block diagram form an ultrasonic diagnostic imaging system constructed in accordance with the principles of the present invention.

FIGURES 2a and 2b illustrate two examples of spatial apodization control of a transducer array.

FIGURE 2c illustrates a pulse width modulated waveform produced by a dual level pulse of the present invention.

FIGURE 3 is a block diagram and schematic illustration of a dual level pulser of the present invention.

FIGURES 4a and 4b illustrate a dual level pulser of the present invention in schematic detail.

FIGURE 5 is a truth table for controlling the

operating states of the dual level pulser of FIGURES 4a and 4b.

FIGURES 6 and 7 illustrate a four-bit control scheme for the pulser of FIGURES 4a and 4b.

FIGURE 8 illustrates the control levels of a transmit waveform produced by one of the pulsers of the dual level pulser of FIGURES 4a and 4b.

Referring first to FIGURE 1, an ultrasound system constructed in accordance with the principles of the present invention is shown in block diagram form. Reference numeral 10 indicates the transducer array and beamformer of the ultrasound system. These components may all be contained within an ultrasound probe as shown in US Pat. 6,102,863 (Pflugrath et al.) Alternatively, the beamformer may be partitioned between a probe containing a microbeamformer which produces partially beamformed signals, and a mainframe system which performs the rest of the beamforming as described in US Pat. 5,229,933 (Larson, III). More conventionally, the probe will contain just the transducer stack and the transmit and receive beamformers are located in the mainframe system. The transmit beamformer 38 contains a plurality of transmitters which drive the transducer elements 28 of the transducer array stack 12. Echo signals received by the transducer elements are coupled by conductors 42_1, 42_2,... 42_N to preamplifiers and delays 46 of the receive beamformer 40. The amplified and delayed signals are coupled to a summer 48 which combines the delayed signals to produce coherent echo signals at an output 50. The coherent echo signals are coupled to an image processor 58 which produces an ultrasound image of tissue, flow or motion in the region of the body being scanned ultrasonically. A controller 52

controls the transmit and receive beamformers so that they operate in a properly interleaved manner, first transmitting transmit waves, then receiving and processing echoes in response. An input 56 is shown to the preamplifiers and delays 46 which sets the appropriate time delay for the signals from each transducer element. An input 54 is shown to the transmit beamformer which, in an implementation of the present invention, controls a dual level pulser.

As previously mentioned, the transducer array and beamformer can be partitioned differently in different embodiments. For instance, when the ultrasound probe only includes a transducer stack 12, conductors 42_1, 42_2,... 42_N will be conductors of the cable connecting the probe to the system mainframe and to the inputs 44_1, 44_2,... 44_N of the system mainframe beamformer. The brackets of groups of amplified and delayed signal lines between the preamplifiers and delays 46 and the summer 48 indicate that groups of signals may be combined in the probe and these partially beamformed signals coupled to the system mainframe where channels of the system mainframe beamformer complete the beamforming of the partially beamformed signals. In that implementations the final beamformer summer 48 will be in the system mainframe.

FIGURE 2a is a spatial illustration of transmit apodization which may be performed by a typical transmitter pulse of the prior art. The numbers 1... 32... 64... 128 along the bottom of the figure represent the transducer element numbers of a 128-element transducer array. In this example the transmit pulser does not drive elements 1-28 or elements 101-128. The elements that are driven to produce a transmit pulse in this example are elements 29-100 as

shown by the HV1 level in association with those elements. Those elements are pulsed at the HV1 voltage level at times appropriate for the steering and focusing of the desired transmit beam.

FIGURE 2b illustrates the type of apodization control which is possible with a dual level pulser of the present invention. The dual level pulser allows each transducer element to be driven at one of two transmit levels. In this example transducer elements 1-28 and 101-128 are not driven at all as in the previous example. However, of the active elements, elements 29-48 and elements 79-98 are pulsed at voltage level HV2 and elements 49-78 are pulsed at voltage level HV1. Each element is independently controlled by its own pulser as explained below. The choice of multiple levels affords the system designer enhanced control over the transmit waveform for transmission at selected depths or with improved sidelobe control.

FIGURE 3 is a partial block and schematic diagram of a dual level pulser of the present invention. Two output drive stages 110 and 120, each consisting of a stack of two oppositely poled MOSFET transistors 112,118 and 122,128 and diode pairs 114,116 and 124,126 are coupled by a common output to drive transducer element 28 with a transmit pulse. The drive stage 110 is powered by positive and negative high voltages HV1+ and HV1-, and the drive stage 120 is powered by positive and negative high voltages HV2+ and HV2-. Echo signals received by the transducer element 28 are coupled during reception by closure of a transmit/receive switch T/R to a preamplifier of the receive beamformer 40,46. In accordance with one aspect of the present invention an active pull-to-ground bipolar stage capable of

bilateral (bidirectional) current conduction, energized by logic power supply VDD and ground (GND), and including a bipolar stack of MOSFET transistors 102,104 and diodes 105,107, is also coupled to the pulser output. All of the transistors are switched by logically developed signals produced by pulser control 100, which is coupled to the gates of each of the six MOSFET transistors shown in FIGURE 3. The control signals produced by the pulser control 100 provide pulse width modulation control of the pulser and the bipolar high voltage output levels enable waveforms of controlled durations, frequencies, and amplitudes to be produced by each transducer element, as exemplified by the pulse width modulated waveform of FIGURE 3b.

FIGURES 4a and 4b illustrate a dual level pulser with its control logic in accordance with the present invention in schematic detail. The implementation of FIGURES 4a and 4b is constructed entirely of MOSFET transistors, diodes, and resistors and is capable of being fully integrated in integrated circuit form. Various semiconductor processes may be used. The dual level pulser is controlled by four digital control bits shown on the left side of FIGURE 6. A transmit enable bit (txen) enables the pulser for operation. A select bit (sel) selects one of the dual pulsers for operation. Input bits in1 and in2 control the selected pulser to produce either a positive high voltage (vhp_1 or vhp_2) or a negative high voltage (vhn_1 or vhn_2) or a reference (ground) drive voltage output pulse, with the width of the output pulse controlled by the bit duration. The four control bits are buffered and their complements produced by serial inverter pairs as shown in FIGURE 6.

A pulser for one bipolar high voltage (vhp_1 and vhn_1) is illustrated in FIGURE 4a and a pulser for another high voltage (vhp_2 and vhn_2) is illustrated in FIGURE 4b. The two pulsers are schematically the same, with the differences being in the applied control signals. Additionally, the positive and negative high voltage sections of each pulser are the same with the difference being the transistor polarity is reversed, respectively. This duality of design affords multiple dual level pulsers to be quickly and easily laid out for the same integrated circuit chip by replication. The pulser of FIGURE 4a will be described below, with the understanding that its description applies also to the complementary circuitry of the pulser of FIGURE 4b.

The txen_buf signal is coupled to an input of NAND gate 60 and an input of NAND gate 70 to enable the dual pulsers. When the sel_buf signal is high, the pulser of FIGURE 4a is selected for operation, and when the sel_buf signal is low, its complement sel_n (see FIGURE 6b) at the input of NAND gate 70 selects the pulser of FIGURE 4b for operation. The state of the sel bit thus selects which pulser is to be used for pulsing the transducer element coupled to the output "out." The NAND gate 60 selects the pulser of FIGURE 4a by switching the current source transistors 18 and 8 of two differential amplifier pairs into conduction to provide current for one of the differential pairs. The current source transistors 18 and 8 are biased to low voltage logic levels vdd and ground (gnd), respectively.

The differential amplifier pair of transistors 3,4 is enabled when the pulser of FIGURE 4a is to produce a negative high voltage (vhn_1) pulse and its mirrored replica, differential pair 13,14 is enabled

when the pulse is to produce a positive high voltage pulse. The differential amplifier pair 13,14 is enabled by the in1_buf signal applied to the gate of transistor 14 and its inverted complement is applied to the gate of transistor 13. Thus, differential pair 13,14 is enabled by the in1 bit (see FIGURE 6c). Similarly, differential pair 3,4 is enabled for a negative high voltage drive pulse by the in2_buf signal applied to NAND gate 62. The complement of in1_buf, in1_n, is applied to the other input of NAND gate 62. Since one input signal for this NAND gate is double buffered and the other is single buffered, a race condition at the input of NAND gate 62 and between gates 61 and 62 are prevented. Thus, differential pair 3,4 is enabled by the in2 bit (see FIGURE 6d). Supply current is provided to the supply electrodes of the differential pairs by current mirror circuits 6a,6b and 16a,16b, respectively. A single-ended output signal is used from the differential pairs, taken from the source electrodes of transistors 4 and 14, respectively.

The current drawn by the active one of the differential pairs drives a bipolar stack of transistors 20b,20a or 30b,30a, respectively, into conduction. The positive high voltage stack 30b,30a is coupled between the positive high voltage vhp_1 and ground, and the negative high voltage stack 20b,20a is coupled between the negative high voltage vhn_1 and ground. The flow of current through the two-transistor stack, biased by a resistor 24 or 34 to the respective high voltage supply, will pull the gate voltage of the respective high voltage drive transistor 40 or 42 toward ground, switching the drive transistor into conduction. When drive transistor 42 is conductive a positive high voltage

pulse (vhp_1) is produced at out, and when drive transistor 40 is conductive a negative high voltage pulse (vhn_1) is produced at the output terminal out.

The pulser of FIGURE 4b operates in a similar manner when it is selected by a high sel_n signal. When this pulser is selected and a positive in1 bit applied, transistor 42' will be conductive to produce a positive high voltage pulse (vhp_2) at the output terminal out, and a positive in2 bit will produce a negative high voltage pulse (vhn_2) at the output terminal. The logic truth table for the control signal bits for the pulser is shown in FIGURE 5.

As previously mentioned, this implementation of a dual level pulser also includes an active pull-to-ground function, which is provided by the coupling of transistors 50,52 to the output terminal by diodes 54,46 and 56,44, respectively. The pull-to-ground stage is powered by low voltage levels vdd and gnd and is controlled by the decoder logic shown in FIGURE 7. When the dual pulser is enabled by bit txen and producing either a positive or negative high voltage pulse, transistors 50 and 52 are turned off by control signals zero and zero_n. But when neither a positive or negative high voltage pulse is produced and the dual pulser remains enabled, the transistors 50 and 52 are switched on to pull the output terminal to ground potential (gnd). This enables control of the ringdown effect of the transducer being driven, as an active turn-off of the drive signal will dampen the ringdown effect.

But when the dual pulser is not selected (txen=zero), the transistors 50 and 52 are rendered nonconductive to neither source or sink current from the output terminal. This presents a high impedance to the transducer coupled to the output terminal.

Additionally the low txen bit (and low txen_buf signal) will render the sink current transistors 8,18 of the differential pair nonconductive and the transistors 32,34 and 22,24 will drain off any remaining charge at the input and output of the bipolar stacks 20b,20a and 30b,30a and away from the gate electrodes of the high voltage drive transistors 40,42. The dual pulser will thus be completely turned off and draw no current, a distinct advantage in battery-powered applications where current consumption is important.

The operation of the dual level pulser may be appreciated by referring to the switched pulser waveform of FIGURE 8. The txen bit will enable both pulsers and the sel bit will select one of the two pulsers to produce the illustrated waveform, which will produce a pulse of either the vhn_1 or vhp_1 level if the pulser of FIGURE 4a is selected, or a pulse of either the vhn_2 or vhp_2 level when the pulser of FIGURE 4b is selected. After these two bits are set, the setting of the in1 bit will cause the pulser to produce a +HV level pulse for the duration that the in1 bit is set, where +HV equals either vhp_1 or vhp_2. When the in1 bit is reset to zero the active pull-to-ground transistors 50,52 (106) are turned on to actively pull the output to the GND (gnd) level. When the in2 bit is set an output pulse at the -HV level is produced, where -HV equals either vhn_1 or vhn_2. When this pulse ends with the resetting of the in2 bit, the waveform is actively pulled back to the GND level by the pull-to-ground transistor pair 106. Thereafter the txen bit is reset to turn off the pulsers and the pulser output will present a high impedance to the output terminal out, as indicated by the dashed line Z.

Modifications and extensions of the principles of the present invention will readily occur to those skilled in the art. For example, additional pulser stages can be added and connected to the output terminal to produce transducer drive pulses of additional drive pulse levels. A three, four, or more level pulser can be produced thereby. In such a case the number of control bits must be increased to control the additional pulsers. More sophisticated transmit waveforms and apodization characteristics may thereby be implemented. The dual pulser of the present invention may be integrated in integrated circuit chips which contain 64 of the pulsers for 64 transducer elements, 128 pulsers for a 128-element array, or some other desirable level of circuit integration.

WHAT IS CLAIMED IS:

1. An ultrasonic diagnostic imaging system transmitter for driving an ultrasound transducer element with a plurality of bipolar drive pulse levels comprising:

a first pair of high voltage drive transistors coupled between a first set of bipolar high voltage supply levels and having a pair of control inputs and an output coupled to an output terminal;

a second pair of high voltage drive transistors coupled between a second set of bipolar high voltage supply levels and having a pair of control inputs and an output coupled to the output terminal; and

control logic, responsive to control signals for selecting one of the pairs of drive transistors and one of the bipolar voltage levels of the selected pair for an output pulse, is coupled to the control inputs of the first and second pairs of high voltage drive transistors.

2. The ultrasonic diagnostic imaging system transmitter of Claim 1, wherein the control logic is energized by a low voltage supply level.

3. The ultrasonic diagnostic imaging system transmitter of Claim 2, wherein the control signals comprise a plurality of control bits and wherein the control logic comprises at least one of decoder logic and buffer logic.

4. The ultrasonic diagnostic imaging system transmitter of Claim 2, further comprising:

level translation circuitry coupled between the control logic and the high voltage drive transistors

which is operable for translating low level control signals to high level drive signals for the high voltage transistors.

5. The ultrasonic diagnostic imaging system transmitter of Claim 4 wherein the level translation circuitry further comprises:

a plurality of differential amplifier pairs, each having an input responsive to the control logic and an output coupled to a control input of one of the drive transistors of a pair of high voltage drive transistors for translating a logic level drive signal to a high voltage transistor drive signal.

6. The ultrasonic diagnostic imaging system transmitter of Claim 5 wherein the level translation circuitry further comprises:

a pair of stacked bipolar transistors each having an input coupled to the output of a differential amplifier and an output coupled to the control input of a drive transistor and operable for switching the high voltage drive transistor.

7. The ultrasonic diagnostic imaging system transmitter of Claim 1, wherein the high voltage drive transistors comprise MOSFET transistors.

8. The ultrasonic diagnostic imaging system transmitter of Claim 1, wherein the control signals are operable for causing the high voltage drive transistors to produce pulse width modulated high voltage drive pulses of a plurality of high voltage levels.

9. The ultrasonic diagnostic imaging system transmitter of Claim 1, wherein the control signal are further operable to cause the transmitter to present a high impedance output at the output terminal.

10. An ultrasonic diagnostic imaging system transmitter for driving an ultrasound transducer element with bipolar drive pulse levels comprising:

a pair of high voltage drive transistors coupled between a set of bipolar high voltage supply levels and having a pair of control inputs and an output coupled to an output terminal;

control logic, responsive to control signals and coupled to the control inputs of the high voltage drive transistors for selecting one of the high voltage supply levels for an output pulse; and

an active pull-to-ground circuit responsive to a control signal for pulling the output terminal voltage to a reference level.

11. The ultrasonic diagnostic imaging system transmitter of Claim 10, wherein the reference level further comprises a ground level intermediate the high voltage supply levels.

12. The ultrasonic diagnostic imaging system transmitter of Claim 11, wherein the active pull-to-ground circuit further comprises a pair of transistors coupled between a low voltage supply level and ground level, each transistor having an input electrode responsive to a control signal and an output electrode coupled to the output terminal.

13. The ultrasonic diagnostic imaging system

transmitter of Claim 10, further comprising:

a second pair of high voltage drive transistors coupled between a second set of bipolar high voltage supply levels and having a pair of control inputs coupled to the control logic and an output coupled to an output terminal;

wherein the active pull-to-ground circuit is operable following the production of an output pulse by either the first pair of high voltage drive transistors or the second pair of high voltage drive transistors.

14. The ultrasonic diagnostic imaging system transmitter of Claim 1, further comprising an integrated circuit on which are integrated either 64 or 128 of the transmitter circuits of Claim 1.

15. The ultrasonic diagnostic imaging system transmitter of Claim 10, further comprising an integrated circuit on which are integrated 128 of the transmitter circuits of Claim 10.

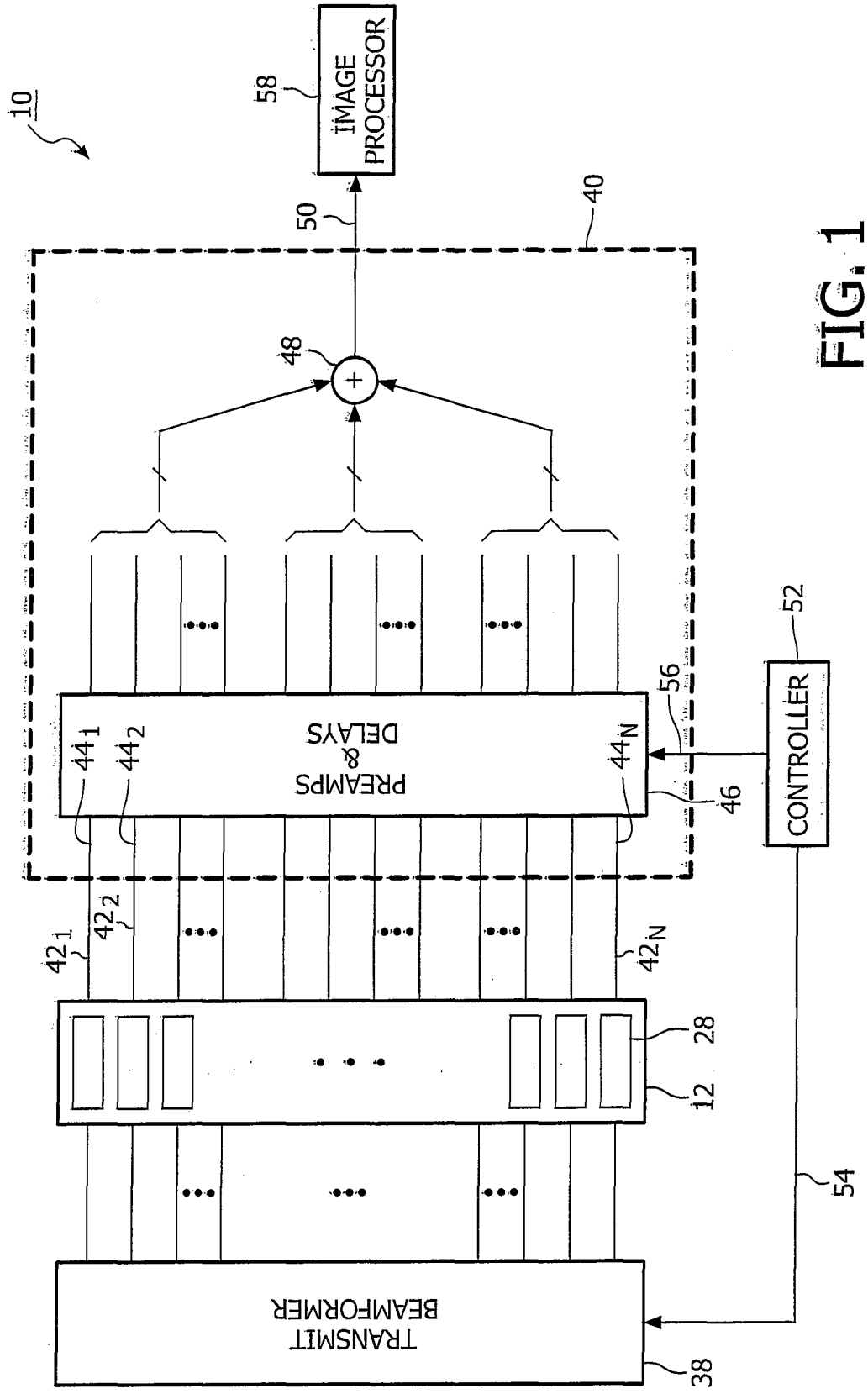

10
58
IMAGE PROCESSOR
50
40
48
52
56
PREAMPS & DELAYS
CONTROLLER
46
42 1
42 2
42N
28
12
54
TRANSMIT BEAMFORMER
38

FIG. 1

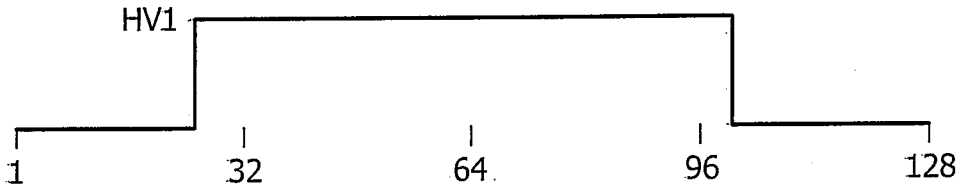


FIG. 2a

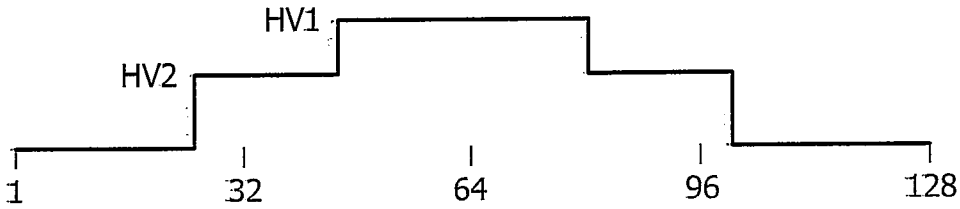


FIG. 2b

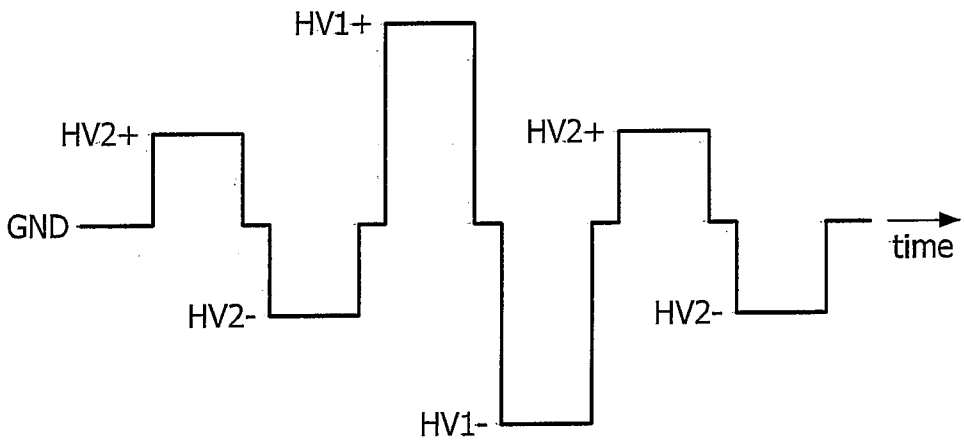


FIG. 2c

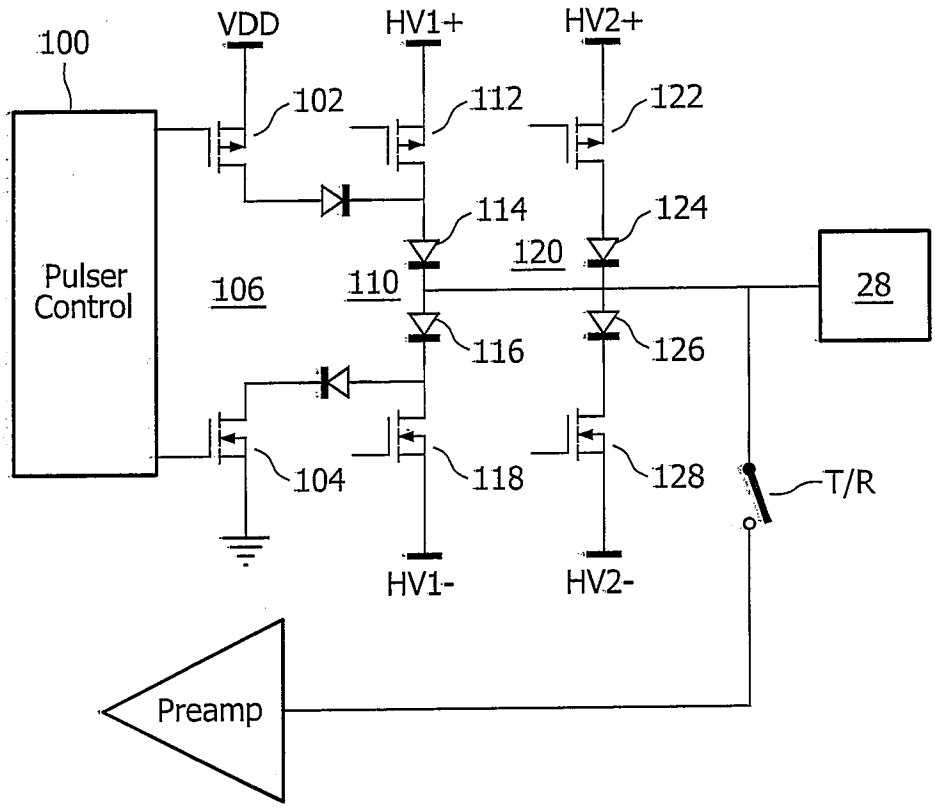


FIG. 3

PULSER TRUTH TABLE

in1	in2	sel	txen	out
X	X	X	0	Z
0	0	1	1	GND
0	1	1	1	-HV1
1	0	1	1	+HV1
1	1	1	1	+HV1
0	0	0	1	GND
0	1	0	1	-HV2
1	0	0	1	+HV2
1	1	0	1	+HV2

FIG. 5

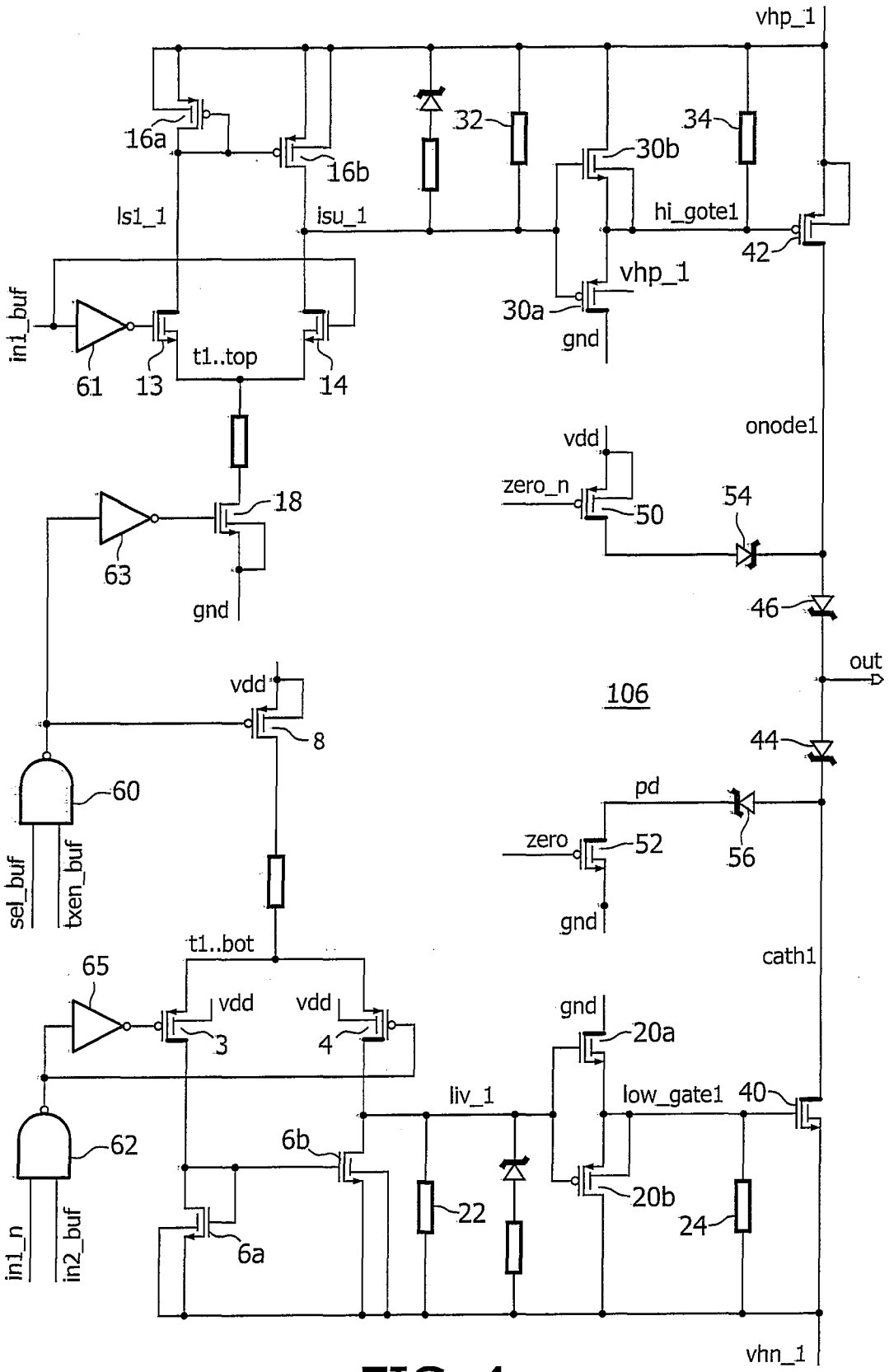
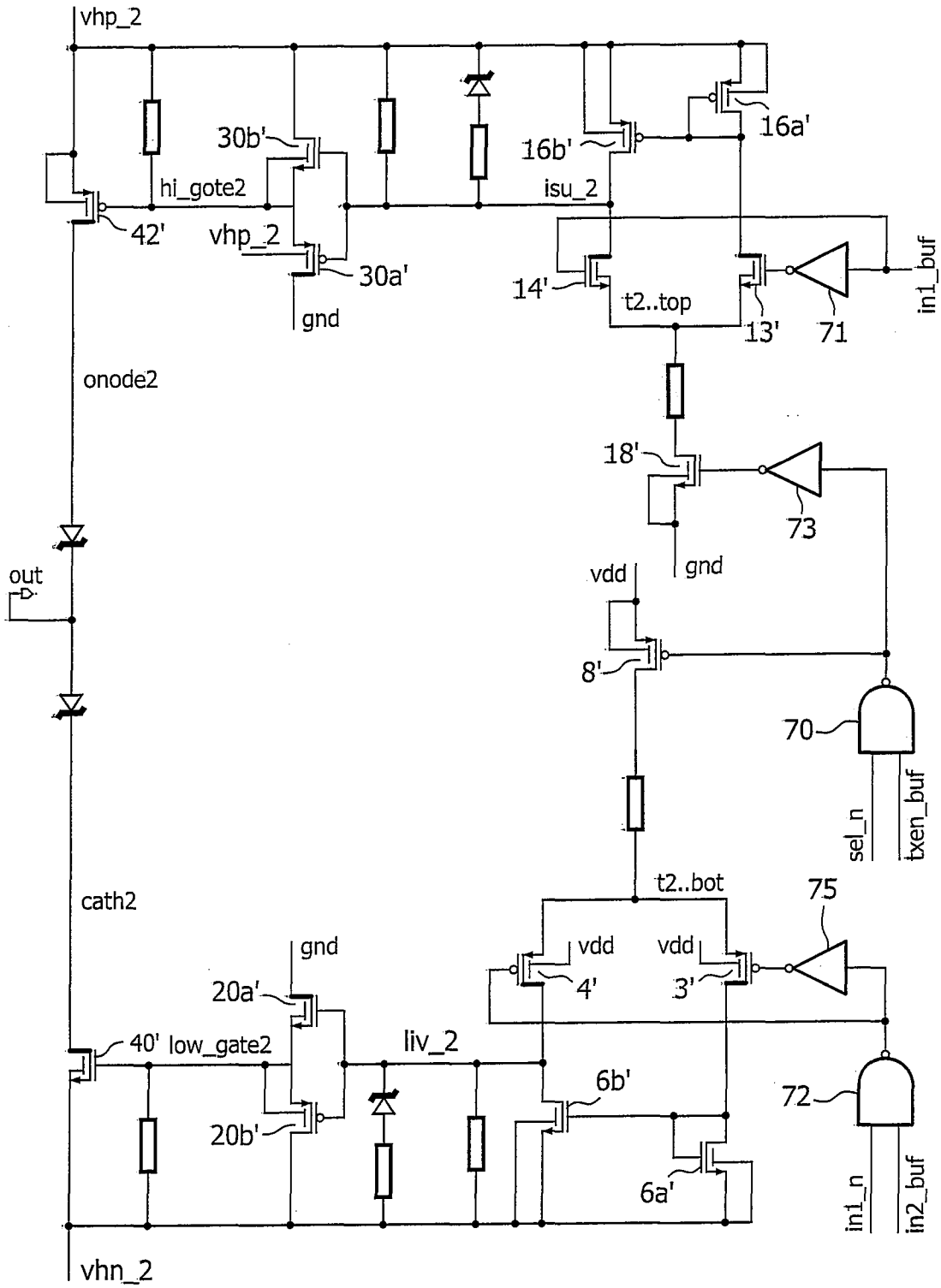

vhp_1
16a
16b
32
34
30b
ls1_1
isu_1
hi_gote1
42
vhp_1
30a
gnd
in1_buf
61
13
t1..top
14
onode1
vdd
zero_n
50
54
18
63
gnd
46
out
106
vdd
8
44
60
pd
zero
52
56
sel_buf
txen_buf
gnd
t1..bot
cath1
65
vdd
vdd
3
4
gnd
20a
liv_1
low_gate1
40
62
6b
22
20b
24
in1_n
in2_buf
6a
vhn_1

FIG. 4a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30b'
16b'
16a'
hi_gote2
isu_2
42'
vhp_2
30a'
gnd
14'
t2..top
13'
71
in1_buf
onode2
18'
73
gnd
out
vdd
8'
70
sel_n
txen_buf
t2..bot
75
cath2
gnd
vdd
vdd
20a'
4'
3'
40'
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72
20b'
6a'
in1_n
in2_buf
vhn_2

FIG. 4b

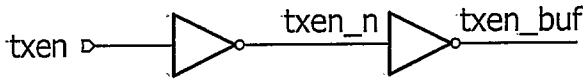

FIG. 6a

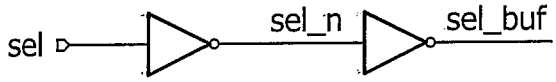

FIG. 6b

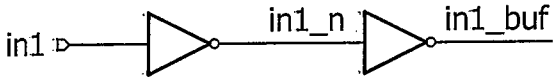

FIG. 6c

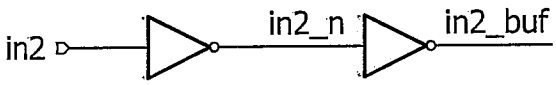

FIG. 6d

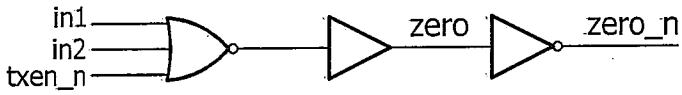

FIG. 7

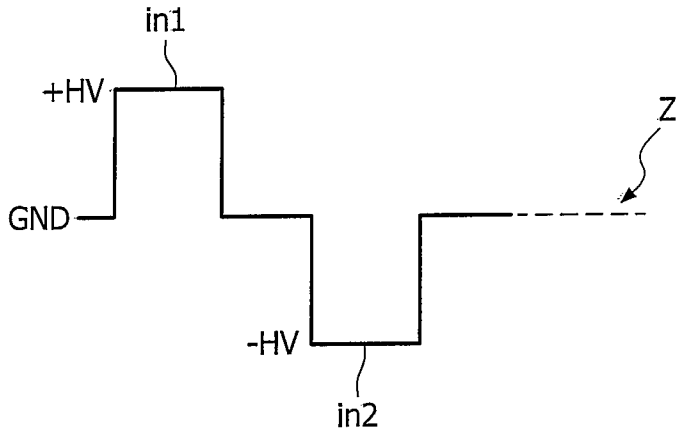

FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/054752

A. CLASSIFICATION OF SUBJECT MATTER
INV. B06B1/02 G01S7/52 G01S7/524

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
B06B G01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2004/254459 A1 (KRISTOFFERSEN KJELL [NO] ET AL) 16 December 2004 (2004-12-16) abstract; figures 1,2,4,5,14 paragraphs [0001] - [0011] paragraphs [0039] - [0053] -----	1-15
X	US 6 432 055 B1 (CARP STUART L [US] ET AL) 13 August 2002 (2002-08-13) abstract; figures 1,21 column 1, line 5 - column 3, line 7 column 5, line 31 - column 6, line 21 column 12, line 37 - column 13, line 10 -----	1-15
X	US 2008/066552 A1 (AMEMIYA SHINICHI [JP]) 20 March 2008 (2008-03-20) abstract; figures 1,2 paragraph [0001] - paragraph [0011] paragraph [0033] - paragraph [0049] -----	10-13,15
	-/--	

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 January 2010	08/02/2010

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Zaneboni, Thomas

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2009/054752

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 2005/154300 A1 (WODNICKI ROBERT G [US] ET AL) 14 July 2005 (2005-07-14) the whole document	1-15
A	HATFIELD J V ET AL: "A beam-forming transmit ASIC for driving ultrasonic arrays" SENSORS AND ACTUATORS A, ELSEVIER SEQUOIA S.A., LAUSANNE, CH, vol. 92, no. 1-3, 1 August 2001 (2001-08-01), pages 273-279, XP004274057 ISSN: 0924-4247 Section "5. High-voltage output stage"	1-15
A	US 5 138 187 A (MATSUSHIMA TETSUYA [JP] ET AL) 11 August 1992 (1992-08-11) the whole document	1-15
A	JP 2006 101997 A (TOSHIBA CORP; TOSHIBA MEDICAL SYS CORP) 20 April 2006 (2006-04-20) the whole document	1-15

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2009/054752

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2004254459 A1	16-12-2004	DE 102004027025 A1	30-12-2004
		JP 2005000663 A	06-01-2005
US 6432055 B1	13-08-2002	NONE	
US 2008066552 A1	20-03-2008	CN 101144797 A	19-03-2008
		DE 102007043956 A1	30-04-2008
		JP 2008068014 A	27-03-2008
		KR 20080025324 A	20-03-2008
US 2005154300 A1	14-07-2005	DE 102004063413 A1	28-07-2005
		JP 2005193036 A	21-07-2005
US 5138187 A	11-08-1992	JP 1787634 C	10-09-1993
		JP 2044273 A	14-02-1990
		JP 4079586 B	16-12-1992
JP 2006101997 A	20-04-2006	NONE	