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(54) **PROCESS FOR POLISHING A SEMICONDUCTOR WAFER**

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(57) **ABSTRACT**

A process is for the simultaneous polishing of the front surface and the back surface of a semiconductor wafer between two rotating polishing plates covered with polishing cloth while a polishing fluid is supplied, the polishing cloth of the lower polishing plate having a smooth surface and the polishing cloth of the upper polishing plate having a surface which is interrupted by channels. The semiconductor wafer lying in a cutout in a carrier plate is held on a defined geometric path. The front surface of the semiconductor wafer, during polishing, is in contact with the polishing cloth of the lower polishing plate. The back surface of the semiconductor wafer, during polishing, is in contact with the polishing cloth of the upper polishing plate.

PROCESS FOR POLISHING A SEMICONDUCTOR WAFER

CROSS REFERENCE TO RELATED APPLICATION

[0001] Priority is claimed under 35 U.S.C. §119 of German Application No. 103 21 940.4 filed May 15, 2003.

BACKGROUND OF THE INVENTION

[0002] 1. Field of the Invention

[0003] The present invention relates to a process for polishing a semiconductor wafer which results in an improved nanotopology of the polished semiconductor wafer. Semiconductor wafers of this type are suitable for use in the semiconductor industry, in particular for the fabrication of electronic components.

[0004] 2. The Prior Art

[0005] A semiconductor wafer which is intended to be suitable in particular for the fabrication of electronic components with line widths of less than or equal to 0.10 μm must have a large number of particular properties. One particularly important property is what is known as the nanotopology of the semiconductor wafer.

[0006] The term "nanotopology" or "nanotopography" is defined by SEMI (Semiconductor Equipment and Materials International) as the planarization deviation of the entire wafer front surface in the range of spatial wavelengths from 0.2 to 20 mm (lateral correlation length) and within the "quality zone" (FQA: fixed quality area; surface area for which the properties required by the product specification have to be satisfied). The nanotopology is measured by scanning the entire wafer surface completely and with an overlap using measurement fields of different sizes. None of the height variations in the surface (peak to valley) found in these measurement fields may exceed the required maximum value for the entire wafer. The sizes of the measurement fields are dependent on specifications and are defined, for example, at 2×2 mm^2, 5×5 mm^2 and 10×10 mm^2.

[0007] The final nanotopology of a semiconductor wafer is generally produced by a polishing process. To improve the flatness of a semiconductor wafer, apparatus and processes for the simultaneous polishing of front and back surfaces of the semiconductor wafer have been made available and developed further.

[0008] This so-called double-side polishing is described, for example, in U.S. Pat. No. 3,691,694. According to an embodiment of double-side polishing which is described in EP208315B1, semiconductor wafers in carrier plates made from metal or plastic which have suitably dimensioned cutouts are moved between two rotating polishing plates covered with a polishing cloth, in the presence of a polishing fluid, on a path which is predetermined by the machine and process parameters and are thereby polished (in the specialist literature, carrier plates are also referred to as templates).

[0009] The double-side polishing step is carried out using a polishing cloth made from homogenous, porous polymer foam with a hardness of from 60 to 90 (Shore A), as described, for example, in DE10004578C1. This document also discloses the fact that the polishing cloth which adheres to the upper polishing plate has a network of channels, and the polishing cloth which adheres to the lower polishing plate has a smooth surface without any such texture. This measure is intended firstly to ensure a homogenous distribution of the polishing abrasive used during polishing, and secondly to prevent the semiconductor wafer from sticking to the upper polishing cloth when the upper polishing plate is lifted off after the polishing has ended.

[0010] For double-side polishing, the semiconductor wafer is placed into a cutout in a carrier plate in such a way that the back surface of the semiconductor wafer rests on the lower polishing plate. During polishing, therefore, the back surface of the semiconductor wafer is polished by the untextured polishing cloth which adheres to the lower polishing plate, and the front surface of the semiconductor wafer is polished by the textured polishing cloth adhering to the upper polishing plate. The front surface of the semiconductor wafer is the surface which is intended for the fabrication of electronic components. After the polishing step, the semiconductor wafers are generally transferred into an aqueous bath, for example with the aid of a vacuum suction means.

[0011] This process according to the prior art is not able to satisfy the ever increasing demands imposed with regard to the nanotopology of semiconductor wafers which have undergone double-side polishing for future generations of components.

SUMMARY OF THE INVENTION

[0012] Therefore, it is an object to provide a process which makes it possible to produce a semiconductor wafer with an improved nanotopology, so that it satisfies even the demands imposed for the fabrication of particularly demanding components.

[0013] The above object is achieved according to the present invention which provides a process for the simultaneous polishing of the front surface and the back surface of a semiconductor wafer between two rotating polishing plates covered with polishing cloth while a polishing fluid is supplied, the polishing cloth of the lower polishing plate having a smooth surface and the polishing cloth of the upper polishing plate having a surface which is interrupted by channels, and the semiconductor wafer lying in a cutout in a carrier plate and being held on a defined geometric path, wherein the front surface of the semiconductor wafer, during polishing, is in contact with the polishing cloth of the lower polishing plate, and wherein the back surface of the semiconductor wafer, during polishing, is in contact with the polishing cloth of the upper polishing plate.

[0014] The starting product for the process is a semiconductor wafer which has been separated from a crystal in a known way, for example has been separated from a silicon single crystal which has been cut to length and rounded by grinding, and the front and/or back surface of which has been machined by means of a grinding or lapping step. It is also possible for the edge of the semiconductor wafer to be rounded at a suitable point in the process sequence by means of an appropriately profiled grinding wheel. Moreover, it is possible for the surface of the semiconductor wafer to be etched following the grinding step.

[0015] According to the invention, to prepare for double-side polishing, the semiconductor wafer is placed into a

cutout in a carrier plate in such a manner that its front surface rests on the polishing cloth of the lower polishing plate. During double-side polishing, therefore, the front surface of the semiconductor wafer is in contact with the smooth polishing cloth of the lower polishing plate, while the back surface of the semiconductor wafer is in contact with the textured polishing cloth of the upper polishing plate. Otherwise, the double-side polishing is carried out in the manner with which the person skilled in the art is familiar.

[0016] The end product of the process is a semiconductor wafer which has undergone double-side polishing and has a significantly improved nanotopology.

[0017] The process according to the invention can in principle be used to produce a body in wafer form which consists of a material which can be processed using the chemo-mechanical double-side polishing process employed. Materials of this type, the further processing of which is predominantly in the semiconductor industry, but is not restricted to this particular application, include, for example, silicon, silicon-germanium, silicon dioxide, silicon nitride, gallium arsenide and further III-V semiconductors. Silicon in single crystal form, for example crystallized by a Czochralski pulling process or a float zone pulling process, is preferred. Silicon with a **(100)**, **(110)** or **(111)** crystal orientation is particularly preferred.

[0018] The process is particularly suitable for the production of silicon wafers with diameters of in particular 200 mm, 300 mm, 400 mm and 450 mm and thicknesses from a few hundred μm to a few cm, preferably from 400 μm to 1200 μm. The semiconductor wafers can either be used directly as starting material for the fabrication of semiconductor components or, after a final polishing step has been carried out in accordance with the prior art and/or after layers, such as back surface sealing layers or an epitaxial coating of the wafer front surface with silicon or other suitable semiconductor materials, have been applied and/or after conditioning by means of a heat treatment, can be fed to their intended use.

[0019] The process will be described further on the basis of the example of the production of a silicon wafer.

[0020] In principle, it is possible for a silicon wafer which has been sawn using an annular sawing or wire sawing process and which, depending on the diameter and type of sawing process, has areas with a damaged crystal lattice down to a depth of from 10 to 40 μm, to be subjected to the double-side polishing step according to the invention directly. However, it is preferable for the sharply defined and therefore mechanically highly sensitive wafer edge to be rounded with the aid of a suitably profiled grinding disc prior to the double-side polishing. Furthermore, to improve the geometry and partially remove the damaged crystal layers, it is possible for the silicon wafer to be subjected to a mechanical abrasion step, such as lapping or grinding, in order to reduce the amount of material removed in the polishing step according to the invention. An etching step may follow at this point in order to remove the areas of the crystal at the wafer surface and edge which have inevitably been damaged in the mechanical process steps and to remove any impurities which may be present, for example metallic impurities which are bound up in the damage. This etching step may be carried out either as a wet-chemical treatment of the silicon wafer in an alkaline or acidic etching mixture, or as a plasma treatment.

[0021] A commercially available double-side polishing machine of suitable size, as described, for example in IBM Technical Report TR22.2342, can be used to carry out the polishing step according to the invention. The polishing machine substantially comprises a lower polishing plate, which can rotate freely in the horizontal plane, and an upper polishing plate, which can rotate freely in the horizontal plane, both of these plates being covered with a polishing cloth, and allows material-removing polishing of both sides of semiconductor wafers, in this case silicon wafers, when a polishing fluid of a suitable chemical composition is supplied continuously.

[0022] It is possible to polish just one silicon wafer. In general, however, for cost reasons a multiplicity of silicon wafers are polished simultaneously, the number being dependent on the construction of the polishing machine. The silicon wafers are held on a geometric path which is defined by machine and process parameters during polishing by carrier plates which have cutouts of sufficient size to hold the silicon wafers. The carrier plates are in contact with the polishing machine by means for example of a pin gearing or an involute gearing via a rotating inner pin or toothed ring and a generally opposite rotating outer pin or toothed ring, and are thereby set in rotary motion between the two polishing plates.

[0023] Examples of parameters which influence the path of the silicon wafers in relation to the upper and lower polishing plates during the polishing operation include the dimensions of the polishing plates, the design of the carrier plates and the rotational speeds of the upper polishing plate, of the lower polishing plate and the carrier plate. If there is in each case one silicon wafer in the center of a carrier plate, the silicon wafer moves in a circle around the center of the polishing machine. If a plurality of silicon wafers are positioned eccentrically in a carrier plate, rotation of the carrier plates about their own axis results in a hypocycloidal path. A hypocycloidal path is preferred for the polishing process according to the invention. The simultaneous use of four to six carrier plates, which each carry at least three silicon wafers arranged at regular intervals on a circular path, is particularly preferred.

[0024] In principle, the carrier plates which are used in the process according to the invention can be made from any material which is sufficiently mechanically stable with respect to the mechanical loads caused by the drive, in particular the compressive and tensile loads. Moreover, the material must not be significantly chemically and mechanically attacked by the polishing fluid used and the polishing cloths, in order to ensure a sufficient service life of the carrier plates and to prevent contamination of the polished silicon wafers. Furthermore, the material must be suitable for the production of highly planar, stress-free and undulation-free carrier plates of the desired thickness and geometry. In principle, the carrier plates may, for example, be made from metal, plastic, fiber-reinforced plastic or plastic-coated metal. Carrier plates made from steel or from fiber-reinforced plastic are preferred; carrier plates made from stainless chromium steel are particularly preferred.

[0025] The carrier plates have one or more cutouts, preferably circular in shape, for holding one or more silicon wafers. To ensure that the silicon wafer can move freely in the rotating carrier plate, the cutout has to be slightly larger

in diameter than the silicon wafers which are to be polished. A diameter which is larger by 0.1 mm to 2 mm is preferred; a diameter which is larger by 0.3 to 1.3 mm is particularly preferred. To prevent damage to the edge of the wafer from the inner edge of the cutout in the carrier plate during polishing, it is expedient and therefore preferred for the inner side of the cutout to be provided with a plastic lining of the same thickness as the carrier plate, as proposed in EP208315B1.

[0026] The carrier plates for the polishing process according to the invention have a preferred thickness of from 400 to 1200 μm, preferably depending on the final thickness of the polished silicon wafers, as described in DE19905737A1. The amount of silicon removed by the polishing step is from 5 to 100 μm, preferably from 10 μm to 60 μm, and particularly preferably from 20 to 50 μm.

[0027] Within the context of the statements made with regard to the orientation of the semiconductor wafers with the front surface facing downward, the double-side polishing step is preferably carried out in the manner which is known to the person skilled in the art. Polishing cloths with a wide range of properties are commercially available. It is preferable to carry out the polishing using commercially available polyurethane polishing cloth with a hardness of from 40 to 120 (Shore A). Polyurethane cloths with incorporated polyethylene fibers in a hardness range of from 60 to 90 (Shore A) are particularly preferred. In the case of the polishing of silicon wafers, the continuous supply of a polishing fluid with a pH of preferably from 9 to 12, particularly preferably 10 to 11, comprising preferably 1 to 10% by weight (% by weight), particularly preferably 1 to 5% by weight, of SiO_2 in water, is recommended, the polishing pressure preferably being from 0.05 to 0.5 bar, particularly preferably from 0.1 to 0.3 bar. The silicon removal rate is preferably from 0.1 to 1.5 μm/min and particularly preferably from 0.4 to 0.9 μm/min.

[0028] The percent by weight of SiO_2 is based upon the total weight of the polishing fluid.

[0029] When the polished semiconductor wafers are being unloaded from the lower polishing plate, the semiconductor wafers are preferably placed into a standard process rack which treats them further with their surfaces in the correct orientation in subsequent process steps. It is possible to avoid the need to turn the semiconductor wafers through 180° if the rack into which the semiconductor wafers are placed is arranged rotated through 180° compared to conventional double-side polishing, in which the semiconductor wafers are polished with the front surface facing upward. This measure can be carried out equally well with manual unloading or with automatic unloading by a robot. A measure of this nature is also conceivable when loading the lower polishing plate with semiconductor wafers.

[0030] The polished semiconductor wafers are removed from the lower polishing plate either manually or by means of an automatic removal apparatus; in both cases, it is preferred to use a vacuum suction means. A suitable vacuum suction means is described in DE19958077A1 (page 6, lines 23-30). The semiconductor wafers are preferably transferred, immediately after removal, into a liquid, preferably aqueous bath. In this way, it is possible to effectively prevent polishing abrasive from drying on and to prevent the formation of imprints of the vacuum suction means or, in general terms, of the removal appliance.

[0031] After the polishing has ended, any adhering polishing fluid is cleaned off the silicon wafers and the wafers are dried.

[0032] Depending on their further use, it may be necessary for the front surface of the wafers to be subjected to final polishing in accordance with the prior art, for example, using a soft polishing cloth with the aid of an alkaline polishing fluid based on SiO_2.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0033] Other objects and features of the present invention will become apparent from the following detailed description considered in connection with the accompanying examples. It is to be understood, however, that the examples are designed as an illustration only and not as a definition of the limits of the invention.

EXAMPLES

[0034] A commercially available double-side polishing machine of type AC2000 P^2 produced by Peter Wolters, Rendsburg, Germany was used for the Example, and the Comparative Example. The polishing machine was equipped with five carrier plates made from stainless chromium steel with a lapped surface and a thickness of 720 μm, each having six circular cutouts with an internal diameter of 200.5 mm, which were arranged at regular intervals on a circular path and were lined with polyvinylidene fluoride, allowing the simultaneous polishing of 30 silicon wafers with a diameter of 200 mm per batch. The upper and lower polishing plates were covered with a commercially available polyurethane polishing cloth reinforced with polyethylene fibers, SUBA500 produced by Rodel with a hardness of 74 (Shore A). The polishing cloth stretched over the lower polishing plate had a smooth surface; the surface of the polishing cloth stretched over the upper polishing plate had a chessboard-like pattern of milled channels with a width of 1.5 mm and a depth of 0.5 mm, having the profile of a segment of a circle, which channels were arranged at intervals of 30 mm.

COMPARATIVE EXAMPLE

[0035] In each case 30 silicon wafers with an etched surface and a diameter of 200 mm were placed manually into the cutouts in the carrier plates with the front surface facing upward. The polishing process was carried out with a continuous supply of an aqueous polishing abrasive of type Levasil 200 produced by Bayer, Leverkusen, Germany, with a fixed SiO_2 solids content of 3.1% by weight (w %) and a pH which was set to 11.4 by additions of potassium carbonate and potassium hydroxide. The polishing was carried out under a pressure of 0.2 bar at a temperature of the upper and lower polishing plate of in each case 38° C. and led to a material-removal rate of 0.58 μm/min. 15 μm of silicon was removed from each surface of the wafer. After the polished wafers had reached a thickness of 725 μm, the supply of polishing abrasive was ended and was replaced by the supply of a stopping agent for a period of 2 min. The stopping agent used was an aqueous solution of 1 w % Glanzox 3600 produced by Fujimi, Japan. After the stopping step had ended and the installation had been opened, the silicon wafers positioned in the carrier plates were com-

pletely wetted with stopping liquid. The silicon wafers were transferred into a rack located in an aqueous bath using a commercially available unloading station produced by Peter Wolters. Then, the silicon wafers were dried in a batch cleaning installation with a bath sequence of $TMAH/H_2O_2$; HF/HCl; ozone; Hcl and using a commercially available dryer operating in accordance with the Marangoni principle. The nanotopology of the cleaned wafers was measured on an ADE SQM CR83 using the measurement fields 2 mm×2 mm (HCT 2×2) and 10 mm×10 mm (HCT 10×10). A total of 1968 silicon wafers were polished and their nanotopology was then examined.

EXAMPLE (INVENTION)

[0036] A total of 2157 silicon wafers with an etched surface and a diameter of 200 mm were treated in a similar way to the Comparative Example. The only difference with respect to the Comparative Example was that the silicon wafers were placed into the cutouts in the carrier plates with the front surface facing downward and then polished in this orientation. The results of the statistical analysis of the nanotopology values are given in the table.

Measurement	Comparative Example: 1968 Silicon wafers		Example: 2157 Silicon wafers	
field	HCT 2x2	HCT 10x10	HCT 2x2	HCT10x10
Mean	18.50	40.48	15.24	33.06
Standard deviation	4.87	9.65	2.06	5.66

[0037] The comparison reveals a significantly improved nanotopology of the silicon wafers, if they were polished with the front surface facing downward, for both sizes of measurement field.

[0038] Accordingly, while a few embodiments of the present invention have been shown and described, it is to be understood that many changes and modifications may be made thereunto without departing from the spirit and scope of the invention as defined in the appended claims.

What is claimed is:

1. A process for the simultaneous polishing of a front surface and a back surface of a semiconductor wafer between two rotating polishing plates covered with polishing cloth while a polishing fluid is supplied,

the polishing cloth of a lower polishing plate having a smooth surface and the polishing cloth of an upper polishing plate having a surface which is interrupted by channels, and said semiconductor wafer lying in a cutout in a carrier plate and being held on a defined geometric path,

wherein the front surface of the semiconductor wafer, during polishing, is in contact with the polishing cloth of the lower polishing plate, and

wherein the back surface of the semiconductor wafer, during polishing, is in contact with the polishing cloth of the upper polishing plate.

2. The process as claimed in claim 1,

wherein following the simultaneous polishing of the front surface and the back surface of the semiconductor wafer,

transferring said semiconductor wafer into an aqueous bath with the aid of a vacuum suction means.

3. The process as claimed in claim 1, comprising

subjecting the front surface of the semiconductor wafer to final polishing following the simultaneous polishing of the front surface and the back surface.

4. The process as claimed in claim 1,

wherein the semiconductor wafer is a silicon wafer.

5. The process as claimed in claim 1,

wherein the semiconductor wafer is placed into the cutout in the carrier plate with the front surface in a facing downward orientation, and

polishing said wafer in said downward orientation.

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