(12) UK Patent Application (19) GB (11) 2 250 866 (13) A

(43) Date of A publication 17.06.1992

(21) Application No 9125275.9

(22) Date of filing 27.11.1991

(30) Priority data
(31) 02321183 (32) 27.11.1990 (33) JP
03285718 04.10.1991

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(51) INT CL[5]
H05K 3/24

(52) UK CL (Edition K)
H1R RAF R14

(56) Documents cited
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GB 1492506 A GB 1310880 A GB 1228651 A

(58) Field of search
UK CL (Edition K) C7F FHAA FHAB, H1R RAD RAE RAF RAG RAH RAV
INT CL[5] H05K
Online databases: WPI

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(54) Method of coating solder on a printed circuit

(57) A method of preparing a printed circuit comprises forming a wiring pattern on a substrate and coating a solder alloy including tin and lead as major components on the wiring pattern by means of electroless plating. The substrate is dipped in a solution to wet it and then dipped in a plating solution including 0.1 mole/l of tin, 0.01 mole/l of lead, 0.2 mole/l of organic sulfonic acid and 2 mole/l of thiourea. A solder resist may be applied to those parts of the wiring pattern not to be coated with solder. The printed circuit may include a multi-layered substrate.

Preparation of a printed wiring substrate having a wiring pattern

Process 8-1
Degreasing

Process 8-2
Soft-etching

Process 8-3
Pickling

Process 8-4
predipping

Process 8-5
Electroless solder plating

Process 8-6
Activating solder surface

FIGURE I

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy.

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FIGURE 1

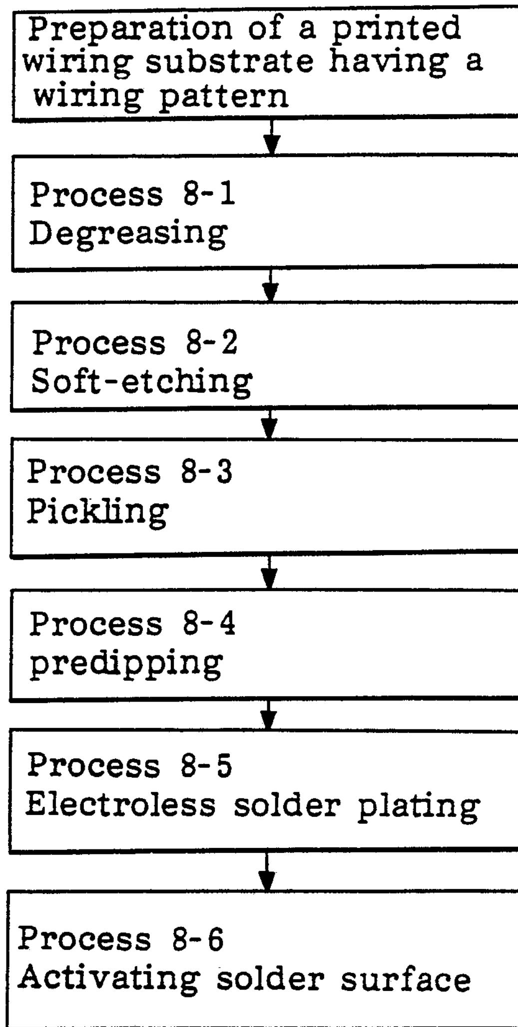


FIGURE 2

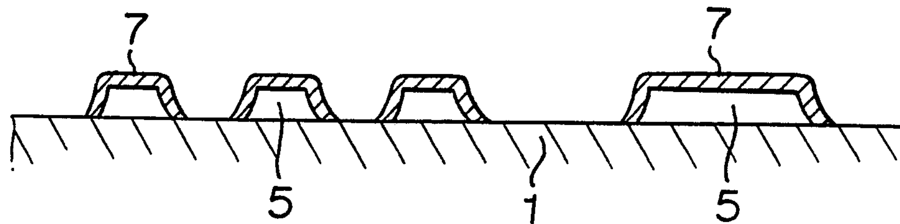
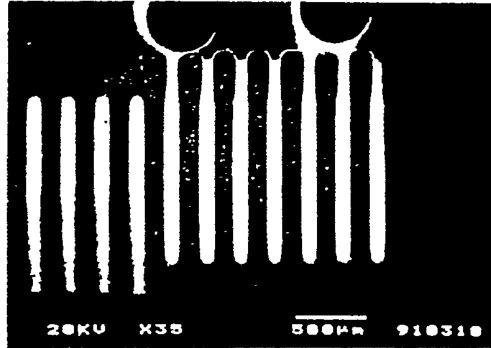


FIGURE 3

(A)



(B)

FIGURE 4

Number	Film thickness (μm)	Composition (Sn%)
1	12.5	58
2	11.8	57
3	10.7	61
4	11.2	59
5	12.6	63
6	12.2	62
7	11.4	55
8	12.3	65
9	12.8	57
10	11.8	59
Average	11.9	59.6

FIGURE 5

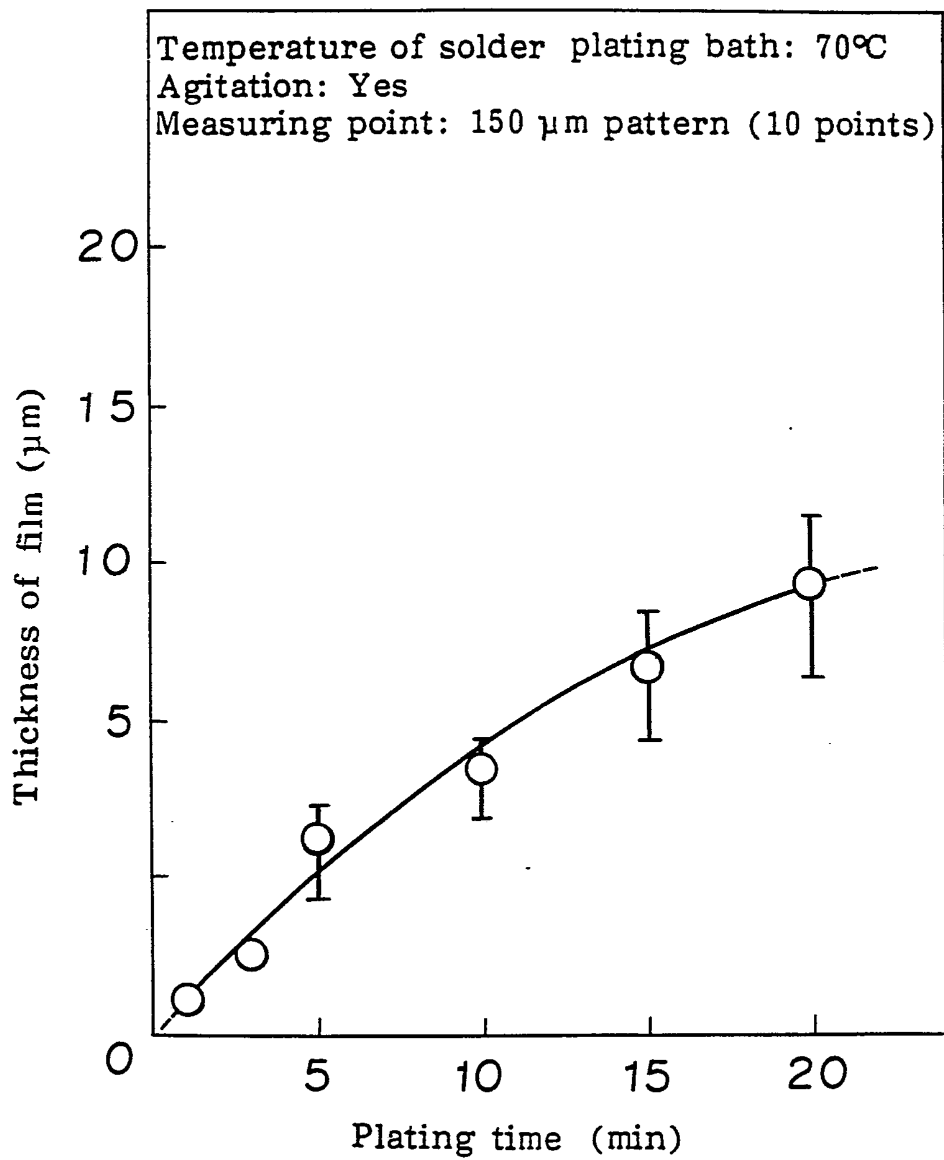
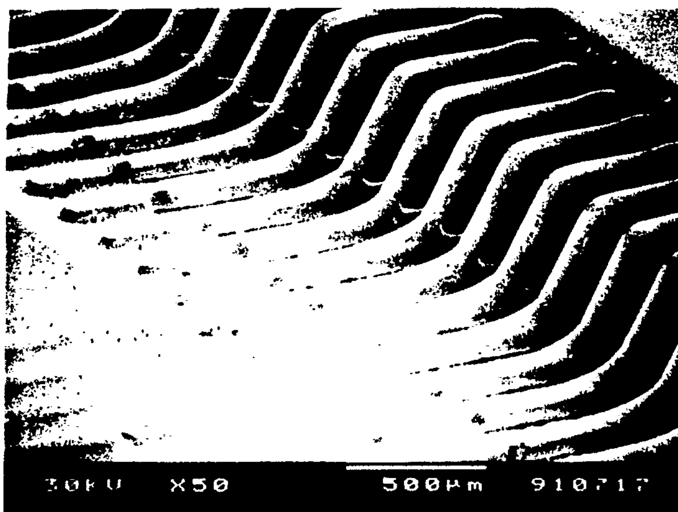


FIGURE 6

(A)



(B)

FIGURE 7

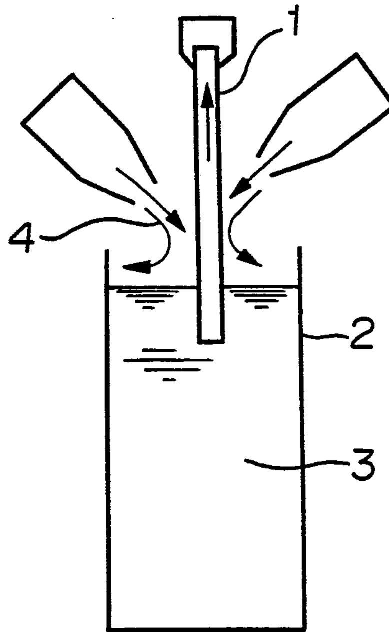


FIGURE 8

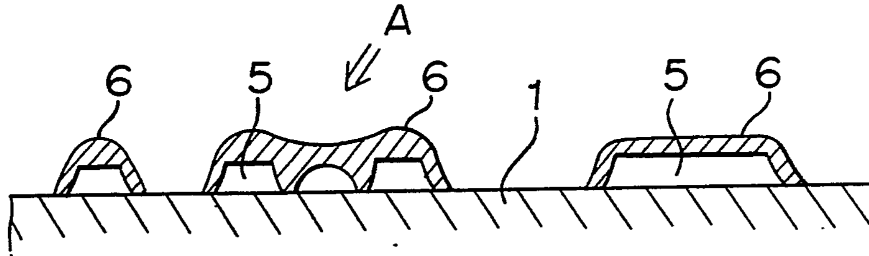
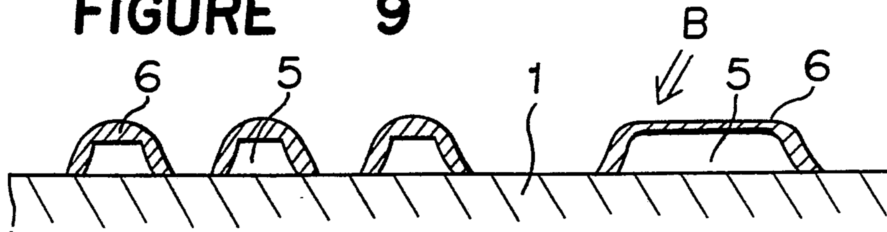


FIGURE 9



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METHOD OF PREPARING A PRINTED SUBSTRATE

The present invention relates to a method of
5 preparing a printed substrate. More particularly, it
relates to a method of preparing a printed substrate in
which solder is coated on a wiring pattern.

A conventional method of coating solder on a wiring
pattern of copper on a substrate will be described, by
10 taking a hot-air-leveling method as an example, with
reference to Figure 7.

The printed substrate 1 which has been subjected to a
patterning operation and the coating operation of a
solder resist is immersed for a predetermined time in a
15 vessel 2 in which the solder 3 is received in a molten
state. When the printed substrate 1 is raised from the
vessel, gas 4 of high temperature and high pressure is
blasted on the substrate surface to blow off an excessive
amount of solder deposited on the wiring pattern of
20 copper; thus the solder is covered at a predetermined

portion of the wiring pattern of copper.

A method of preparing a multi-layered printed substrate in which the above-mentioned solder coating technique is used will be described.

5 Process 1: patterning electric conductive plates which constitute inner layers.

Process 2: treating the surface of the electric conductive plates constituting inner layers (blackening).

Process 3: laminating layers including the inner

10 layers and pressing the lamination.

Process 4: forming a through hole in the lamination.

Process 5: copper-plating the lamination.

Process 6: patterning wire lines on the lamination.

Process 7: printing a solder resist and symbols.

15 Process 8: hot-air-leveling of solder.

Process 9: processing the outer configuration of the printed substrate.

However, the conventional method of preparing a printed substrate had problems as follows. Namely, as

20 shown in Figures 8 and 9, it was difficult to uniformly and evenly cover the solder 6 on the copper wiring pattern 5, and the thickness of the solder layer was apt to be large due to the interfacial tension of the solder 6 at the portion where the surface area of the copper

25 wiring pattern was small and the distance between the patterned wires was narrow, whereby there was a danger of short-circuitting between adjacent wires (as indicated by

A in Figure 8). On the other hand, when a pressure of gas 4 for blowing off an excessive amount of the solder 6 was made large in order to avoid the danger of short-circuitting, the thickness of the solder layer on the
5 wiring pattern became insufficient (indicated by B in Figure 9), wettability became inferior when structural elements were mounted and reliability to the connection of the elements was reduced.

Further, when element mounting positions were to be
10 determined by means of an image recognition device, accurate positions could not be obtained because the solder has a curved surface which tends to be glossy and therefore, a sight around the solder was reflected.

It is an object of the present invention to provide a
15 method of preparing a printed substrate capable of coating uniformly and evenly solder on the wiring pattern irrespective of the magnitude of the surface area in which the wiring pattern is formed, without causing unevenness in the surface of the solder, eliminating a
20 danger of short-circuitting even at a portion in which the surface area of the wiring pattern is small and the distance between adjacent wires is narrow, providing high reliability to the connection of the structural elements, improving recognizing capability of an image recognition
25 device when the structural elements are to be mounted, and increasing the positional precision of the elements.

In accordance with the present invention, there is

provided a method of preparing a printed substrate comprising a step of forming a wiring pattern on a substrate and a step of coating a solder alloy including tin and lead as major components on the wiring pattern by
5 means of electroless plating.

In accordance with the present invention, there is provided a method of preparing a printed substrate comprising a step of forming a wiring pattern on a substrate, a step of applying a solder resist to a part
10 of the wiring pattern, and a step of coating a solder alloy including tin and lead as major components on the remaining exposure portion of the wiring pattern by means of electroless plating.

In the method of preparing the printed substrate
15 according to the present invention, a plating solution for electroless plating including 0.1 mole/ℓ of tin, 0.01 mole/ℓ of lead, 0.2 mole/ℓ of organic sulfonic acid and 2 mole/ℓ of thiourea as major components is used.

Since the electroless plating is used for the present
20 invention, solder coated on an exposed metal wiring pattern has a flat surface and an even thickness.

In drawings:

Figure 1 is a flow chart showing the processes of electroless plating as major processes in detail in a
25 method of preparing a printed substrate according to Example 1 of the present invention;

Figure 2 is a diagram in cross-section which shows a

surface portion of the printed substrate prepared by the electroless plating in Example 1;

Figure 3A is a picture showing the surface area of a solder layer formed on the printed substrate;

5 Figure 3B is a picture which shows a part of the solder layer in a large scale;

Figure 4 is a characteristic diagram showing relations of the thickness of the solder layer and the formulation of tin in the layer shown in Figure 3;

10 Figure 5 is a characteristic diagram showing the relation of plating time and the thickness of the solder layer in an electroless plating process in Figure 1;

Figure 6 shows an example obtained by soldering an IC package on the solder layer in Figure 3 wherein Figure 6A 15 is a picture showing a state at a soldered portion and Figure 6B is a picture showing a part of the soldered portion in a large scale;

Figure 7 is a diagram illustrating how solder is coated on a printed substrate by means of hot-air- 20 leveling method;

Figure 8 is a diagram in cross-section showing a surface area of a printed substrate prepared by a conventional method; and

Figure 9 is a diagram in cross-section showing 25 another example of a surface area of a printed substrate prepared by a conventional method.

Preferred embodiment of the method of a printed

substrate of the present invention will be described.

EXAMPLE 1

An example of preparing a printed substrate having a wiring pattern of copper, will be described.

5 Process 1: patterning electric conductive plates which constitute inner layers.

Process 2: treating the surface of each of the electric conductive plates.

Process 3: laminating plates including the inner

10 conductive plates, and pressing them.

Process 4: drilling a through hole in the lamination.

Process 5: copper-plating of a panel.

Process 6: patterning a multi-layered electric conductive plate (by a pattern-plating method or a

15 tenting method).

Process 7: printing a solder resist and symbols.

Process 8: electroless solder plating.

Process 9: processing the outer configuration of the multi-layered electric conductive plate.

20 By the above-mentioned processes, a printed wiring board in which solder is coated on the copper wiring pattern by means of electroless plating is obtainable.

In the above-mentioned processes, the processes 8 and 9 may be substituted for each other.

25 Next, the process of electroless solder plating in the process 8 will be described in detail.

Process 8-1: degreasing (an acid type)

Stain and oil on the surface of the printed wiring board and oxides on the copper wiring pattern are removed.

Process 8-2: soft-etching (ammonium persulfate aqueous solution)

The surface of the copper wiring pattern is etched by about 0.5 μm-2 μm to expose a clean copper surface.

Process 8-3: pickling (dilute sulfuric acid)

Oxides on the copper surface are removed.

Process 8-4: predipping

Before conducting the regular dipping of the printed substrate, it is dipped into a liquid having the same pH and the same concentration of an additive as those of the regular solder bath to wet the printed substrate so as to stabilize the precipitation of the solder, to prevent impurities from entering in the regular solder bath and to prolong the service life of the plating solution.

Process 8-5: electroless solder plating (acid type)

A plating solution for electroless plating including 0.1 mole/ℓ of tin, 0.01 mole/ℓ of lead, 0.2 mole/ℓ of organic sulfonic acid and 2 mole/ℓ of thiourea as major components was used. Electroless plating was conducted on a copper foot pad pattern on a substrate having a pitch of 250 μm and a width of 100 μm at plating temperature of 70°C for 15 minutes.

Figure 3 shows a state of the solder layer coated on the copper foot pad pattern which is obtained in

accordance with the above-mentioned process. Figure 4 shows the relation of the thickness of the solder layer and the formulation of tin.

In the case of using the plating solution for 5 electroless plating having the composition described above, the solder layer having a desired thickness can be formed on the copper foot pad pattern by adjusting a plating time as shown in Figure 5.

A reaction takes place at the interface of 10 copper/plating solution in the electroless plating of solder whereby a solder layer is formed without suffering any influence from an adjacent copper foot pad pattern. Further, since the reaction takes place only at the interface of copper/plating solution, the original shape 15 of the copper foot pad pattern can be maintained even when the solder layer is precipitated, and the upper portion of the copper foot pad pattern 5 can keep a flat state as shown in Figure 2.

Thus, according to this Example, a flat solder layer 20 7 can be accurately formed on the copper foot pad pattern having a minute pitch.

Figures 6A and 6B show an example wherein an IC package is soldered by a pulse heat method at 270°C for 5 minutes on the foot pad pattern on which a solder layer 25 is coated in accordance with the processes described above.

On measuring peel strength at the soldered portion,

it was found that a lead wire of the IC package is broken without peeling at the soldered portion. Thus, an excellent result could be obtained.

As described above, in this Example, a solder layer
5 having a thickness which is precisely controlled can be formed on a foot pad pattern having a minute pitch of a printed substrate, and accordingly, an IC package having a minute pitch can be easily attached by soldering to the foot pad pattern.

10 Process 8-6: Activating the solder surface (acid type)

Stain and oxides on the solder layer are removed.

EXAMPLE 2

In the above Example 1, the solder resist is applied to a part of the wiring pattern and the solder alloy is
15 coated on the remaining exposed portion by electroless plating. In this Example, however, the solder alloy is coated on the entire wiring pattern without the application of the solder resist, by electroless plating. The same effect can be obtained in this Example.

20 The solder alloy coated on the copper wiring pattern may contain antimony of 1 wt% or less.

The degreaser used for the process 8-1 may be of an alkali type.

For the soft-etching in the process 8-2, a solution
25 comprising sodium persulfate, potassium persulfate, sulfuric acid + hydrogen peroxide, or ammonium persulfate + sulfuric acid as major components may be used.

For the pickling in the process 8-3, organic acid, hydrochloric acid or nitric acid may be used.

The copper wiring pattern may be formed by a fully additive process or a semi-additive process.

5 One or more processes among the processes 8-1 to 8-6 for the electroless solder plating may be omitted.

In the printed substrate, a copper wiring pattern may be formed on a single surface or both surfaces of the substrate. Further, the printed substrate may be a
10 multi-layered substrate such as one consisting of four or more laminated layers. Further, the substrate may be of ceramics, plastics formed by injection molding, or glass. Further, the substrate may have a curved surface.

As described above, in accordance with the present
15 invention, a wiring pattern is formed on a substrate and a solder alloy including tin and lead as major components is coated entirely or a part of the wiring pattern by electroless plating wherein a solder resist may be applied after forming the wiring pattern. Accordingly,
20 the solder alloy can be coated on the wiring pattern in uniform and flat manner irrespective of the dimensions of the wiring pattern and the distance between adjacent wires in the wiring pattern, whereby reliability to the connection of the elements in mounting and accuracy in
25 positional relation of the elements can be improved.

CLAIMS:

1. A method of preparing a printed substrate comprising a step of forming a wiring pattern on a substrate and a step of coating a solder alloy including tin and lead as
5 major components on said wiring pattern by means of electroless plating.

2. The method according to Claim 1, wherein said substrate is a multi-layered substrate.

3. The method according to Claim 1, wherein said
10 substrate is dipped in a solution to wet the same before the electroless plating.

4. The method according to Claim 1, wherein a plating solution for electroless plating including 0.1 mole/ℓ of tin, 0.01 mole/ℓ of lead, 0.2 mole/ℓ of organic sulfonic
15 acid and 2 mole/ℓ of thiourea as major components is used.

5. A method of preparing a printed substrate comprising a step of forming a wiring pattern on a substrate, a step of applying a solder resist to a part of said wiring
20 pattern, and a step of coating a solder alloy including tin and lead as major components on the remaining exposure portion of the wiring pattern by means of electroless plating.

6. the method according to Claim 5, wherein said
25 substrate is a multi-layered substrate.

7. The method according to Claim 5, wherein a plating solution for electroless plating including 0.1 mole/ℓ of

tin, 0.01 mole/ℓ of lead, 0.2 mole/ℓ of organic sulfonic acid and 2 mole/ℓ of thiourea as major components is used.

8. A method of preparing printed substrate substantially as herein described with reference to Figures 1 to 6 of the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report)

Application number

9125275.9

Relevant Technical fields

(i) UK Cl (Edition K) C7F (FHAB,FHAA): H1R (RAD,RAE, RAF,RAH,RAV)

(ii) Int Cl (Edition 5) H05K

Search Examiner

H COLLINGHAM

Databases (see over)

(i) UK Patent Office

(ii) ONLINE DATABASES: WPI

Date of Search

30 JANUARY 1992

Documents considered relevant following a search in respect of claims 1-8

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
X	GB 2228269 A (OKUNO CHEMICAL) WHOLE DOCUMENT	1,4,5,7
X	GB 2192197 A (HARIMA CHEMICALS) SEE PARTICULARLY PAGE 3	1,5
X	GB 2137421 A (STC) SEE PARTCICULARLY PAGE 2 LINES 54-61	1,5
X	GB 1492506 A (AMP INC) WHOLE DOCUMENT	1,5
X	GB 1310880 A (MICROPONENT) SEE PARTICULARLY PAGE 4 LINES 37-39	1,2,5,6
Y	GB 1228651 A (TELEFUNKEN) SEE PARTICULARLY PAGE 3 LINES 17-19	1,2,5,6

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

X: Document indicating lack of novelty or of inventive step.

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E: Patent document published on or after, but with priority date earlier than, the filing date of the present application.

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