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(71) Applicant *(for all designated States except US)*: **NXP B.V.** [NL/NL]; High Tech Campus 60, NL-5656 AG Eindhoven (NL).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **MEUNIER-BEILLARD, Philippe** [FR/BE]; c/o NXP Semiconductors, Betchworth House, 57-65 Station Road, Redhill Surrey RH1 1DL (GB). **HERINGA, Anco** [NL/NL]; c/o NXP Semiconductors, Betchworth House, 57-65 Station Road, Redhill Surrey RH1 1DL (GB). **DUFFY, Raymond, J.** [IE/BE]; c/o NXP Semiconductors, Betchworth House, 57-65 Station Road, Redhill Surrey RH1 1DL (GB).

(74) Agents: **WILLIAMSON, Paul, L.** et al.; c/o NXP Semiconductors, IP Department, Betchworth House, 57-65 Station Road, Redhill Surrey RH1 1DL (GB).

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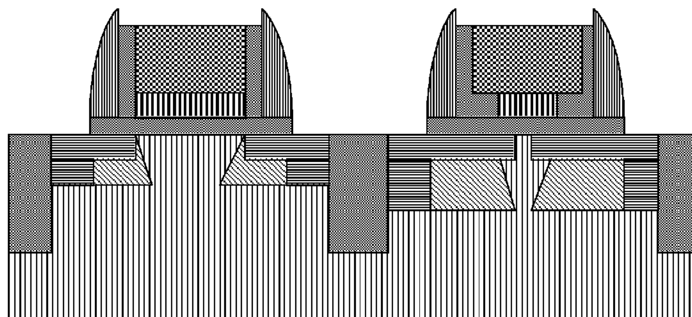

FIG. 10

(57) **Abstract**: The present invention relates to a MOS transistor for RF applications with a notched gate. The phrase "metal-oxide-semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material. Instead of metal (usually aluminum in the very old days), current gate electrodes (including those up to the 65 nanometer technology node) are almost always made from a different material, polysilicon, but the terms MOS and CMOS nevertheless continue to be used for the modern descendants of the original process. Metal gates have made a comeback with the advent of high-k dielectric materials in the CMOS process.

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Low cost MOS transistor for RF applications

FIELD OF THE INVENTION

The present invention relates to a MOS transistor for RF applications. The phrase "metal–oxide–semiconductor" is a reference to the physical structure of certain field-effect transistors, having a metal gate electrode placed on top of an oxide 5 insulator, which in turn is on top of a semiconductor material. Instead of metal, current gate electrodes (including those up to the 65 nanometer technology node) are almost always made from a different material, polysilicon, but the terms MOS and CMOS nevertheless continue to be used for the modern descendants of the original process. Metal gates have made a comeback with the advent of high-k dielectric 10 materials in the CMOS process.

BACKGROUND OF THE INVENTION

A lot of effort has been spent in research and development in order to develop CMOS technology for logic applications. The aggressive gate length 15 downscaling has shown that the CMOS transistors can now reach new frequency domains previously only possible with bipolar transistors. It is usually possible to find a CMOS node fulfilling the RF frequency application requirements.

Bipolar transistors are usually the key enablers to improve the RF performance in old CMOS generations. A bipolar transistor seems an excellent 20 candidate to achieve good RF performance at reasonable costs for the novel technologies. However, it has major disadvantages adding bipolar transistors to CMOS technologies, because generally complex additional processing steps such as epitaxy and Chemical Mechanical Polishing, which are both layout processing dependant and such complex processing steps usually require special attention 25 (dedicated qualifications / monitoring per product) that makes them unpopular in a production environment running many different products.

In a MOSFET, the cut-off frequency Ft (one of the important RF Figures Of Merit) is inversely proportional to the channel length. The standard way to make shorter channels is usually:

A) Use aggressive shrinking of an existing process. Such an aggressive shrinking adds design difficulties and/or restrictions (poor gate control like CD, uniformity, etches at corners etc.).

When such shrinking is not possible in the processing as used:

B) to use more advanced lithography tools. This approach is pretty similar to use a newer process generation. This option requires substantial investments and is usually expensive.

Various documents relate to MOS transistors for RF applications. US6124177 discloses a method for making improved MOSFET structures. A Si_3N_4 and a SiO_2 layer are deposited and patterned to have openings for gate electrodes over device areas on a substrate. A second Si_3N_4 layer is deposited and etched back to form arc-shaped sidewall spacers in the openings. An anti-punchthrough implant and a gate oxide are formed in the openings between the Si_3N_4 sidewall spacers. A polysilicon layer is deposited and polished back to form gate electrodes. The SiO_2 and the Si_3N_4 layers, including the sidewall spacers, are removed to form freestanding gate electrodes that increase in width with height, and having arc-shaped sidewalls. An implant through the edges of the arc-shaped gate electrodes results in lightly doped source/drains that are graded both in junction depth and dopant concentration to reduce hot electron effects. A second SiO2 layer is deposited and etched back to form insulating sidewall spacers that include air spacers to reduce the gate-to-drain capacitance. Another implant is used to form source/drain contact areas. A salicide process is used which forms a silicide on the polysilicon gate electrodes and on the source/drain contact areas. The arc-shaped structure allows MOSFETs to be formed with reduced channel lengths while maintaining a wider silicide area on the gate electrodes for reduced resistance.

The way the T-shaped gate is implemented is ,however, quite critical for this invention, and thus hampers implementation thereof.

US2003235943 discloses methods for forming notched gates and semiconductor devices utilizing the notched gates are provided. The methods utilize the formation of a dummy gate on a substrate. The dummy gate is etched to form

notches in the dummy gate, and sidewall spacers are formed on the sidewalls of the notched dummy gate. The dummy gate is removed, and a notched gate is formed. The methods allow the height and depth of the notches to be independently controlled, and transistors having shorter channel lengths are formed.

5 The transistor described herein has a gate electrode with a notched shape. The notch is generally formed before the formation of the source and drain regions, and the formation of the notch allows the source and drain extension to be formed closer together than is generally possible when using traditional fabrication methods. Further, it is the dopant diffusion that brings the extension closer.

10 US2004259340 discloses a transistor having a gate electrode with a T-shaped cross section, which is fabricated from a single layer of conductive material using an etching process. A two process etch is performed to form sidewalls having a notched profile. The notches allow source and drain regions to be implanted in a substrate and thermally processed without creating excessive overlap capacitance with

15 the gate electrode. The reduction of overlap capacitance increases the operating performance of the transistor.

WO9950900 discloses a method of reducing an effective channel length of a lightly doped drain transistor, including the steps of forming a gate electrode and a gate oxide over a semiconductor substrate and implanting a drain

20 region of the substrate with a sub-amorphous implant at a large tilt to thereby supply interstitials at a location under the gate oxide. The method also includes forming a lightly doped drain extension region in the drain region of the substrate and forming a drain in a drain region and forming a source extension region and a source in a source region of the substrate. Lastly, the method includes thermally treating the substrate,

25 wherein the interstitials enhance a lateral diffusion under the gate oxide without substantially impacting a vertical diffusion of the extension regions , thereby reducing the effective channel length without an increase in a junction depth of the drain and the drain extension region or the source and the source extension region.

The patent proposes a method to promote the lateral diffusion of the

30 dopant (compared to the vertical diffusion). The invention uses a shallow implant with a large tilt angle (together with the extension) in order to create/place interstitials under the gate oxide at the extension corner.

In general the patents cited pay special attention to the design and the fabrication of the extension (which is nowadays a very quite shallow highly doped drain extension).

The above disclosures all provide a semiconductor device comprising a MOS transistor with limited frequency - breakdown voltage tradeoff performance and a bad parasitic gate capacitance performance, which is a major factor determining the frequency performance.

Thus there is a need of an improved semiconductor device. The present invention aims to solve one or more of the above mentioned problems.

SUMMARY OF THE INVENTION

Thus the present invention relates to a method of forming a semiconductor device comprising a MOS transistor with improved frequency - breakdown voltage performance, as well as a semiconductor device comprising said transistor, and to a device comprising said semiconductor device. The improvements are e.g. evidenced by the Figures presented below, specifically Figs. 11-18. The cut-off frequency Ft may be improved by about 50% without degrading too much the breakdown voltage. Depending on the node under investigation, the cut-off frequency improvement may vary somewhat.

The present invention relates to a method to fabricate a MOS transistor with good RF performance at low cost, without relying on the use of additional complex processing steps such as epitaxy and CMP. The purpose of the invention is to implement a simple method (applicable for advanced CMOS processing) to improve the cut-off frequency (Ft), without compromising the breakdown voltage. The invention promotes the lateral extension diffusion to create a shorter effective channel length. Such an enhanced diffusion creates “smooth” junctions that preserve good breakdown voltage but increases the punch-through and the gate capacitance. The use of a poly notched gate suppresses the extra parasitic gate capacitance and allows good frequency (Ft) performance.

In general the prior art pays special attention to the design and the fabrication of the extension, which is nowadays a very quite shallow highly doped drain extension, whereas in the present application it is more a Lightly Doped Drain: a

lower doped part of a drain extension (LDD) ,which is “merged” (through diffusion) together with the HDD.

The advantages of the present invention are as follows:

- The obtained transistor provides promotion of the lateral diffusion of the extensions or LDD. It creates a shorter effective channel length with smooth junctions that ensure a good frequency breakdown voltage trade-off.

The obtained transistor creation of a T-shape or notched gate structure allows suppression (or reduction) of the unwanted source/drain overlap capacitance and ensures a good RF performance.

The present invention is not limited to a notch that has to be created “before” the extension implant. The gate pattern is typically not used for implantations purposes. Additionally, the channel length is not reduced to less than that defined by a layer of the gate.

Further, in the present invention a highly doped part of a drain extension (LDD) is “merged” (through diffusion) together with a HDD.

In the present invention the notch structure does not control the location of an initial implant of the source and drain extensions. The location of the dopant is controlled by means of diffusion, instead of localization with the implantation.

In summary, the present invention creates a lowly doped drain extension by enhanced diffusion due to high dose implants. The resulting higher overlap capacitance between the extension and the gate is remedied by making in this overlap area the distance between gate and extension larger by removal of part of the gate in the overlap area. The resulting transistor features a relatively high breakdown voltage, a relatively short channel length and a relatively low gate capacitance. This allows high frequency operation in combination with high operating voltages. The novelty is the combination in the processing of a method to process a notched gate and the usage of enhanced high concentration diffusion.

It is further noted that much more better and realistic source / drain profiles may be made in order to obtain good performance and without (or reduced) punch-through.

Further, the present invention is also applicable in advanced CMOS nodes where the aggressive junction is limiting the breakdown voltage.

DETAILED DESCRIPTION OF THE INVENTION

In a first aspect the invention relates to a method of forming a semiconductor device comprising a MOS transistor with improved RF breakdown performance and suppressed parasitic gate capacitance, comprising the steps of:

5 - providing a transistor comprising a substrate,

- providing a notched or T-shaped gate, preferably a poly gate, and providing adequate extensions by ion implantation, by one or more implantation steps of the substrate, wherein the notch or T-shaped profile resembles a combination of a rectangle and a trapezoid.

10 Tuning the shape of doping profile is essential, because then an even better performance is obtained in terms of the advantages of the present invention.

The term “notch” relates to a “V” or “T”-shape. In the present invention it further relates to a small cut/undercut. Due to implantation and thermal treating of the device typically a precise defined shaped is not obtainable and not 15 needed. However an overall notch shaped gate shape is well achievable.

The present invention solves one or more of the above mentioned problems. Further it provides an improved RF breakdown performance and suppressed parasitic gate capacitance, as is shown below.

By providing adequate extensions by ion implantation it is meant that 20 the gate doping profile is such that the above mentioned effects are achieved. Such effects may be achieved by varying implantation steps in terms of number of steps, species used, energy used, doses used etc.

Implantation steps are, if appropriate, used to define wells, doped substrate, HDD (highly doped drain) terminal regions, LDD (lightly doped drain) 25 terminal regions or auxiliary terminal regions and/or so-called pockets or halos. Doping can either be of N-type or P-type, as in standard CMOS processing.

The extension profile shape is amongst others achieved by one or more implantations under a tilt angle; it is noted that the notch shape/structure only applies to the gate. Typically, the implants are used for the extensions engineering. The shape 30 of the source drain junctions will as a consequence more look like a “balloon” and not look like a notch; this is also encompassed by the present invention. The implant tilt angle is preferably from 5-35 degrees, more preferably from 10 –25 degrees. If the angle is too small, no or hardly any halo shaped profile is achieved. If the angle is too

high, the implant species can not enter the substrate deep enough. It has been found that the best effect, e.g. in terms of breakdown and/or suppression of parasitic capacitance, is achieved with tilt of approximately 25 degrees.

The transistor of the present invention relates to any T-shaped or similar structure. It is clearly not limited to the use of SiGe in the poly-gate, though being preferred.

The transistor comprises a gate, a source and a drain.

The substrate may be formed of a semiconducting material, such as silicon.

The present doping profiles will look like the “prior art” source/drain profile, except that they will be “broader” or multiplied by a factor (such as larger than 1, preferably larger than 1.5) in the depth and lateral directions. The larger the factor, the better the performance. The factor is clearly limited by the length of the profile.

In a preferred embodiment the present invention relates to a method, wherein two or more implantation steps are used, preferably three or more, to create source and drain regions, wherein as implantation species one or more of P, As, B, BF_2 and In are used, at a respective energy range of 5-60 keV, 10-300 keV, 1-60 keV, 1-20 keV and 30-600 keV, ate a respective dose of $1.10^{13} – 1.10^{15}$, $1.10^{12} – 1.10^{16}$, $1.10^{13} – 1.10^{16}$, $1.10^{13} – 1.10^{16}$, and $1.10^{13} – 1.10^{15}$ cm^{-2}.

The present target for advanced CMOS process nodes allows for a factor (from 0.25 – 4.0) for energies and doses applicable for the HDD and LDD. That does not apply to the WELL implants. Taking into account the source/drain modifications, this gives the following ranges:

Element	Energy range (keV)	Dose (cm^{-2})
P	5-60	1.10^{13}-1.10^{15}
As	10-300	1.10^{12}-1.10^{16}
B	1-60	1.10^{13}-1.10^{16}
BF2	1-20	1.10^{13}-1.10^{16}
In	30-600	1.10^{13}-1.10^{15}

In a preferred embodiment the present invention relates to a method, wherein the species are preferably In, P, or As.

Preferences for n-MOS type processing are as follows:

* HDD: As + P

* extension: As + P. Standard CMOS process will preferably only use As.

5 * pocket: B + In. Standard CMOS process will preferably only use B.

Preferences for p-MOS type processing are as follows:

* HDD: B

* extension: BF2 + B. Standard CMOS process will preferably only use BF2.

10 * pocket: As + P. Standard CMOS process will preferably only use As.

In a preferred embodiment the present invention relates to a method, further comprising the steps of:

providing a substrate,

forming at least standard STI regions and/or N- and/or P-type wells,

15 providing one or more dedicated implants,

forming a gate oxide,

forming a first conducting layer, preferably of poly Si/SiGe,

forming a second conducting layer, preferably of poly Si,

subsequently patterning a gate,

20 forming an extension, preferably by a standard CMOS process, such as by implantation,

applying a resist, preferably by spinning,

exposing the resist,

optionally providing an implantation and a selective SiGe etch,

25 stripping the resist,

oxidizing the second conducting layer (in the preferred embodiment the poly-Si),

forming an oxide and depositing nitride,

forming nitride spacer, preferably by nitride dry etch stopping on

30 oxide,

etching oxide, preferably wet etch,

providing a standard CMOS source/drain implantation, and

optionally providing standard CMOS back end processing.

In a second aspect the present invention relates to a semiconductor device comprising a transistor with improved RF breakdown performance and suppressed parasitic gate capacitance, which transistor comprises a gate, a source and a drain, wherein the gate comprises poly-silicon and a second layer on top of a gate oxide, formed of a semi-conducting material in the center, preferably poly-silicon/germanium, and an isolating material at the edge, preferably an oxide, wherein a source and/or drain extension extends substantially towards the semiconducting material.

In a preferred embodiment the present invention relates to a semiconductor device, wherein the gate region is notched shaped.

In a preferred embodiment the present invention relates to a semiconductor device,, wherein the notch or T-shaped profile resembles a combination of a rectangle and a trapezoid.

In a third aspect the present invention relates to a device, comprising a semiconductor device according to the invention.

The present invention is further elucidated by the following Figures and examples, which are not intended to limit the scope of the invention. The person skilled in the art will understand that various embodiments may and can be combined.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1-10 show a schematic process flow. Therein the left part of the Figures relate to prior art CMOS processing, whereas the righ part relates to the present invention.

Figs. 11-14 show doping concentration profiles as a function of doping species.

Figs. 15-16 show Id-Vd curves.

Fig. 17 shows various curves as function of the Vds.

Fig. 18 shows various curves as function of the Vg.

DETAILED DESCRIPTION OF THE DRAWINGS

Figs. 1-10 show a schematic process flow. Therein the left part of the Figures relate to prior art CMOS processing, whereas the righ part relates to the present invention.

Figures are not to scale, but schematic. In summary the Figures relate to: Fig. 1 illustrates the STI isolation and p-well formation. An extra n-type implant like Vt adjust has been used in this feasibility study (Fig. 2). This implant is optional and uses the same mask as the one for the notched gate formation in Fig. 5. The gate oxide is formed and a Poly SiGe/Si stack is deposited. The Poly gate is then patterned using a dry etch stopping on oxide (Fig. 3) and the standard extension is formed (Fig. 4). A mask is used to select the wanted devices (Fig. 5). Selective SiGe etch is performed and additional implants can be done. These extra implants have to be such that they will promote a lateral diffusion during the CMOS RTA without creating punch-through. The rest of the processing steps (Fig. 6 to Fig. 10) uses the standard CMOS processing. In more detail:

Fig. 1 shows standard STI and well formation (100) in a substrate (110), e.g. silicon.

Fig. 2 shows dedicated implants in the substrate, using a mask (220), for the notched gate structure (resulted doping profile in substrate not shown). The special well implant can be used to remedy effects such as punch-through, which may occur due to the proposed enhanced diffusions of source/drain. The mask which can be used for this implant is needed later in the process flow anyhow (so no extra mask has to be made), but the processing is extra and thus this implant will be avoided, if possible.

Fig. 3 shows gate oxide (300), poly Si/SiGe (330), poly Si deposition (340), substrate (310), and subsequent gate patterning.

Fig. 4 shows standard CMOS extension formation (450,460) (i.e. implantation), and further the elements of figure 3, gate oxide (400), poly Si/SiGe (430), poly Si deposition (440), and substrate (410).

Fig. 5 shows resist spinning (520), exposure, optional implantation and selective SiGe etch (not oxide etch). It is noted that the etch selectivity is usually not perfect, so that some silicon and oxide are also etched. Arrows indicate the implantation of ion species, e.g. under a specific angle. The implantation regions (as in figure 4 (450) and (460), respectively) are also visible, as well as the newly implanted region (565).

Fig. 6 shows the result of resist strip.

Fig. 7 shows Poly oxidation, oxide (700) and nitride deposition (770). It is noted that occassionally one oxide formation step is not sufficient. This will depend on e.g. the notch thickness/void. The poly oxidation typically creates 3 nm of oxide (at 900 C) in advanced CMOS processing, and also probably in very advanced
5 CMOS processing. A second thicker oxide (at lower temperature) is then necessary and followed by the nitride deposition. The nitride spacer is formed by etching the nitride and stopping on oxide. Thick oxide is then preferred for process control. A standard CMOS spacer is formed with oxide and nitride. The oxide layer is issued to prevent gate leakage and has to be thick enough to allow the nitride spacer formation
10 (i.e. nitride dry etch stopping on oxide). The spacer stack is typically 8 nm oxide / 55 nm nitride in advanced CMOS and 20 nm oxide / 60nm nitride in very advanced CMOS. It further is necessary to fill the gap.

Fig. 8 shows nitride spacer formation (nitride dry etch stopping on oxide).

15 Fig. 9 shows oxide wet etch and standard CMOS source / drain implantation (980). A similar source/drain implant is used for the standard and modified present transistor. It is noted that typically there has to be a dedicated mask for the notched gate anyhow, and this mask/step can be used as well to tune the S/D implants and the accompanying diffusion for these devices (see next Figure).

20 Fig. 10 shows standard CMOS processing (diffusion of dopants). As such the extensions are modified, by adding more dopants, so providing more diffusion. The right has then more diffusion than the left side for a similar thermal budget. Thus the right is different from the left because the present invention uses higher doses implantation (see Fig. 5). Higher dopant concentration gives more
25 diffusion.

The process integration scheme is further illustrated below. We will consider only an n-mos transistor for clarity purpose.

The following shows a summary of the invention illustrated by TCAD. Technology CAD (or Technology Computer Aided Design, or TCAD) is a branch of
30 electronic design automation that models semiconductor fabrication and semiconductor device operation. The modeling of the fabrication is termed Process TCAD, while the modeling of the device operation is termed Device TCAD. Included are the modelling of process steps (such as diffusion and ion implantation), and

modelling of the behavior of the electrical devices based on fundamental physics, such as the doping profiles of the devices.

The simulations presented in this paragraph are aimed to provide general guidelines to implement the invention. It is noted that these are not yet finalized or optimized results. The person skilled in the art will appreciate that given the guidelines results may be optimized for specific layouts.

One of the key components of the invention is to promote the lateral diffusion of the extensions without creating punch-through.

The diffusion is illustrated in Fig. 11, showing the net doping concentration as function of Phosphorus dosis, where we added a phosphorus implantation (at 5 keV, tilt=0) to the existing standard extensions. When the dopant concentration is increased in the extensions one creates more diffusion. This diffusion is vertical and horizontal. When the concentration becomes too high the p-type well is over-doped by the n-type dopants of the extensions. It is then needed to adjust other implants (well (fig.2) or extension (n-type LDD on top surface (not visible on figure)) and p-type pocket deeper in substrate (Fig.5) as shown in Fig. 12.

Fig. 12 illustrates an enhanced diffusion (both lateral and vertical) by using a phosphorus implantation at 5 keV, dose of 2.10^{14} cm^{-2}, no tilt and with an Indium implantation at 150 keV with a 25 degree tilt (same tilt as used for standard CMOS pocket formation). The extensions are made with the standard CMOS extensions with an extra phosphorus implant of 2.10^{14} cm^{-2} at 5keV. The relevant function of the indium pocket resides under the channel where the punch-through occurs and where the well concentration is lower. The left picture shows that the p-well is over-doped by the extensions. It is then needed to increase the doses of the pocket implantations (like shown in Fig. 12, or for a given pocket implantation condition it is needed to decrease the extension doses).

The effect of extra dedicated implants in Fig. 2 is illustrated in Fig. 13. Net doping, Indium and Arsenic concentration profiles with As implantation (during Well formation) at 5 keV and different doses. The extensions are made with the standard CMOS extensions with an extra phosphorus implant of 2.10^{14} cm^{-2} at 5 keV, and Indium implant of 5.10^{13} cm^{-2} at 150 keV (tilt 25). The corresponding (Id,Vg) simulated curves are presented in Figure 15 (black curves).

The notched gate structure was implemented in these simulations as a simple removal of gate material instead of by the preferential etching of the SiGe layer and a complex process simulation (see Fig. 14). Fig. 14 gives an illustration of the notched gate features with an oxide thickness of 20 nm and different oxide lengths. The well is made with the standard CMOS well and with an extra Arsenic implant of 5.10^{13} cm^{-2} at 5 keV. The extensions are made with the standard CMOS extensions with an extra phosphorus implant of 2.10^{14} cm^{-2} at 5 keV, and Indium implant of 2.10^{14} cm^{-2} at 150 keV (tilt 25).

The Id-Vg and Id-Vd curves with and without the notched gate structure are presented in Fig. 15 and Fig. 16, respectively. Fig. 15 gives Id-Vg curves for Vds=0.05 V. The right solid curve corresponds to the standard MOS, the left and middle curves correspond to the modified MOS extensions with and without the notched gate respectively. The well is made with the standard CMOS well and with an extra Arsenic implant at 5 keV with different doses. The extensions are made with the standard CMOS extensions with an extra phosphorus implant of 2.10^{14} cm^{-2} at 5 keV, and Indium implant of 2.10^{14} cm^{-2} (split in 4 sub-implants of 5.10^{13} dose with different rotation angles) at 150 keV (tilt 25). Fig. 16 gives Id-Vd curves for Vgs= 0 and 1V. The left curve corresponds to the standard MOS, the right and middle curves correspond to the modified MOS extensions with and without the notched gate respectively. The well is made with the standard CMOS well with an extra Arsenic implant at 5 keV with different dosis. The extensions are made with the standard CMOS extensions with an extra phosphorus implant of 2.10^{14} cm^{-2} at 5 keV, and Indium implant of 2.10^{14} cm^{-2} (4 rotation settings each with 5.10^{13} cm^{-2} dose) at 150 keV (tilt 25). As expected the notched gate structure does not change the DC characteristics. The transistor showed a breakdown voltage of around 3.5 volts (avalanche), but 2.5 – 3 volts operation range seems more realistic due to the huge leakage current (punch-through).

The effect of the notched gate structure on the cut-off frequency, conductance and gate capacitance is shown in Fig. 17 as function of the notched length. Fig. 17 gives the cut-off frequency (Ft), conductance (gdg) and gate capacitance (C) curves as function of the Vds (Vg=1V) for different notched gate length (thickness is 20 nm). The solid curve corresponds to the standard MOS, the dotted curves correspond to the modified MOS extensions with different notched gate

length. The well is made with the standard CMOS well and with an extra Arsenic implant of 5.10^{13} cm^{-2} at 5 keV. The extensions are made with the standard CMOS extensions with an extra phosphorus implant of 2.10^{14} cm^{-2} at 5 keV, and Indium implant of 2.10^{14} cm^{-2} (4 rotation settings with 5.10^{13} cm^{-2} dose) at 150 keV (tilt 25).
5 The cut-off frequency improvement clearly comes from the gate capacitance reduction and compensates the lower transconductance.

The invention benefits most of the notched gate structure for a long notched gate structure. The impressive parasitic gate reduction capacitance (Figure 18) compensates the transconductance reduction and the increased junction
10 capacitance. Fig. 18 gives the drain current (Id), transconductance (gm), cut-off frequency (Ft), gate capacitance (Cgg) and feedback capacitance (Cgd) curves as function of the Vg (Vds=1V) with (lower curves left) and without (higher curves) a notched gate structure (thickness of 20 nm and length of 40 nm). The well is made with the standard CMOS well with an extra Arsenic implant at 5 keV with different
15 doses. The extensions are made with the standard CMOS extensions with an extra phosphorus implant of 2.10^{14} cm^{-2} at 5 keV, and Indium implant of 2.10^{14} cm^{-2} (4 rotation settings each with 5.10^{13} cm^{-2} dose) at 150 keV (tilt 25).

CLAIMS:

1. Method of forming a semiconductor device comprising a MOS transistor with improved frequency - breakdown voltage tradeoff performance and suppressed parasitic gate capacitance, comprising the steps of:

- providing a transistor comprising a substrate,
- providing a notched or T-shaped gate therein, preferably a poly gate wherein the shape resembles a combination of a rectangle and a trapezoid, and
- providing adequate extensions by ion implantation,

by one or more implantation steps of the substrate.

2. Method according to claim 1, wherein two or more implantation steps are used, preferably three or more, to create source and drain regions, wherein as implantation species one or more of P, As, B, BF_2 and In are used, at a respective energy range of 5-60 keV, 10-300 keV, 1-60 keV, 1-20 keV and 30-600 keV, ate a respective dose of $1.10^{13} – 1.10^{15}$, $1.10^{12} – 1.10^{16}$, $1.10^{13} – 1.10^{16}$, $1.10^{13} – 1.10^{16}$, and $1.10^{13} – 1.10^{15}$.

3. Method according to any of claims 1-2, wherein the species are preferably In, P, or As.

4. Method of forming a semiconductor device according to any of claims 1-3, further comprising the steps of:

- providing a substrate,
- forming at least standard STI regions and/or N- and/or P-type wells,
- providing one or more dedicated implants,
- forming a gate oxide,
- forming a first conducting layer, preferably of poly Si/SiGe,
- forming a second conducting layer, preferably of poly Si,

subsequently patterning a gate,

- forming an extension, preferably by a standard CMOS process, such as by implantation,
- applying a resist, preferably by spinning,

exposing the resist,

5 optionally providing an implantation and a selective SiGe etch,

stripping the resist,

oxidizing the second conducting layer,

forming an oxide and depositing nitride,

forming nitride spacer, preferably by nitride dry etch stopping on

10 oxide,

etching oxide, preferably wet etch,

providing a standard CMOS source/drain implantation, and

optionally providing standard CMOS back end processing.

15 5. Semiconductor device comprising a transistor with improved RF breakdown performance and suppressed parasitic gate capacitance, which transistor comprises a gate, a source and a drain, wherein the gate comprises poly-silicon and a second layer on top of a gate oxide, formed of a semi-conducting material in the center, preferably poly-silicon/germanium, and an isolating material at the edge,

20 preferably an oxide, wherein a source and/or drain extension extends substantially towards the semiconducting material.

6. Semiconductor device according to claim 5, wherein the gate region is notched shaped.

25

7. Semiconductor device according to any of claims 5-6, wherein the notch or T-shaped profile resembles a combination of a rectangle and a trapezoid.

8. Device, comprising a semiconductor device according to any of claims

30 5-7.

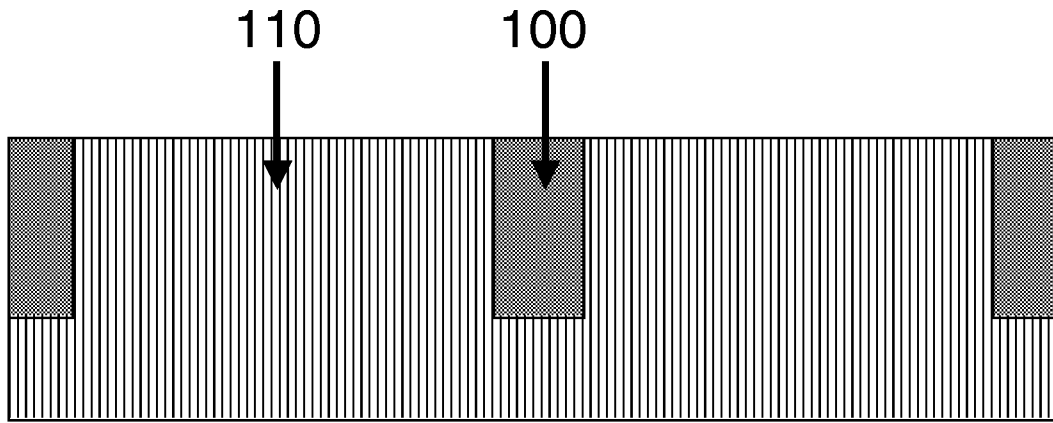


FIG. 1

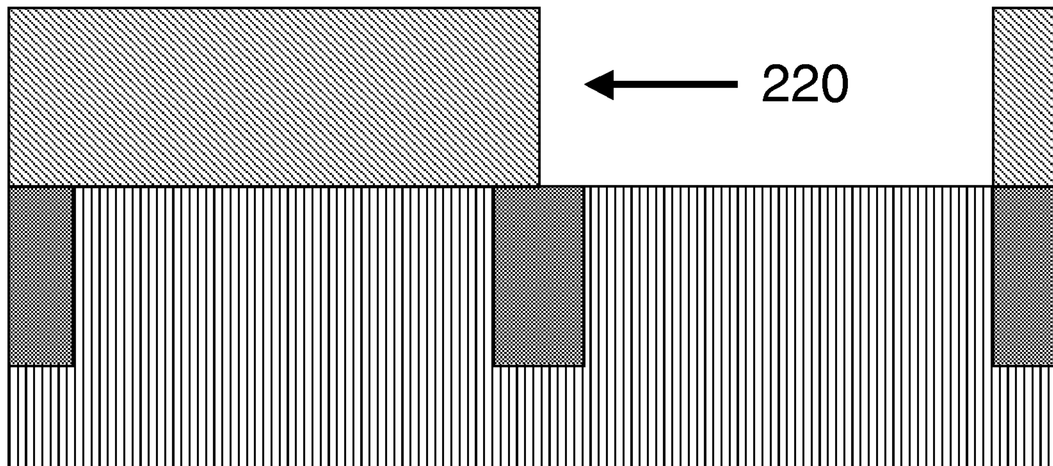


FIG. 2

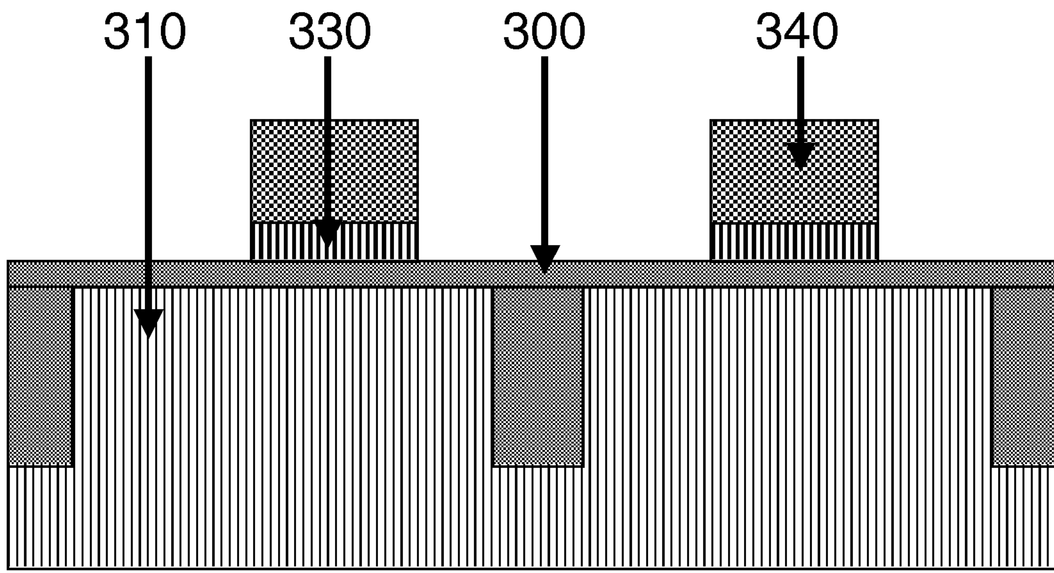


FIG. 3

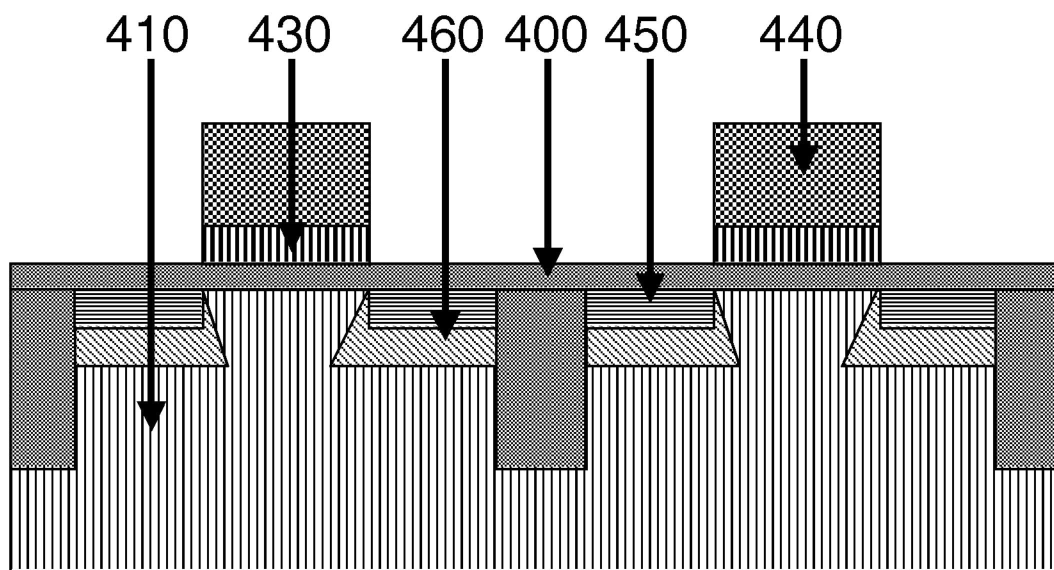


FIG. 4

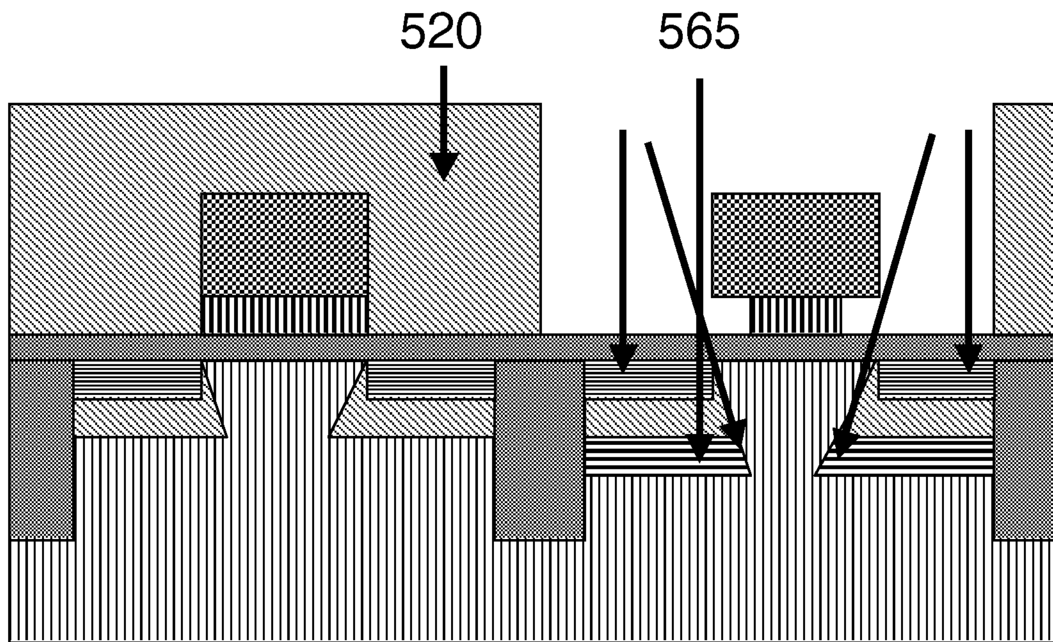


FIG. 5

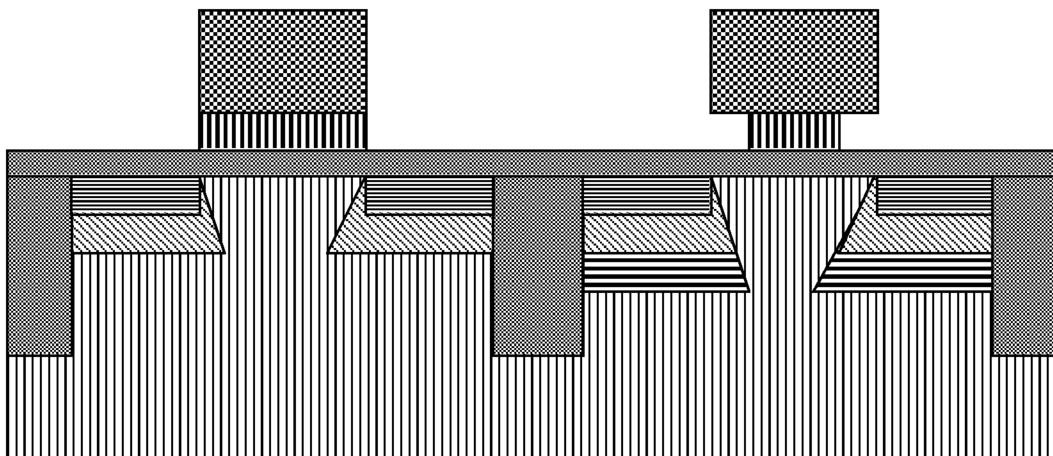


FIG. 6

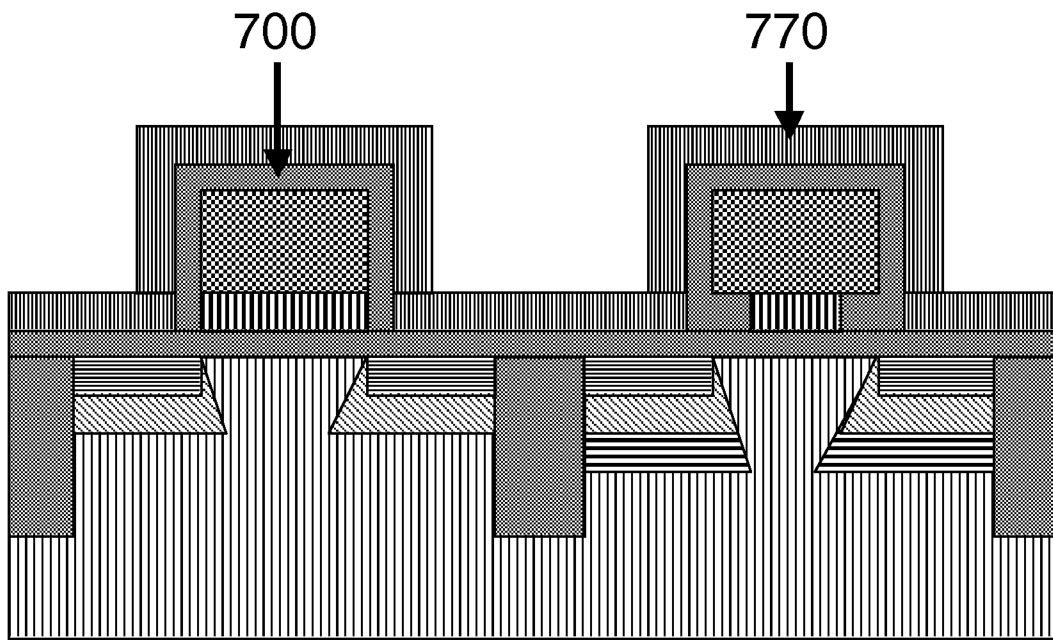


FIG. 7

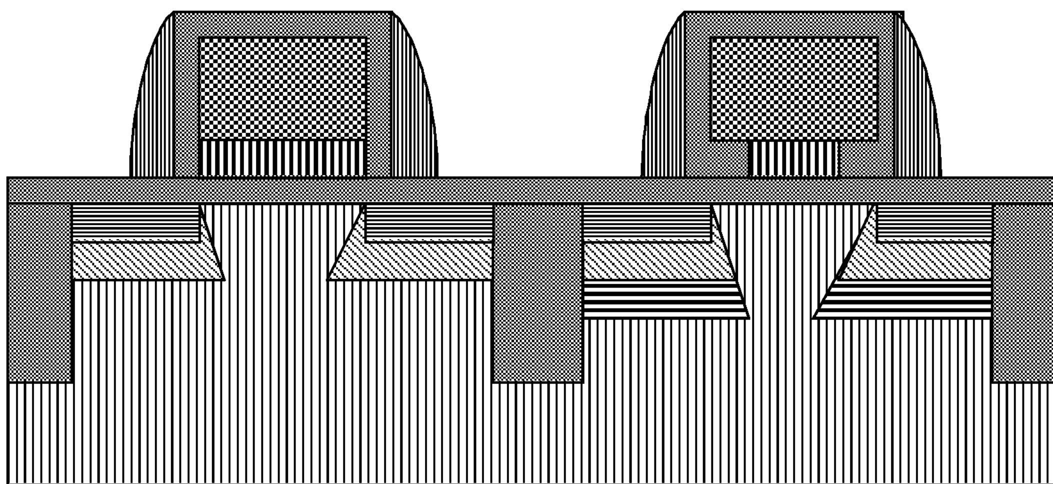


FIG. 8

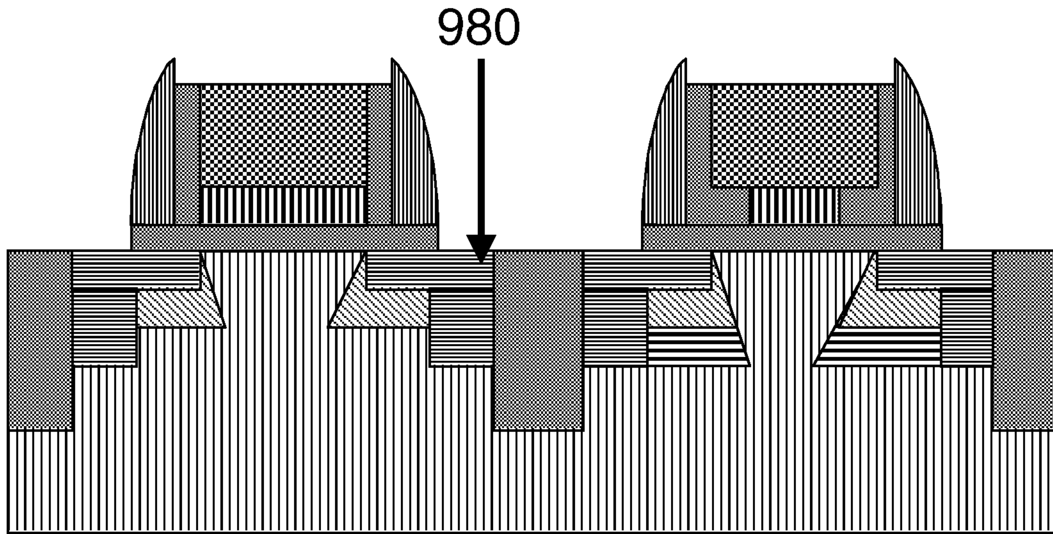


FIG. 9

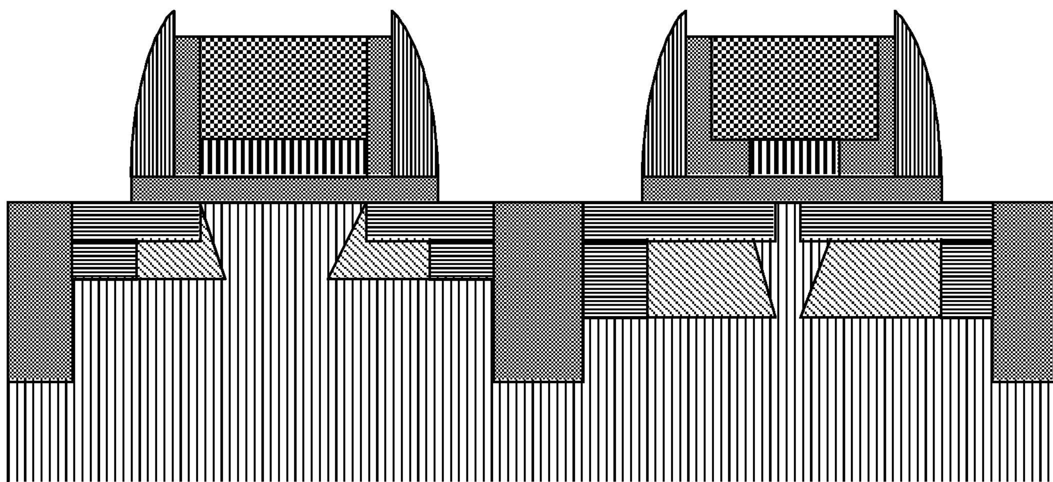


FIG. 10

P 1E13 2E13 3E13 4E13 5E13
Well: PW

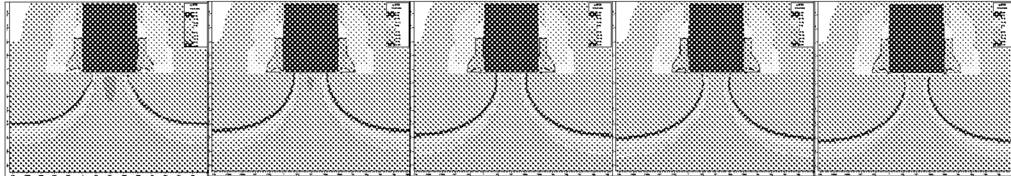
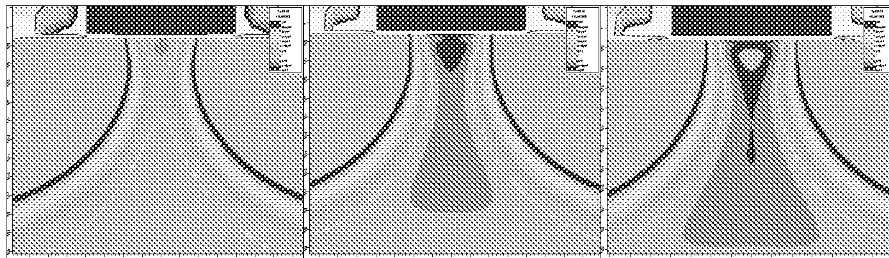


FIG. 11



IND 8E13 2E14 2.4E14

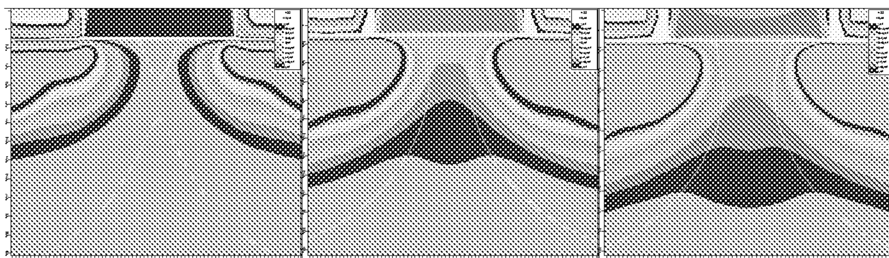


FIG. 12

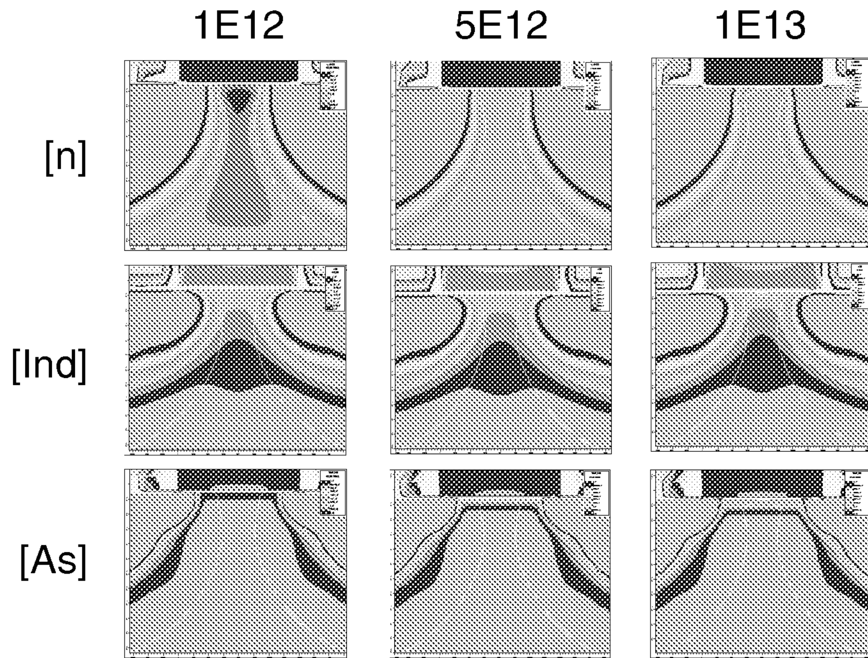


FIG. 13

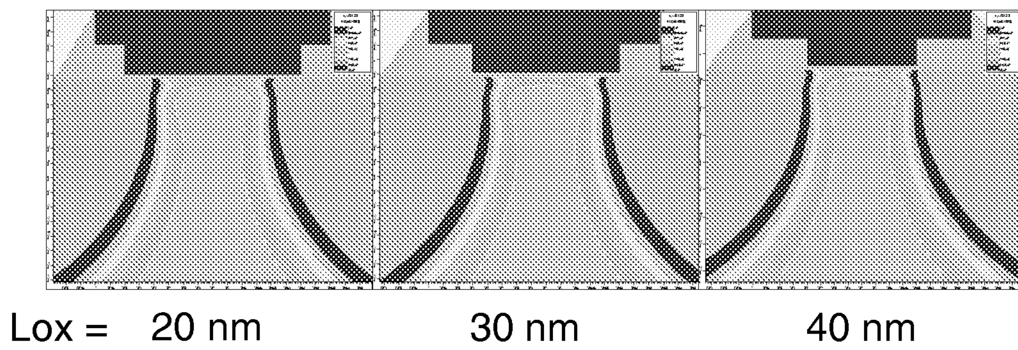


FIG. 14

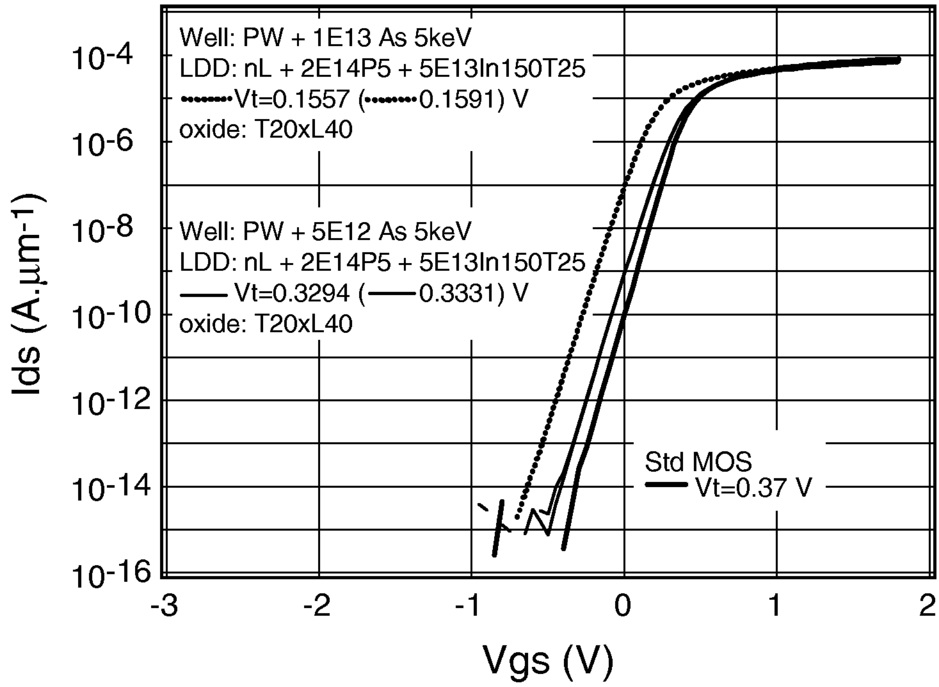


FIG. 15

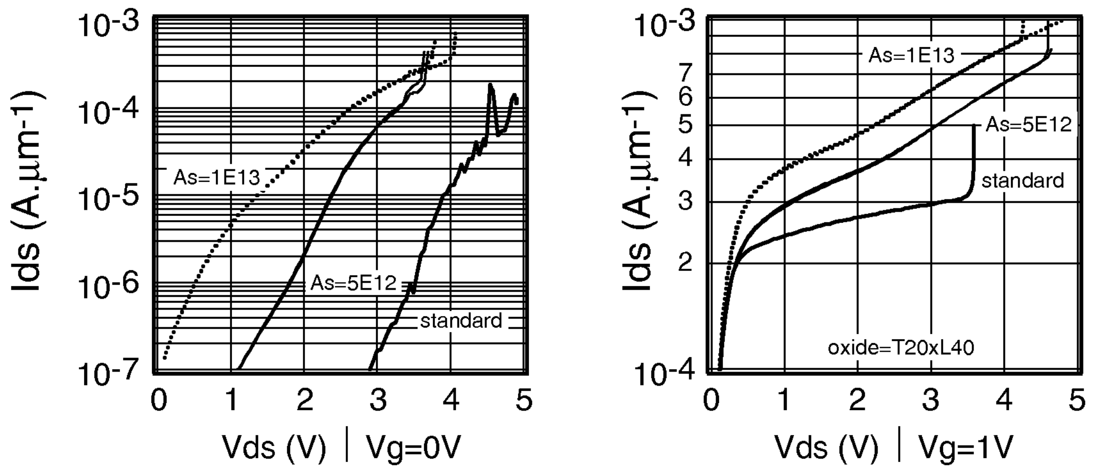


FIG. 16

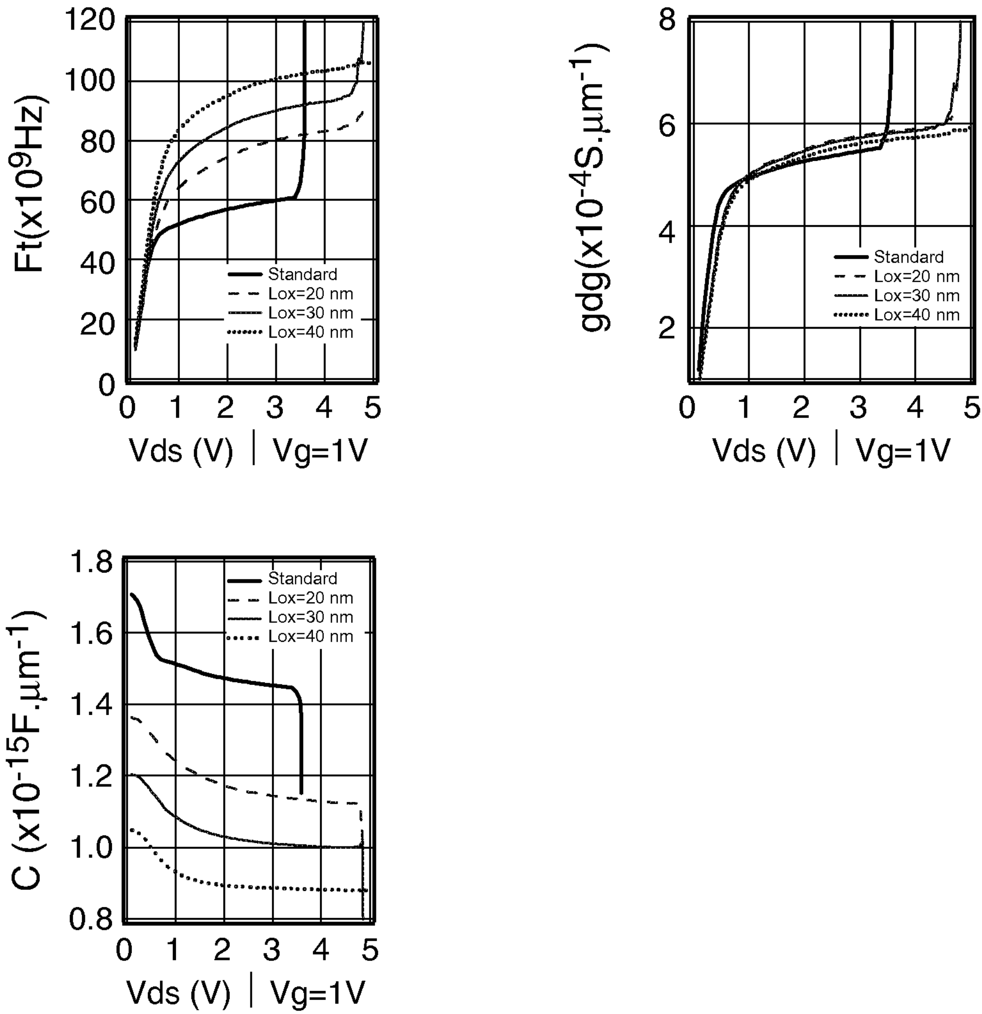


FIG. 17

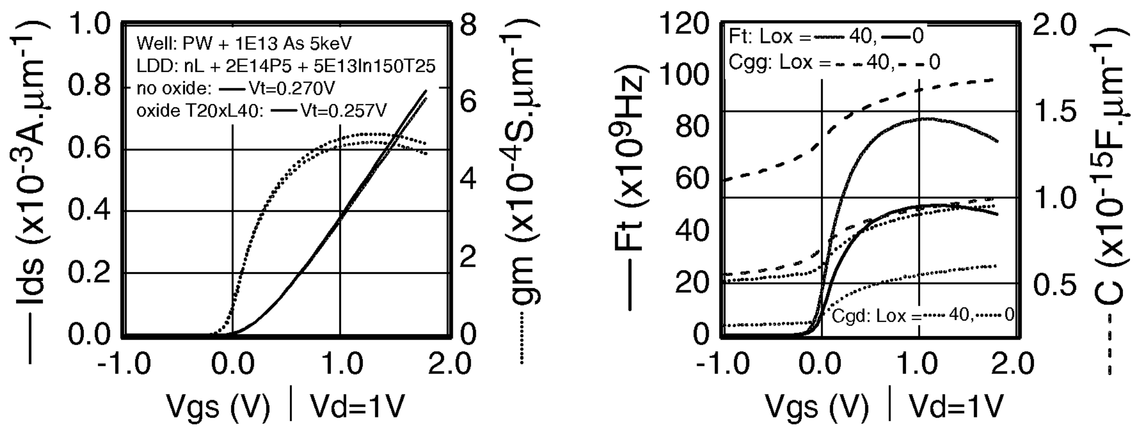


FIG. 18