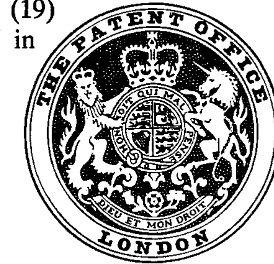
PATENT SPECIFICATION (11) 1 564 617

1 564 617

(21) Application No. 40151/76 (22) Filed 28 Sep. 1976 (19)
(31) Convention Application No's. 2543628 (32) Filed 30 Sep. 1975 in
2543677
(33) Fed. Rep. of Germany (DE)
(44) Complete Specification Published 10 Apr. 1980
(51) INT. CL.^{3} H01L 29/94
(52) Index at Acceptance
H1K 11A3 11C1A 11C4 11D 1FE 4C11
4C14 4H1A 4H3X 9F 9N2 9N3 FE
GAX



(54) IMPROVEMENTS IN OR RELATING TO DATA STORES

(71) We, SIEMENS AKTIENGESELLSCHAFT, a German Company of Berlin and Munich, German Federal Republic, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed to be particularly described in and by the following statement:-

5 The present invention relates to data stores for the storage of data in the form of electric charge carriers, and having at least one dynamic storage element arranged at the surface of a substrate of doped semiconductor material of a predetermined conductivity type having a substrate terminal, and which storage element includes at least one MIS-capacitor, one electrode of which is arranged on an electrically insulating layer on the substrate surface 10 and the counter-electrode of which is formed by a surface zone of the substrate underlying said one electrode.

It is important in data stores to provide storage elements which have a small space requirement in order to increase the data density. In data stores of the type with which this invention is concerned, a high data density can be achieved by the use of dynamic 15 one-transistor storage elements. Such a one-transistor storage element is described, for example, in the article entitled "A One Mill^{2} Single-Transistor-Memory-Cell in n-Silicon-Gate-Technology" by Karl-Ulrich Stein and Hans Friedrich in IEEE Journal of Solid State Circuits, vol. SC 8, No. 5, Oct. 1973. This storage element consists of an MIS-transistor and a MIS-capacitor having an electrode arranged on an electrically insulating layer on a 20 semiconductor substrate. The electrode of the capacitor is connected to an earth line, and the gate electrode of the transistor is connected to a word line. The counter electrode of the capacitor, which is formed in the substrate, is connected via the transistor to a bit line. An exemplary embodiment of such a one-transistor-storage element is illustrated in the article referred to above at page 321, in Figure 4.

25 It is an object of the present invention to provide a data store of the kind referred to above, in which the dynamic storage elements used require a smaller amount of space than do such elements in known data stores of this kind.

According to the invention, there is provided a data store for the storage of data in the form of electrical charge carriers having at least one dynamic storage element arranged at 30 the surface of a doped semiconductor substrate of a given conductivity type, provided with a substrate terminal, the or each said storage element comprising an MIS-capacitor having one electrode arranged on an electrically-insulating layer carried on said substrate, or a plurality of such MIS-capacitors closely spaced from one another, and at least one contact zone in the substrate surface provided with an externally-accessible ohmic contact, said 35 contact zone containing a material which produces a rectifying effect where said contact zone contacts material of said substrate having the given conductivity type, and said contact zone touching a zone of said substrate forming the counter electrode of said MIS-capacitor or at least one of said MIS-capacitors, wherein in the electrically-insulating layer of said MIS-capacitor or capacitors, the value of the numerical ratio ε/d (where ε is the dielectric 40 constant and d is the layer thickness of the electrically-insulating layer), and/or the value of the surface density s (as hereinbefore defined) of the dopant producing the given conductivity type of said substrate on the surface of the substrate in the zone or zones forming the counter electrode or electrodes of said capacitor or capacitors, and/or the value of the surface density (as hereinbefore defined) of a dopant producing the opposite 45 conductivity type to that of said substrate in a zone or zones of said opposite conductivity

type underlying said one electrode or electrodes of said capacitor or capacitors, and/or the thickness of a zone of the opposite conductivity type to that of said substrate underlying said one electrode or electrodes of said capacitor or capacitors, is or are locally varied in such manner that, when a given voltage, preselectable over a wide range, is connected between said substrate terminal and said electrode or electrodes the local distribution of potential in the or each zone forming the counter electrode of said capacitor or capacitors, exhibits a rise from a minimum to a maximum value in the direction leading laterally away from or towards said contact zone, and voltage sources for selectively connecting different voltages within said wide range between said substrate terminal and said electrode or electrodes such that the difference between said minimum and maximum values during read-out of data stored in said storage element is less than during the write-in and storage of data therein.

When a plurality of MIS-capacitors is used, the distance between the capacitors must be sufficiently narrow as to ensure that, during operation, the boundary fields produced by voltages connected to the electrodes extend across the interspace between two adjacent capacitors, and thus that no potential thresholds, which would obstruct charge flow, arise beneath these interspaces. The maximum width of such an interspace which satisfies this condition will depend upon the operating voltage and also upon the doping of the underlying substrate. Generally speaking, a spacing of less than 3 μ can be taken as a guideline. By the term "surface density" of a dopant with reference to a reference surface is to be understood the mathematical expression dN/dF, where dN signifies the overall doping contained in a cylinder on a base surface area dF, and extending at right-angles to the reference surface through the entire doped material. In the present invention, the reference surface will always be the substrate surface.

Data stores according to the invention are preferably so constructed that the electrically-insulating layer of the MIS-capacitor(s) outside the contact zone does not everywhere possess the same value of the numerical ratio ε/d, so that when the substrate is homogeneously doped, the numerical ratio reduces from a higher value to a lower value in a direction leading laterally away from the contact zone; and/or that at least in the zone(s) forming the counter electrode(s) of the MIS-capacitor(s), the surface density of the basic dopant relative to the substrate surface exhibits a drop from a predetermined value to a lower value in the direction laterally away from the contact zone; and/or that the surface density of the dopant in a layer doped oppositely to the substrate, relative to the substrate surface, exhibits a rise from a predetermined value to a higher value in the direction leading laterally away from the contact zone.

All materials which result in a rectifying effect on contact with the substrate having the basic conductivity type are suitable for use in the contact zone. Thus, this zone may, for example, be formed by a Schottky contact which is arranged on the surface of the substrate. However, it is advantageous, so far as the production of the entire store matrix is concerned, if the contact zone consists of a surface zone in the substrate which is doped oppositely to the remainder of the substrate, the doping being higher than that of any other doping in the substrate, and which is provided with an ohmic connection contact on the surface of the substrate.

In the production of a data store in accordance with the invention, for reasons of cost, it is obviously desirable to use as few process steps as possible. In this respect, it is an advantage if the storage element does not embody in itself all the above-mentioned alternatives.

In practice, a data store will usually be constructed in such a manner that a plurality of storage elements are arranged in the form of a matrix in rows and columns on a common substrate, the contact zones of the individual elements of a column being combined to form a single common column line in the form of a doped strip in the substrate, which possesses an ohmic contact, and which leads past the elements in the column, and that the electrodes of the elements in a row are combined to form a single row line in the form of a strip consisting of electrically conductive material which, on an electrically-insulating layer, leads across all the elements of a row.

In operating a data store in accordance with the invention, a reference voltage is connected to the substrate terminal. Then in order to write an item of data into a storage element, the capacitor electrode is connected to an electrode voltage U relative to the reference voltage, which electrode voltage produces a maximum potential difference $\triangle M$ in the MIS-capacitor zone, whilst the contact zone is connected to a voltage which is either larger or smaller in value than the minimum value, whilst for storage purposes the contact zone is connected to a voltage which is larger in value than the minimum value. In order to read out an item of data, the electrode voltage is altered in such a way that $\triangle M$ is reduced, whilst the contact zone is connected to a voltage which is larger in value than the new minimum value.

In comparison with conventional data stores, the data stores of the present invention have a particularly simple construction and a particularly high data density. In addition,

they can be produced using fewer process steps than can conventional stores. The mode of operation of the store is also very simple.

The invention will now be further described with reference to the drawings, in which:-

Figure 1 is a schematic side-sectional view through an MIS-capacitor with an electrically-insulating layer of varying thickness on the surface of the substrate to illustrate the theory of the invention; potential curves occurring in the interior of the substrate being shown alongside;

Figures 2 to *7* are similar side-sectional views of six different forms of storage element for use in six exemplary embodiments of the invention;

Figure 8 is a plan view of part of a storage matrix of a data store in accordance with the invention;

Figures 9 and *10* are sections taken along the line A-A of Figure 8 using storage elements as shown in Figure 2;

Figures 11 to *15* are sections taken along the line A-A of Figure 8 where the storage elements are as shown in Figure 3, Figure 5, Figure 6, Figure 7, and a variant of that shown in Figure 7, respectively;

Figure 16 is a schematic side-sectional view of a dynamic storage element using the ESFI technique, for use in a data store according to the invention;

Figure 17 is a plan view of the storage element of Figure 16;

Figures 18 to *20* are similar schematic side-sectional views of a storage element in a data store according to the invention to illustrate the operation of the storage element;

Figure 21 is a schematic plan view of a 4×4 storage matrix according to the invention;

Figure 22 is a pulse train programme for a data store according to the invention;

Figure 23 is a plan view of a storage matrix according to the invention; and

Figure 24 is a section along the line IX-IX of Figure 23.

The invention is based on the following principle. In an arrangement comprising a doped semiconductor substrate having a substrate terminal and having on a surface thereof an electrically-insulating layer, upon which an electrode is arranged, when a given reference voltage is connected to the substrate terminal and a given voltage is connected to the electrode, it is possible to calculate the potential distribution in the electrically-insulating layer and in the substrate in accordance with the one-dimensional Poisson equation $d^2\varphi / dx^2 = \quad /\varepsilon$ under the limiting conditions that the potential at the substrate surface at the substrate terminal should be equal to the reference voltage, that the potential at the insulator surface beneath the electrode should be equal to the predetermined electrode voltage, and that the potential at the boundaries separating two different materials from one another, is constant. The result indicates first, that in thermal equilibrium, with a given reference voltage at the substrate terminal, there is at least one electrode voltage U_0 at which no electric field is present in the electrically insulating layer between the substrate and the electrode, so that the potential in this layer is constant. This voltage U_0 is dependent merely upon the properties of the material of the electrically-insulating layer (in particular the dielectric constant) and upon the layer thickness of differently doped layers in the substrate and the dopings of the latter. When the electrode voltage diverges from the value U_0, there is a change in the potential maximum in the substrate. (Here and hereafter, the direction from the reference voltage towards U_0 will always be assumed to be positive as regards the potential, irrespective of the actual polarity of U_0). This change will vary with various parameters (layer thicknesses, dopings and dielectric constant).

This will now be further explained with reference to Figure 1, which shows the potential curves occurring in an arrangement as described above. On a surface of a doped substrate 1 having the layer thickness T and provided with a substrate terminal 01, there is arranged an electrically-insulating layer 2 having two different layer thicknesses d_1 and d_2 respectively. In this surface of the substrate there is a layer 3 which is doped oppositely to the rest of the substrate and having a layer thickness t. An electrode 4 is arranged on the electrically-insulating layer. On the right, the curve 11 shows the potential course in the electrically-insulating layer and in the substrate when the voltage U_0 is connected to the electrode. Here, a state of thermal equilibrium is assumed, in which the layer 3, which is oppositely doped to the substrate, is completely impoverished in majority carriers. As can be seen from Figure 1, the potential in the electrically-insulating layer is constant irrespective of the thickness of the layer. The potential maximum in the substrate lies at the surface with the electrically-insulating layer and is referenced M_{11}. If, now, the electrode is connected to a voltage U_1 which is less than U_0, or has a polarity opposite to U_0, the potential course shown by the curve 12 forms below the electrically-insulating layer where it has the smaller layer thickness d_1, whereas the potential course shown by the curve 13 arises beneath the electrically-insulating layer where it has the greater layer thickness d_2. In both cases, the respective potential maxima M_{12} and M_{13} are located inside the substrate, and are spaced apart by a distance ΔM_1. If, on the other hand, the electrode is connected to a

voltage U_2 which is greater than U_0, the potential courses shown by the curves 14 and 15 arise. The potential course of the curve 14 relates to the thinner part of the electrically-insulating layer, and the potential course of the curve 15 to the thicker part of the electrically-insulating layer. The potential maxima M_{14} and M_{15} respectively are spaced apart by a distance $\triangle M_2$ and are located at the substrate surface with the electrically-insulating layer. Generally speaking, it is true to say that for voltages U_1 the absolute potential maximum lies beneath the thicker, electrically-insulating layer, whilst for voltages U_2 it lies beneath the thinner electrically-insulating layer. Moreover, it is generally applicably observed that the potential differences $\triangle M_1$ and $\triangle M_2$ increase with increasing difference of the values U_1 and U_2 from the value U_0. As the voltages U_1 and U_2 approach the voltage U_0, the differences $\triangle M_1$ and $\triangle M_2$ decrease and when $U_1 = U_0$ and $U_2 = U_0$ assume the value 0. The above-described conditions apply in an analogous manner to the extended situation in which for the electrically-insulating layer, we have $d_1/\varepsilon_1 < d_2/\varepsilon_2$ in the electrically-insulating layer. If the layer which is oppositely doped to the rest of the substrate is not present, the conditions are similar. Conditions become more complicated only when the layer which is oppositely doped to the rest of the substrate exhibits a non-uniform doping or a non-uniform layer thickness. In this case, there is no longer just one voltage U_0 but two or more such voltages. In the event of continuous change there may even be a range of voltages U_0. Generally speaking, it is now true that, with the exception of possible exceptional situations, in the case of structures such as are shown in Figure 1 having differing layer thicknesses of the electrically-insulating layer and oppositely doped layers in the substrate, and/or when layers in the substrate exhibit differing, in particular laterally differing, doping, different potential maxima will form in the substrate when a voltage is connected to the electrode. In the event of a change in this electrode voltage, there is generally also a change in the difference $\triangle M$ between two different potential maxima. The effect can be used to construct data stores of the kind with which the present invention is concerned.

Figure 2 illustrates a first exemplary embodiment of such a data store. On a doped semiconductor substrate 20, for example, of p-doped silicon, having a substrate terminal 21, there is arranged a stepped electrically-insulating layer 22, consisting for example, of silicon dioxide, with two different layer thicknesses d_1 and d_2. This electrically-insulating layer carries an electrode 23. The step between the two layer thicknesses d_1 and d_2 lies below the electrode 23. Arranged in the surface of the substrate is a contact zone 24, which is oppositely and more highly doped than the rest of the substrate and is provided with an externally accessible ohmic connection contact 25. The zone 24, of course, consists of the same material as the substrate. The zone 24 is arranged at the edge of the electrode at that side thereof overlying the part of the insulating layer 22 having the greater layer thickness d_2. The operation of the data store illustrated in Figure 2 is as follows. A reference voltage U is connected to the substrate terminal. A voltage U_2 which is greater than the voltage U_0 is connected to the electrode 23. To this data store, the voltage U_0 is determined by the reference voltage U. The polarity of the voltage U_2 should be such that its sign conforms with that of the majority carriers of the doped substrate. The curve 26 shown in the substrate represents the local course of the potential maximum M. The curve 26 exhibits a jump having a value $\triangle M$ below the step in the electrically-insulating layer. The higher potential value is located beneath the thinner part of the electrically-insulating layer. For the input of data, the contact zone 24 is connected via the terminal 25 with a voltage U_K relative to the reference voltage, which is either larger in value than the smallest potential maximum in the substrate beneath the electrode 23 or is smaller in value than and possesses the opposite sign to this potential maximum. In the former case, no charge carriers can flow into the zone 24 beneath the thinner part of the electrically-insulating layer, whereas in the latter case charges can flow into the zone 24. The solid part of the curve 26 lying beneath the contact zone 24 applies to the first situation, whilst the broken-line part of the curve 26 applies to the second situation. For the storage of the inserted data, the contact zone 24 is connected to a voltage which is larger in value than the smallest potential maximum in the substrate. For read-out of the data, the value of the electrode voltage U_2 is changed in the direction towards or beyond the voltage U_0, whilst the contact zone 24 is connected to a voltage which is larger in value than the smallest potential maximum. By changing the electrode voltage in the direction towards U_0, the difference $\triangle M$ between the two potential maxima is reduced, so that any previously introduced charge carriers flow away into the contact zone and the data is thus read out.

The following values can be taken as an example for the data store shown in Figure 2 :- p-doped silicon substrate with a doping of $5 \times 10^{15}.cm^{-3}$ and a thickness $T = 400\ \mu$; n-doped silicon with a doping of $1 \times 10^{20}.cm^{-3}$ as the contact zone, silicon dioxide as the electrically-insulating layer wih $d_1 = 50$ nm and $d_2 = 300$ nm. A voltage of 15 V can be used as the electrode voltage for write-in and storage, and a voltage of 5 V can be used for

read-out. With an electrode voltage of 15 V, the potential maximum beneath the thinner part of the electrically-insulating layer has a value of about 13 V, whilst beneath the thicker part of the electrically-insulating layer, it has a voltage of about 6 V. With an electrode voltage of 5 V, the potential maximum beneath the thinner part of the electrically-insulating layer has a value of about 4 V, whilst beneath the thicker part of the layer, it has a value of about 1 V. Thereafter, M only has a value of 3 V. Thus, during write-in, the voltage across the contact zone 24 must either be greater than or smaller than 6 V, whilst during storage it must be greater than 6 V. On read-out, the voltage across the contact zone muts be greater than 1 V. In practice, at least during storage and read-out, the voltage across the contact zone will be made to be as great as possible, for example, greater than 30 V.

Figure 3 illustrates a variant of a data store corresponding to Figure 2. It differs from the data store shown in Figure 2 only in that, beneath the electrode in the substrate surface carrying the electrically-insulating layer, the substrate is oppositely doped to a depth t to form an oppositely doped zone 37. The other structural parts correspond to those of the data store of Figure 2 and have therefore been given the same reference numerals.

The operation of the data store illustrated in Figure 3, is governed by the potential curves shown in Figure 1. Accordingly, a main difference to the previously described data store consists in that U_0 now differs substantially from the reference voltage U connected to the substrate terminal. Otherwise, this data store is operated similarly to that shown in Figure 2. The following numerical values may be taken as an example for the construction of the data store :- p-doped silicon substrate wih a doping of $5 \times 10^{14}.cm^{-3}$ and a thickness T = 400 μ, n-doped layer with a doping of $10^{15}.cm^{-3}$ and a layer thickness t = 1 μ, an electrically-insulating layer consisting of silicon dioxide with d_1 = 120 nm and d_2 = 1200 nm, and a doping of the contact zone 24 of $10^{20}.cm^{-3}$. In this case, a voltage of 30 V can be used as the electrode voltage during write-in and storage, which leads to a potential maximum beneath the thinner part of the electrically-insulating layer of about 28.4 V and beneath the thicker part of the electrically-insulating layer of about 18.5 V. This corresponds to a value for ΔM of 9.9 V. During read-out, an electrode voltage of 10 V can be used. This voltage leads to a potential maximum of 9.3 V beneath the thinner part, and 6.1 V beneath the thicker part of the electrically-insulating layer, and thus to a reduction in the value of ΔM to 3.2 V. The voltage applied to the contact zone 24 must satisfy the conditions described with reference to Figure 2 in an analogous manner. Preferably, the voltage applied to the contact zone is selected to be greater than 30 V, at least during storage and read-out.

Figure 4 illustrates a variant of the data store shown in Figure 3. It differs from the two data stores described above in that the contact zone 24 is replaced by a contact zone 28 with an ohmic connection contact 29. This contact zone 28 again consists of a highly doped zone in the substrate which is oppositely doped to the substrate. The contact zone 28 is located in the surface of the substrate at the edge of the electrode beneath which lies the thinner part of the electrically-insulating layer having the thickness d_1. All the other parts have the same reference numerals as in Figure 3. Here again, the potential courses shown in Figure 1 govern the operation of the data store. In operation, for the write-in of data, the electrode is connected to a voltage relative to the reference voltage applied to the substrate terminal 21, which is smaller in value than the voltage U_0. The local course of the potential maximum M beneath the electrode and the zone 28 is represented by the curve 46. At the step in the electrically-insulating layer, there exists a potential difference of ΔM and the higher potential maximum is now located beneath the thicker part of the electrically-insulating layer. During write-in, the contact zone 28 is connected to a voltage which is larger than the smallest potential maximum, or is smaller than the latter. For the former situation, the curve 46 is shown as a solid line beneath the contact zone 28, whilst for the latter situation, it is shown in broken line beneath the zone 28. Only in the second case can charges flow beneath the thicker part of the electrically-insulating layer. During the storage of data, the contact zone is connected to a voltage which is larger than the smallest potential maximum. For the read-out of data, the electrode voltage is displaced in the direction towards or beyond the voltage U_0. As a result of the difference ΔM is reduced or may even be reversed. During read-out, it should again be ensured that the voltage across the contact zone is larger than the smallest potential maximum occurring.

By way of example, the following values can be taken for the arrangement of Figure 4 :- p-doped silicon with a doping of $5 \times 10^{14}.cm^{-3}$ for the substrate, n-doped silicon for the layer 37 with a doping of $10^{15}.cm^{-3}$ and a layer thickness t = 3 μ, substrate thickness T = 400 μ, a contact zone 28 consisting of n-doped silicon with a doping of $1 \times 10^{20}.cm^{-3}$, silicon dioxide as the electrically-insulating layer with d_1 = 120 nm and d_2 = 1200 nm. During write-in and storage, a voltage of 0 V can be used as the electrode voltage, which leads to a potential maximum of 3.3 V beneath the thinner part of the electrically-insulating layer, and to a higher potential maximum of 7.4 V beneath the thicker part of the electrically-insulating layer. For read-out, 30 V can be assumed for the electrode voltage,

which leads to a potential maximum of 29.6 V beneath the thinner part of the electrically-insulating layer and to a potential maximum of 27.3 V beneath the thicker part of the electrically-insulating layer. Thus ΔM changes from 4.1 V at 0 V electrode voltage to −2.3 V at 30 V electrode voltage. The voltage applied to the contact zone 28 will be selected as in the above-described processes, and at least for storage and read-out, it should be greater than 30 V.

In the above-described embodiments of the invention, instead of or in addition to varying the thickness of the electrically-insulating layer, it is also possible to change the dielectric constant ε of this layer. It is, however, essential that the quotient ε/d should either increase or decrease. Generally speaking, it is advantageous if the change in the value of ε/d does not occur abruptly but the values changes continuously across the entire element. In this case, a larger area is available for the storage of the data charge. This is naturally conditional upon the availablity of suitable production processes. n-doped semiconductor material, for example n-doped silicon, can also be used as the substrate. During the operation of such elements, it is then only necessary to change the polarity of the operating voltages.

Figure 5 illustrates a data store in accordance with the invention, in which it is possible to dispense with the need to vary the value of d/ε in the electrically-insulating layer. In this embodiment, on a substrate 50, for example of n-doped silicon having a substrate terminal 51, there is arranged an electrically-insulating layer 52 having a constant thickness and a constant dielectric constant. The substrate 50 is divided into two portions I and II arranged next to one another, the portion II being more highly doped than is the portion I. An electrode 53 is arranged on the electrically-insulating layer above the junction between the two portions. On the surface of the substrate there is provided a contact zone 54 in the substrate, which zone is oppositely and more highly doped than the substrate, and is provided with an externally accessible, ohmic connection contact 55. This zone 54 is arranged at the edge of the electrode and entirely in the higher doped portion II of the substrate. In this case, there are two electrode voltages U_{0I} and U_{0II} with which no field exists in the electrically-insulating layer. U_{0I} will be assumed to be the voltage at which no electric field prevails in the electrically-insulating layer above the portion I, and U_{0II} will be assumed to be the voltage at which no field prevails in the electrically-insulating layer above the zone II. For electrode voltages U_{0I} which are equal to or greater than the reference voltage U, or have a polarity which is opposite to that of U, similar potential distributions occur as are represented by the curves 11 and 12 in Figure 1. Here the potential maximum is greater in the portion II than in the portion I and in both cases is located within the substrate. If the electrode voltage is shifted away from U_{0I}, the difference ΔM between the two potential maxima increases. For electrode voltages U_{0II} which are equal to or less than U, similar potential distributions to those shown in the curves 13 and 14 are obtained. The potential maximum in the portion II here is greater in value than that in the portion I and in both cases lies at the substrate surface. If the electrode voltage U is shifted away from U_{0II} the difference ΔM between the potential maxima increases. For electrical voltages between U_{0I} and U_{0II}, conditions are more complicated. However, here again operation is possible. This case will not be explained in detail, as a person skilled in the art will be able to determine the necessary conditions with the aid of the solution to the Poisson equation under the limiting and secondary conditions mentioned above.

The data store shown in Figure 5 is operated in the following manner. For the write-in of data, the electrode 53 is connected to an electrode voltage, and the contact zone 54 is connected to a voltage U_K which is either greater than or smaller than the smallest potential maximum at this electrode voltage. The curve 56 represents the course of the potential maximum M beneath the electrode 53 and the zone 54 showing the potential drop ΔM at the divising surface between the portion I and the portion II. Beneath the contact zone 54, the curve for the first situation is depicted as a broken line and that for the second situation as a solid line. During storage, the contact zone is connected to a voltage which is greater than the smallest potential maximum. For the read-out of the data, the electrode voltage is displaced in a direction in which the potential difference ΔM is reached, and the contact zone is connected to a voltage which again is larger than the smallest potential maximum.

The following data can be used, for example, in such a data store: n-doped silicon as substrate, with a doping of 5×10^{14}.cm^{-3} in the portion I, and a doping of 5×10^{15}.cm^{-3} in the portion II and with a thickness T = 400 μ, p-doped silicon as the contact zone with a doping of 1×10^{20}.cm^{-3}, silicon dioxide as the electrically-insulating layer with a layer thickness of 120 nm. For write-in and storage, an electrode voltage of −15 V can be used, which produces a potential maximum of −13.5 V in the portion I and of −10 V in the portion II, and thus a potential difference ΔM of 3.5 V. A value of −5 V is suitable as the electrode voltage for read-out, as a result of which a potential maximum of −4 V is produced in the portion I and of −2.5 V in the portion II. Thus the potential difference ΔM is reduced to 1.5 V. The voltage across the contact zone 54 is preferably selected to be

greater than −20 V, at least during storage and read-out.

Figure 6 illustrates a data store in which, on a doped substrate 60 provided with a substrate terminal 61, there is arranged an electrically-insulating layer 62 having a constant layer thickness and a constant dielectric constant, and carrying an electrode 63. At the edge of the electrode there is again arranged a contact zone 64, which is doped more highly than and oppositely to the substrate, and is provided with an ohmic connection contact 65. In the substrate at the surface carrying the electrically-insulating layer, there is arranged a layer 66 which is oppositely doped to the substrate and reaches to the contact zone. This layer is divided into two portions I′ and II′, lying next to one another; only the portion I′ is in contact with the contact zone 64. The portion II′ is more highly doped than the portion I′. In addition, the portion I′ is doped to a lesser extent than the contact zone. The thickness t of this layer is less than the thickness of the substrate. This data store is operated in a similar way to that of Figure 5. It is merely necessary to select the voltage values to be used and their polarity differently. The following values can be taken as an example : p-doped silicon with a doping of $8 \times 10^{15}.cm^{-3}$ and a thickness T = 400 μ, as the substrate; the layer 66 in the form of n-doped silicon with a layer thickness of 1 μ, a doping of $8 \times 10^{15}.cm^{-3}$ in the portion I′ and of $16 \times 10^{15}.cm^{-3}$ in the portion II′, and silicon dioxide with a layer thickness of 12 nm as the electrically-insulating layer. For write-in and storage it is possible to connect an electrode voltage to 0 V relative to the reference potential to the substrate terminal by which means an absolute potential maximum of 3.3 V is produced in the portion I′ and of 7.9 V in the portion II′. This corresponds to a potential difference ΔM of 4.6 V. For read-out, it is possible to connect a voltage U_2 of 30 V relative to the reference voltage, by which means an absolute potential maximum of 27.5 V is produced in the portion I′ and of 30.7 V in the portion II′. Thus, ΔM has been reduced by 1.4 V to a value of 3.2 V. The voltage across the contact zone is selected to be greater than 30 V, at least during storage and read-out.

Figure 7 illustrates a data store in which, on a doped substrate 70 provided with a substrate terminal 71, there is again arranged an electrically-insulating layer 72 having a constant layer thickness and a constant dielectric constant, and which carries an electrode 73. At the edge of the electrode there is arranged as before a contact zone 74 which is oppositely doped to the substrate and has an ohmic connection contact 75. In the substrate at the surface carrying the electrically-insulating layer 72 there is a zone 77 consisting of doped semiconductor material which is oppositely doped to the rest of the substrate and which encloses the contact zone. This zone is again divided into two portions I″ and II″ which lie next to one another, only the portion I″ contacting the contact zone. The portion II″ has a greater thickness than the portion I″. The entire zone 77 is homogeneously doped and has a lower doping value than does the contact zone. The potential distributions in this data store and its operation are governed by the same conditions as are the data stores shown in Figure 5 and Figure 6. The portion I″ corresponds to the portions I and I′ of these embodiments, and the portion II″ corresponds to the portions II and II′.

Two examples of such a store will be quoted :-

1. A p-doped silicon substrate with a doping of $10^{14}.cm^{-3}$ and a thickness T = 400 μ, n-doped silicon with a doping of $10^{14}.cm^{-3}$ as the zone 77, with a thickness of 1 μ in the portion I″ and of 9 μ in the portion II″, and a silicon dioxide layer of 100 nm thickness as the electrically-insulating layer. For write-in and storage, an electrode voltage of 30 V can be used, by which means a potential maximum of 29.1 V is produced in the portion I″ and of 29.7 V in the portion II″. This results in a potential difference ΔM of 0.6 V. For read-out, an electrode voltage of 10 V is connected, by which means a potential maximum of 9.5 V is produced in the portion I″ and of 10 V in the zone II″. Accordingly, on read-out, the potential difference has been reduced by 0.1 V to 0.5 V. The voltage connected to the contact zone is preferably selected to be greater than 30 V, at least during storage and read-out.

2. A p-doped silicon substrate with a doping of $8 \times 10^{15}.cm^{-3}$ and a thickness T = 400 μ, n-doped silicon with a doping of $8 \times 10^{15}.cm^{-3}$ as the zone 77 with a thickness of 1 μ in the portion I″ and of 5 μ in the portion II″ and with a silicon dioxide layer of 120 nm thickness as the electrically-insulating layer. For write-in and storage, an electrode voltage of 0 V can be used, by which means a potential maximum of 3.3 V is produced in the portion I″ and a potential maximum of 59 V is produced in the portion II″, which corresponds to a potential difference ΔM of 55.7 V. For read-out, it is possible to use an electrode voltage of 30 V, by which means a potential maximum of 27.5 V is produced in the portion I″ and of 77.4 V in the portion II″. Accordingly, during read-out the potential difference ΔM is reduced by 5.8 V to 49.9 V. The voltage connected to the contact zone is preferably selected to be greater than 30 V, at least during storage and read-out.

In a variant of the data store of Figure 7, the layer thickness of the portion I″ is equal to 0, in other words this zone has the doping substrate. For such a store, the following values can

be used as examples :- a p-doped silicon substrate with a doping of 8 × 10^{15}.cm^{-3} and a thickness T = 400 μ, an n-doped zone II″ with a doping of 8 × 10^{15}.cm^{-3} and a thickness of 1 μ, silicon dioxide with a thickness of 300 nm as the electrically-insulating layer. For write-in and storage, an electrode voltage of 20 V can be connected, by which means a potential maximum of 17.9 V is produced within the layer and of 7.8 V outside the layer, which corresponds to a potential difference of 10.1 V. For read-out, an electrode voltage of 10 V can be connected, by which means a potential maximum of 10.6 V is produced within the layer and of 2.8 V outside the layer. Thus, the potential difference is reduced by 2.3 V to 7.8 V during read-out. At least during storage and read-out, the voltage connected to the contact zone is preferably greater than 20 V.

Each of the data stores shown in Figures 2 to 4 can be combined with one of the data stores shown in Figures 5 to 7, or the variant of Figure 7. The latter can also be combined with one another.

Instead of a p-doped substrate, it is also possible to use an n-doped substrate.

In the data stores illustrated in Figures 5 to 7, and the variant of Figure 7, it is not necessary that the surface density of the doping relative to the substrate surface should, as described, change suddenly in the direction leading laterally away from the contact zone, but it can equally well change continuously.

At this point, it should be stressed that the embodiments illustrated in the drawings represent special embodiments of data stores corresponding to the invention, and that more complex structures within the scope of the invention are also possible.

In data stores in accordance with the invention, the storage elements can be arranged in a very simple manner to form a storage matrix. Figure 8 is a plan view of part of such a matrix. Highly doped lines 81 to 83 oppositely doped to the substrate are arranged as column lines at spaced intervals parallel to one another in a substrate 80 consisting of doped semiconductor material. On the surface of the substrate there is arranged an electrically-insulating layer (not shown). On the latter, strips 84 and 85 of electrically conductive material are arranged next to one another as row lines at intervals transversely to the column lines. Storage elements 814 to 835 are indicated by broken line framings. Figures 9 to 16 show side-sectional views along the line A-A of Figure 8 to illustrate the construction of such a storage matrix for the various forms of storage element illustrated in Figures 2 to 7. The data store represented in Figure 2 is the basis of Figure 9 and Figure 10. The doped lines 81 to 83 here and in the following Figures assume the role of the contact zones of the stores, i.e. all the data stores in a column are connected to a common contact zone. In Figure 9, the electrically-insulating layer 87 is stepped to provide three different thicknesses. In the regions of the actual storage elements 815 to 835, this layer is stepped as shown in Figure 2. In each case, in the intermediate zone between two of these zones 815 to 835, the electrically-insulating layer exhibits, at least beneath the row line, a greater layer thickness d_3 than elsewhere. This serves to separate the individual storage elements from one another. In the embodiment of Figure 10, this separation is effected in a different way, viz. by means of a "channel-stop" diffusion. For this purpose, highly doped channels 91 which possess the same doping type as the substrate are diffused into the substrate surface parallel to the column lines. In addition, in Figure 10, the storage elements 815 to 835 are not arranged on the same side of the column line. As shown in Figure 10, the storage elements 815 to 835 are arranged on the left of the associated column lines 81 and 83, whilst the storage element 825 is arranged on the right of the associated column line 82.

Figure 11 is based on a storage element as shown in Figure 3. It is not necessary in this case to separate the individual elements, so that the insulation layer thickness in the zones between two storage elements can be of any thickness. Preferably, therefore, as illustrated this layer thickness can be the same as the greater or smaller layer thickness in the storage element, which greatly simplifies production. In Figure 11, the layer thickness in the intervals between storage elements is shown as being the same as the greater layer thickness in a storage element. A storage matrix can be constructed in a similar way to that illustrated in Figure 11, but based on the storage element shown in Figure 4. The greater layer thickness in the region of the storage element then lies beneath the column line.

Figure 12 illustrates the construction of a matrix based on the storage element shown in Figure 5. Along the row line, the substrate is divided alternately into weakly doped zones I and highly doped zones II. Although not shown in Figure 12, the individual storage elements 815 to 835 are again separated by arranging that in the intervals between two such elements, the electrically-insulating layer 87 possesses a greater layer thickness, at least beneath the row line.

Figure 13 shows the construction of a matrix which is based on the storage element illustrated in Figure 6. The thickness of the electrically-insulating layer 87 can in this case remain constant since the layers 66, consisting of the two portions I′ and II′ are already effectively separated from one another.

Figure 14 shows the construction of a storage matrix which is based on the data store illustrated in Figure 7. Here too, the electrically-insulating layer can have a constant thickness, since the layers 76 consisting of the two portions I″ and II″ are already effectively separated from one another.

Figure 15 illustrates the construction of a storage matrix in which the variant of the data store illustrated in Figure 7 previously described, is used as the storage element. The individual storage elements must in this case, however, be separated from one another. This is again effected by ensuring that the electrically-insulating layer possesses a greater layer thickness in the intervals between storage elements than elsewhere, at least below the row lines.

An embodiment of the invention which is particularly simple to operate is illustrated in Figures 16 and 17 and will now be described. The storage element in this case is of a particularly simple design when constructed using the ESFI technique. Advantageously, it is possible to store considerably more of the charge representing the data, than was previously possible with corresponding known storage elements.

As stated above, this storage element is preferably produced using the SOS technique, in particular the ESFI technique. As shown in Figure 16, on an electrically-insulating substrate 1′ which may consist, for example, of spinel or sapphire, there are arranged silicon islands 2′. An electrically-insulating layer 32′, which is a thin oxide layer, is applied to the silicon layer 2′. By means of a photolithographic masking process, this thin oxide layer 32′ is reinforced at given points to form a thick oxide layer 33′. The thickness 3′ of the thin oxide layer 32′ may, for example, be 100 nm, and the thickness 31′ of the thick oxide layer 33′ may, for example, be 800 nm. A metal conductor path 4′, preferably made of aluminium, which serves as word line, is arranged on the arrangement described above. The silicon island 2′ is preferably p-doped (e.g. to a charge carrier density of $10^{15}.cm^{-3}$) beneath both the thick oxide layer 33′ and the thin oxide layer 32′. The thick oxide layer 33′ is adjoined by an oppositely doped, preferably an n^+-doped, zone 21′ (having, for example, a charge carrier density of $10^{19}.cm^{-3}$) which represents the bit line. The storate element is operated via the bit line 21′ and the conductor path 4′, which forms the word line.

In operation, the thin oxide layer 32′ is exploited as a storage capacitor, whilst the thick oxide layer 33′ is used as a switching means, with the aid of which the electrical isolation from the bit line 21′ is effected, use being made of the fact that in accordance with the formula :-

$$U_{T32',33'} = \left[d_{3',31'}/\varepsilon_{ox}).(2q.\varepsilon_{Si}.N)^{\frac{1}{2}}.(2Ø_F)^{\frac{1}{2}} \quad + 2Ø_F\right]$$

the thin oxide layer 32′ has a lower starting voltage $U_{T32'}$ than that of the thick oxide layer 33′. In the formula given, $d_{3',31'}$ is the thickness of the thin oxide layer or of the thick oxide layer, as the case may be, ε_{ox} is the dielectric constant of the gate oxide, q is the elementary charge, ε_{Si} is the dielectric constant of silicon, N is the doping of the basic material (i.e. the doping of the silicon islands 2′ beneath the thick oxide layer 33′ and the thin oxide layer 32′) and $Ø_F$ is the Fermi potential.

Operation of the arrangement shown in Figures 16 and 17 will now be described with reference to Figures 18 to 20. Elements of these figures which have already been described in association with Figures 16 and 17 have been given the same reference numerals, but differences in doping have not been indicated. As a commencing state for Figure 18, it will be assumed that a voltage of 0 V is applied to the bit line 21′ and that the gate voltage U_G of the MOS-capacitor, which latter consists of the doped semiconductor layer 22′, the thin oxide layer 32′ and the thick oxide layer 33′, and the conductor path 4′, is greater than $U_{T33'}$ at a terminal 41′ which is connected to the aluminium conductor path 4′. An inversion layer is therefore formed beneath the two dielectric zones of the MOS-capacitor. To enable charge to be stored, the gate voltage is reduced below the starting voltage of the thick oxide layer $U_{T33'}$ by a small amount ΔU. This is shown in Figure 19. The inversion layer beneath the thick oxide layer 33′ then disappears, whilst the charge beneath the thin oxide layer 32′ remains stored in the potential well corresponding to the voltage $U_G = U_{T33'} - \Delta U$.

To enable the data to be read out, the bit line 21′ is precharged to a reference potential U_{ref} and then, as illustrated in Figure 20, the gate voltage is reduced from a value of $U_{T33'} - \Delta U$ to, for example, 0 V. As a result of the disappearance of the potential well, the charge carriers which had previously accumulated at that point can move into the layer 22′. A part of these charge carriers flows to the bit line 21′ which has been precharged to as high a reference potential as possible, where it gives rise to a read-out signal, on the basis of which the data is re-written in via a regenerator circuit additionally provided for this purpose. The charge carriers which do not reach the bit line recombine in the layer 22′. With a suitable choice of dimensions, it is possible to reach a compromise between the capture

cross-section, (i.e. the active surface 23′ between the n^+-doped zone 21′ and the p-doped substrate 2′) and the simultaneously increasing bit line capacitance.

The signal which reaches the bit line 21′ changes the voltage U_{ref} of a capacitor 6′. The corresponding signal is amplified by an amplifier 61′.

5 Figure 21 illustrates a 4 × 4 matrix according to the invention. The individual storage elements 10′, 20′, 30′, and 40′ are each constructed as shown in Figues 16 and 17. The storage element 10′ and the storage element 30′ are connected to a bit line 211′. The storage elements 20′ and 40′ are connected to a bit line 212′. The storage elements 10′ and 20′ are connected to one another via a word line 42′. The storage elements 30′ and 40′ are 10 connected to one another via a word line 43′.

In the following, explanation of the operation of such a matrix, a thick oxide start voltage $U_{T33'}$ of +10 V will be assumed, whilst the thin oxide start voltage $U_{T32'}$ will be assumed to be 0 V. It will be additionally assumed that charge is located beneath the thin oxide layer of the storage element 40′, and that all the word and bit lines are charged to a voltage of 8 V in 15 the rest state. It is now established that a binary "0" is stored in each of the elements 10′, 20′ and 30′ and a binary "1" is stored in the element 40′.

The write-in of a binary "1" into the element 10′ will now be explained with reference to Figure 22. At a time t_1, the bit line 211′ is connected to 0 V and at a time t_2 the word line 42′ starts charging to 15 V. As already explained above with reference to Figure 18, a cohesive 20 inversion layer is formed beneath the two parts 101′ and 102′ of the MOS-capacitance of the element 10′. At a time t_3 the voltage U_{42} connected to the word line 42′ start reducing to a value of 8 V, whereby the thick oxide start voltage is undershot and the inversion layer beneath the thick oxide layer 101′ of the element 10′ disappears. However, as a result of the potential well corresponding to the voltage U_{42} (= 8 V) connected to the word line 42.049, 25 the charge remains stored beneath the thin oxide layer 102′ of the element 10′, and this also in no way changes when the voltage U_{211} connected to the bit line 211′ is increased at a time t_4 to a value of 8 V. Thus the rest state is again reached.

Read-out takes place row by row, i.e. the bit lines 42′ and 43′ are precharged to a reference potential U_{ref} and in the selection of a word line, a read-out signal appears on all 30 the bit lines, which is processed by read-out amplifiers 62′ connected to the bit lines. When, for example, at a time t_5, the reference potential U_{ref} is set up on the bit lines 211′ and 212′, and at a subsequent time t_6, the word line 43′ is connected to a voltage of 0 V, no read-out signal arises on the bit line 211′, which corresponds to a stored binary "0", whilst a read-out signal corresponding to the stored binary "1" of the storage element 40′ occurs on the bit 35 line 212′. As can be seen from the pulse train programe of Figure 22, the regenerator circuit 62′ connected to the bit line 212′ must trigger the re-write-in of the binary "1" into the element 40′. The binary "0" which does not produce a read-out signal on the bit line 211′ also does not require to be specially regenerated. At times t_7 and t_8, as a result of the lowering of the voltage U_{212} to 0 V on the bit line 212′ (at the time t_7) and the raising of the 40 voltage U_{43} to 15 V (at the time t_8) on the word line 43′, the binary "1" is again written into the element 40′.

Advantageously, the operation is not sensitive in respect of phase shifting of the drive pulse trains. That is to say, it is quite possible for the time t_2 to precede or coincide with the time t_1. The same also applies to the following times t_3 and t_4.

45 A further advantage consists in the relatively long regeneration time. The binary "1" is represented by the presence of charge carriers beneath the thin oxide layer 32′. The number of charge carriers will increase due to thermal pair formation.

Figure 23 is a plan view of a form of storage matrix in accordance with the basic circuit of Figure 21. Details of Figure 23 which have already been described with reference to Figure 50 21 have been given the same reference numerals. Figure 24 is a section on the line IX-IX of Figure 23.

As can be seen from Figure 23, in order to increase the read-out signal, the bit lines 211′ and 212′ are each arranged at three sides of the storage element, which is in the form of a rectangle. For example, the bit line 211′ adjoins the thick oxide layer 101′ on three sides. 55 As a result, as described in detail above, the capture cross-section of the bit line 211′ is increased in relation to the fundamental circuit diagram of Figure 1.

It is also possible to design the storage element using the solid silicon technique. However, isolating diffused zones are then necessary to prevent the data content of adjoining elements being influenced on read-out of data from a storage element.

60 Although not specifically illustrated, it will be appreciated that, as previously stated, in each of the illustrated embodiments of storage element for use in the invention, the single MIS-capacitor can be replaced by a plurality of MIS-capacitors, provided that these are so closely spaced (e.g. by less than 3μ) that no potential thresholds which would obstruct charge flow arise in the substrate beneath the interspaces between the individual capacitors.

WHAT WE CLAIM IS:-

1. A data store for the storage of data in the form of electrical charge carriers having at least one dynamic storage element arranged at the surface of a doped semiconductor substraye of a given conductivity type, provided with a substrate terminal, the or each said storage element comprising an MIS-capacitor having one electrode arranged on an electrically-insulating layer carried on said substrate, or a plurality of such MIS-capacitors closely spaced from one another, and at least one contact zone in the substrate surface provided with an externally-accessible ohmic contact, said contact zone containing a material which produces a rectifying effect where said contact zone contacts material of said substrate having the given conductivity type, and said contact zone touching a zone of said substrate forming the counter electrode of said MIS-capacitor or at least one of said MIS-capacitors, wherein in the electrically-insulating layer of said MIS-capacitor or capacitors, the value of the numerical ratio ε/d (where ε is the dielectric constant and d is the layer thickness of the electrically-insulating layer), and/or the value of the surface density s (as hereinbefore defined) of the dopant producing the given conductivity type of said substrate on the surface of the substrate in the zone or zones forming the counter electrode or electrodes of said capacitor or capacitors, and/or the value of the surface density (as hereinbefore defined) of a dopant producing the opposite conductivity type to that of said substrate in a zone or zones of said opposite conductivity type underlying said one electrode or electrodes of said capacitor or capacitors, and/or the thickness of a zone of the opposite conductivity type to that of said substrate underlying said one electrode or electrodes of said capacitor or capacitors, is or are locally vaired in such manner that, when a given voltage, preselectable over a wide range, is connected between said substrate terminal and said electrode or electrodes the local distribution of potential in the or each zone forming the counter electrode of said capacitor or capacitors, exhibits a rise from a minimum to a maximum value in the direction leading laterally away from or towards said contact zone, and voltage sources for selectively connecting different voltages within said wide range between said substrate terminal and said electrode or electrodes, such that the difference between said minimum and maximum values is less during read-out of data stored in said storage element is less than during the write-in and storage of data therein.

2. A data store as claimed in Claim 1, wherein the value of the ratio ε/d for the electrically-insulating layer of the or each MIS-capacitor falls laterally in the direction away from said contact zone from a higher to a lower value, and/or that, at least in the zone of the or each MIS-capacitor, the surface density relative to the substrate surface of the basic doping of said substrate drops from a first value to a lower value in the direction leading laterally away from said contact zone, and/or that the surface density relative to the substrate surface of said oppositely doped zone rises from a first value to a higher value in the direction leading laterally away from said contact zone.

3. A data store as claimed in Claim 1 or Claim 2, wherein said contact zone is a zone in the surface of said substrate which is oppositely doped to and more highly than any other part of the substrate, and which has an ohmic contact at the surface of the substrate.

4. A data store as claimed in Claim 3, wherein with the exception of said contact zone, the substrate is only doped with a dopant producing said given conductivity type.

5. A data store as claimed in Claim 4, wherein said substrate is homogeneously doped.

6. A data store as claimed in Claim 3, wherein in the substrate there is arranged a doped zone of predetermined constant depth, which is oppositely doped to the substrate, and which at least in the region of the or each MIS-capacitor adjoins the substrate surface and the contact zone, the remainder of the substrate, with the exception of the contact zone, being homogeneously doped with a dopant producing said given conductivity type.

7. A data store as claimed in Claim 6, wherein said oppositely doped zone is homogeneously doped.

8. A data store as claimed in any one of the preceding Claims, wherein the numerical ratio ε/d of the electrically-insulating layer of the or each MIS-capacitor is constant throughout the layer.

9. A data store as claimed in any one of Claims 4 to 7, wherein ε is constant in the or each MIS-capacitor.

10. A data store as claimed in Claim 9, wherein the thickness of said electrically-insulating layer varies in a stepwise manner between a higher and a lower value in a lateral direction away from or towards said contact zone.

11. A data store as claimed in Claim 4, wherein in the region of the or each MIS-capacitor, the substrate is divided into two juxtaposed portions having different homogeneous dopings, only one of said portions adjoining the contact zone and the doping in that portion being higher than in the other portion.

12. A data store as claimed in Claim 6, wherein said oppositely-doped zone is divided into two portions having different homogeneous dopings, only that portion having the

weaker doping adjoining said contact zone.

13. A data store as claimed in Claim 6, wherein said oppositely-doped zone is homogeneously doped and is divided into two portions of different thickness, only the thinner of said portions adjoining said contact zone.

14. A data store as claimed in Claim 6, wherein said oppositely-doped zone is homogeneously doped and has a constant layer thickness, said layer being spaced away from said contact zone.

15. A data store as claimed in any one of Claims 1 to 14, comprising a plurality of said storage elements arranged in rows and columns to form a matrix on a common substrate, the contact zones of the individual elements of a column being combined to form a single common column line in the form of a doped strip in the substrate, which strip is provided wih an ohmic connection contact, and extends past the elements in the column, and the electrodes of the elements in a row are combined to form a single row line in the form of a strip of electrically-conductive material which is led across all the elements of the row on said electrically-insulating layer.

16. A data store as claimed in Claim 15, wherein adjacent elements of a row line are electrically separated from one another by a portion of said electrically-insulating layer having an increased thickness lying between said adjacent elements, at least beneath the row line.

17. A data store as claimed in Claim 15, wherein adjacent elements of a row line are electrically separated from one another by a highly doped surface zone of the substrate lying between said adjacent elements, at least beneath the row line.

18. A data store as claimed in Claim 10, wherein said insulating layer has a thinner part arranged on a first zone of a doped semiconductor layer serving as said substrate, and a thicker portion arranged on a second zone of said semiconductor layer laterally adjoining said first zone, said semiconductor zone having a third zone laterally adjoining said second zone and oppositely doped to said first and second zones, said oppositely doped zone representing the bit line of said storage element and forming said contact zone, and a conductor path extending over both the thinner and thicker portions of said insulating layer representing the word line of said storage element and forming the electrode or electrodes of said capacitor or capacitors.

19. A data store as claimed in Claim 18, wherein said thicker portion of said insulating layer is arranged in the form of an at least partial ring or rectangle around the thinner portion of said insulating layer, and said third zone is arranged in the form of an at least partial ring or rectangle around said second zone.

20. A data store as claimed in Claim 18, wherein said thinner portion of the insulating layer is in the form of a rectangle, and said thicker portion of said insulating layer surrounds said rectangle on three sides, and that said third zone surrounds said second zone on three sides thereof.

21. A data store as claimed in any one of Claims 18 to 20, constructed using the ESFI(SOS)-technique.

22. A data store as claimed in Claim 21, wherein said semiconducting layer is supported on a spinel or sapphire body.

23. A data store as claimed in any one of Claims 18 to 22, wherein said semiconducting layer consists of silicon.

24. A data store as claimed in any one of Claims 18 to 21, constructed using the solid-silicon-technique, the individual storage elements being electrically separated by doped zones in said substrate.

25. A data store as claimed in any one of Claims 18 to 24, wherein said thinner portion of said insulating layer is a 100 nm thick silicon dioxide layer, and the thicker portion of said insulating layer is an 800 nm thick silicon dioxide layer.

26. A data store as claimed in any one of Claims 18 to 25, wherein said second zone is p-doped with a charge carrier density of $10^{15}.cm^{-3}$, and that said third zone is n^+-doped with a charge carrier density of $10^{19}.cm^{-3}$.

27. A data store as claimed in any one of Claims 18 to 26, wherein said conductor path consists of aluminium.

28. A data store substantially as hereinbefore described with reference to and as shown in any one of Figures 2 to 7, or Figure 8 and any one of Figures 9 to 15, or Figures 16 to 20, or Figures 21 to 24, of the drawings.

29. A method of operating a data store as claimed in any one of the preceding Claims, wherein said substrate terminal is connected to a reference voltage, wherein for the write-in of data into a storage element, said electrode is connected to voltage U relative to said reference voltage, which produces a maximum potential difference ΔM between the maximum and the minimum of the maximum potential distribution curve in the MIS-capacitor and said contact zone is connected to a voltage which is either larger or

smaller than the smallest potential maximum, wherein for storage of write-in data, the contact zone is connected to a voltage which is larger than the smallest potential maximum, and wherein for read-out of data from said element, the voltage applied to said electrode is altered so as to reduce the value of ΔM and the contact zone is then connected to a voltage which is larger than the new smallest potential maximum.

For the Applicants,
G.F. REDFERN & CO.,
Marlborough Lodge,
14 Farncombe Road,
Worthing,
West Sussex.

Printed for Her Majesty's Stationery Office, by Croydon Printing Company Limited, Croydon, Surrey, 1980.
Published by The Patent Office, 25 Southampton Buildings, London, WC2A 1AY, from which copies may be obtained.

Fig.1

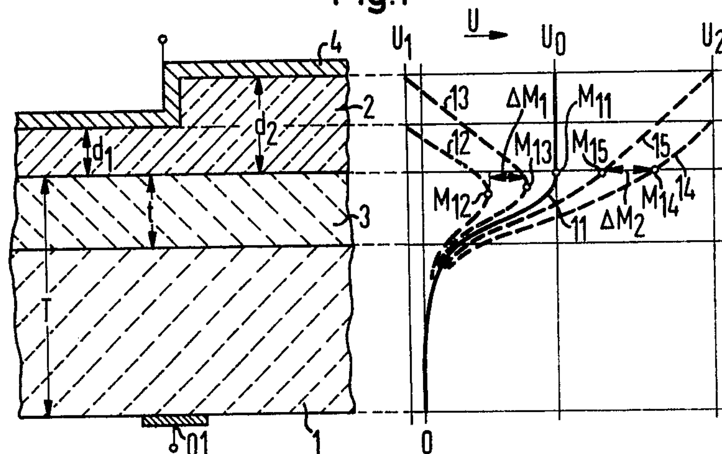


Fig.2

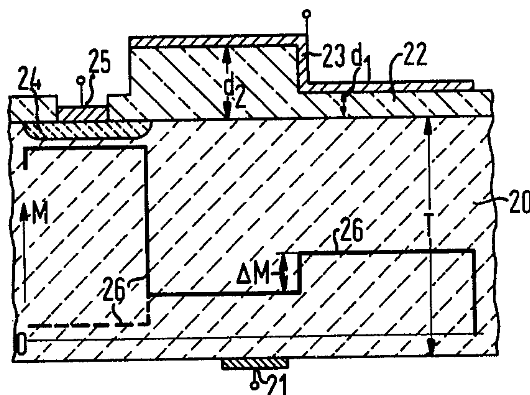


Fig.3

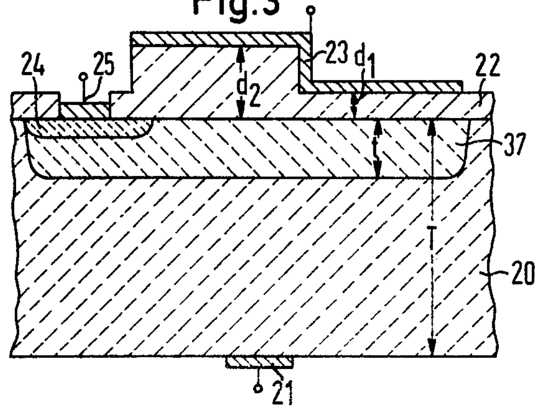


Fig.4

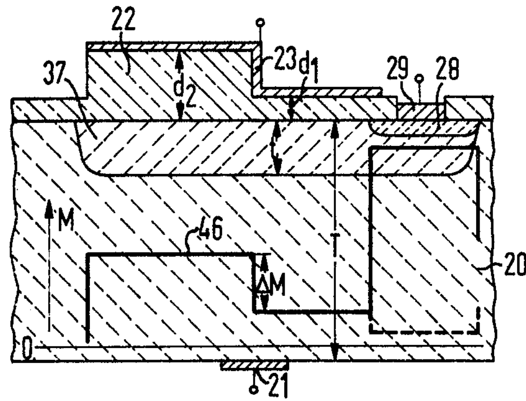


Fig.5

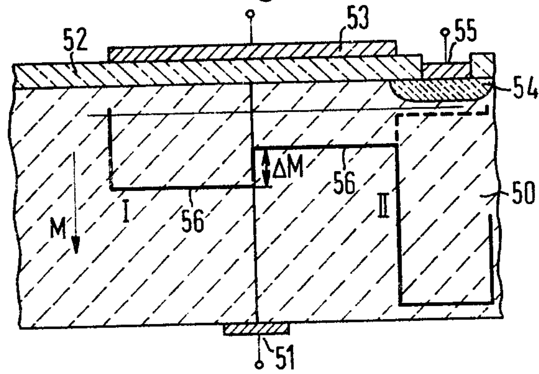


Fig.6

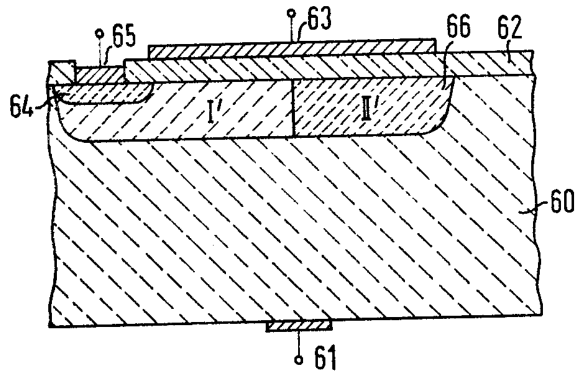


Fig.7

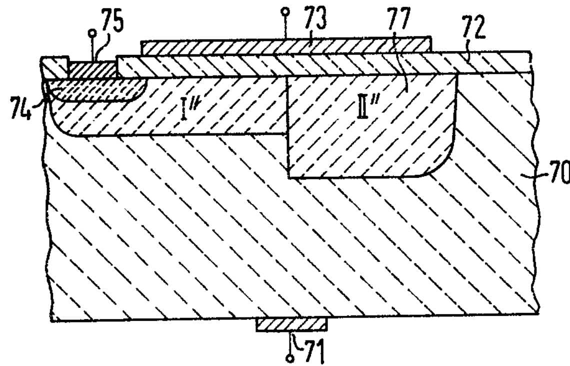


Fig.8

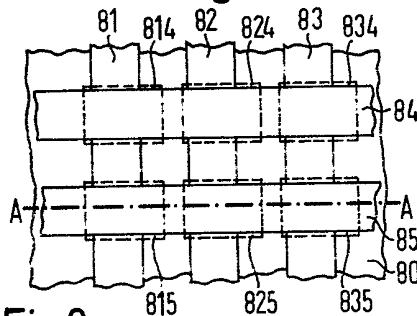


Fig.9

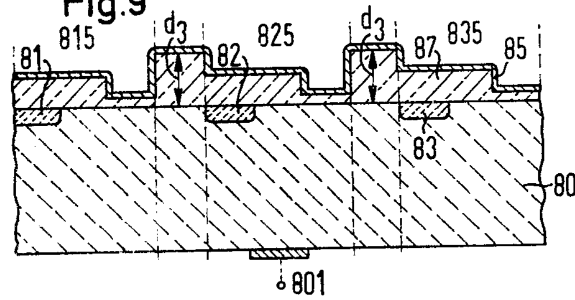


Fig.10

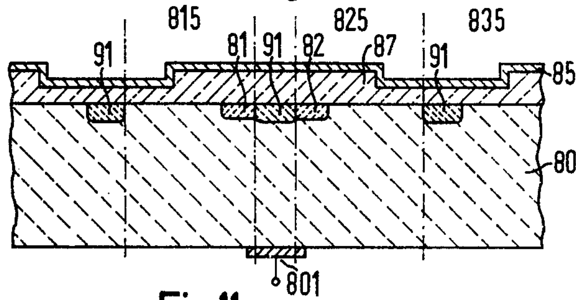


Fig.11

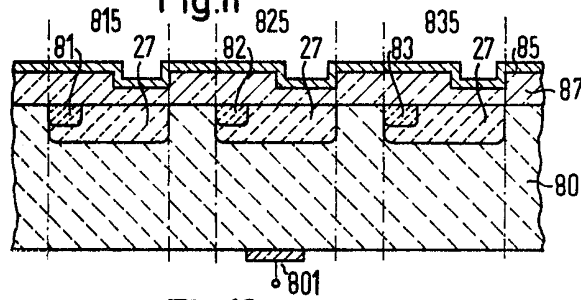


Fig.12

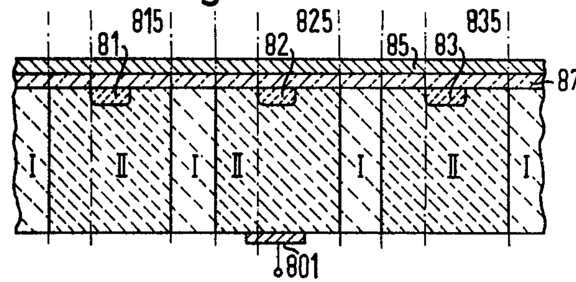


Fig.13

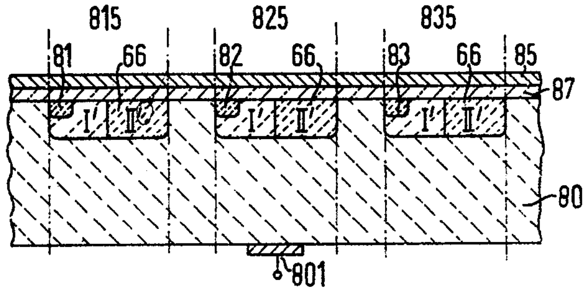


Fig.14

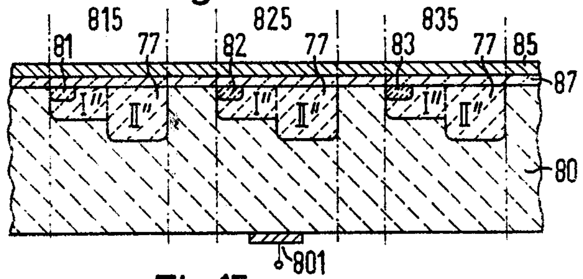


Fig.15

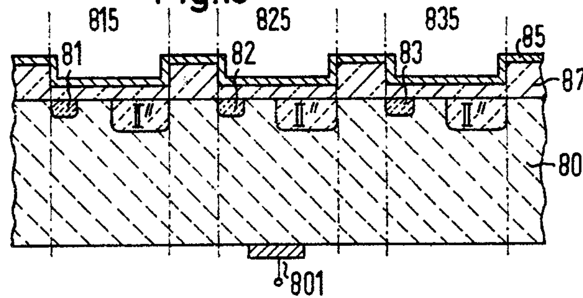


Fig. 16

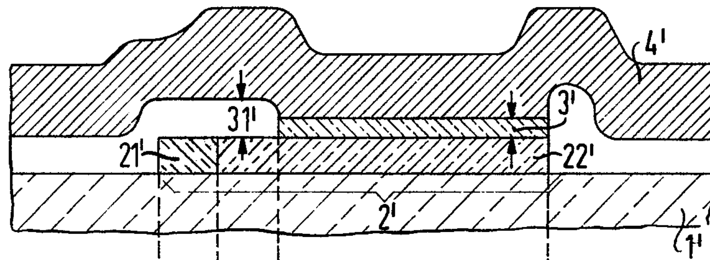


Fig. 17

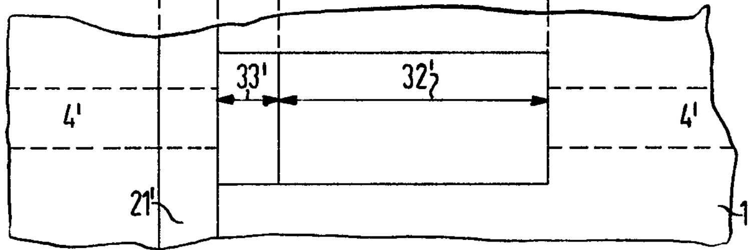


Fig. 18

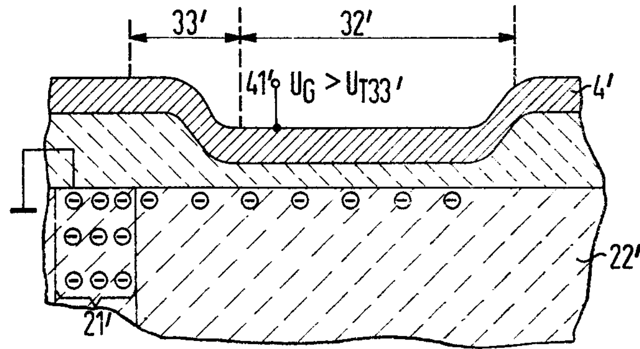


Fig. 19

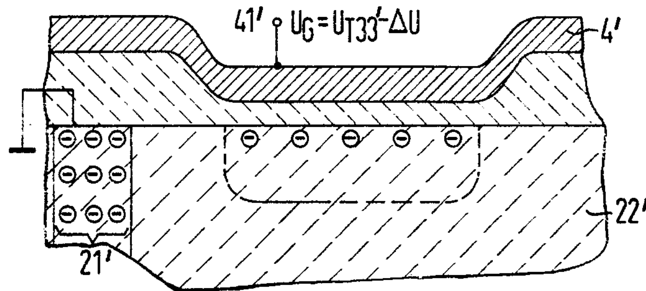


Fig. 20

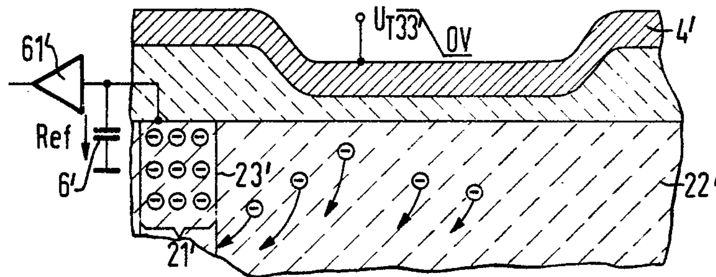


Fig. 21

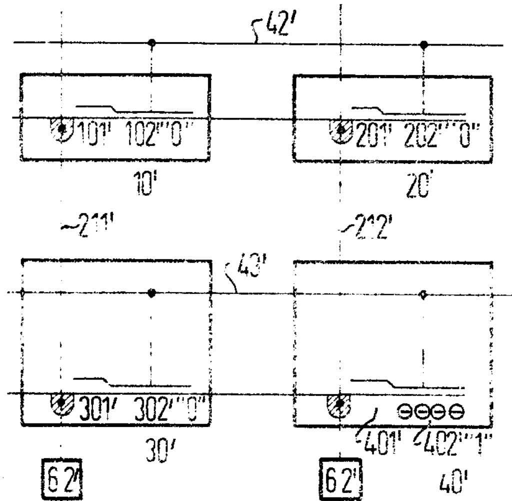


Fig. 22

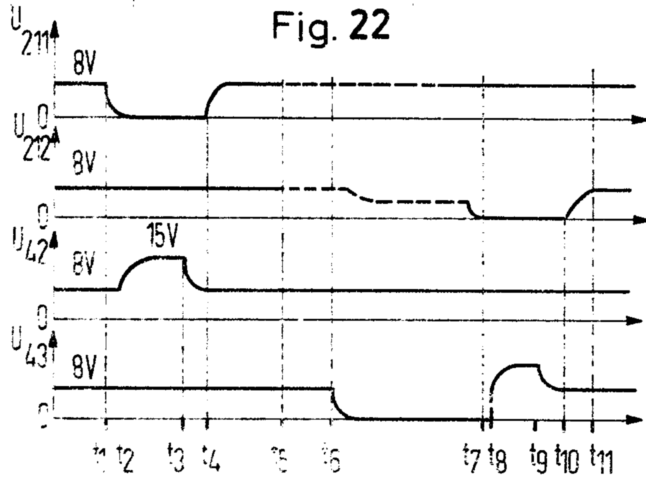


Fig. 23

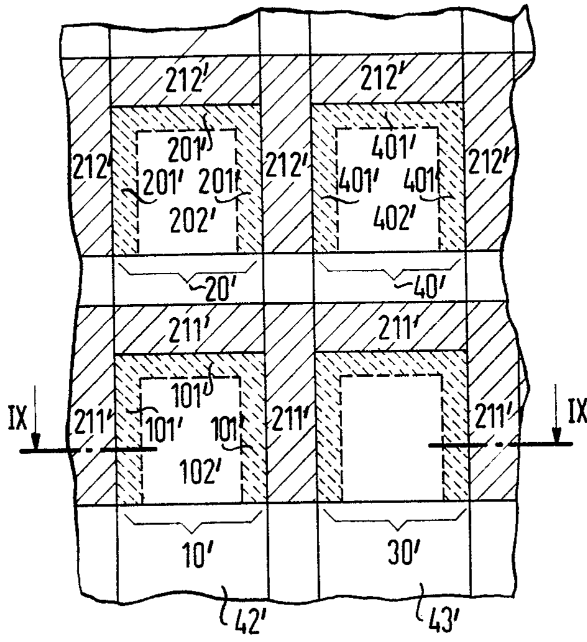


Fig. 24