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(54) Title: AN ALGORITHM FOR 64-BIT ADDRESS MODE OPTIMIZATION

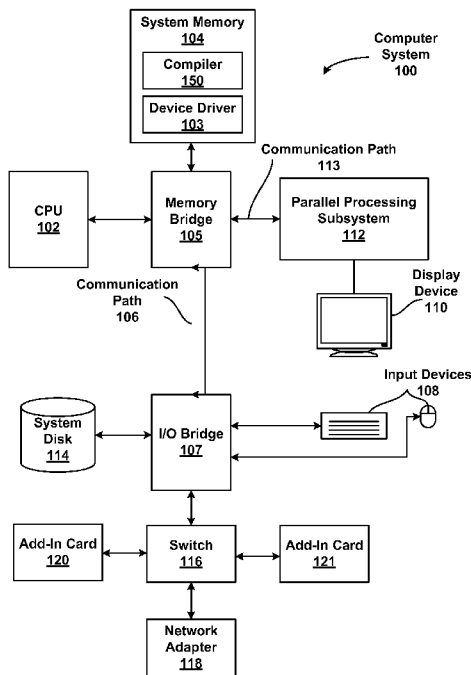


Figure 1

(57) Abstract: One embodiment of the present invention sets forth a technique for extracting a memory address offset from a 64-bit type-conversion expression included in high-level source code of a computer program. The technique involves receiving the 64-bit type-conversion expression, where the 64-bit type-conversion expression includes one or more 32-bit expressions, determining a range for each of the one or more 32-bit expressions, calculating a total range by summing the ranges of the 32-bit expressions, determining that the total range is a subset of a range for a 32-bit unsigned integer, calculating the memory address offset based on the ranges for the one or more 32-bit expressions, and generating at least one assembly-level instruction that references the memory address offset.



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A. CLASSIFICATION OF SUBJECT MATTER IPC(8) - G06F 9/45 (2012.01) USPC - 717/151 According to International Patent Classification (IPC) or to both national classification and IPC		
B. FIELDS SEARCHED Minimum documentation searched (classification system followed by classification symbols) IPC(8): G06F 9/45 (2012.01) USPC: 717/151 Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched USPC: 717/140; 717/146; 711/200 (keyword limited; terms below) Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) PatBase; Google Scholar; Google Patents; FreePatentsOnline. Search terms used: 64-bit, 32-bit, address, memory, processor microprocessor CPU GPU SPU DSP ASIC, optimize minimize, type-conversion convert, high-level, compiler assembler, expression algorithm equation, address, range offset, constant zero, extract parse, variable, minimum lower-bound,		
C. DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X - Y	US 5,613,117 A (DAVIDSON et al.) 18 March 1997 (18.03.1997) entire document, especially Abstract; col 12, ln 21-29; col 29, ln 20-46, 60 to col 30, ln 4; col 33, ln 48-53; col 34, ln 20-54; col 35, ln 56-64; col 37, ln 6-21; col 43, ln 30-48; col 58, ln 40-45; col 63, ln 40-60; col 67, ln 18-22	1-4, 7-10 ----- 5, 6
Y	US 2011/0078653 A1 (DENEAU) 31 March 2011 (31.03.2011) entire document, especially Abstract; para [0015], [0018], [0030], [0034], [0037], [0044], [0046], [0049]	5, 6
A	US 2005/0197977 A1 (BUCK et al.) 08 September 2005 (08.09.2005) entire document	1 - 10
A	US 2005/0071823 A1 (LIN et al.) 31 March 2005 (31.03.2005) entire document	1 - 10
A	US 6,757,892 B1 (GOKHALE et al.) 29 June 2004 (29.06.2004) entire document	1 - 10
A	US 2003/0028864 A1 (BOWEN) 06 February 2003 (06.02.2003) entire document	1 - 10
A	US 6,256,784 B1 (GROVE) 03 July 2001 (03.07.2001) entire document	1 - 10
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Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201		Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774