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(54) **Title:** NITRIDE-BASED SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF

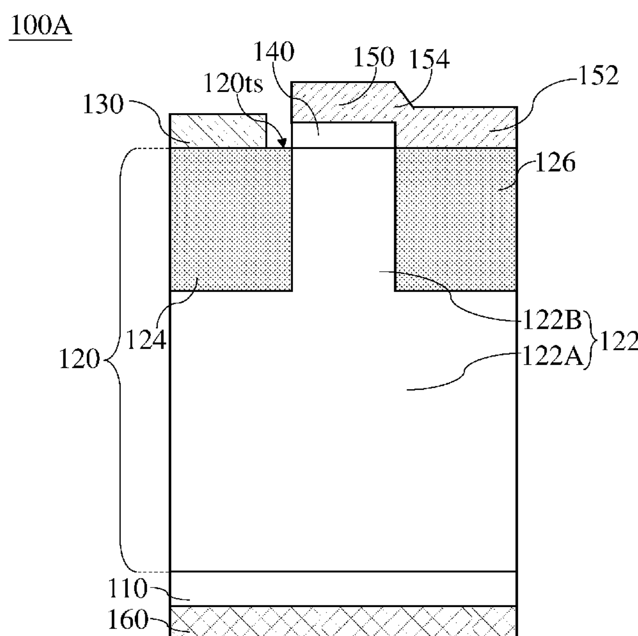

FIG. 1C

(57) **Abstract:** A nitride-based semiconductor device includes a first nitride-based semiconductor layer, a second nitride-based semiconductor layer, a gate electrode, a first source electrode, a second source electrode, and a drain electrode. The second nitride-based semiconductor layer includes a drift region doped, a first barrier region, and a second barrier region. The first and second barrier regions extend downward from a top surface of the second nitride-based semiconductor layer and are separated from each other by a portion of the drift region. The gate electrode is disposed on the first barrier region. The first source electrode is disposed on the portion of the drift region. The second source electrode is disposed on the second barrier region and is electrically coupled with the first source electrode. The drain electrode is connected to the first nitride-based semiconductor layer.

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NITRIDE-BASED SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF

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Field of the Disclosure:

[0001] The present disclosure generally relates to a nitride-based semiconductor device. More specifically, the present disclosure relates to a nitride-based semiconductor device for a vertical junction gate field-effect
10 transistor integrated with a diode.

Background of the Disclosure:

[0002] In recent years, intense research on power semiconductor devices has been prevalent for rapid development in different technical fields, such
15 as hybrid and electric vehicles, solar cells, military and aerospace. Examples of power semiconductor devices can include IGBT (insulated gates bipolar transistor), IGCT (integrated grid change transistor), MOSFET (metal oxides semiconductor field effect transistor), high-electron-mobility transistor (HEMT) and JFET (junction gate field-effect transistor).
20 [0003] In a JFET device, carriers can pass through a channel region and thus flow from a source electrode to a drain electrode. The channel width can be modulated by way of changing a voltage applied to a gate electrode, thereby allowing a predetermined current to pass therethrough. The electrical characteristics of JFETs satisfy the demands of high
25 power/frequency devices.

Summary of the Disclosure:

[0004] In accordance with one aspect of the present disclosure, a nitride-based semiconductor device is provided. A nitride-based semiconductor
30 device includes a first nitride-based semiconductor layer, a second nitride-based semiconductor layer, a gate electrode, a first source electrode, a second source electrode, and a drain electrode. The first nitride-based semiconductor layer is doped to a first conductivity type. The second nitride-based semiconductor layer is disposed over the first nitride-based
35 semiconductor layer and includes a drift region doped to a second

conductivity type, a first barrier region doped to a third conductivity type, and a second barrier region doped to the third conductivity type. The first and second barrier regions extend downward from a top surface of the second nitride-based semiconductor layer and are separated from each other by a portion of the drift region. The gate electrode is disposed on the first barrier region. The first source electrode is disposed on the portion of the drift region. The second source electrode is disposed on the second barrier region and is electrically coupled with the first source electrode. The drain electrode is connected to the first nitride-based semiconductor layer.

[0005] In accordance with another aspect of the present disclosure, a method for manufacturing a semiconductor device is provided. The method includes steps as follows. A first nitride-based semiconductor layer is formed. A second nitride-based semiconductor layer having a drift region is formed on the first nitride-based semiconductor layer. A first second barrier region and a second barrier region are formed on the drift region, such that the first and second barrier regions are separated from each other by a portion of the second nitride-based semiconductor layer. A gate electrode is formed on the first barrier region. A first source electrode is formed on the portion of the second nitride-based semiconductor layer. A second source electrode is formed on the second barrier region. The first source electrode is electrically coupled with the second source electrode. A drain electrode is formed to connect to the first nitride-based semiconductor layer.

[0006] In accordance with one aspect of the present disclosure, a nitride-based semiconductor device is provided. The nitride-based semiconductor device includes a first nitride-based semiconductor layer, a second nitride-based semiconductor layer, a gate electrode, a first source electrode, a second source electrode, and a drain electrode. The first nitride-based semiconductor layer is doped to a first conductivity type. The second nitride-based semiconductor layer is disposed over the first nitride-based semiconductor layer and includes a drift region and a first barrier region and a second barrier region. The drift region is doped to a second conductivity type. The first barrier region and the second barrier region are doped to a third conductivity type. The first and second barrier regions extend inward

from opposite sidewalls of the second nitride-based semiconductor layer to confine an inlet of the drift region. The gate electrode is disposed on the first barrier region and is electrically connected to a first electrical node. The first source electrode is disposed on the drift region and is electrically connected to a second electrical node different from the first electrical node. The second source electrode is disposed on the second barrier region and is electrically connected to the second electrical node. The drain electrode is connected to the first nitride-based semiconductor layer.

[0007] With such a configuration, a vertical junction gate field-effect transistor (JFET) and a diode can be integrated into the same semiconductor device, which means the operation of the semiconductor device can be switched between a JFET mode and a diode mode. Moreover, to comply with the different requirements for the JFET and diode modes, the barrier regions can vary features such as dopant concentrations, the widths or lengths of the various regions, or combinations thereof.

Brief Description of the Drawings:

[0008] Aspects of the present disclosure are readily understood from the following detailed description when read with the accompanying figures. It should be noted that various features may not be drawn to scale. That is, the dimensions of the various features may be arbitrarily increased or reduced for clarity of discussion. Embodiments of the present disclosure are described in more detail hereinafter with reference to the drawings, in which:

[0009] FIG. 1A is a top view of a nitride-based semiconductor device according to some embodiments of the present disclosure;

[0010] FIG. 1B is a vertical cross-sectional view across a line 1B-1B' of the semiconductor device in FIG. 1A;

[0011] FIG. 1C is a vertical cross-sectional view across a line 1C-1C' of the semiconductor device in FIG. 1A;

[0012] FIG. 1D is a circuit diagram of the semiconductor device in FIG. 1A according to some embodiments of the present disclosure;

[0013] FIG. 2A, FIG. 2B, and FIG. 2C show different stages of a method for manufacturing a semiconductor device according to some embodiments of the present disclosure;

[0014] FIG. 3A and FIG. 3B show different stages of a method for manufacturing a semiconductor device according to some embodiments of the present disclosure;

[0015] FIG. 4 is a cross-sectional view of a semiconductor device according to some embodiments of the present disclosure;

[0016] FIG. 5 is a cross-sectional view of a semiconductor device according to some embodiments of the present disclosure;

[0017] FIG. 6 is a cross-sectional view of a semiconductor device according to some embodiments of the present disclosure; and

[0018] FIG. 7 is a cross-sectional view of a semiconductor device according to some embodiments of the present disclosure.

Detailed Description:

[0019] Common reference numerals are used throughout the drawings and the detailed description to indicate the same or similar components. Embodiments of the present disclosure will be readily understood from the following detailed description taken in conjunction with the accompanying drawings.

[0020] Spatial descriptions, such as "on," "above," "below," "up," "left," "right," "down," "top," "bottom," "vertical," "horizontal," "side," "higher," "lower," "upper," "over," "under," and so forth, are specified with respect to a certain component or group of components, or a certain plane of a component or group of components, for the orientation of the component(s) as shown in the associated figure. It should be understood that the spatial descriptions used herein are for purposes of illustration only, and that practical implementations of the structures described herein can be spatially arranged in any orientation or manner, provided that the merits of embodiments of this disclosure are not deviated from by such arrangement.

[0021] Further, it is noted that the actual shapes of the various structures depicted as approximately rectangular may, in actual devices, be curved, have rounded edges, have somewhat uneven thicknesses, etc. due to device

fabrication conditions. The straight lines and right angles are used solely for convenience of representation of layers and features.

[0022] In the following description, semiconductor devices/dies/packages, methods for manufacturing the same, and the likes are set forth as preferred examples. It will be apparent to those skilled in the art that modifications, including additions and/or substitutions may be made without departing from the scope and spirit of the present disclosure. Specific details may be omitted so as not to obscure the present disclosure; however, the disclosure is written to enable one skilled in the art to practice the teachings herein without undue experimentation.

[0023] In the present disclosure, a doping region can have a conductive type expressed as a combination of a doping type and a plus/minus sign. For example, with respect to n-type dopant, there are three conductive types, including "n^{+}", "n^{-}", and "n". An n^{+} doping region has a doping concentration higher/heavier than an n-doping region; and an n-doping region has a doping concentration than higher an n^{-}-doping region. Doping regions of the same symbol may have different absolute doping concentrations. For example, two different n^{+} doping regions may have the same or different absolute doping concentrations. The definition can be applied to the p-type doping. In some embodiments, the n-type dopant can include, but are not limited to, silicon (Si), carbon (C), germanium (Ge), Selenium (Se), tellurium (Te), or the like. In some embodiments, the p-type dopant can include, but are not limited to, magnesium (Mg), beryllium (Be), zinc (Zn), or the like. In the exemplary illustrations of the present disclosure, although the element is illustrated as a single layer, it can include multiple layers therein.

[0024] FIG. 1A is a top view of a nitride-based semiconductor device 100A according to some embodiments of the present disclosure. FIG. 1B is a vertical cross-sectional view across a line 1B-1B' of the semiconductor device 100A in FIG. 1A. The semiconductor device 100A includes nitride-based semiconductor layers 110 and 120, a gate electrode 130, nitride-based semiconductor layer 140, source electrodes 150 and 152, and a drain electrode 160.

[0025] The nitride-based semiconductor layer 110 can be doped to have a first conductivity type. In some embodiments, the nitride-based semiconductor layer 110 is doped to have an n+ conductivity type. In some embodiments, the dopant concentration of the nitride-based semiconductor layer 110 is in a range from about 1×10^{19} cm^{-3} to about 1×10^{21} cm^{-3}. The exemplary materials of the nitride-based semiconductor layer 110 can include, for example but are not limited to, nitrides or group III-V compounds, such as GaN, AlN, InN, $In_xAl_yGa_{(1-x-y)}N$ where $x+y \leq 1$, $Al_yGa_{(1-y)}N$ where $y \leq 1$.

[0026] The nitride-based semiconductor 120 is disposed on/over the nitride-based semiconductor 110. The nitride-based semiconductor 120 includes a drift region 122 and barrier regions 124 and 126.

[0027] The drift region 122 is connected to the barrier regions 124 and 126. The barrier regions 124 and 126 extend downward from a top surface 120ts of the nitride-based semiconductor layer 120. The barrier regions 124 and 126 are separated by a portion of the drift region 122. To be more specific, the drift region 122 includes a base portion 122A and an extended portion 122B extending upward from the middle of the base portion 122A. The barrier regions 124 and 126 are located on and in contact with the base portion 122A and are spaced apart by the extended portion 122B. The extended portion 122B is located between the barrier regions 124 and 126 forms interfaces with the barrier regions 124 and 126.

[0028] The extended portion 122B of the drift region 122 can serve as a cut-off region that can be modulated to control the flow of carriers between the barrier regions 124 and 126. To achieve the modulation, the drift region 122 and the barrier regions 124 and 126 may have opposite doping types. For example, the drift region 122 may be doped to have a second conductivity type, and the barrier regions 124 and 126 are doped to have a third conductivity type, in which the second and third are opposite conductivity types. As such, a depletion region can arise at a p-n junction formed between the drift region 122 and the barrier regions 124 and 126. In this regard, bias (e.g., a forward or reverse bias) applied to the p-n junction will make the depletion region laterally expand across the extended portion 122B. Accordingly, at an off-state, the depletion region can cause the flow

of carriers to be disrupted in the extended portion 122B. Correspondingly, at an on-state, the drift region 122 can provide a path through which carriers flow with a vertical direction.

[0029] In some embodiments, the drift region 122 can be doped to have
5 an n^- conductivity type such that the doping concentration of the nitride-based semiconductor layer 120 is lighter than that of the nitride-based semiconductor layer 110. In some embodiments, the n-type dopant of the drift region 122 is in a range from about 1×10^{12} cm^{-3} to about 1×10^{16} cm^{-3}. In some embodiments, the barrier regions 124 and 126 can be doped to each
10 have a p conductive type. In some embodiments, the concentration of the p-type dopant of the barrier region 124 or 126 is in a range from about 1×10^{16} cm^{-3} to about 1×10^{18} cm^{-3}. In some embodiments, the barrier region 124 or 126 may have the concentrations referring to such range but being different than or the same as each other.

15 [0030] The exemplary materials of the nitride-based semiconductor layer 120 can include, for example but are not limited to, nitrides or group III-V compounds, such as GaN, AlN, InN, $In_xAl_yGa_{(1-x-y)}N$ where $x+y \leq 1$, $Al_yGa_{(1-y)}N$ where $y \leq 1$. In some embodiments, the nitride-based semiconductor layers 110 and 120 are made of the same material. For
20 example, the nitride-based semiconductor layers 110 and 120 each include GaN. That is, the drift region 122 and the barrier regions 124 and 126 each include GaN.

[0031] The gate electrode 130 is disposed on the barrier region 124. The gate electrode 130 is electrically coupled to the barrier region 124. Whether
25 the flow of carriers is disrupted in the extended portion 122B of the drift region 122 can be controlled by a bias applied to the gate electrode 130. More specially, the semiconductor device 100A can be modulated to become a normally-off vertical junction gate field-effect transistor (JFET), which depends on various conditions, including the width of extended portion 122B,
30 the dopant concentrations in the barrier region 124 or 126, or the dopant concentrations in the extended portion 122B. Accordingly, when a voltage on the gate electrode 130 is zero or below a threshold voltage, the extended portion 122B would be cut off and thus the semiconductor device 100 is at an off state. In contrast, when a voltage on the gate electrode 130 reaches a

positive threshold voltage, the extended portion 122B can be turned on (i.e., which allows the flow of carriers to pass through), and thus the semiconductor device 100 is at an on state.

[0032] The exemplary materials of the gate electrode 130 may include metals or metal compounds. The gate electrode 130 may be formed as a single layer, or plural layers of the same or different compositions. The exemplary materials of the metals or metal compounds can include, for example but are not limited to, W, Au, Pd, Ti, Ta, Co, Ni, Pt, Mo, TiN, TaN, metal alloys or compounds thereof, or other metallic compounds.

[0033] The nitride-based semiconductor layer 140 is disposed on the extending portion 122B of the drift region 122. The nitride-based semiconductor layer 140 is in contact with the extending portion 122B. The nitride-based semiconductor layer 140 is located between the barrier regions 124 and 126. The nitride-based semiconductor layer 140 can be doped to have a conductivity type identical with the nitride-based semiconductor layer 110. For example, the nitride-based semiconductor layer 140 is doped to have an n+ conductivity type. In some embodiments, the dopant concentration of the nitride-based semiconductor layer 110 ranges from about 1×10^{19} cm^{-3} to about 1×10^{21} cm^{-3}. The nitride-based semiconductor layer 140 can act as a highly doped contact region on the cut-off region, so as to lower the contact resistance between the cut-off region and a layer/an electrode to be formed thereon. The exemplary materials of the nitride-based semiconductor layer 140 can include, for example but are not limited to, nitrides or group III-V compounds, such as GaN, AlN, InN, $In_xAl_yGa_{(1-x-y)}N$ where $x+y \leq 1$, $Al_yGa_{(1-y)}N$ where $y \leq 1$. In some embodiments, the nitride-based semiconductor layers 110, 120, and 140 each include GaN.

[0034] The source electrode 150 is disposed on the nitride-based semiconductor layer 140. The source electrode 150 is in contact with the nitride-based semiconductor layer 140. The source electrode 150 can have a width equal to or less than that of the nitride-based semiconductor layer 140. The nitride-based semiconductor layer 140 is located between the extending portion 122B of the drift region 122 and the source electrode 150 such that the source electrode 150 can be electrically coupled to the extending portion 122B via the nitride-based semiconductor layer 140. The

source electrode 150 is located between the barrier regions 124 and 126. More specifically, the source electrode 150 can be arranged to be free from vertically overlapping with the barrier regions 124 and 126, which avoids any physical contact between the source electrode 150 and the barrier regions 124 and 126. Similarly, the source electrode 150 can be physically separated from the gate electrode 130 to avoid physical contact therebetween.

[0035] The source electrode 152 is disposed on the barrier region 126. The source electrode 152 is in contact with the barrier region 126. The source electrode 152 is electrically coupled to the barrier region 126. The source electrode 152 can be physically separated from the gate electrode 130 to avoid physical contact therebetween. A bias (e.g., a forward or reverse bias) applied to source electrode 152 will affect the depletion region to laterally expand across the extended portion 122B.

[0036] The drain electrode 160 is disposed on the nitride-based semiconductor layer 110. The drain electrode 160 is connected to the nitride-based semiconductor layer 110. The drain electrode 160 can make contact with the nitride-based semiconductor layer 110. The nitride-based semiconductor layers 110 and 120 are between the gate electrode 130 and the drain electrode 160. The nitride-based semiconductor layers 110 and 120 are between the source electrode 150 and the drain electrode 160. The nitride-based semiconductor layers 110 and 120 are between the source electrode 152 and the drain electrode 160.

[0037] FIG. 1C is a vertical cross-sectional view across a line 1C-1C' of the semiconductor device 100A in FIG. 1A. As shown in FIG. 1A and FIG. 1C, the source electrodes 150 and 152 are connected to each other, such that the source electrode 150 is electrically coupled with source electrode 152. In the exemplary illustration of FIG. 1C, the semiconductor device 100A further includes a conductive bridge 154. The conductive bridge 154 can connect the source electrode 150 to the source electrode 152. The conductive bridge 154 can extend upward from the source electrode 152 to the source electrode 154 because the source electrode 152 is in a position higher than the source electrode 150.

[0038] As afore-described, once a voltage applied to the gate electrode 130 reaches a positive threshold voltage, the extended portion 122B of the drift region 122 can be turned on, such that the flow of carriers is allowed to pass therethrough. In the exemplary illustration of FIG. 1B, the carriers can flow from the source electrode 150 to the drain electrode 160 (or from the drain electrode 160to the source electrode 150). Furthermore, the p-n junction formed between the base portion 122A and the barrier region 124 can provide a diode (e.g., an integrated body diode), which may be effective between the source electrode 152 and the drain electrode 160. In this regard, the source electrode 152 in contact with the p-type doping can serve as a p-side terminal of the diode, and the drain electrode 160 in contact with the n+-type doping can serve as an n-side terminal of the diode.

[0039] The source electrodes 150, 152 and the drain electrode 160 can include, for example but are not limited to, metals, alloys, doped semiconductor materials (such as doped crystalline silicon), compounds such as silicides and nitrides, other conductor materials, or combinations thereof. The exemplary materials of the source electrodes 150, 152 and the drain electrode 160 can include, for example but are not limited to, Ti, AlSi, TiN, or combinations thereof. Each of the source electrodes 150, 152 and the drain electrode 160 may be a single layer, or plural layers of the same or different composition. In some embodiments, the source electrodes 150, 152 form ohmic contacts with the nitride-based semiconductor layer 120, and the drain electrode 160 form ohmic contact with the nitride-based semiconductor layer 110. The ohmic contact can be achieved by applying Ti, Al, or other suitable materials. The conductive bridge 154 can have material identical with or similar with those of the source electrodes 150, 152 and the drain electrode 160.

[0040] In some embodiments, the source electrodes 150 and 152 can be formed from the same material. In some embodiments, the source electrodes 150 and 152 can be formed to have the same thickness. Such a configuration is advantageous to the formation of the source electrodes 150 and 152. For example, the source electrodes 150 and 152 can be formed from a single blanket conductive layer. In some embodiments, the source

electrodes 150 and 152 and the conductive bridge 154 can be formed from a single blanket conductive layer so that they have the same composition. In addition, the gate electrode 130 and the source electrode 152 can be arranged to be asymmetrical about the source electrode 150. For example, 5 the thicknesses of the gate electrode 130 and the source electrode 152 are asymmetrical about the source electrode 150. A distance from the gate electrode 130 to the source electrode 150 and a distance from the source electrode 152 to the source electrode 150 is asymmetrical about the source electrode 150. The asymmetry is advantageous to the operation of the 10 semiconductor device 100A, which will be described below.

[0041] With such a configuration, a vertical JFET and a diode can be integrated into the semiconductor device 100A. FIG. 1D is a circuit diagram of the semiconductor device 100A in FIG. 1A according to some embodiments of the present disclosure. As shown in FIG. 1B and 1D, in 15 the circuit, the gate electrode 130 is labeled as “gate G” and electrically connected to an electrical node N1; the source electrodes 150 and 152 are together labeled as “source S” and electrically connected to an electrical node N2 because they are electrically coupled with each other; and the drain electrode 160 is labeled as “drain D” and electrically connected to an 20 electrical node N3. The electrical nodes can be electrically connected to different electrical potential sources, which can feed one or more voltages to the respective electrodes.

[0042] The operation of the semiconductor device 100A can be switched between two modes, a JEFT mode and a diode mode. In the JEFT mode, 25 the gate G is biased by a voltage higher than the threshold, and the source S and the drain D have different electrical potentials such that carriers can flow between the source S and the drain D. In the diode mode, a voltage applied to the gate G is zero or less than the threshold, and the source S has an electrical potential higher than that of the drain D, such that at least one 30 current can flow from the source S to the drain D.

[0043] Referring to FIG. 1B again, the barrier regions 124 and 126 are related to the JFET mode and the diode mode, respectively, and thus the barrier regions 124 and 126 can have different features, which will be advantageous to the operation for the two modes. In some embodiments,

the barrier regions 124 and 126 are doped to p-type with different p-doping concentrations. For example, the barrier region 124 can have the p-doping concentration less than the p-doping concentration of the barrier region 126. The reason for such relationship is to adapt to the JFET mode and the diode
5 mode.

[0044] Different stages of a method for manufacturing the semiconductor device 100A are shown in FIG. 2A, FIG. 2B, and FIG. 2C, as described below. In the following, deposition techniques can include, for example but are not limited to, atomic layer deposition (ALD), physical vapor deposition
10 (PVD), chemical vapor deposition (CVD), metal organic CVD (MOCVD), plasma enhanced CVD (PECVD), low-pressure CVD (LPCVD), plasma-assisted vapor deposition, epitaxial growth, or other suitable processes.

[0045] Referring to FIG. 2A, a substrate 102 is provided. The nitride-based semiconductor layers 110 and 120 can be formed over the substrate
15 102 in sequence by using deposition techniques, in which the nitride-based semiconductor layer 120 has a drift region 122 on the nitride-based semiconductor layer. Then, a mask layer 170 can be on the nitride-based semiconductor layer 120 and at least one portion of the nitride-based semiconductor layer 120 is exposed. Barrier regions 124 and 126 are
20 formed by implanting dopants into a top surface of the nitride-based semiconductor layer 120 using the mask layer 170, which can be called masked implantation techniques. The barrier regions 124 and 126 are formed on the drift region 122 and are separated from each other by a portion of the drift region 122. In some embodiments, after the ion implantation, an
25 annealing step can be performed to activate the dopant atoms.

[0046] Referring to FIG. 2B, the mask layer 170 is removed. A blanket nitride-based semiconductor layer 172 is formed on the nitride-based semiconductor layer 120 to cover the drift region 122 and the barrier regions 124 and 126. A mask layer 174 can be on the blanket nitride-based
30 semiconductor layer 172 and at least one portion of the blanket nitride-based semiconductor layer 172 is exposed. Then, a patterning process can be performed for removing excess portions of the blanket nitride-based

semiconductor layer 172. In some embodiments, the patterning process can include an etching process.

[0047] Referring to FIG. 2C, after the patterning process, a nitride-based semiconductor layer 140 is formed, in which the barrier regions 124 and 126 are exposed. A gate electrode 130 and source electrodes 150 and 152 are formed. The gate electrode 130 is formed on the barrier region 124. The source electrode 150 is formed on the drift region 122 and on the nitride-based semiconductor layer 140. The source electrode 150 is formed on the barrier region 126. With respect to the formation of the source electrodes 150 and 152, it can be achieved by forming a blanket conductive layer on the nitride-based semiconductor layer. Then, the blanket conductive layer is patterned to form the source electrodes 150 and 152 and a conductive bridge 154 connecting the source electrodes 150 and 152. Thereafter, the substrate 102 can be removed and a drain electrode can be formed to connect to the nitride-based semiconductor layer 110, thereby obtain the structure as shown in FIG. 1B and FIG. 1C.

[0048] The formation of the barrier regions 124 and 126 can be achieved by another way. Different stages of a method for forming the barrier regions 124 and 126 are shown in FIG. 3A and FIG. 3B.

[0049] Referring to FIG. 3A, a substrate 102 is provided. The nitride-based semiconductor layers 110 and 120 can be formed over the substrate 102 in sequence by using deposition techniques, in which the nitride-based semiconductor layer 120 has a drift region 122 on the nitride-based semiconductor layer 110. Then, a mask layer 180 can be formed on the nitride-based semiconductor layer 120 such that at least one portion of the nitride-based semiconductor layer 120 is exposed. Then, the exposed portion of the nitride-based semiconductor layer 120 is removed such that the nitride-based semiconductor layer 120 is recessed.

[0050] Referring to FIG. 3B, epitaxial layers can be formed from a p-type material to form barrier regions 124 and 126. The barrier regions 124 and 126 can extend inward from opposite sidewalls of the nitride-based semiconductor layer 120 to confine an inlet of the drift region 122. In some embodiments, the barrier regions 124 and 126 can be formed as being

coplanar with the drift region 122 of the nitride-based semiconductor layer 120. After the formation of the barrier regions 124 and 126, the subsequent processes can be identical with or similar with FIG. 2B and FIG. 2C.

[0051] FIG. 4 is a cross-sectional view of a semiconductor device 100B according to some embodiments of the present disclosure. In the exemplary illustration of FIG. 4, the semiconductor device 100B further includes a dielectric layer 170, contact 172, 174, and 176, and a patterned conductive layer 180.

[0052] The dielectric layer 170 is disposed on the nitride-based semiconductor layer 120 and covers the gate electrode 130 and the source electrodes 150 and 152. The contact 172, 174, and 176 are located within the dielectric layer 170. The contact 172 is connected to the gate electrode 130. The contact 174 is connected to the source electrode 150. The contact 176 is connected to the source electrode 152. The contact 172, 174, and 176 may have different lengths. The patterned conductive layer 180 is disposed on the dielectric layer 170 and has portions 182 and 184 spaced apart from each other. The portion 182 of the patterned conductive layer 180 covers the contact 172 to electrically couple with the gate electrode 130. The portion 184 of the patterned conductive layer 180 covers the contacts 174 and 176 to electrically couple with the source electrodes 174 and 176.

[0053] By such a configuration, the gate electrode 130 can be further connected to an external electrical potential source different from another external electrical potential source electrically coupled to the source electrodes 174 and 176. The dielectric layer 170, the contact 172, 174, and 176, and the patterned conductive layer 180 can be formed after the stage of FIG. 2C.

[0054] FIG. 5 is a cross-sectional view of a semiconductor device 100C according to some embodiments of the present disclosure. In the exemplary illustration of FIG. 5, the semiconductor device 100C further includes a substrate 102.

[0055] The substrate 102 may be a semiconductor substrate. The exemplary materials of the substrate 102 can include, for example but are not limited to, Si, SiGe, SiC, gallium arsenide, p-doped Si, n-doped Si, sapphire, semiconductor on insulator, such as silicon on insulator (SOI), or other

suitable substrate materials. In some embodiments, the substrate 102 can include, for example, but is not limited to, group III elements, group IV elements, group V elements, or combinations thereof (e.g., III-V compounds). In other embodiments, the substrate 102 can include, for
5 example but is not limited to, one or more other features, such as a doped region, a buried layer, an epitaxial (epi) layer, or combinations thereof.

[0056] The nitride-based semiconductor layer 110 is located between the substrate 102 and the nitride-based semiconductor layer 120. The nitride-based semiconductor layer 110 has a width greater than the nitride-based
10 semiconductor layer 120 so that the nitride-based semiconductor layer 110 has a top surface expanding/extending outside the nitride-based semiconductor layer 120. That is, the top surface of the nitride-based semiconductor layer 110 can be free from coverage of the nitride-based semiconductor layer 120. The drain electrodes 160 are disposed on the top
15 surface of the nitride-based semiconductor layer 110. Although the configuration with respect to the drain electrodes 160 vary, the semiconductor device 100C can still be operated to switch between the JFET and the diode modes.

[0057] FIG. 6 is a cross-sectional view of a semiconductor device 100D
20 according to some embodiments of the present disclosure. In the exemplary illustration of FIG. 6, the barrier regions 124 and 126 are doped to p-type with different dimensions. That is, the barrier regions 124 and 126 can have different downward-extending lengths for the top surface of the nitride-based semiconductor layer 120. For example, to comply with the requirement for
25 the JFET and diode modes, the barrier region 124 can have a downward-extending length greater than the downward-extending length of the barrier region 126.

[0058] FIG. 7 is a cross-sectional view of a semiconductor device 100E according to some embodiments of the present disclosure. In the exemplary
30 illustration of FIG. 7, the barrier regions 124 and 126 are doped to p-type with different dimensions. That is, the barrier regions 124 and 126 are doped to p-type with different widths. For example, to comply with the requirement for the JFET and diode modes, the barrier region 124 has a width less than the width of the barrier region 126.

[0059] It should be noted that the above semiconductor devices can be manufactured by the afore-mentioned different processes in order to meet different electrical requirements. Furthermore, to comply with the requirement for the JFET and diode modes, it is available to combine the different embodiments describe above. For example, the two barrier regions can have different widths and downward-extending lengths.

[0060] The embodiments were chosen and described in order to best explain the principles of the disclosure and its practical application, thereby enabling others skilled in the art to understand the disclosure for various embodiments and with various modifications that are suited to the particular use contemplated.

[0061] As used herein and not otherwise defined, the terms "substantially," "substantial," "approximately" and "about" are used to describe and account for small variations. When used in conjunction with an event or circumstance, the terms can encompass instances in which the event or circumstance occurs precisely as well as instances in which the event or circumstance occurs to a close approximation. For example, when used in conjunction with a numerical value, the terms can encompass a range of variation of less than or equal to ±10% of that numerical value, such as less than or equal to ±5%, less than or equal to ±4%, less than or equal to ±3%, less than or equal to ±2%, less than or equal to ±1%, less than or equal to ±0.5%, less than or equal to ±0.1%, or less than or equal to ±0.05%. The term "substantially coplanar" can refer to two surfaces within micrometers of lying along a same plane, such as within 40 μm, within 30 μm, within 20 μm, within 10 μm, or within 1 μm of lying along the same plane.

[0062] As used herein, the singular terms "a," "an," and "the" may include plural referents unless the context clearly dictates otherwise. In the description of some embodiments, a component provided "on" or "over" another component can encompass cases where the former component is directly on (e.g., in physical contact with) the latter component, as well as cases where one or more intervening components are located between the former component and the latter component.

[0063] While the present disclosure has been described and illustrated with reference to specific embodiments thereof, these descriptions and

illustrations are not limiting. It should be understood by those skilled in the art that various changes may be made and equivalents may be substituted without departing from the true spirit and scope of the present disclosure as defined by the appended claims. The illustrations may not necessarily be drawn to scale. There may be distinctions between the artistic renditions in the present disclosure and the actual apparatus due to manufacturing processes and tolerances. Further, it is understood that actual devices and layers may deviate from the rectangular layer depictions of the FIGS. and may include angles surfaces or edges, rounded corners, etc. due to manufacturing processes such as conformal deposition, etching, etc. There may be other embodiments of the present disclosure which are not specifically illustrated. The specification and the drawings are to be regarded as illustrative rather than restrictive. Modifications may be made to adapt a particular situation, material, composition of matter, method, or process to the objective, spirit and scope of the present disclosure. All such modifications are intended to be within the scope of the claims appended hereto. While the methods disclosed herein have been described with reference to particular operations performed in a particular order, it will be understood that these operations may be combined, sub-divided, or re-ordered to form an equivalent method without departing from the teachings of the present disclosure. Accordingly, unless specifically indicated herein, the order and grouping of the operations are not limitations.

Claims

1. A nitride-based semiconductor device, comprising:

a first nitride-based semiconductor layer doped to a first conductivity type;

5 a second nitride-based semiconductor layer disposed over the first nitride-based semiconductor layer and comprising a drift region doped to a second conductivity type, a first barrier region doped to a third conductivity type, and a second barrier region doped to the third conductivity type, wherein the first and second barrier regions extend 10 downward from a top surface of the second nitride-based semiconductor layer and are separated from each other by a portion of the drift region;

a gate electrode disposed on the first barrier region;

a first source electrode disposed on the portion of the drift region;

a second source electrode disposed on the second barrier region and 15 electrically coupled with the first source electrode; and

a drain electrode connected to the first nitride-based semiconductor layer.

2. The semiconductor device of any preceding claim, wherein the first 20 and second barrier regions are doped to p-type with different p-doping concentrations.

3. The semiconductor device of any preceding claim, wherein the first barrier region has the p-doping concentration less than the p-doping 25 concentration of the second barrier region.

4. The semiconductor device of any preceding claim, wherein the first and second barrier regions are doped to p-type with different downward-extending lengths.

5 5. The semiconductor device of any preceding claim, wherein the first barrier region has the downward-extending length greater than the downward-extending length of the second barrier region.

6. The semiconductor device of any preceding claim, wherein the first
10 and second barrier regions are doped to p-type with different widths.

7. The semiconductor device of any preceding claim, wherein the first barrier region has the width less than the width of the second barrier region.

15 8. The semiconductor device of any preceding claim, wherein the gate electrode and the second source electrode are asymmetrical about the first source electrode.

9. The semiconductor device of any preceding claim, further
20 comprising:

a conductive bridge connecting the first source electrode to the second source electrode, wherein the first and second source electrodes and the conductive bridge are the same material.

10. The semiconductor device of any preceding claim, further comprising:

a first contact connected to the first source electrode;

a second contact connected to the second source electrode; and

5 a patterned conductive layer electrically connected the first contact to the second contact.

11. The semiconductor device of any preceding claim, wherein the first nitride-based semiconductor layer is doped to n^+ type, and the drift region is

10 doped to n^- type.

12. The semiconductor device of any preceding claim, wherein the first source electrode is free from vertically overlapping with the first and second barrier regions.

15

13. The semiconductor device of any preceding claim, wherein the gate electrode is physically separated from the first and second source electrodes.

14. The semiconductor device of any preceding claim, wherein the first

20 and second source electrodes have the same thickness.

15. The semiconductor device of any preceding claim, further comprising a third nitride-based semiconductor layer located between the second nitride-based semiconductor layer and the first source electrode and

25 doped to the first conductivity type.

16. A method for manufacturing a semiconductor device, comprising:

forming a first nitride-based semiconductor layer;

forming a second nitride-based semiconductor layer having a drift
5 region on the first nitride-based semiconductor layer;

forming a first second barrier region and a second barrier region on the drift region, such that the first and second barrier regions are separated from each other by a portion of the second nitride-based semiconductor layer;

forming a gate electrode on the first barrier region;

10 forming a first source electrode on the portion of the second nitride-based semiconductor layer;

forming a second source electrode on the second barrier region;

electrically coupling the first source electrode with the second source electrode; and

15 forming a drain electrode connected to the first nitride-based semiconductor layer.

17. The method of any preceding claim, wherein the first and second barrier regions are formed with different p-doping concentrations.

20

18. The method of any preceding claim, wherein the first and second barrier regions are formed with different dimensions.

19. The method of any preceding claim, wherein the electrically coupling the first source electrode with the second source electrode comprises:

forming a blanket conductive layer on the second nitride-based
5 semiconductor layer; and

patterning the blanket conductive layer to form the first source electrode, the second source electrode, and a conductive bridge connecting the first source electrode to the second source electrode.

10 20. The method of any preceding claim, wherein the electrically coupling the first source electrode with the second source electrode comprises:

forming a first contact connected to the first source electrode;

forming a second contact connected to the second source electrode; and

15 forming a patterned conductive layer electrically connected the first contact to the second contact.

21. A nitride-based semiconductor device, comprising:

a first nitride-based semiconductor layer doped to a first conductivity
20 type;

a second nitride-based semiconductor layer disposed over the first nitride-based semiconductor layer and comprising:

a drift region doped to a second conductivity type; and

a first barrier region and a second barrier region doped to a third
25 conductivity type, wherein the first and second barrier regions extend

inward from opposite sidewalls of the second nitride-based semiconductor layer to confine an inlet of the drift region;

a gate electrode disposed on the first barrier region and electrically connected to a first electrical node;

5 a first source electrode disposed on the drift region and electrically connected to a second electrical node different from the first electrical node;

a second source electrode disposed on the second barrier region and electrically connected to the second electrical node; and

a drain electrode connected to the first nitride-based semiconductor layer.

10

22. The semiconductor device of any preceding claim, wherein the first and second barrier regions are doped to p-type with different p-doping concentrations.

15 23. The semiconductor device of any preceding claim, wherein the first and second barrier regions are doped to p-type with different dimensions.

24. The semiconductor device of any preceding claim, further comprising:

20 a conductive bridge connecting the first source electrode to the second source electrode, wherein the first and second source electrodes and the conductive bridge have the same material.

25. The semiconductor device of any preceding claim, further

25 comprising:

a first contact connected to the first source electrode;

a second contact connected to the second source electrode; and

a patterned conductive layer electrically connected the first contact to the second contact.

5

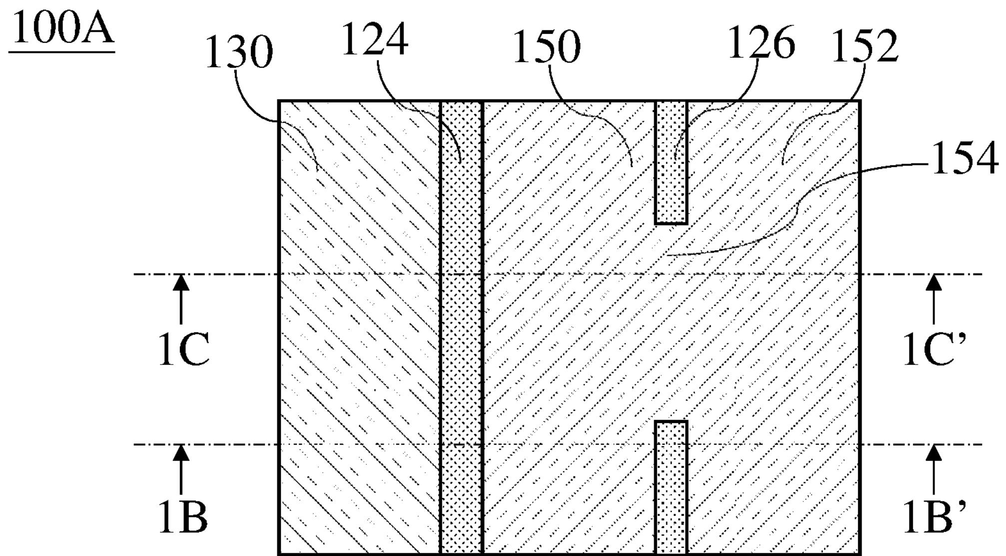

FIG. 1A

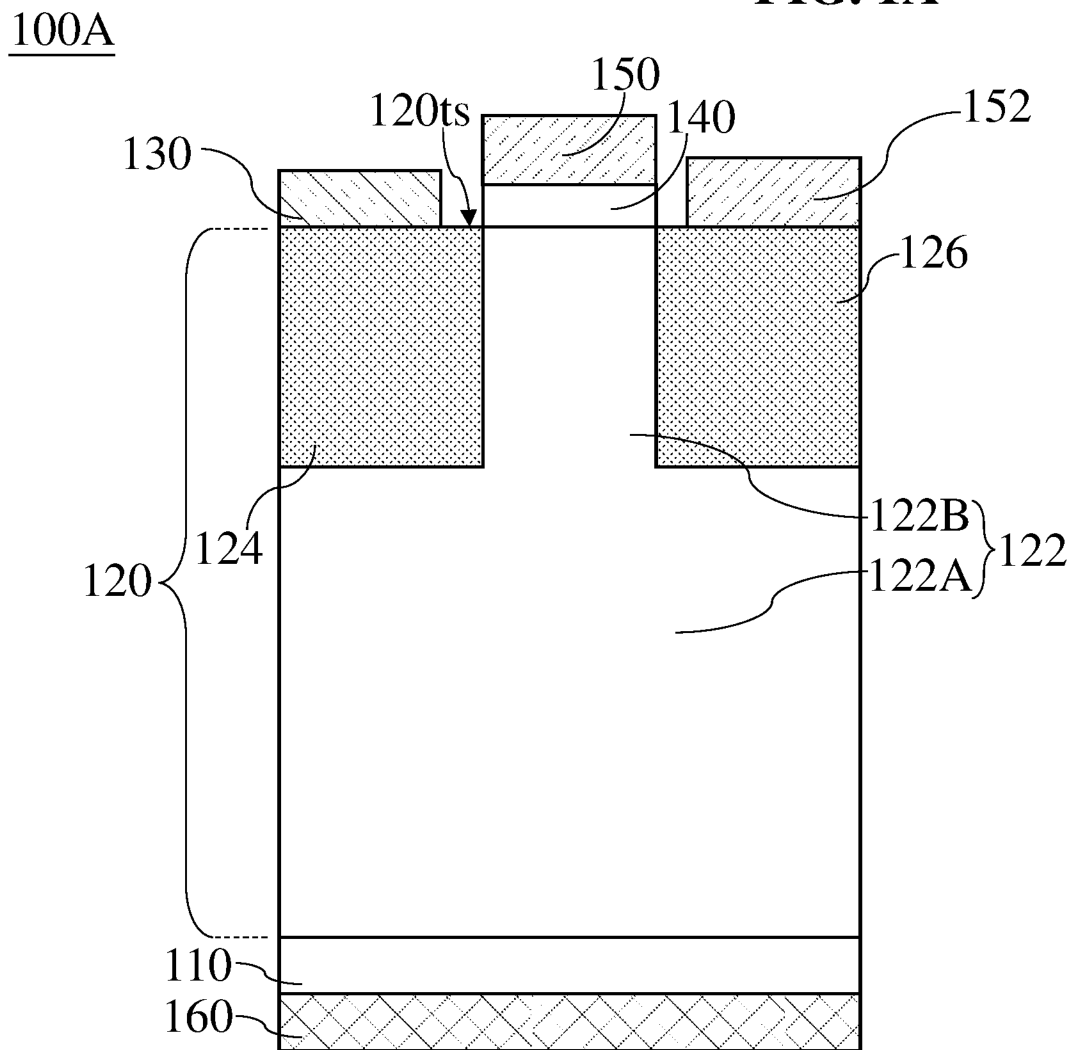

FIG. 1B

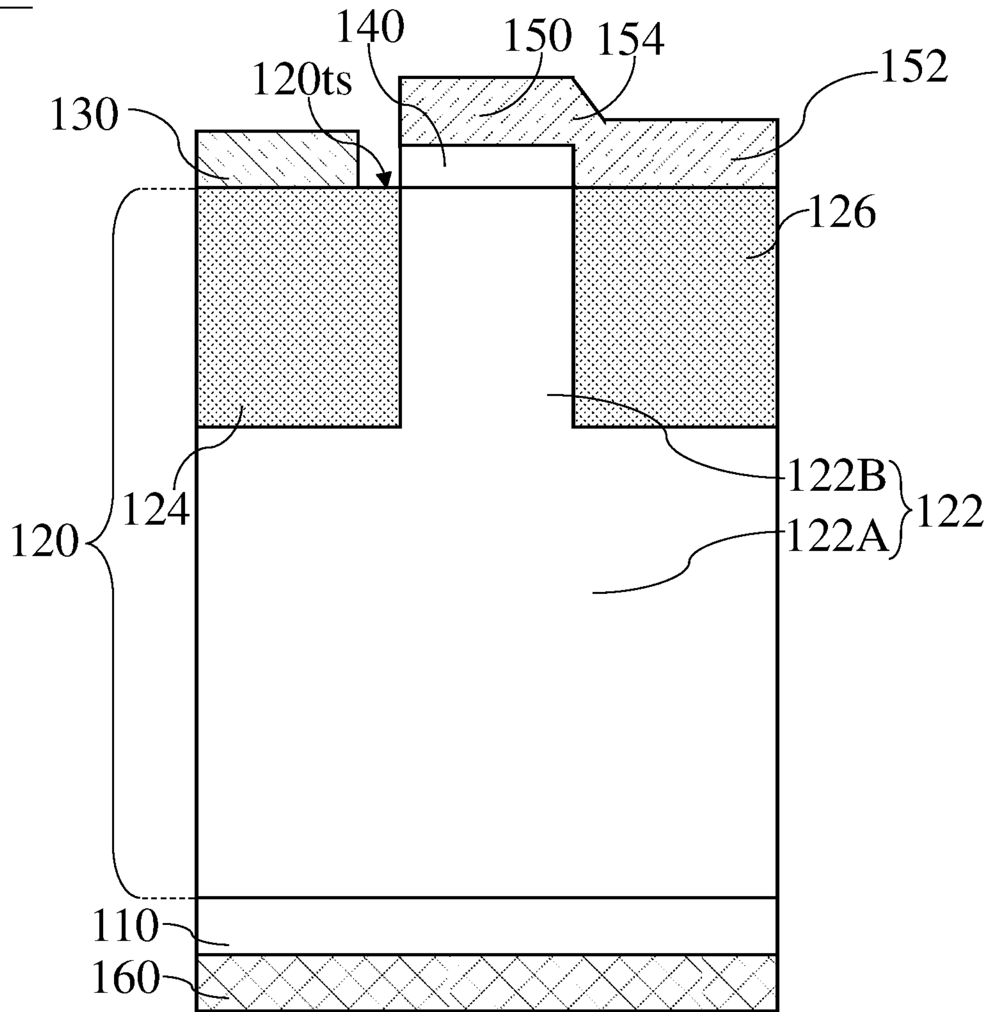

FIG. 1C

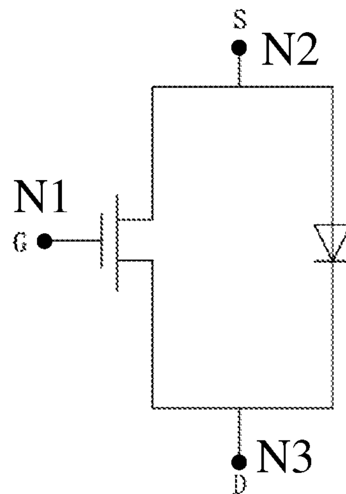

FIG. 1D

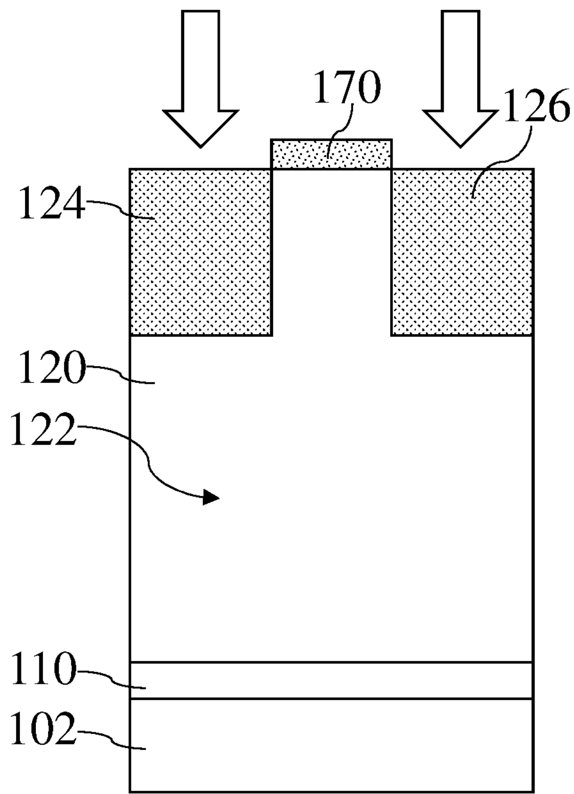

FIG. 2A

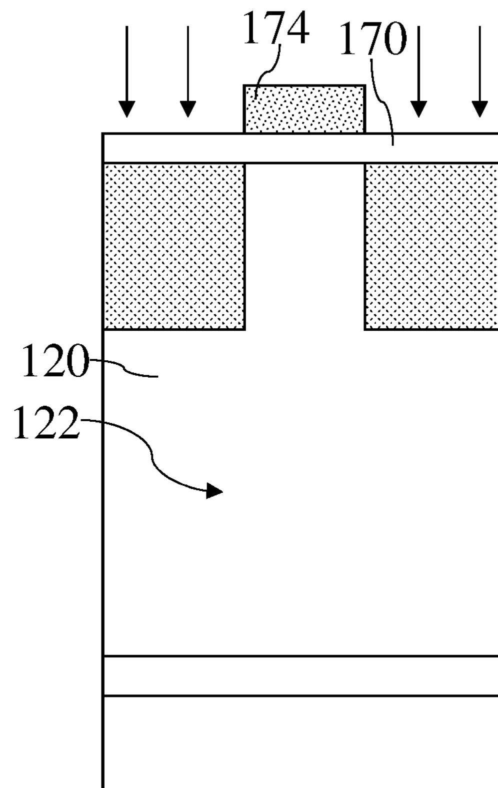

FIG. 2B

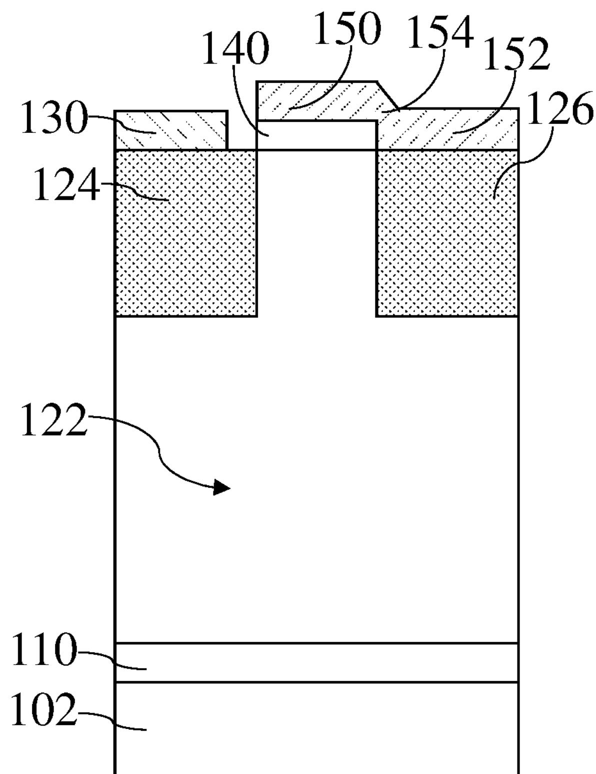

FIG. 2C

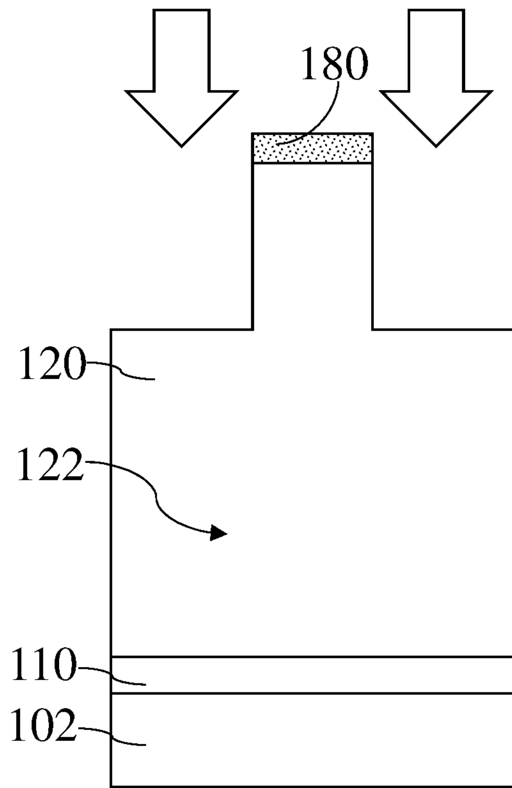

FIG. 3A

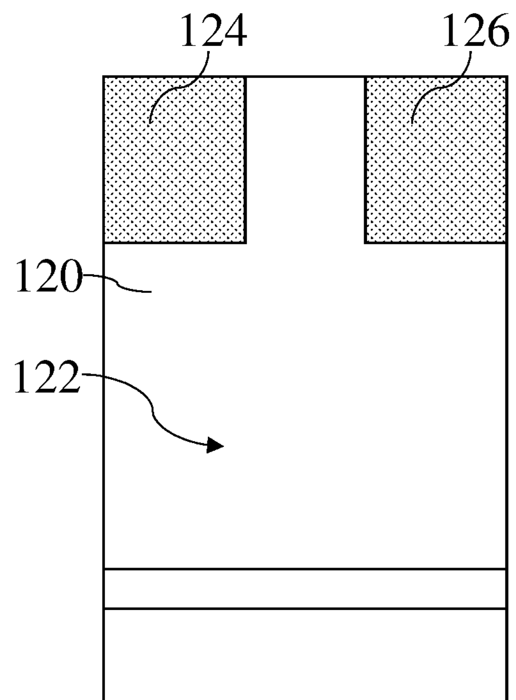

FIG. 3B

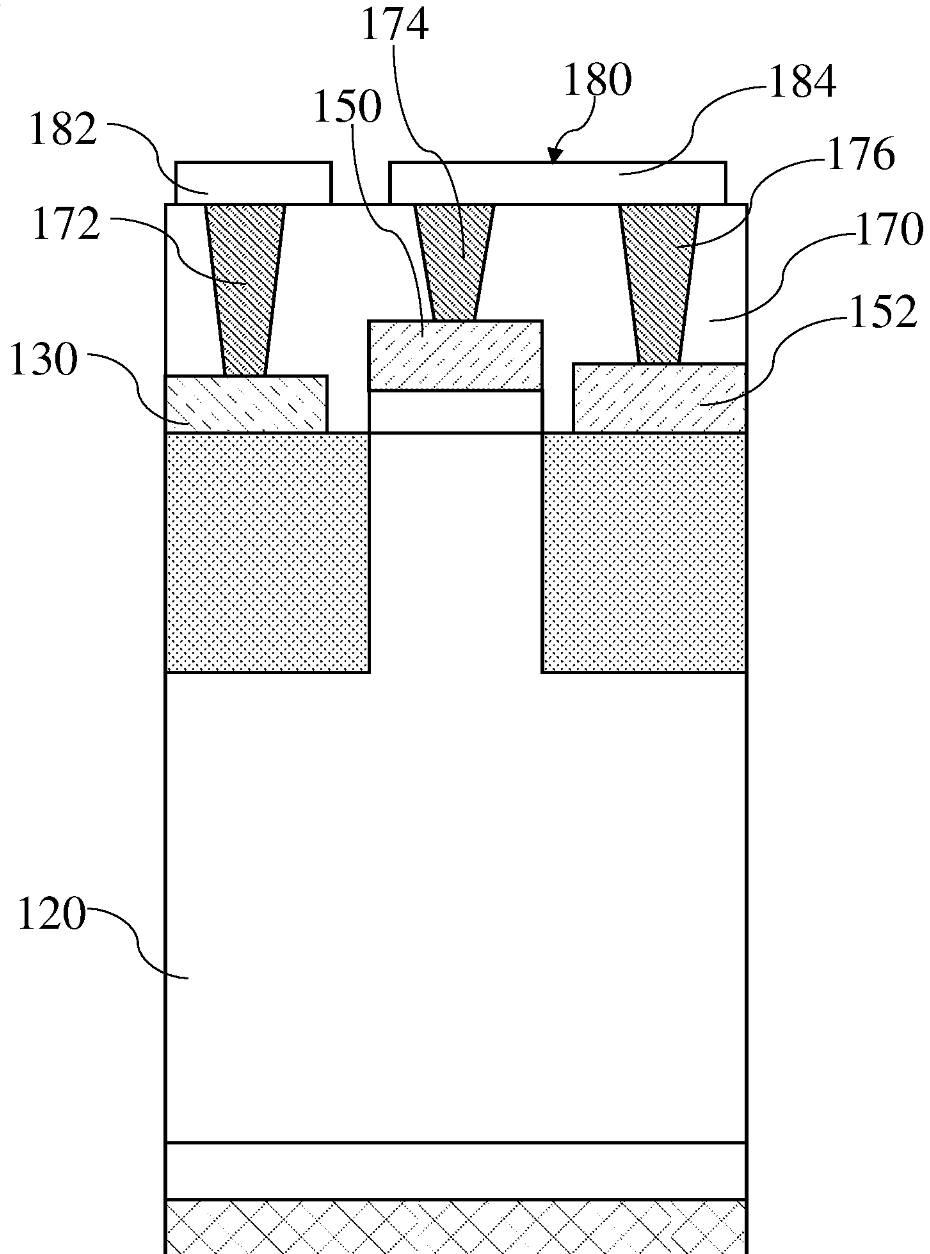

FIG. 4

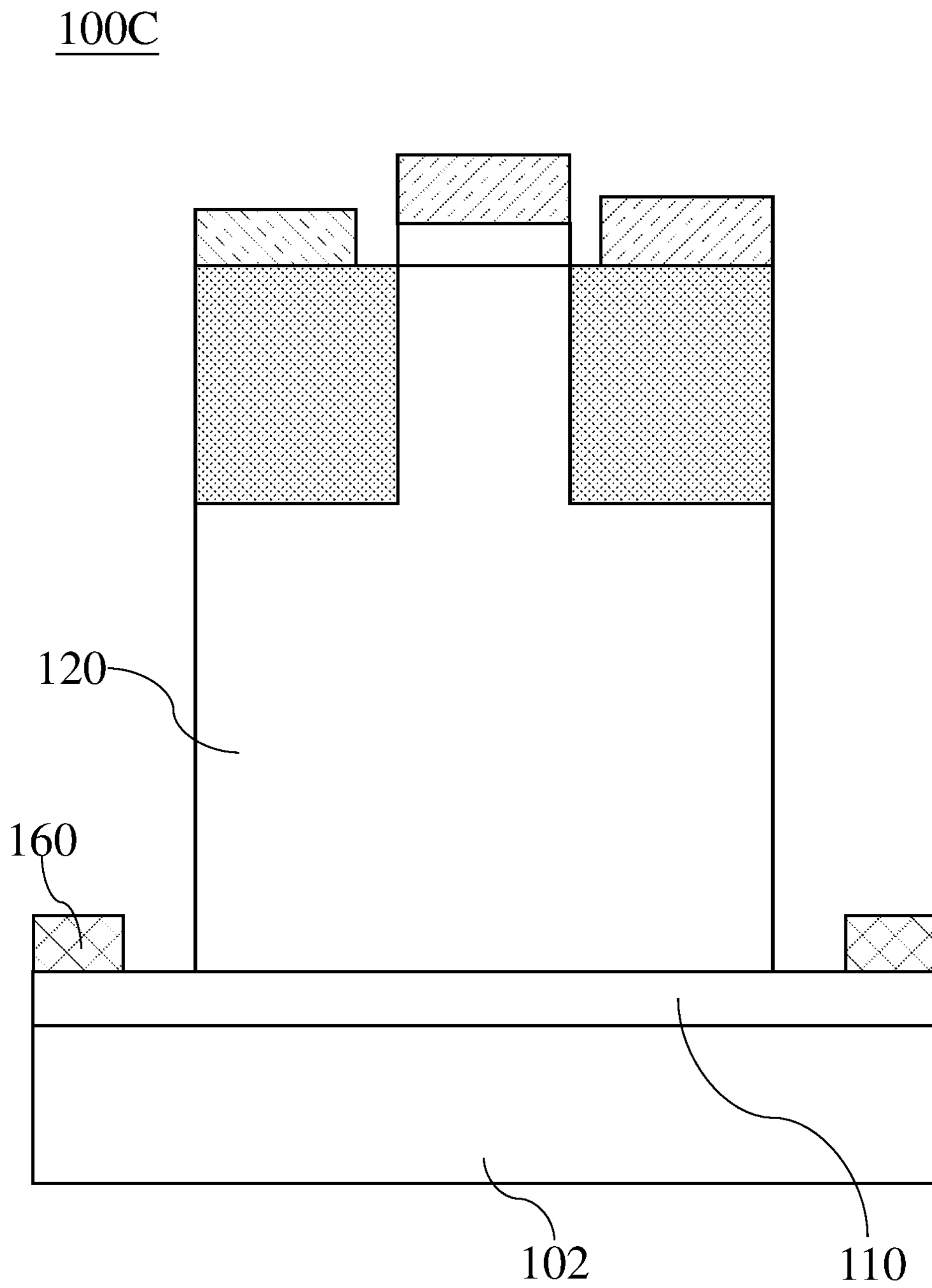

FIG. 5

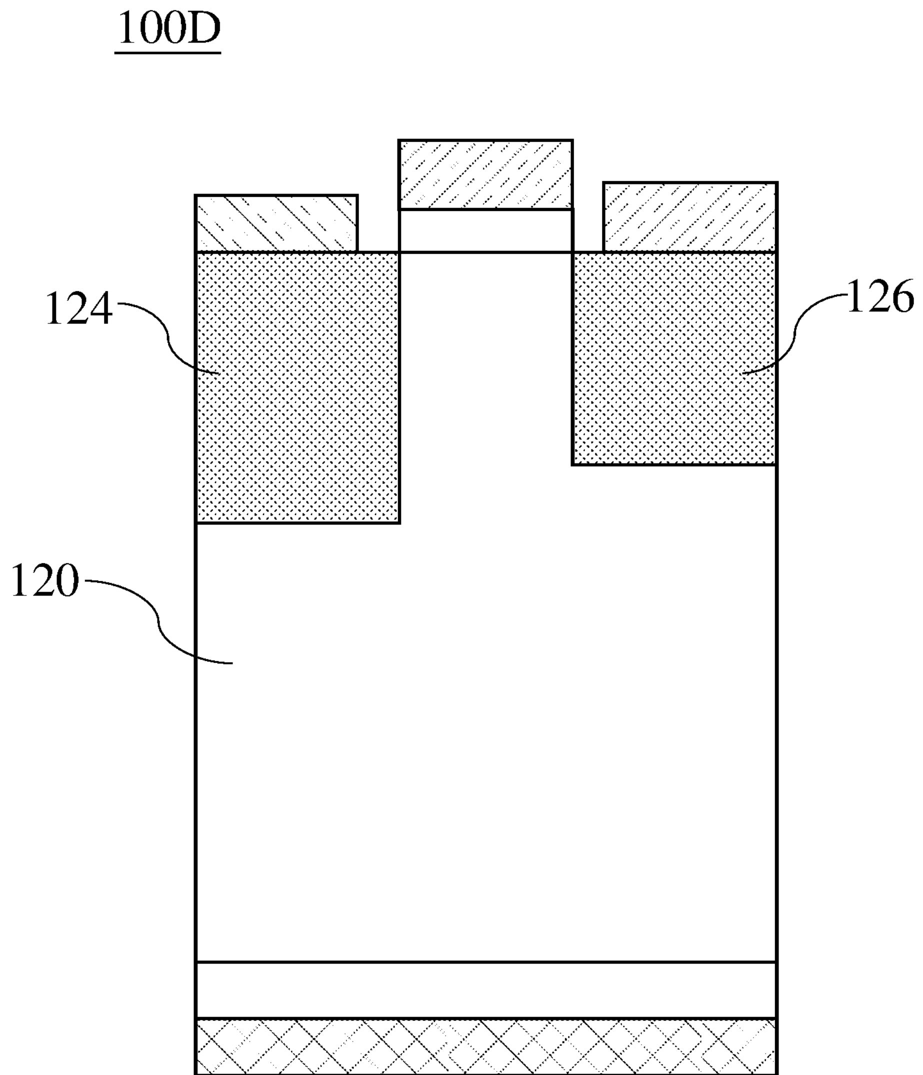

FIG. 6

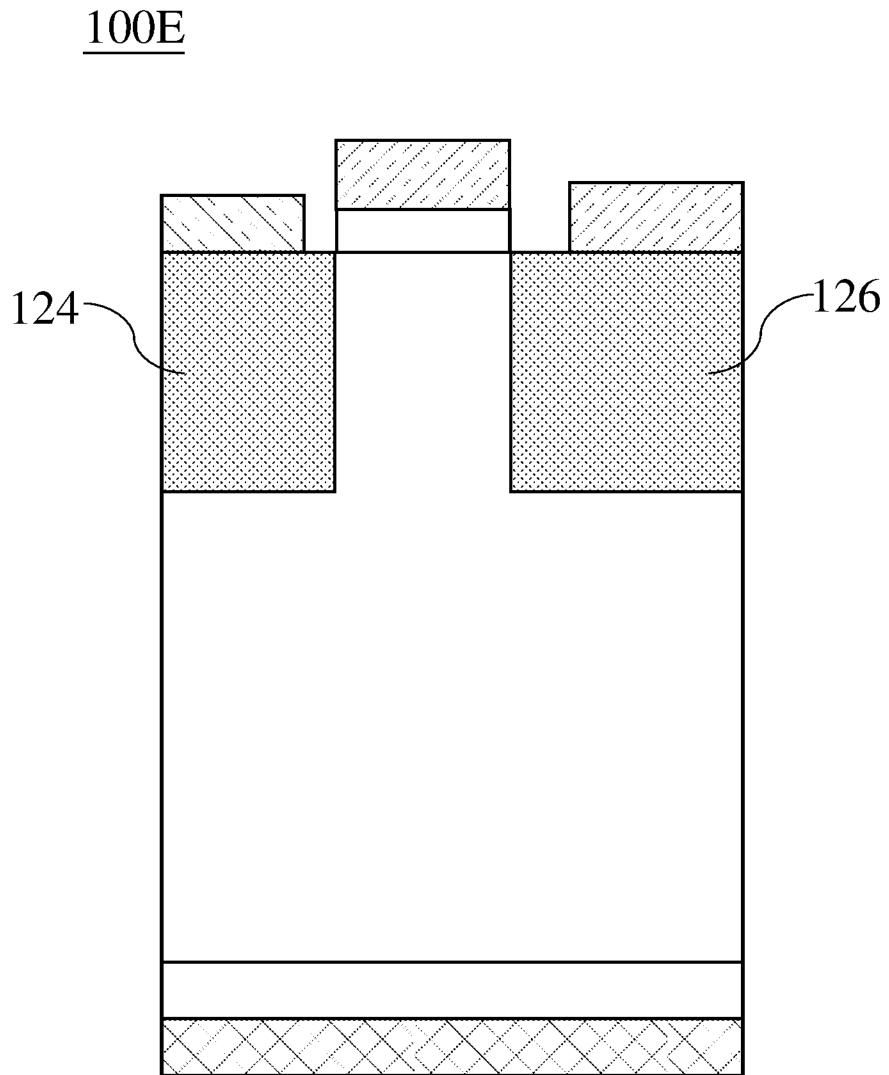

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/CN2021/100070

A. CLASSIFICATION OF SUBJECT MATTER

H01L 29/808(2006.01)i； H01L 29/66(2006.01)i； H01L 31/112(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPODOC, WPI, CNKI, CNPAT: diode, JFET, J-FET, junction gate field transistor, Junction FET, drift, source, gate, barrier, block, GaN, nitride

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2007252178 A1 (ONOSE, Hidekatsu) 01 November 2007 (2007-11-01) description, paragraphs [0031]-[0051], figures 1-9	1-25
A	US 2018122931 A1 (INFINEON TECHNOLOGIES AG) 03 May 2018 (2018-05-03) the whole document	1-25
A	US 2014231883 A1 (INFINEON TECHNOLOGIES AUSTRIA AG) 21 August 2014 (2014-08-21) the whole document	1-25
A	CN 112420694 A (UNIVERSITY OF ELECTRONIC SCIENCE AND TECHNOLOGY OF CHINA) 26 February 2021 (2021-02-26) the whole document	1-25
A	CN 105103295 A (AVOGY INC.) 25 November 2015 (2015-11-25) the whole document	1-25

☐ Further documents are listed in the continuation of Box C.　　☑ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
10 February 2022	**24 February 2022**

Name and mailing address of the ISA/CN	Authorized officer
National Intellectual Property Administration, PRC 6, Xitucheng Rd., Jimen Bridge, Haidian District, Beijing 100088, China	**ZHAO,Zhimin**
Facsimile No. **(86-10)62019451**	Telephone No. **86-(10)-53961446**

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/CN2021/100070

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