

(12) UK Patent Application (19) GB (11) 2 179 792 (13) A

(43) Application published 11 Mar 1987

(21) Application No 8620788

(22) Date of filing 28 Aug 1986

(30) Priority data

(31) 60/191013
60/198217

(32) 28 Aug 1985
5 Sep 1985

(33) JP

(51) INT CL⁴

H01L 21/34

(52) Domestic classification (Edition I):

H1K 1AA1 3E1M 3E5A 3E5C3 3E5CY 3P5 3T1C 3T5
3U6A 3U6B 5C3A 8PC 9B1 9C2 9D1 9E 9R2 MWX

(56) Documents cited

None

(58) Field of search

H1K

Selected US specifications from IPC sub-class H01L

(71) Applicant

Mitsubishi Denki Kabushiki Kaisha

(Incorporated in Japan)

2-3 Marunouchi 2-chome, Chiyoda-ku, Tokyo, Japan

(72) Inventors

Kakutaro Suda
Tadashi Hirao

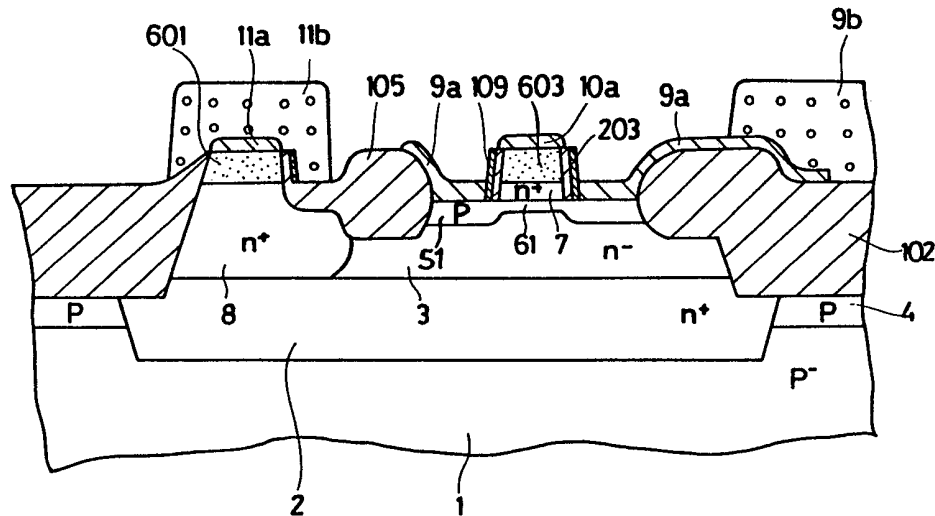
(74) Agent and/or Address for Service

Beresford & Co,
2-5 Warwick Court, High Holborn, London WC1R 5DJ

(54) Bipolar transistor

(57) In a method for fabricating a bipolar transistor a base electrode (9a) of metal silicide is formed being separated from an emitter region (7) only by the thickness of a double-layered insulator film (109, 203). The interfaces between the base (61) and emitter (7) regions and between the base (61) and base electrode (9a) lie in the same plane. The emitter region (7) is formed in a mesa by diffusion of impurity from an overlying doped polysilicon layer (603).

FIG.5K



GB 2 179 792 A



FIG. 1A

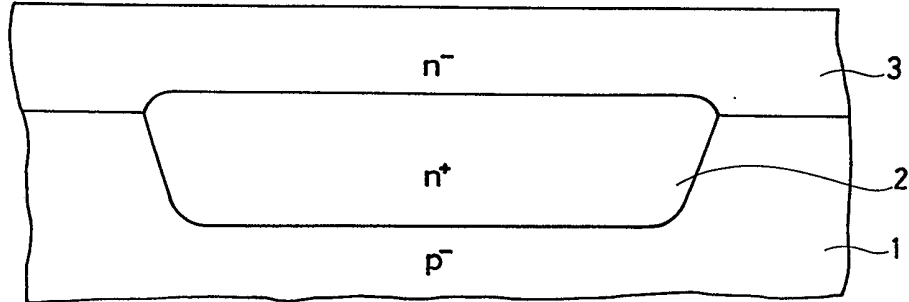


FIG. 1B

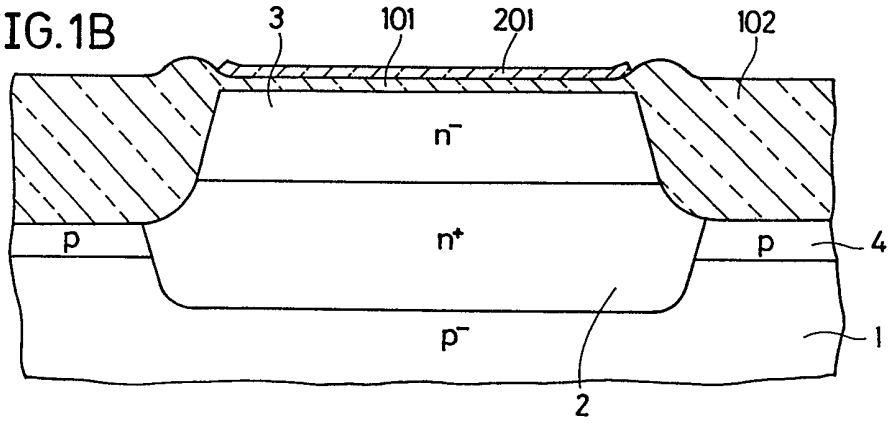
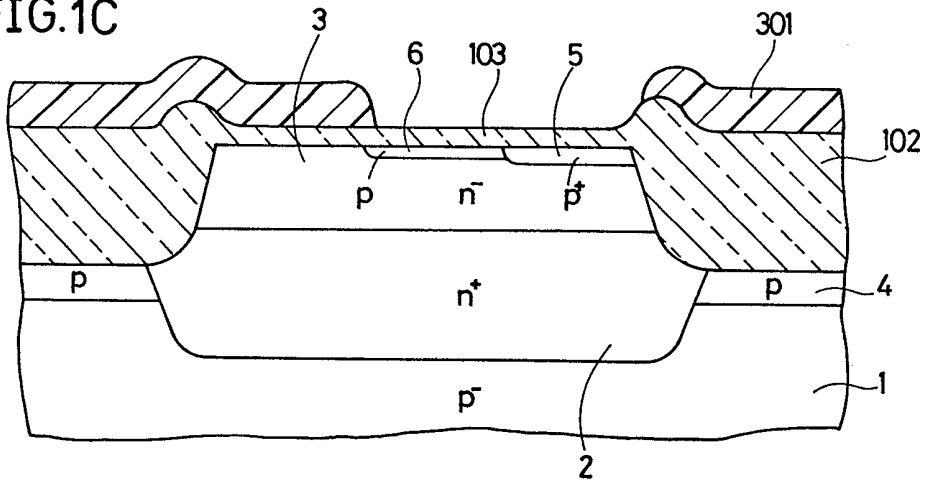


FIG. 1C



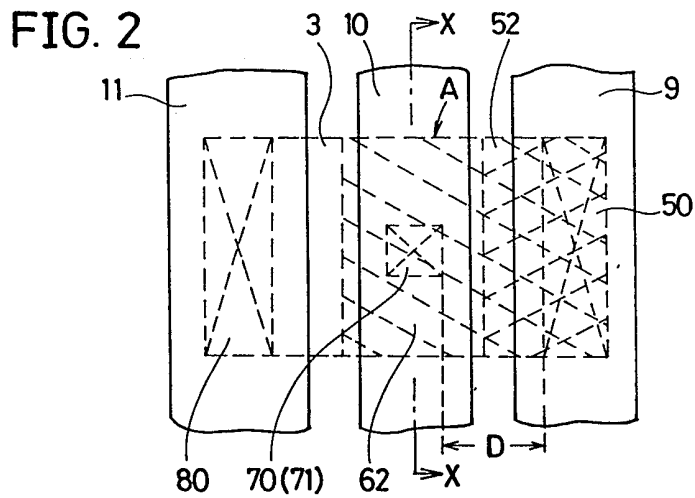
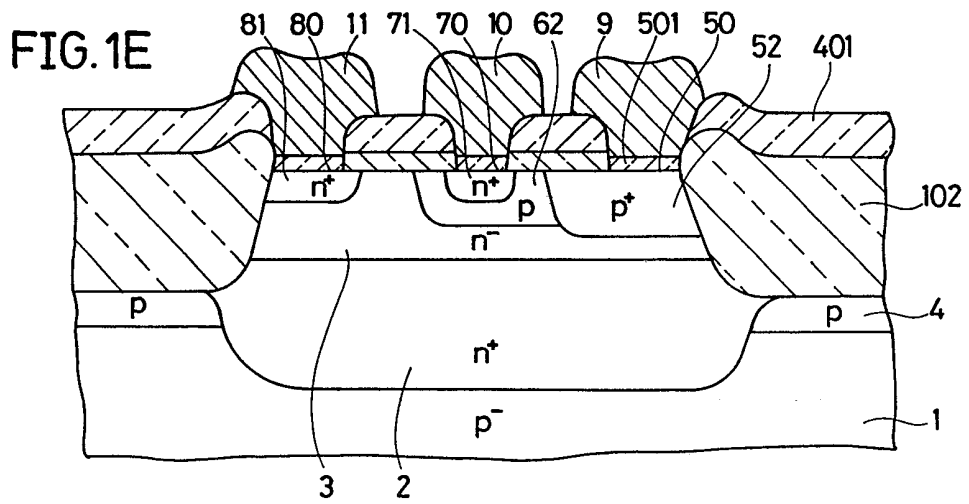
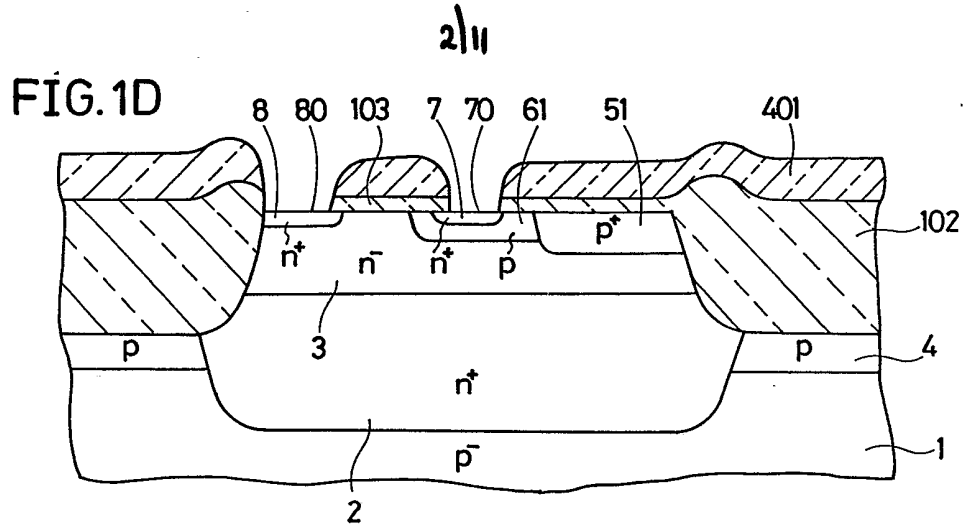


FIG. 3A

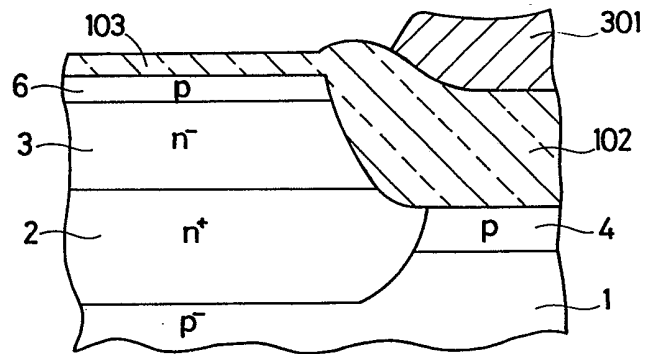


FIG. 3B

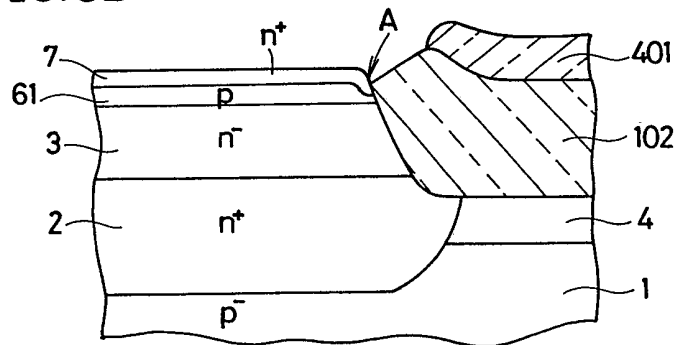
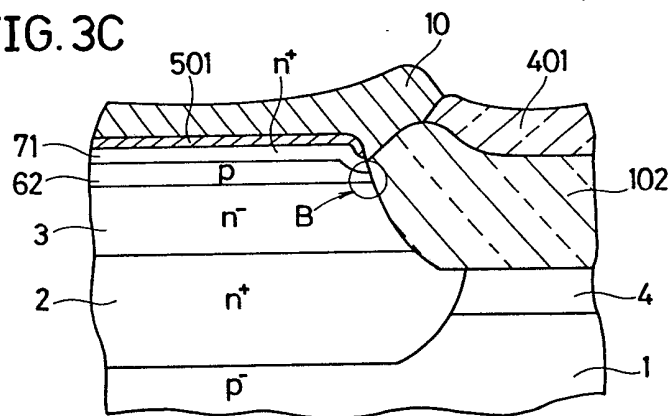
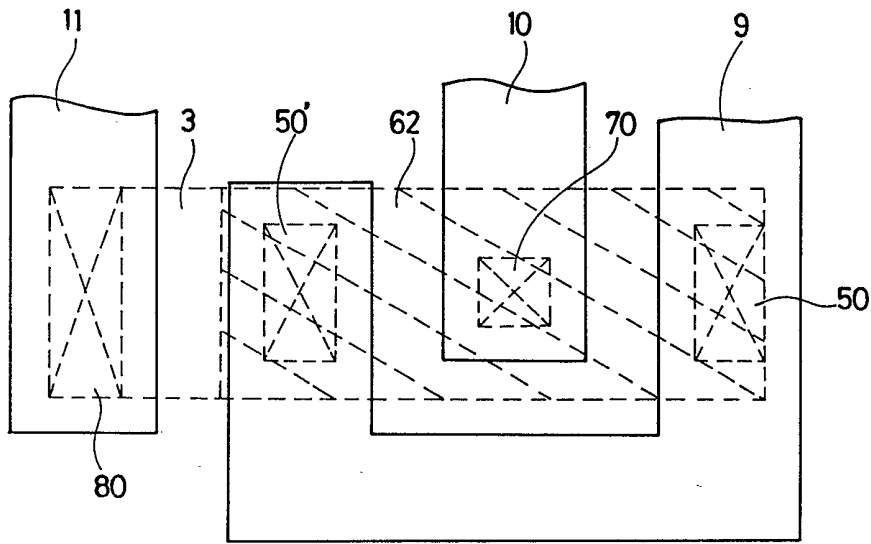


FIG. 3C



4/11

FIG. 4



slu

FIG. 5A

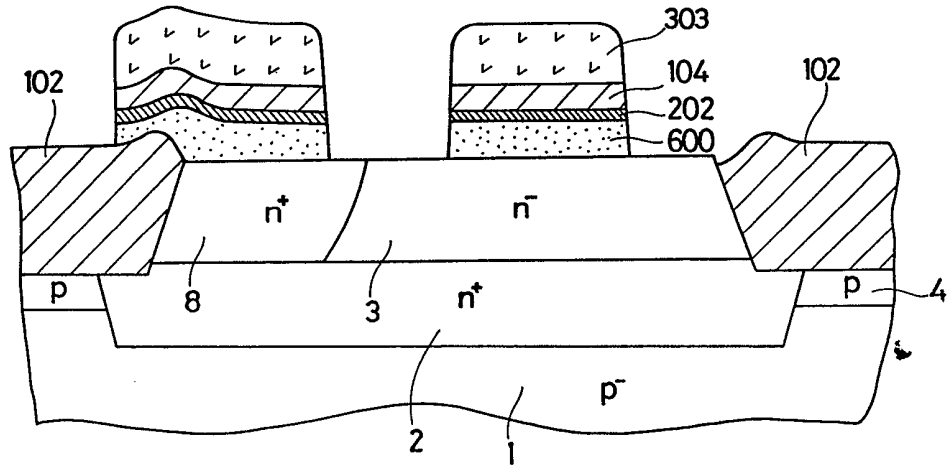
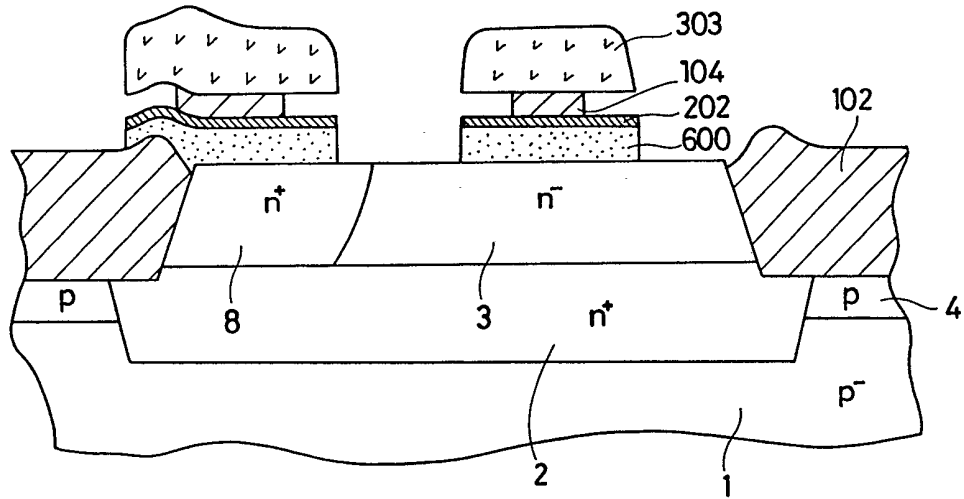


FIG. 5B



6/11

FIG. 5C

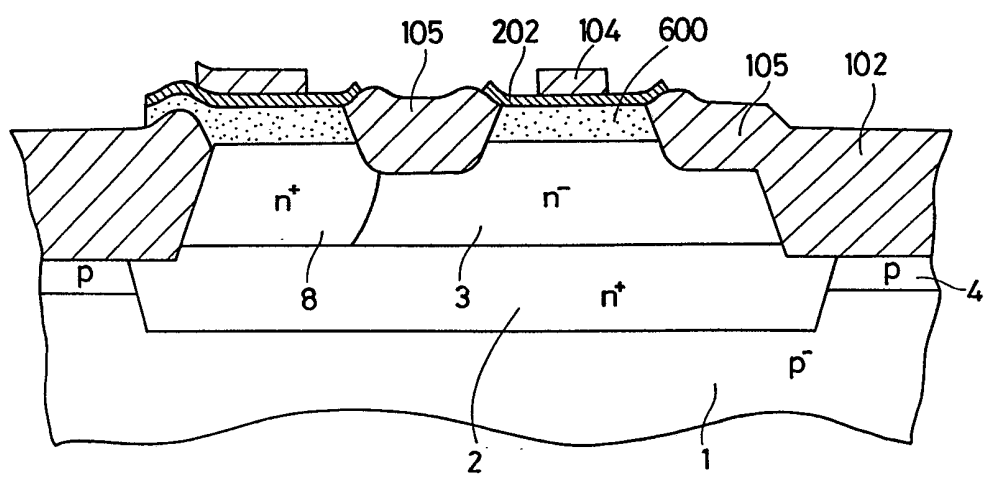
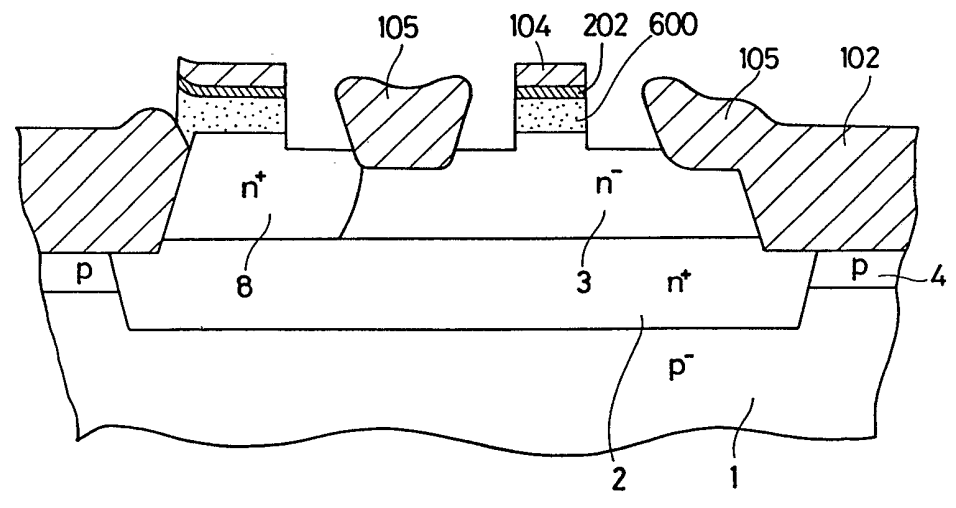


FIG. 5D



7/11

FIG. 5E

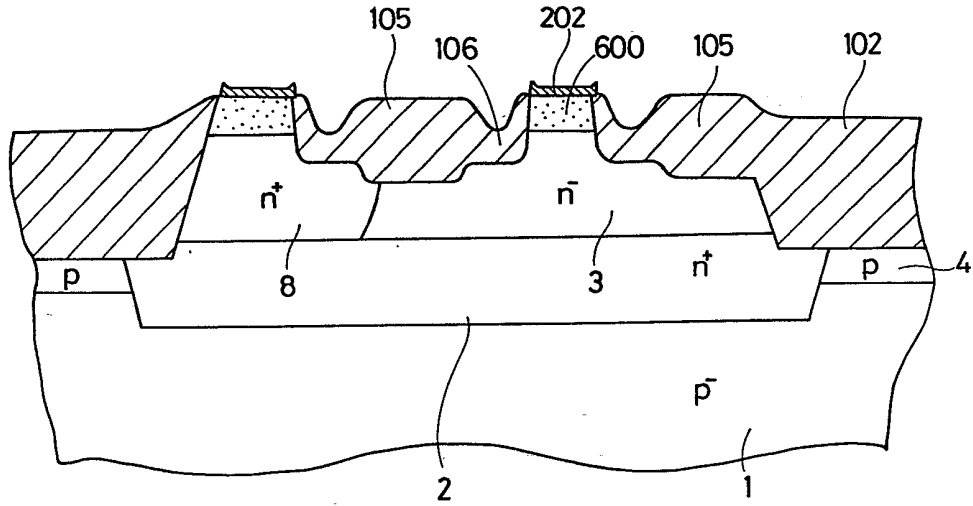
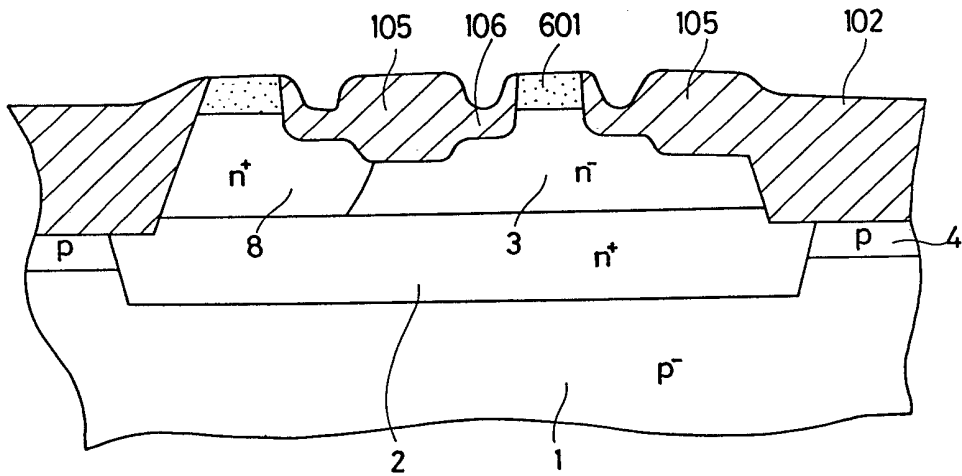


FIG. 5F



शु
FIG. 5G

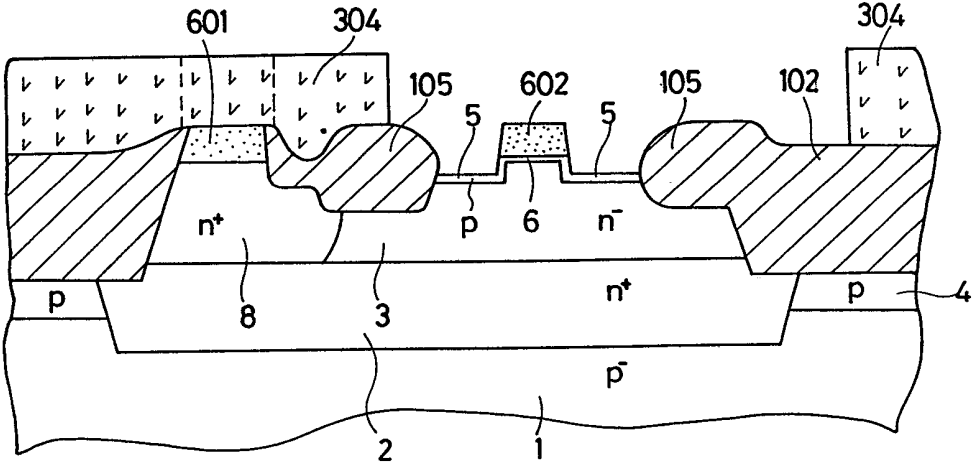
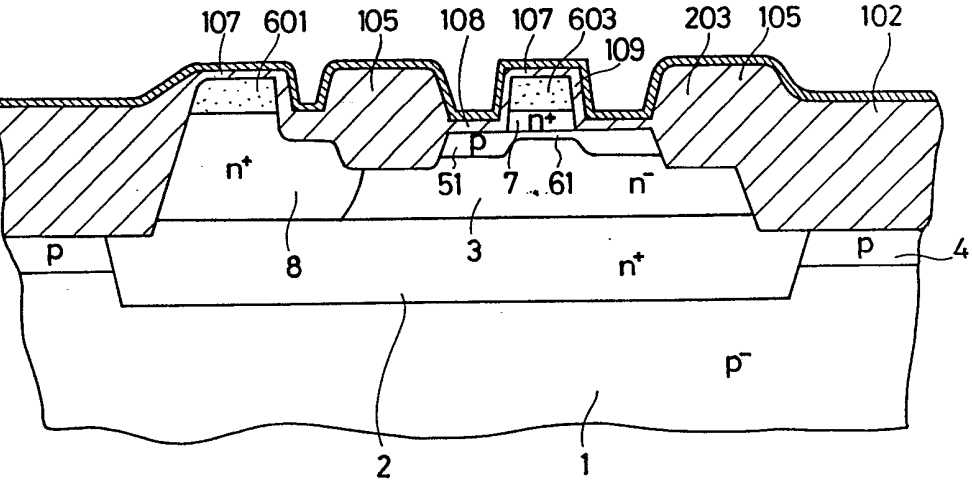


FIG. 5H



9/11

FIG. 5I

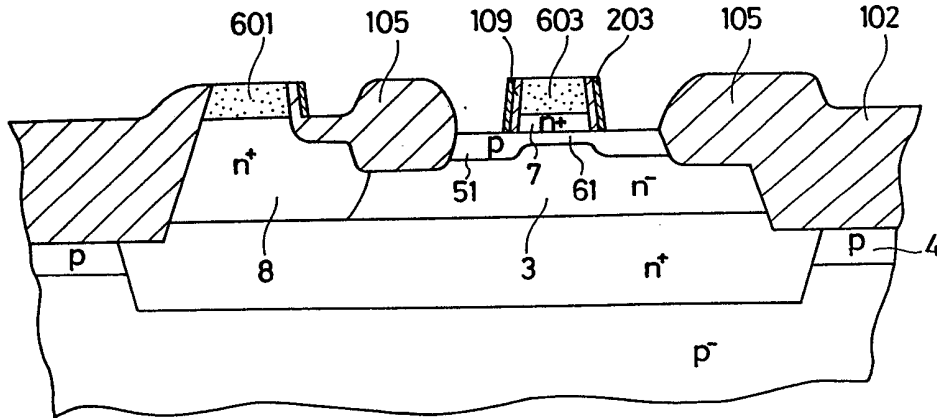
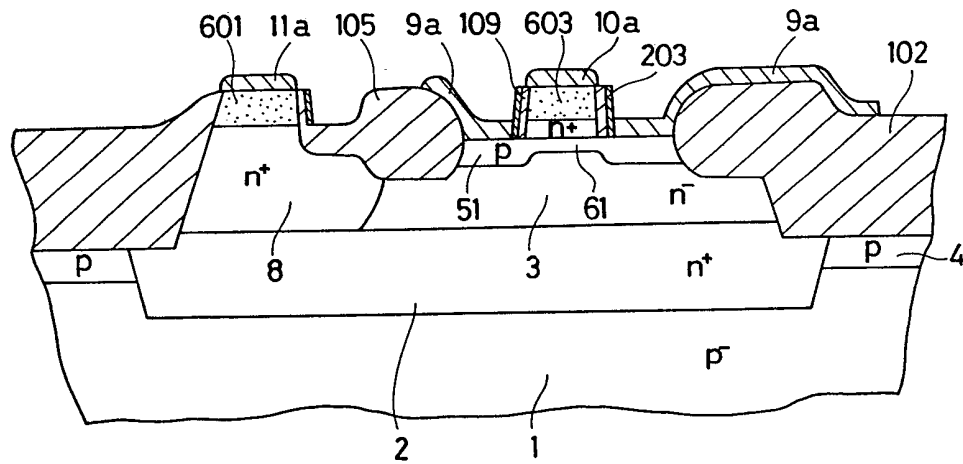


FIG. 5J



10/11
FIG.5K

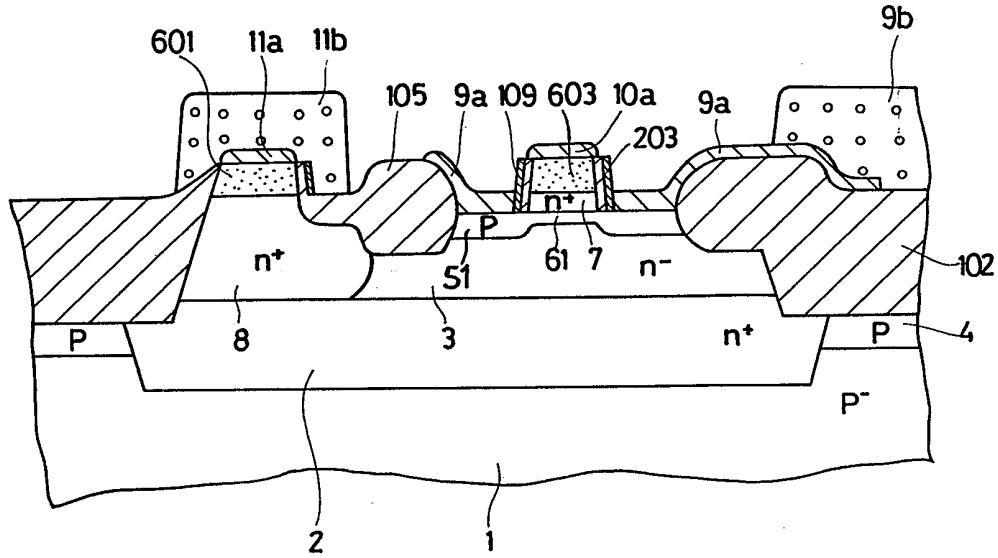


FIG.6

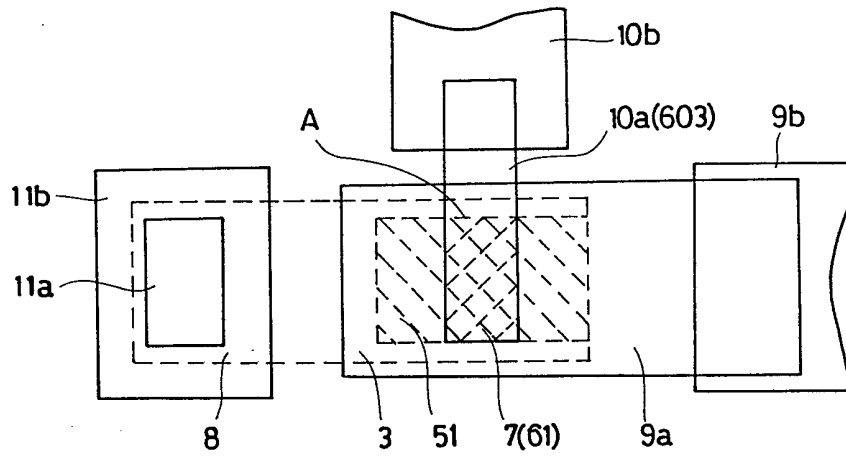
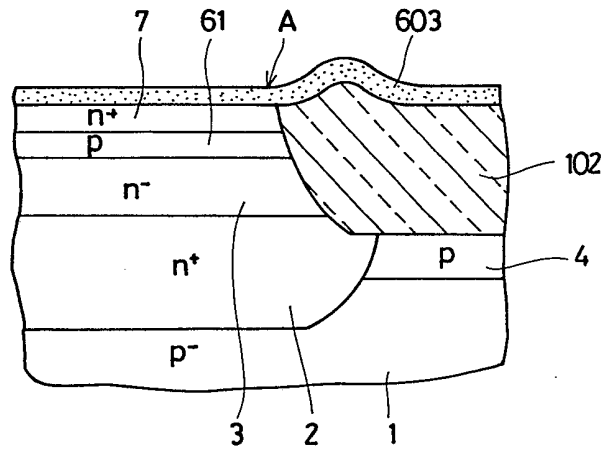




FIG.7



SPECIFICATION

Method for fabricating bipolar transistor in integrated circuit

5

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention generally relates to a method for fabricating a bipolar transistor in an integrated circuit (IC), and more particularly, it relates to an improvement in a method for fabricating electrode contact portions of the bipolar transistor.

15 Description of the Prior Art

In general, a bipolar transistor in an IC is formed in an island which is isolated electrically by a method such as p-n junction isolation, oxide film isolation or triple diffusion.

20 Such a semiconductor device is disclosed in, e.g., U.S. Patent No. 4,445,268, and formation of a self-aligned semiconductor device is disclosed in "Subnanosecond Self-Aligned P⁺L/MTL Circuits", IEEE Transactions on Electron Device, Vol. ED-27, No. 8, August 1980, P. 1379. Further, silicides for IC applications are described by T. Hirao et al. in Extended Abstracts of the 17th Conference on Solid State Devices and Materials, Tokyo, 1985, pp. 381-384 and by B.P. Murarka in BILICIDES FOR VLSI APPLICATIONS, pp. 66-69, 1983, Academic Press.

25 Figs. 1A to 1E are cross-sectional views showing the principal steps of a conventional method of fabricating a bipolar transistor in an IC. The conventional method is now described with reference to these drawings. An n⁻-type layer 2 of high impurity concentration for implementing a buried collector layer is selectively formed on a p⁻-type silicon substrate 1 of low impurity concentration, followed by growth of an n⁻-type epitaxial layer 3 thereover (Fig. 1A).

35 Then, the substance is selectively oxidized by utilizing a nitride mask film 201 on an under-layer oxide film 101, whereby a thick isolation oxide film 102 is formed while a p-type channel-cut layer 4 is simultaneously formed under the isolation oxide film 102 (Fig. 1B).

40 The nitride film 201 and the under-layer oxide film 101 are then removed to newly form an oxide film 103 for preventing ion channelling in the silicon crystal during ion implantation by which a p⁺-type layer 5 for implementing an extrinsic base layer at a later stage is formed with a photoresist mask film (this mask film is not shown). Thereafter, the photoresist film is removed to newly form a photoresist mask film 301 with which a p-type layer 6 for implementing an active base layer at a later stage is formed by ion implantation (Fig. 1C).

45 The photoresist film 301 is then removed and the substance is covered by a passivation film 401 generally made of phospho-silicate

glass (PSG). The substance is then subjected to a heat treatment for annealing the ion implanted layers 5 and 6 to form an extrinsic base layer 51 and an active base layer 61 at an intermediate stage as well as densifying the PSG film 401, followed by formation of holes 70 and 80 through both the PSG film 401 and the oxide film 103 to form an n⁺-type layer 7 for implementing an emitter layer and an n⁺-type layer 8 for implementing a low resistance layer underneath a collector electrode by ion implantation (Fig. 1D).

70 Thereafter, the respective ion implanted layers are annealed to complete an extrinsic base layer 52 and an active base layer 62 and to form an emitter layer 71 and a low resistance layer 81, followed by formation of hole 50 for a base electrode. Then, the respective holes 50, 70 and 80 are provided with films 85 501 of metal silicide such as platinum silicide (Pt-Si) or palladium silicide (Pd-Si) for preventing junction-spike of the electrodes, followed by formation of a base lead wire 9, an emitter lead wire 10 and a collector lead wire 11 made of a low-resistance metal such as aluminum (Al) (Fig. 1E).

90 Fig. 2 is a plan view showing a pattern of single-base structure which corresponds to Fig. 1E.

95 Generally, the frequency characteristic of a bipolar transistor depends on the base-collector capacitance and the base resistance, both of which must be decreased for improving the frequency characteristic. The p⁻-type extrinsic base layer 52 is provided for lowering the base resistance in the aforementioned structure, whereas the provision of the same leads to increase in the base-collector capacitance. In Fig. 2, an inactive base area between the emitter area 71 and an isolation oxide film boundary A also increases the base-collector capacitance. Thus, the emitter area 71 may be bounded by the isolation oxide film to be in walled emitter structure. However, such a method involves various disadvantages as will be seen from Figs. 3A to 3C.

100 Figs. 3A to 3C are partial enlarged sectional views taken along the line X—X in Fig. 2. In Fig. 3A, boron is injected with a photoresist mask film 301 to form a base layer. Then, etching in the walled emitter structure is enhanced at the boundary of an isolation oxide film 102 as indicated by a character A in Fig. 3B, and thus the emitter layer 71 is locally deepened as shown at B in Fig. 3C. Thus, lowered is controllability of the current amplification factor and increased is possibility of emitter-collector short circuit at the point B in Fig. 3C.

105 Further, as shown in Fig. 2, the base resistance depends on a separation D between the emitter area 71 and the base electrode 501 (hole 50), i.e., the separation between the base wire 9 and the emitter wire 10 plus the total width of margins of the respective wires

130

9 and 10 extending beyond the respective width of holes 50 and 70, and such margins inevitably remain even if the distance between the lead wires 9 and 10 is reduced by improving accuracy of photoetching.

The transistor may also be brought in the double-base structure as shown in Fig. 4 for reducing the base resistance, as well known in the art. However, the increased base area in the double-base structure results in increase of the base-collector capacitance.

Further, in the conventional fabricating method, the emitter-base interface is formed deeper than the base surface on which the base electrode is formed as seen in Fig. 1E, and this fact causes a problem that the current amplification factor is strongly dependent on the current. Namely, in the range of small current, the current is partly absorbed due to the recombination of electrons and positive holes in the vicinity of the emitter-base interface, and thus the controllability of the current amplification factor is not good.

25 SUMMARY OF THE INVENTION

In view of the prior art, it is a principal object of the present invention to provide a method for fabricating a bipolar transistor in an IC, the frequency characteristic of which is improved by lowering both the base resistance and the base-collector capacitance.

It is another object of the present invention to provide a method for fabricating a bipolar transistor, the current amplification factor of which is less dependent on the current even in the range of small current.

A method for fabricating a bipolar transistor in accordance with the present invention comprises the steps of: preparing a collector layer of a first conductivity type surrounded by an isolation oxide layer on a semiconductor substrate; forming a multilayered film pattern by etching with a photoresist layer mask thereon, the multilayered film including a polysilicon layer, a nitride layer and an oxide layer stacked in this order on the collector layer; retracting the oxide layer into between the nitride layer and the photoresist layer by side etching; selectively forming a first oxide film on the collector layer, utilizing the nitride layer as a mask; etching down through the nitride layer and the polysilicon layer to a prescribed depth of the collector layer by anisotropic etching, utilizing both the side-etched oxide layer and the first oxide film as a mask; forming a second oxide film on the etched and exposed surface area between the nitride layer region and the first oxide film region; removing the nitride layer; introducing an impurity of the first conductivity type into the polysilicon layer, utilizing the second oxide film as a mask; removing some of the second oxide film regions to expose regions in which a base layer and an emitter layer are going to be formed; implanting impurity ions into the

exposed region to form a second conductivity type layer for implementing the base layer; implanting silicon ions into not only the exposed region but also predetermined regions of the first oxide film, the predetermined regions neighboring on the exposed region; subjecting the substrate to a heat treatment to complete the base layer by annealing the second conductivity type layer and simultaneously form an emitter layer by diffusion of the first conductivity type impurity from one of the polysilicon layer regions; subjecting the substrate to an oxidation treatment at a relatively lower temperature to cover the exposed region with an oxide film, followed by formation of a nitride film thereover to provide a double-layered insulator film; anisotropically etching the double-layered insulator film to leave it only on the side walls of both the emitter layer and the polysilicon layer thereon; and forming a base electrode and an emitter electrode on the silicon-implanted region, which are made of a metal silicide and insulated from each other by the double-layered insulator film.

These objects and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1E are sectional views showing the principal steps of a conventional method of fabricating a bipolar transistor in an IC;

Fig. 2 is a plan view showing a surface pattern of single-base structure of the transistor shown in Fig. 1E;

Figs. 3A to 3C are partial enlarged sectional views for illustrating a transistor fabricated by a conventional method such that an emitter layer is bounded by an isolation oxide film;

Fig. 4 is a plan view showing a pattern of double-base structure of a conventional transistor;

Figs. 5A to 5K are sectional views showing the principal steps of a method of fabricating a bipolar transistor according to an embodiment of the present invention;

Fig. 6 is a plan view showing a pattern of double-base structure of the transistor shown in Fig. 5K; and

Fig. 7 is a partial enlarged sectional view showing a state in which an emitter layer of the transistor shown in Fig. 5K is bounded by an isolation oxide film.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Figs. 5A to 5K are sectional views showing the principal steps of a method of fabricating a bipolar transistor according to an embodiment of the present invention, and elements equivalent to those in Figs. 1A to 1E are indi-

cated by the same reference numerals.

Referring to Fig. 5A, similarly to the steps of the conventional method as shown in Figs. 1A and 1B, formed on a p⁻-type silicon substrate 1 are an n⁺-type buried collector layer 2, an n⁻-type epitaxial layer region 3, an n⁺-type epitaxial layer region 8 for collector contact, a p-type channel-cut layer 4 and an isolation oxide layer 102, and then removed are a nitride mask 201 and an under-layer oxide film 101. Thereafter, the surface of the substance is covered with a multilayered film which comprises a polysilicon layer 600, a nitride layer 202 and an oxide layer 104 stacked in this order. The multilayered film is then etched and patterned with a photoresist mask 303 to leave the multilayered film regions only over the areas where a collector contact and an emitter are going to be formed.

Referring to Fig. 5B, the oxide layer 104 in the multilayered film is retracted into between the nitride layer 202 and the photoresist layer 303 by side etching.

In Fig. 5C, a first oxide film pattern 105 is formed on the epitaxial layer 3, 8, utilizing the nitride layer 202 as a mask.

In Fig. 5D, the surface of the substance is etched down through the nitride layer 202 and the polysilicon layer 600 to a prescribed depth of the epitaxial layer 3, 8 by anisotropic etching, utilizing both the side-etched oxide layer 104 and the first oxide film 105 as a mask. The prescribed depth enables a base-emitter interface to be level with an interface between a base layer and a base electrode so that the current dependency of the current amplification factor may become smaller. Namely, the current amplification factor is surely controlled even in the range of small current by decreasing current absorption due to the recombination of electrons and positive holes in the vicinity of the base-emitter interface.

Referring to Figs. 5D and 5E, after removal of the oxide layer 104, a second oxide film pattern 106 of 200-300m thickness is formed on the etched and exposed surface area between the nitride layer region 202 and the first oxide film region 105. The side walls of the polysilicon layer 600 are also covered with the second oxide film 106.

Referring to Figs. 5E and 5F, the nitride layer 202 is removed to introduce n⁻-type impurity into the polysilicon layer 600, utilizing the second oxide film 106 as a mask. The polysilicon layer 601 containing the n⁻-type impurity acts as an impurity source for forming an emitter at a later stage.

Referring to Figs. 5F and 5G, the second oxide thin film regions 106 on the n⁻-type epitaxial layer region 3 are removed, utilizing a resist layer mask 304 which is formed except around an area where a base and an emitter are going to be formed. On the other hand, the first oxide film pattern 105 is left to isolate a collector contact area from a base con-

tact area. Therefore, the first oxide film pattern 105 is formed to 1m thickness at the stage shown in Fig. 5C. Then, with the resist mask 304, p-type impurity ions are implanted in the surface layer of the n⁻-type epitaxial layer region 3. Ion-injected layer regions 5 beneath areas, where the second oxide layer regions 106 have been removed, are formed for implementing extrinsic base layer regions at a later stage. An ion-injected region 6 beneath the polysilicon layer region 602 is formed for implementing an active base layer at a later stage. The ion-injected layer region 6 for an active base layer is naturally made thinner than the ion-injected layer regions 5 for extrinsic base layer regions, since the impurity ions must penetrate the polysilicon layer 602 to form the former region. Then, after opening a hole (shown by broken lines in Fig. 5G) through the resist layer 304 at an area for a collector contact, silicon ions are injected, utilizing the resist layer 304 as a mask. Those silicon atoms injected into areas which are not covered with the resist mask 304 are consumed later to form metal silicide electrodes.

Referring to Figs. 5G and 5H, after removal of the resist mask 304, the p-type ion-injected layer regions 5, 6 are annealed and simultaneously n⁻-type impurity is diffused from the polysilicon layer 602 into the epitaxial layer 3. As a result, an emitter 7, extrinsic base regions 51 and an active base region 61 are formed in a self-aligned manner. The extrinsic base regions 51 are naturally formed a little deeper than the active base region 61 and have a relatively lower resistivity. Then, with oxidation at a relatively lower temperature (800-900°C), relatively thicker oxide film regions 107 are formed on the top surfaces of the n⁻-type polysilicon layer regions 603, 601; relatively thicker oxide film regions 109 are formed on side walls of both the polysilicon layer 603 and the emitter 7; and relatively thinner oxide film regions 108 are formed on the extrinsic base regions 51. It is known that silicon or polysilicon regions containing n-type impurity are oxidized at a higher rate at a relatively lower temperature. After the oxidation, a nitride film is formed to cover the entire surface of the substance.

Referring to Figs. 5H and 5I, the nitride film 203 is anisotropically etched to leave it only on the side walls of both the polysilicon layer 603 and the emitter layer 7, and then similarly oxide film regions 107, 108 are also etched away. As a result, double-layered insulator film regions comprising oxide layer 109 and nitride layer 203 are left only on the side walls of both the polysilicon layer 603 and the emitter layer 7.

Referring to Fig. 5J, the entire surface of the substance is covered with a film of a metal such as platinum (Pt) or titanium (Ti) to form a metal silicide film by annealing over the areas where silicon ions have been injected as

described referring to Fig. 5G. However, any silicide film is not formed on the side walls of both the polysilicon layer 603 and the emitter layer 7, since the side walls are covered with the double-layered insulator films. The remaining metal film regions which have not been silicidized are removed by aqua regia. As a result, a base electrode 9a, an emitter electrode 10a and a collector electrode 11a are formed of metal silicide.

In Fig. 5K, a base lead wire 9b, an emitter lead wire 10b (not shown in this figure) and collector lead wire 11b are formed with a low resistive metal such as aluminum (A1). As seen in Fig. 5K, the base electrode 9a is separated from the emitter region 7 only by the thickness of the double-layered film 109, 203, so that the base resistance becomes very small. Further, the base area is remarkably reduced with no wide separation area between the base and emitter electrodes 9a, 10a, so that the base-collector capacitance is also reduced. Accordingly, the frequency characteristic of the transistor is much improved.

Fig. 6 is a plan view showing a surface pattern of the transistor shown in Fig. 5K. As seen from Figs. 5K and 6, the polysilicon film 603 have served as a diffusion source for the emitter layer 7 which is thus bounded by the isolation oxide film 102 at a portion A. The base thickness is not narrowed at the boundary A of the isolation oxide film 102 as shown in Fig. 3 but constant, since the emitter layer 7 and the active base layer 61 are simultaneously formed in a self-aligned manner to be substantially parallel to each other as shown in Fig. 7.

Further, as seen in Fig. 6, the base electrode 9a is formed around three sides of the emitter region 7 to automatically implement double-base structure, so that the base resistance can be further reduced without increasing the base region.

The width of the polysilicon layer 603 is narrowed as a result of side etching in Fig. 5B and also by invasion of the so-called bird beak of the second oxide film 106 during oxidation, so that the width finally becomes less than 1/3 of the initial one shown in Fig. 5A.

Therefore, an emitter with a submicron width can be readily realized.

Further, the emitter-base interface is made to be level with the interface between the base layer 51 and the base electrode 9a. Accordingly, the current dependency of the current amplification factor becomes small.

Although formation of an n-p-n transistor has been described in the above embodiment, it goes without saying that the present invention is applicable to formation of a p-n-p transistor.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be

taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

70 CLAIMS

1. A method for fabricating a bipolar transistor, comprising the steps of:

preparing a collector layer (3, 8) of a first conductivity type surrounded by an isolation oxide layer (102) on a semiconductor substrate;

forming a multilayered film pattern by etching with a photoresist layer mask (303) thereon, said multilayered film including a polysilicon layer (600), a nitride layer (202) and an oxide layer (104) stacked in this order on said collector layer (3, 8);

retracting said oxide layer (104) into between said nitride layer (202) and said photoresist layer (303) by side etching;

selectively forming a first oxide film (105) on said collector layer (3, 8), utilizing said nitride layer (202) as a mask;

etching down through said nitride layer (202) and said polysilicon layer (600) to a prescribed depth of said collector layer (3, 8) by anisotropic etching, utilizing both said side-etched oxide layer (104) and said first oxide film (105) as a mask;

forming a second oxide film (106) on the etched and exposed surface area between said nitride layer region (202) and said first oxide film region (105);

removing said nitride layer (202); introducing an impurity of said first conductivity type into said polysilicon layer (600), utilizing said second oxide film (106) as a mask;

removing some of said second oxide film regions (106) to expose a regions in which a base layer and an emitter layer are going to be formed;

implanting impurity ions into said exposed region to form a second conductivity type layer (5, 6) for implementing said base layer;

implanting silicon ions into not only said exposed region but also predetermined regions of said first oxide film (105), said predetermined regions neighboring on said exposed region;

subjecting said substrate to a heat treatment to complete said base layer (51, 61) by annealing said second conductivity type layer (5, 6) and simultaneously forming an emitter layer (7) by diffusion of said first conductivity type impurity from one (602) of said polysilicon layer regions;

subjecting said substrate to an oxidation treatment at a relatively lower temperature to cover said exposed region with an oxide film (107, 108, 109), followed by formation of a nitride film (203) thereover to provide a double-layered insulator film;

anisotropically etching said double-layered insulator film to leave it only on said side

walls of both said emitter layer (7) and said polysilicon layer (603) thereon; and

forming a base electrode (9a) and an emitter electrode (10a) on said silicon-implanted region, which are made of a metal silicide and insulated from each other by said double-layered insulator film (109, 203).

2. The method in accordance with claim 1, wherein said prescribed depth in the fifth step is such as to enable the base-emitter interface to be level with the interface of said base layer (51) and said base electrode (9a).

3. A transistor having substantially coplanar interfaces between the base and emitter and between the base and a base terminal.

4. A transistor as claimed in claim 3, wherein the base terminal embraces three sides of the emitter.

5. A transistor as claimed in claim 3 or 4, wherein a thin insulating wall separates the emitter and base terminal.

6. A transistor as claimed in any of claims 3 to 5, wherein the base thickness is not reduced at the edges of the base.

7. A method of fabricating a transistor in which an epitaxial layer of one conductivity type is formed with a mesa, a covering layer of the other conductivity type is formed on the mesa and surrounding epitaxial layer, a polysilicon layer is formed on the layer on the mesa, and the covering layer is annealed and impurity of said one conductivity type is diffused from the polysilicon layer to the epitaxial layer, so that the mesa is transformed into an emitter and the covering layer is transformed into a base having a substantially flat surface on which the emitter stands.

8. A transistor fabricated using the method of any of claims 1, 2 and 7.

9. A method of fabricating a transistor substantially as described in the description with reference to Figures 5 to 7 of the drawings.

10. A transistor substantially as described in the description with reference to Figures 5 to 7 of the drawings.