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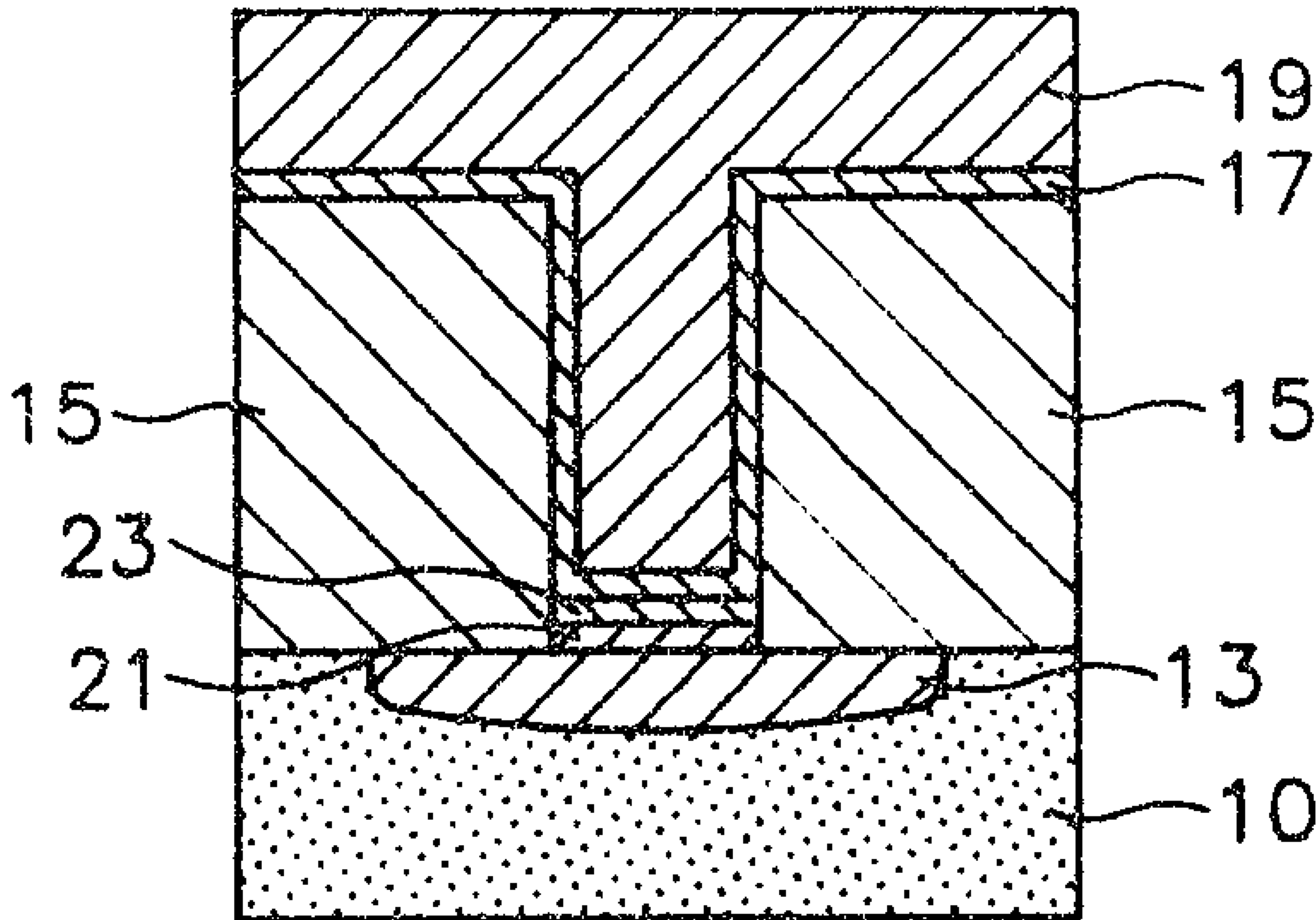
(54) Titre : STRUCTURE DE CONTACT OHMIQUE POUR DISPOSITIF A SEMICONDUCTEUR A DEGRE D'INTEGRATION ELEVE ET METHODE DE FABRICATION DE CETTE STRUCTURE

(54) Title: OHMIC CONTACT STRUCTURE OF HIGH INTEGRATED SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE SAME



(57) Abrégé/Abstract:

The present invention relating to an ohmic contact structure for connection of an electrode to a high integrated semiconductor device and a method for making the same, may be usefully applied to low resistance of electronic lines and high reliability in high integrated semiconductor devices, by forming selectively on a contact hole a material having a smaller bandgap than that of a substrate material to lower a contact resistance and by forming a material of hetero-junction structure under the above material to minimize stress and strain between a metal and a semiconductor.

ABSTRACT OF THE DISCLOSURE

The present invention relating to an ohmic contact structure for connection of an electrode to a high integrated semiconductor device and a method for making
5 the same, may be usefully applied to low resistance of electronic lines and high reliability in high integrated semiconductor devices, by forming selectively on a contact hole a material having a smaller bandgap than that of a substrate material to lower a contact
10 resistance and by forming a material of hetero-junction structure under the above material to minimize stress and strain between a metal and a semiconductor.

OHMIC CONTACT STRUCTURE OF HIGH INTEGRATED-SEMICONDUCTOR DEVICE AND METHOD FOR MAKING THE SAME

BACKGROUND OF THE INVENTION

(1) Field of the Invention

5 The present invention relates to a manufacture of a semiconductor device. More particularly, it relates to an ohmic contact structure for connecting an electrode to a high integrated semiconductor device and a method for making the ohmic contact structure.

10 (2) Description of the Prior Art

High density degree of integration circuits has been improved double every year. Nowadays, there has begun mass production of 16M dynamic random access memory devices with a sub-half micron design rule, and 15 performance speed is improved but resistance-capacitance delay and characteristics of the lines are degraded due to microminiaturization of lines by high integration of circuits and increase in the length of the lines. Accordingly, a technique of forming a contact hole in 20 the sub-half micron age takes up an important position in respect of low resistance and high reliability of the semiconductor devices.

Connecting an electrode to a semiconductor device is generally performed through a contact hole formed on 25 an insulating layer such as a silica glass or a boro-phosphorous silicate glass. Junction between a metal and a semiconductor through a contact hole is characterized as a rectifying contact and a non-rectifying contact

first proposed by Shottky in 1940. In the theory, the non-rectifying contact is formed in the following two cases: first, a work function of a metal material is smaller than a work function of a semiconductor material in an n-type semiconductor substrate; second, a work function of a metal material is larger than a work function of a semiconductor substrate in a p-type semiconductor substrate.

It is too difficult for today's art technology to form an ideal Shottky contact, i.e. achieve a contact between a metal and a semiconductor with a resistance near zero. A hypothesis thereabout is described in detail in U.S. Patent No. 4,738,937.

A representative technique for forming a contact hole to lower the contact resistance is shown in FIG. 1 (refer to U.S. Patent No. 5,108,954). As illustrated, a junction region 3 to which impurity of a predetermined contact hole is implanted, is formed on a part within a semiconductor substrate 1, and a metal layer 9, wiring electrode, is deposited on a surface of an insulating layer 5 including the region of a contact hole (not illustrated) to cover a part of the above junction region 3 exposed by the contact hole by a metal layer 9. If the metal layer having a considerable thickness is formed serially from the bottom of the contact hole to the surface of the insulating layer 5 along sidewalls of the contact hole, electrical contact is formed between

a substrate and a wiring electrode. And a diffusion prevention layer 7 of titanium nitride (TiN) or titanium tungstenite (TiW) is formed in order to prevent metal or silicon electromigration resulted from diffusion of
5 metal and silicon between the substrate 1 and wiring electrode 9.

At the time of subsequent thermal treatment, i.e. formation of silicide $TiSi_2$ made by heat treatment of titanium and silicon, out-diffusion occurs, which causes
10 a sharp drop of the concentration of the dopant in the interface of the diffusion-prevention layer 7. The contact resistance is increased thereby. The relationship between the contact resistance and the dopant concentration will be described.

15 A plug implantation technique of additionally ion-implanting the dopant after the contact hole formation is used to prevent the out-diffusion of the dopant and supplement the reduced dose.

As shown in FIG. 2, according to such a plug
20 implantation, a protrusion 3a is formed under the junction region 3 adjacent to the contact hole. This protrusion 3a does not cause any serious problem in a conventional semiconductor device having a relatively-deep junction in a substrate.

25 However, as in the case of a very large-sized integrated circuit (VLSI) in which a large number of devices are assembled in a unit area, this protrusion

may cause short-circuit conductivity in a semiconductor device having a shallow junction, which is adverse to the requirement for improving the performance speed.

5 Besides, the impurity level exceeds the solubility limit in a junction area, the junction area is saturated with the impurity and a deposit of the doped impurity is shown as a separate phase.

Therefore, the impurity level in the junction area is limited. If the deposit is shown in the junction
10 region, the increase of the impurity or dose cannot increase carrier density any more.

The deposit in a lot of silicon grains causes diffusion of carrier and facilitates reunion of the carrier.

15 SUMMARY OF THE INVENTION

The present invention seeks to lower a contact resistance of a semiconductor device.

It is a first object of the present invention to provide a low resistance contact structure of a high
20 integrated semiconductor device that may reduce a contact resistance by forming selectively on a contact hole a material having a band gap smaller than that of a substrate material on the contact hole, and may minimize stress and strain between a metal and a
25 semiconductor by forming a material having a hetero-junction structure thereunder.

It is a second object to provide a method for

forming effectively an ohmic contact structure having a hetero-junction.

According to this invention, an ohmic contact structure of a semiconductor device, comprises:

5 a junction region doped with an impurity on a semiconductor substrate;

a first resistance control layer having a reduced resistivity and selectively provided on a contact hole over the junction region with a material of a hetero-

10 junction structure whose work function is lower than a substrate material;

a second resistance control layer having a reduced resistivity provided with a material whose work function is lower than a substrate material on said first

15 resistance control layer; and

a conductive layer forming a wiring electrode provided on the second resistance control layer.

A method for making a semiconductor device comprises the steps of:

20 forming a junction region implanted with an impurity on a predetermined portion of a semiconductor substrate;

forming an insulating layer on the semiconductor substrate and forming a contact hole by opening the

25 insulating layer in order to expose a part of the junction region;

forming a first resistance control layer on the

contact hole;

forming a second resistance control layer on the first resistance control on the first resistance control layer;

5 forming at least one barrier layer on the second resistance control layer and insulating layer and performing a heating treatment thereon; and

forming a conductive layer on the barrier layer.

As another aspect of the present invention, the 10 present invention uses bandgap engineering that has been studied, making compound semiconductor an object of its study. The contact resistance depends on the following expression:

15

$$Rc \fallingdotseq A \exp \left[\frac{4\pi \ \varepsilon_s m^*}{h} \left(\frac{\psi_B}{N_D} \right) \right]$$

20 Rc : contact resistance ψ_B : barrier layer height

N_D : dopant concentration m^* : effective mass

A : constant ε_s : permittivity

h : planck constant

According to this expression, internal factors to 25 lower a contact resistance are low barrier layer height, i.e. low work function between a metal and a semiconductor, high concentration dopant, and small effective mass, i.e. high mobility. In order to meet this requirement, Ge which has a more excellent physical 30 characteristic than that of Si and is in the same family as Si, is used as a second resistance control layer of

the present invention. For reference, table 1 shows comparison of properties of matter between two materials:

Table 1

	Si		Ge
Structure of Crystal	diamond		diamond
Bandgap (300°K)	1.12eV		0.66eV
Mobility (cm^2/V Sec)	electron	1500	3,900
	hole	450	1,900

In order to minimize stress and strain generated by difference of each lattice constant, a first resistance control layer of hetero-junction structure, e.g. $Si_{1-x}Ge_x$ is provided to be inserted between silicon and the second resistance control layer. Accordingly, reactions between the metal and semiconductor layer such as out-diffusion of the dopant, formation of the protrusion by excessive ion-implantation and eduction phenomenon of the doped impurity is effectively controlled by the first and second resistance control layers crossing the wiring electrode and semiconductor layer. As a result of the reduced resistance, turn may reduce the size of the contact hole that makes possible miniaturization of a semiconductor device. In such a structure, the resistance control layer is formed to be even and thin by treating the surface of the semiconductor layer by means of a proper atmospheric gas, by an epitaxial

process, or by depositing a proper material.

Accordingly, in one aspect, the present invention provides an ohmic contact structure of a semiconductor device, comprising: a semiconductor substrate; a junction
5 region doped with an impurity on said semiconductor substrate; a first resistance control layer having a reduced resistivity and selectively provided on a contact hole over said junction region with a material of a heterojunction structure whose band gap is narrower than that of a material
10 of said semiconductor substrate; a second resistance control layer formed of Ge, having a reduced resistivity, and having a work function which is lower than that of said first resistance control layer; and a conductive layer forming a wiring electrode provided on said second resistance control
15 layer.

In a further aspect, the present invention provides an ohmic contact structure of a semiconductor device, comprising: a junction region doped with an impurity on a semiconductor substrate; a first resistance control layer
20 having a reduced resistivity and selectively provided on a contact hole over the junction region with a material of a heterojunction structure whose work function is lower than a substrate material; a second resistance control layer having a reduced resistivity provided with a material whose work
25 function is lower than a substrate material on said first

resistance control layer; and a conductive layer forming a wiring electrode provided on the second resistance control layer.

In a still further aspect, the present invention
5 provides a method for making a semiconductor device comprising the steps of: forming a junction region implanted with an impurity on a predetermined portion of a semiconductor substrate; forming an insulating layer on said semiconductor substrate and forming a contact hole by opening
10 the insulating layer in order to expose a part of the junction region; forming a first resistance control layer on said contact hole; forming a second resistance control layer on said first resistance control on said first resistance control layer; forming at least one barrier layer on said
15 second resistance control layer and insulating layer and performing a heating treatment thereon; and forming a conductive layer on said barrier layer.

The present invention will be apparently described with reference to the accompanying drawings.

20

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view showing a typical contact structure of a semiconductor device in a conventional way;

Fig. 2 is a sectional view showing the other conventional contact structure and its problem;

Figs. 3A to 3E are steps in the manufacture of a contact structure of a semiconductor device in accordance with a preferred embodiment of this invention;

Figs. 4A to 4C are steps in the manufacture of a contact
5 structure of a semiconductor device in accordance with a second preferred embodiment of this invention;

Fig. 5 is a graph showing the relationship between flow rate of 10% GeH_4 and composition ratio of $Si_{1-x}Ge_x$; and

Fig. 6 is a graph summing up resultants produced by
10 gauging a contact resistance between metal and a semiconductor, according to each contact structure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figs. 3A to 3E show a preferred embodiment of this invention, and depict the steps in the manufacture of a
15 contact structure by an epitaxial process.

Referring to FIG. 3A, a first step is ion-implanting impurity of a predetermined conductivity type on one portion of a semiconductor substrate 10 to form a junction region 13. As a second step, an insulating
5 layer 15 such as silica glass or boro-phosphorous silicate glass is applied to the semiconductor substrate 10 and the junction region 13, and a contact hole 16 is formed by opening the insulating layer 15 to expose a part of the above junction region 13.

10 A third step is forming an $Si_{1-x}Ge_x$ epi-layer 21, a first resistance control layer 21 on the contact hole 16 (FIG. 2B). SiH_2Cl_2 and GeH_4 using H_2 as a carrier gas are used as a reaction gas for the formation of the epi-layer. Besides, Ge source is made by mixing 10% GeH_4 to
15 H_2. A condition of formation of the Si_{1-x} Ge_x epi-layer 21 is as follows: 600 - 900 °C; flow rate of 20 sccm to 200 sccm. Preferably, the amount of SiH_2Cl_2 is changed to 20 - 200 sccm at 625°C, 20slm of H_2 flow rate, and 1 - 10 sccm of GeH_4 flow rate. As the flow rate of 10% GeH_4
20 changes, the Ge concentration is also changed, and the thicker the Ge concentration is, the more the growth speed is increased. And the growth speed of the Si_{1-x} Ge_x epi-layer 21 is 23 Å/min, if Ge is 12%, i.e. in case of 0.88 Si and 0.12 Ge. In case of 0.67 Si and 0.36 Ge, the
25 growth speed is 126 Å/min.

By increasing the flow rate of 10% GeH_4 gradually in such a condition, the $Si_{1-x}Ge_x$ epi-layer 21 is grown to a

thickness of 100Å - 500Å, preferably, about 200 Å.

FIG. 5 is a graph showing a relationship of change in the content of Ge according to the flow rate of 10% GeH_4. When it comes to the composition ratio of $Si_{1-x}Ge_x$
5 epi-layer, composition ratio of x is changed to 0.4 according to the graph of FIG. 5. The grown $Si_{1-x}Ge_x$ epi-layer 21 does not contain dopant but doped $Si_{1-x}Ge_x$ may be used, if necessary.

A doped epitaxial layer is formed by flowing B_2H_6
10 gas or PH_3 gas at the time of epitaxial process. A fourth step is forming a second resistance control layer 23, and uses the epi-process like the third step (FIG. 3C). As widely known, its condition is the same as the growth condition of the $Si_{1-x}Ge_x$ epi-layer 21, and the flow rate
15 of SiH_2Cl_2 is zero to form the Ge epi-layer 23. The thickness of the Ge epi-layer 23 is about 50Å - 100Å. If the conductivity type of the junction region 13 is P+, the 3rd group element in the periodic table, e.g. B or BF_2 is ion-implanted.

20 In case of N+ type junction region 13, As or P is ion-implanted. The ion-implantation is performed at 20 - 50 KeV, at a dose of $5x10^{14}$ - $1x10^{15}$ (ions/cm^2).

A fifth step is forming a barrier layer 17 on the second resistance control layer 23 and the insulating
25 layer 15 formed through the above process, and performing heating treatment.

In this embodiment, only one barrier layer 17 is

provided, and two barrier layers may be provided in a second embodiment that will be described after. First, titanium is deposited by sputtering to a thickness of about 500Å - 1500Å, and annealed at about 600 °C -900°C in a passive ambient of N for a short time period to form a structure as shown in FIG. 3D. Such a heating treatment performed for a very short time period may be available by means of rapid thermal annealing (RTA) device. While titanium contacting the second resistance control layer 23 comes to be $TiGe_x$ by annealing, the rest titanium that does not contact the second resistance control layer 23 reacts with N_2 in the atmosphere and titanium nitride serving as a diffusion barrier layer is formed thereon. Finally, a conductive layer is formed to be used as an electronic line by burying the contact hole with the metal layer, as shown in FIG. 3E.

FIGS. 4A to 4C show the steps in the manufacture of a contact structure of a semiconductor device in accordance with a second preferred embodiment of this invention, and correspond to FIGS. 3A to 3E. The common description will be omitted, and like reference numerals and letters designate like parts.

In this embodiment, a first resistance control layer is formed by post heating treatment after Ge is ion-implanted not by epitaxial process but by ion-implantation. First, by using a photosensitive layer 18 as a mask, Ge is ion-implanted at a accelerating voltage

of 10 - 30 KeV and at a dose of $1x10^{15}$ - 10^{16} ions/cm2, with low energy to form a Ge implantation layer 22 in the junction region 13, as shown in FIG. 4A. If the accelerating voltage is 20 KeV, the projected range is about 200 Å, and if the accelerating voltage is 30 KeV, the projected range is about 260 Å. If the accelerating voltage is 10 KeV, the projected range is about 125 Å.

Referring now to FIG. 4B, after the photoresist layer 18 is removed, Ge and Ti are serially deposited on the Ge implantation layer 22 and the insulating layer 15 to form a Ge deposition layer 24 and a Ti deposition layer 17, respectively to a thickness of about 100 - 500 Å at a deposition speed of 10 - 50 Å/sec and at substrate temperatures of 200°C, by a sputtering device.

In the step as shown in FIG. 4C, the above Ge implantation layer 22 comes to be a first resistance control layer 21' of

$Si_{1-x}Ge_x$, according to activation effect by high temperature heating treatment and reaction with the silicon.

The Ge deposition layer 24 on the above Ge implantation layer 22 is remained as a second resistance control layer 23' of Ge. The Ge deposition layer 24 on the upper and side portions of the insulating layer 15 comes to be a first barrier layer 17a of $TiGe_x$ by reacting with Ti. TiN is deposited by sputtering to a thickness of about 500 Å - 1500 Å and serves as a second

barrier layer 17b. After serially deposition of Ti and TiN, heating treatment may be used. Rapid thermal annealing is performed for 20 - 60 seconds at 600°C - 900°C in an ambient of N_2, or the heating treatment is
5 performed for 30 - 60 minutes in an ambient of N_2 at 450°C - 600°C in an ambient of N_2. For reference, the first barrier layer 17a, $TiGe_x$, is formed to have the lowest sheet resistance (20μΩ/cm^2), if the rapid thermal annealing is performed for 20 seconds at 800°C.

10 As described above, the present invention provides a contact structure of hetero-junction of Ge and $Si_{1-x}Ge_x$ whose bandgap is lower than a substrate material to the interface between the metal and semiconductor, which may be usefully applied to low resistance of electronic
15 lines and high reliability in high integrated semiconductor device. The effect of the present invention is shown more obviously by graph of FIG. 6.

FIG. 6 sums up resultants produced by gauging a contact- resistance between the metal and semiconductor
20 by using as a test pattern a contact string having 1200 contact holes.

A resultant of Ge/$Si_{1-x}Ge_x$ hetero-contact structure of this invention is indicated by "A" in the graph. "B" is a contact structure to which only Ge is ion-
25 implanted, and "C" is a conventional contact structure to which Ge is not ion-implanted. The size of each contact hole is 0.5μm and the semiconductor layer is a

P+ type area to which BF_2 is ion-implanted at a dose of $1x10^{15}$. The heating treatment is performed for 120 minutes at 850°C at an ambient of N_2. According to the contact structure of this invention, the contact
5 resistance is reduced about twice.

While this invention has been described in connection with what is presently considered to be the most practical and preferred embodiments, it is to be understood that the invention is not limited to the
10 disclosed embodiments, but, on the contrary, it is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

WHAT IS CLAIMED IS:

1. An ohmic contact structure of a semiconductor device, comprising:

a junction region doped with an impurity on a semiconductor substrate;

a first resistance control layer having a reduced resistivity and selectively provided on a contact hole over the junction region with a material of a hetero-junction structure whose work function is lower than a substrate material;

a second resistance control layer having a reduced resistivity provided with a material whose work function is lower than a substrate material on said first resistance control layer; and

a conductive layer forming a wiring electrode provided on the second resistance control layer.

2. The ohmic contact structure according to claim 1, wherein said first resistance control layer is formed of $Si_{1-x}Ge_x$.

3. The ohmic contact structure according to claim 1, said second resistance control layer is formed of Ge.

4. The ohmic contact structure according to claim 1, further comprising at least one barrier layer inserted between the conductive layer and second resistance control layer in order to prevent reaction between the junction region and conductive layer.

5. The ohmic contact structure according to claim 2, wherein

said x is in a range of $0 < x < 1$.

6. A method for making a semiconductor device comprising the steps of:

forming a junction region implanted with an impurity on a predetermined portion of a semiconductor substrate;

forming an insulating layer on said semiconductor substrate and forming a contact hole by opening the insulating layer in order to expose a part of the junction region;

forming a first resistance control layer on said contact hole;

forming a second resistance control layer on said first resistance control on said first resistance control layer;

forming at least one barrier layer on said second resistance control layer and insulating layer and performing a heating treatment thereon; and

forming a conductive layer on said barrier layer.

7. The method according to claim 6, wherein said step for forming said first resistance control layer is performed by ion-implantation.

8. The method according to claim 6, wherein said step for forming said first resistance control layer is performed by an epitaxial process.

9. The method according to claim 6, wherein said step for forming said first resistance control layer is

performed by a chemical vapor deposition process.

10. A method for making a contact hole of a semiconductor device comprising the steps of:

forming a junction region implanted with an
5 impurity on a predetermined portion of a semiconductor substrate;

forming an insulating layer on said semiconductor substrate and forming a contact hole by opening said insulating layer in order to expose a part of the
10 junction region;

ion-implanting Ge within the junction region through said contact hole;

serially depositing Ge and metal over said contact hole and insulating layer;

15 performing a heating treatment to form a first resistance control layer, a second resistance control layer and at least one barrier layer, as a reaction result among silicon, Ge and metal of said junction region; and

20 forming a conductive layer on said barrier layer.

11. An ohmic contact structure of a semiconductor device, comprising:

a semiconductor substrate;

a junction region doped with an impurity on said semiconductor substrate;

a first resistance control layer having a reduced resistivity and selectively provided on a contact hole
5 over said junction region with a material of a heterojunction structure whose band gap is narrower than that of a material of said semiconductor substrate;

a second resistance control layer formed of Ge,
10 having a reduced resistivity, and having a work function which is lower than that of said first resistance control layer; and

a conductive layer forming a wiring electrode provided on said second resistance control layer.

15 12. The ohmic contact structure according to claim 11, wherein:

said first resistance control layer is formed of Si_{1-x} Ge_x.

13. The ohmic contact structure according to
20 claim 12, wherein:

said x of said Si_{1-x} Ge_x is within a range of $0<x<1$.

14. The ohmic contact structure according to claim 11, further comprising:

at least one barrier layer inserted between said conductive layer and second resistance control layer, said at least one barrier layer preventing a reaction between said junction region and said conductive
5 layer.

FIG.1(Prior Art)

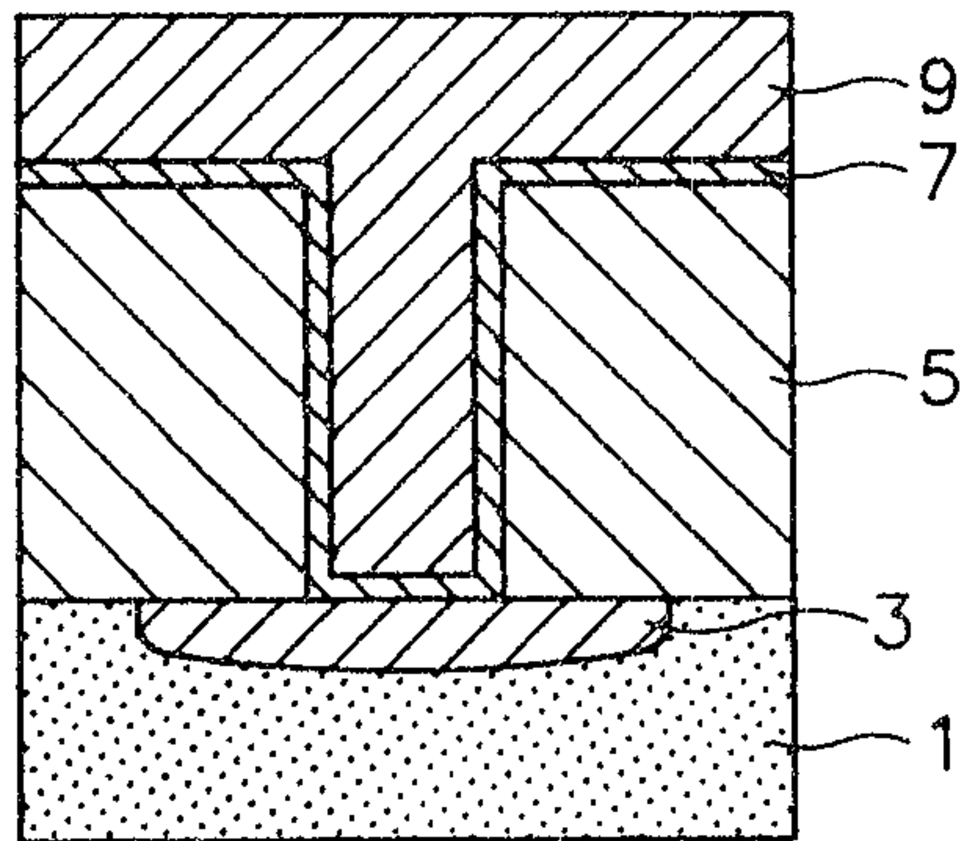


FIG.2(Prior Art)

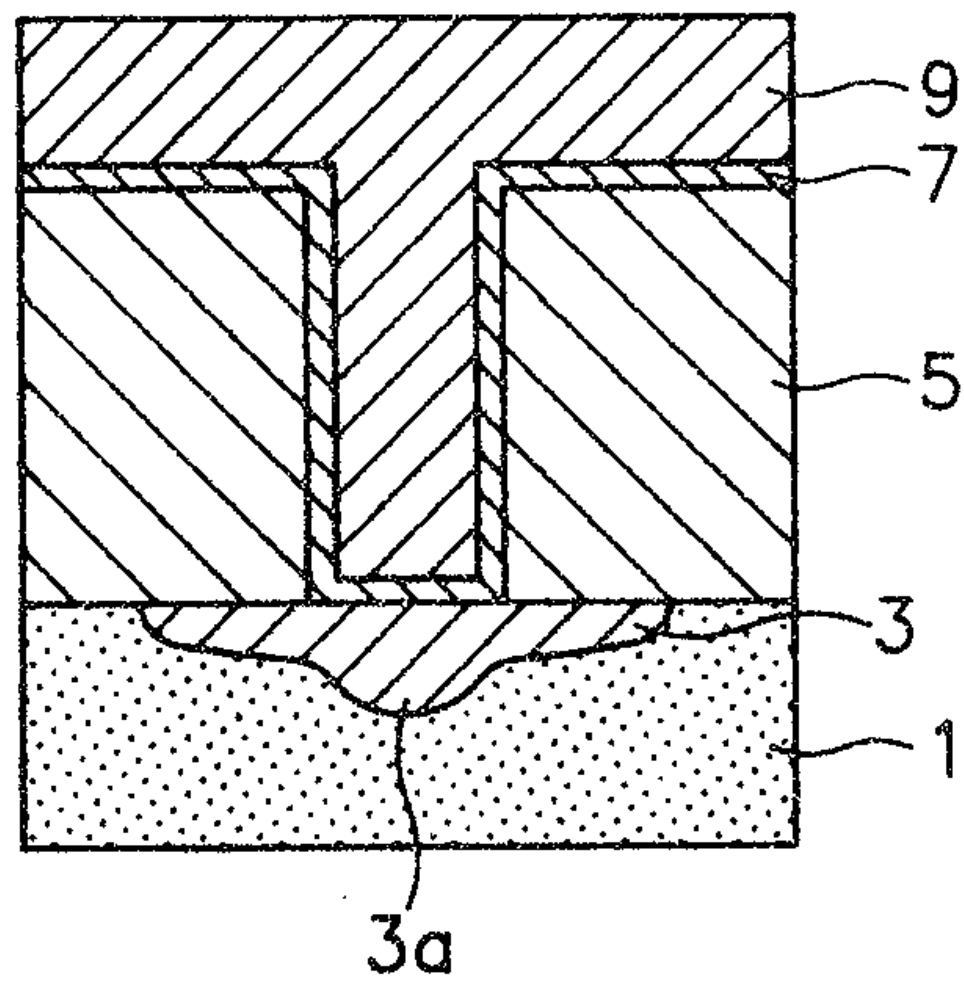


FIG.3A

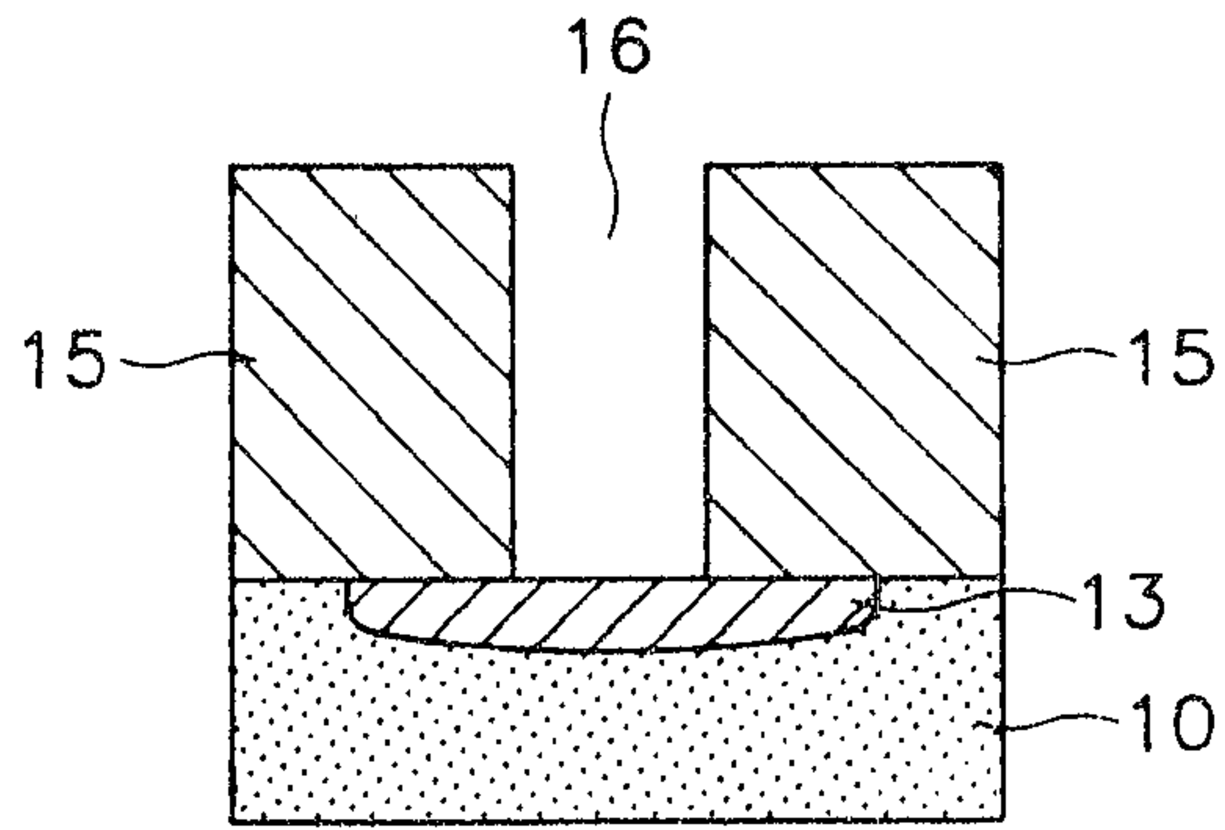


FIG.3B

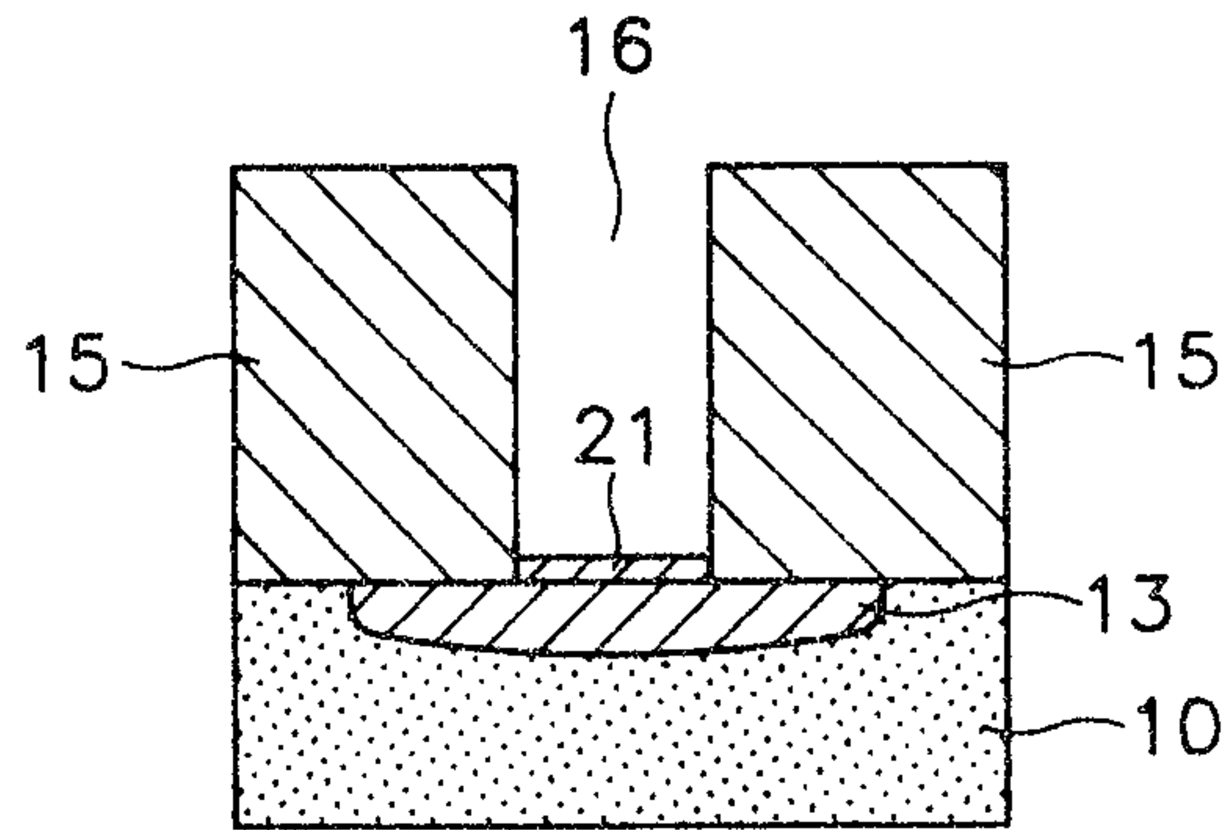


FIG.3C

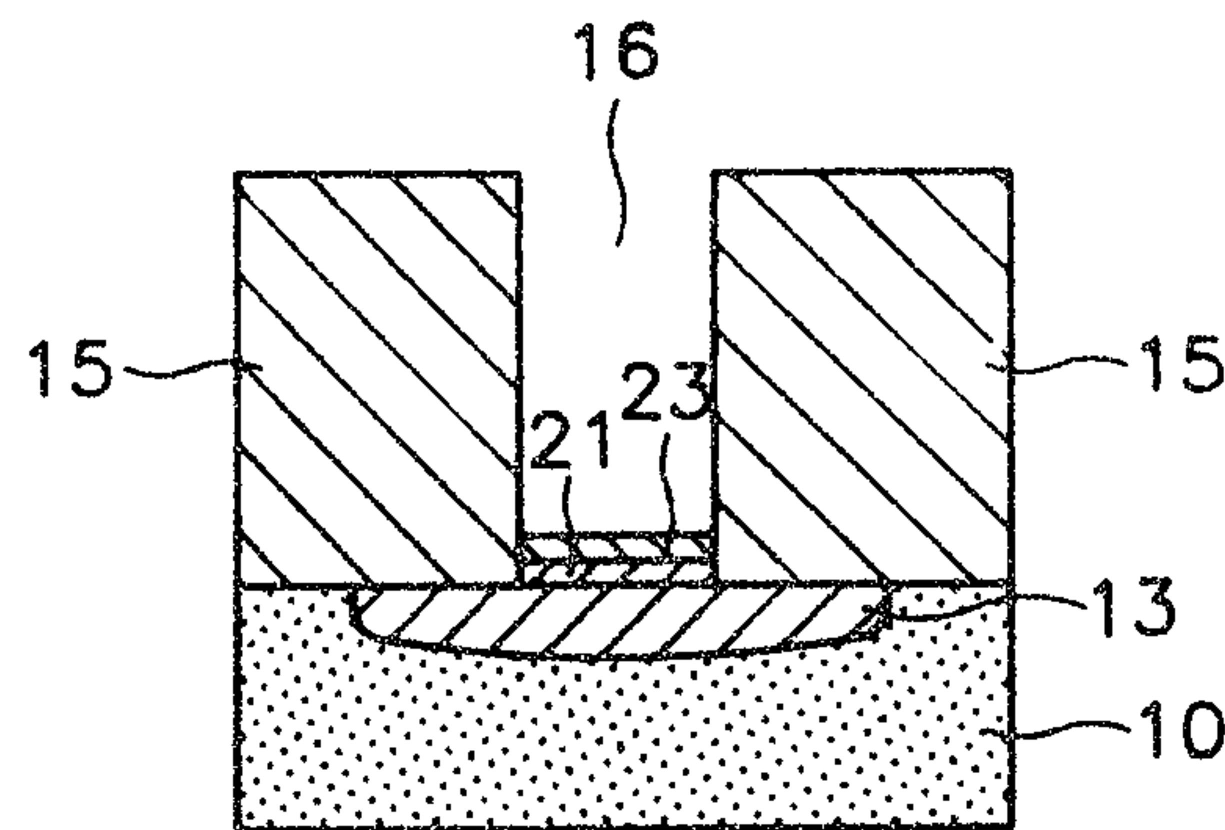


FIG.3D

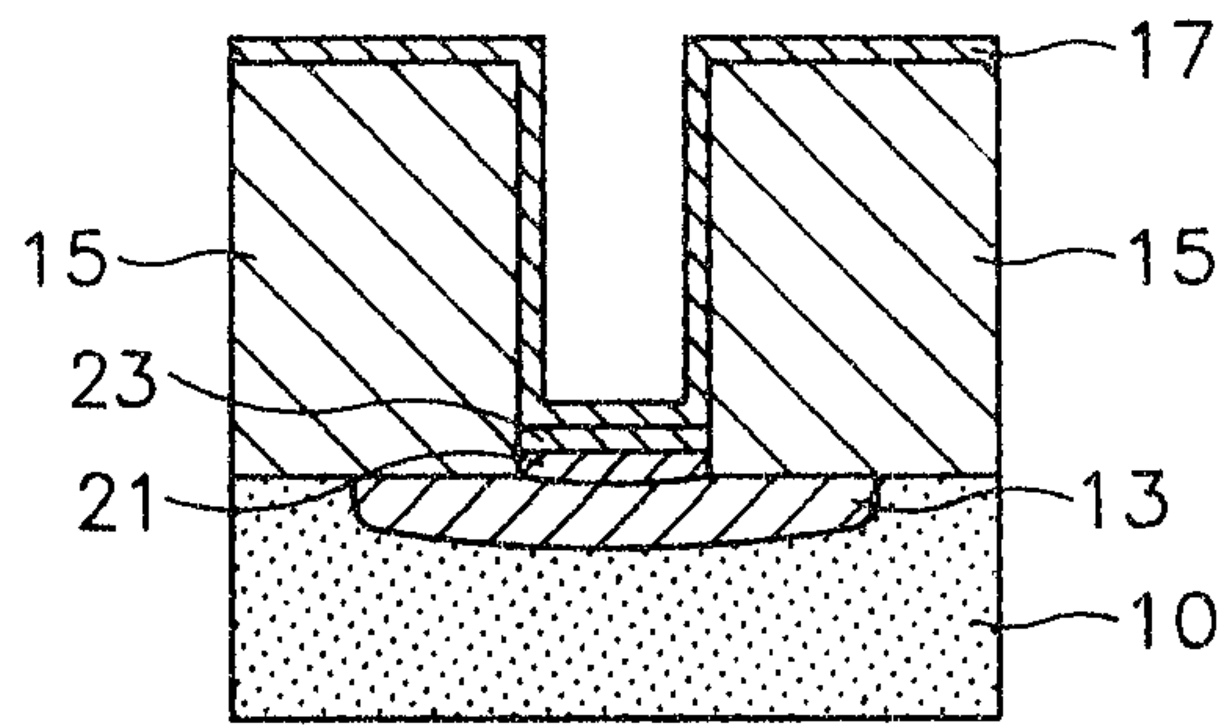


FIG.3E

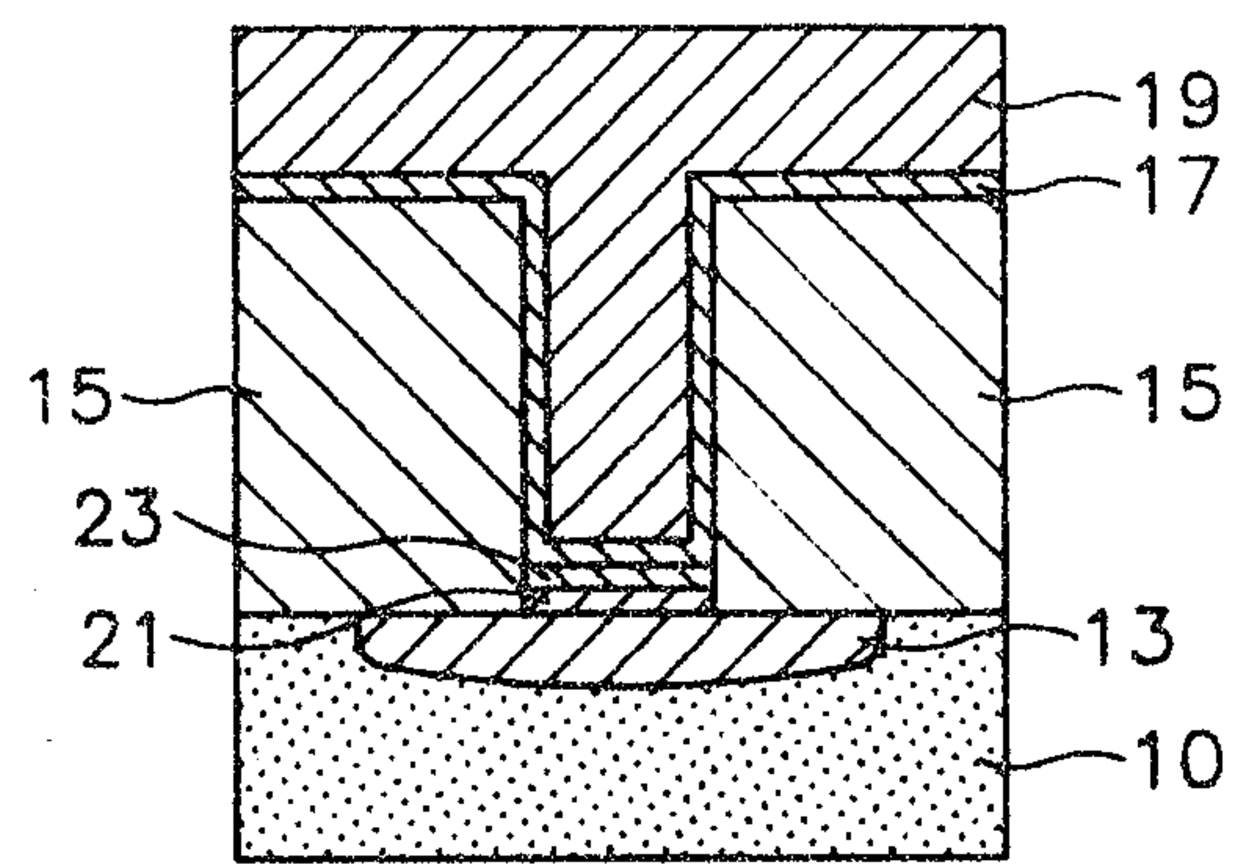


FIG.4A

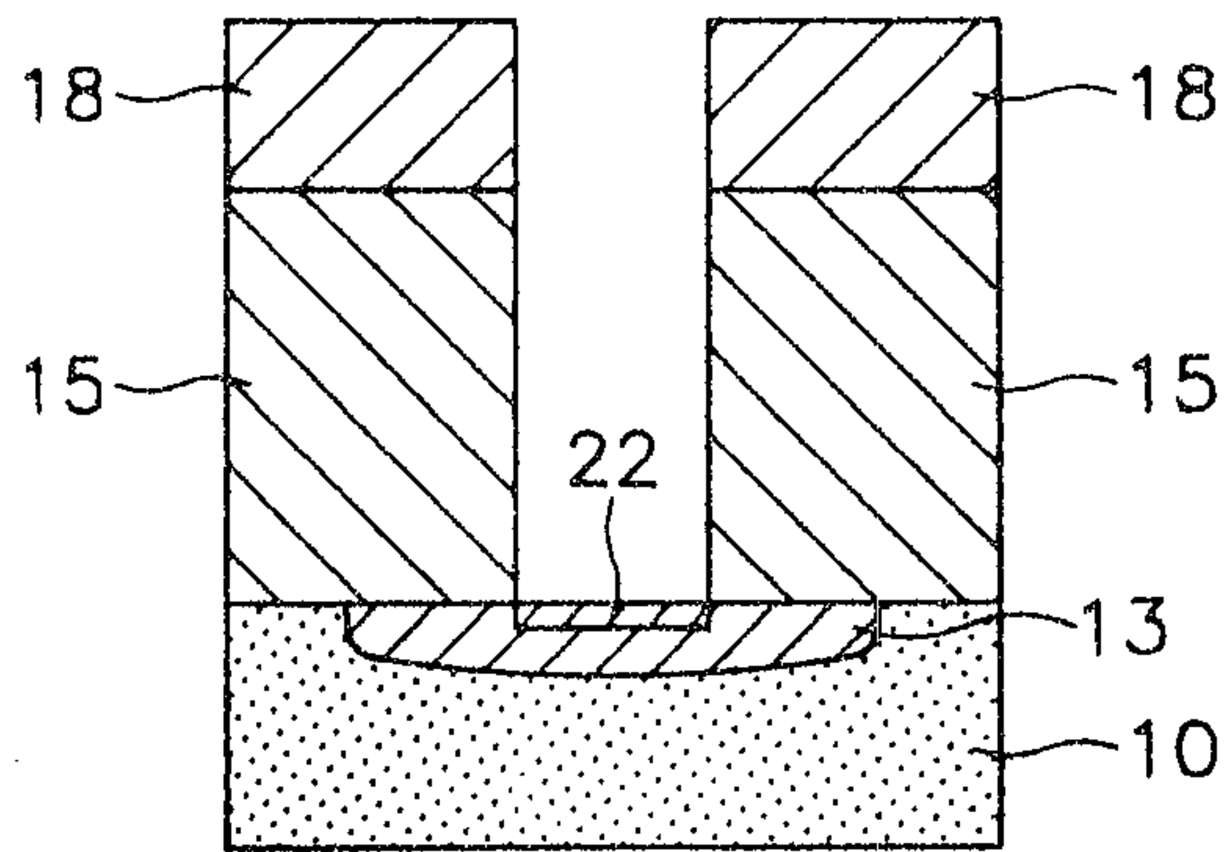


FIG.4B

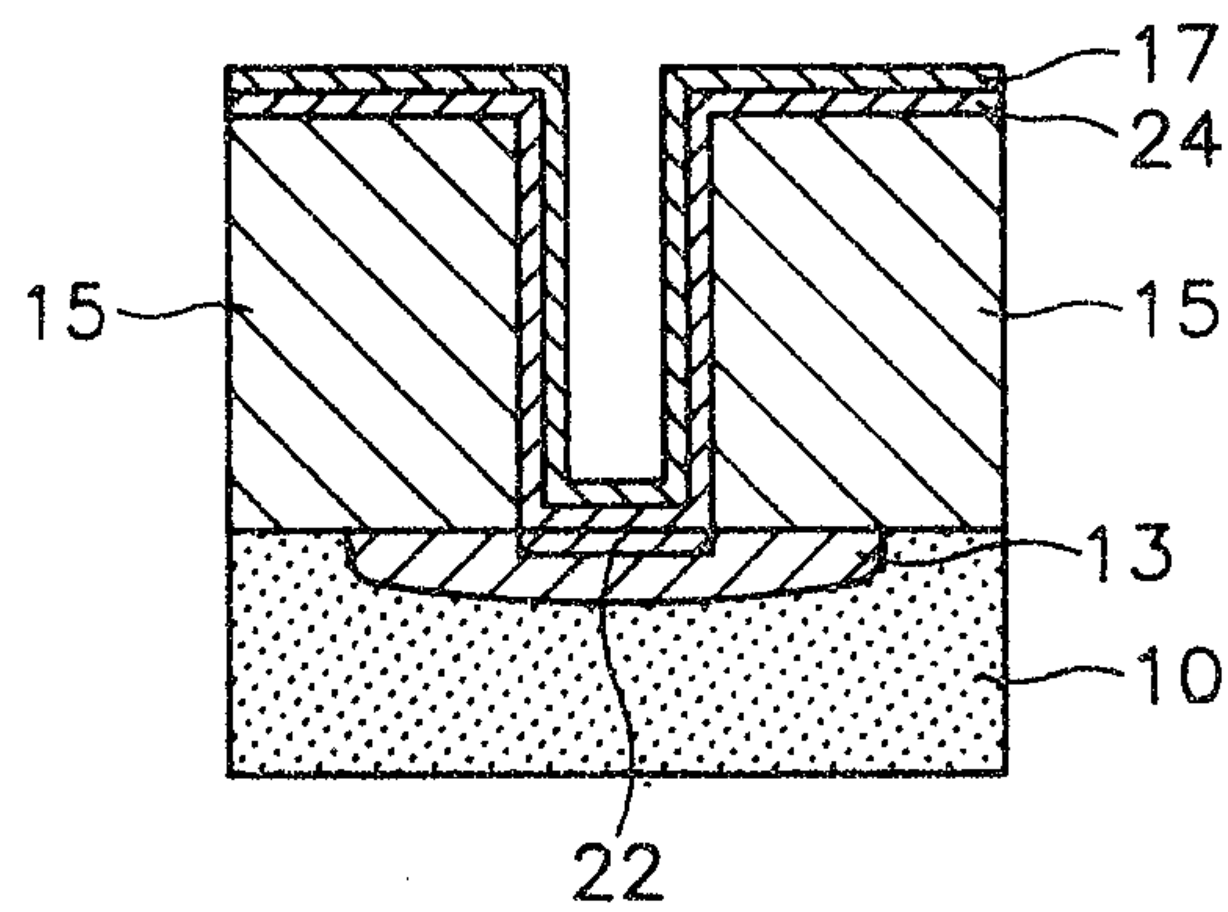


FIG.4C

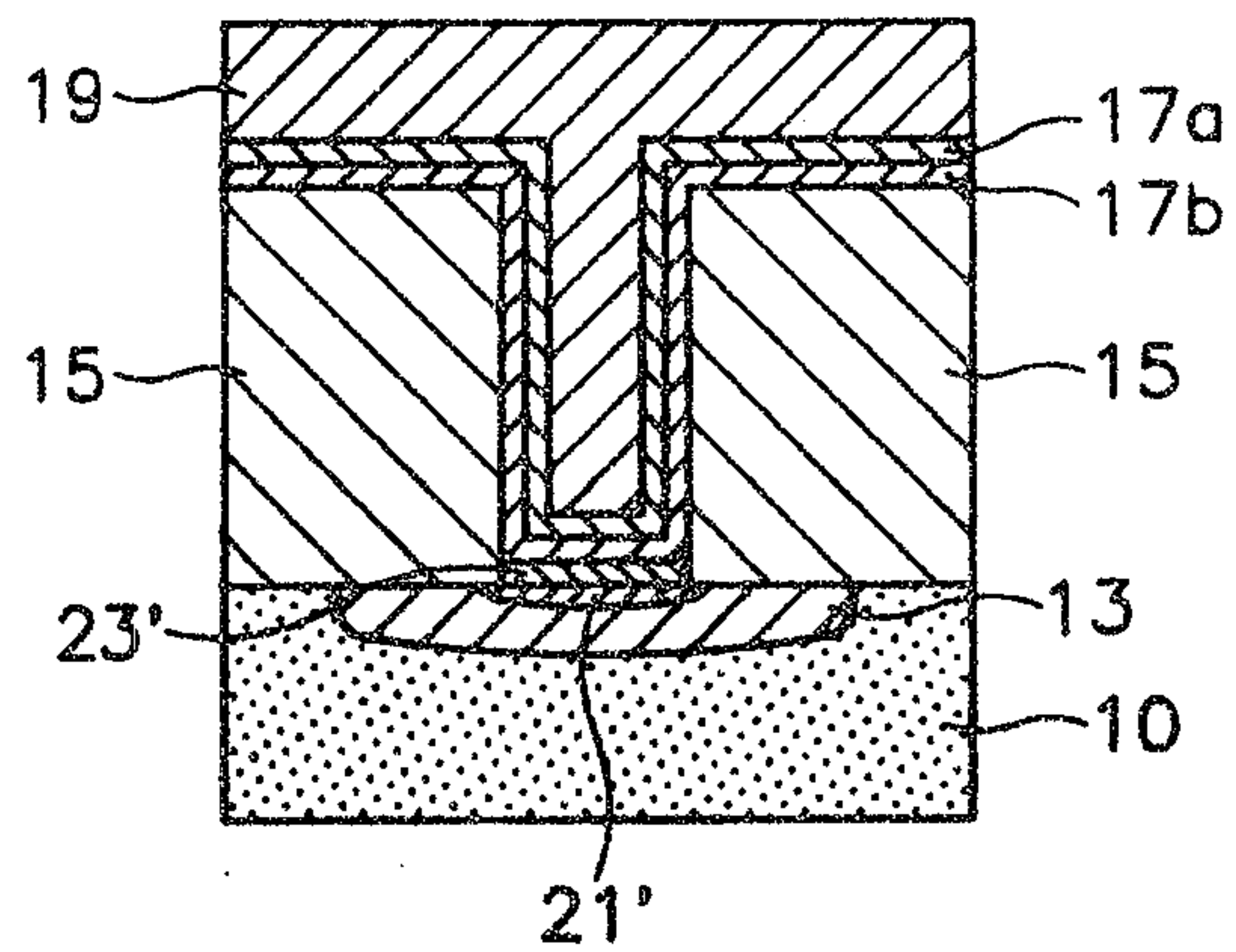


FIG.5

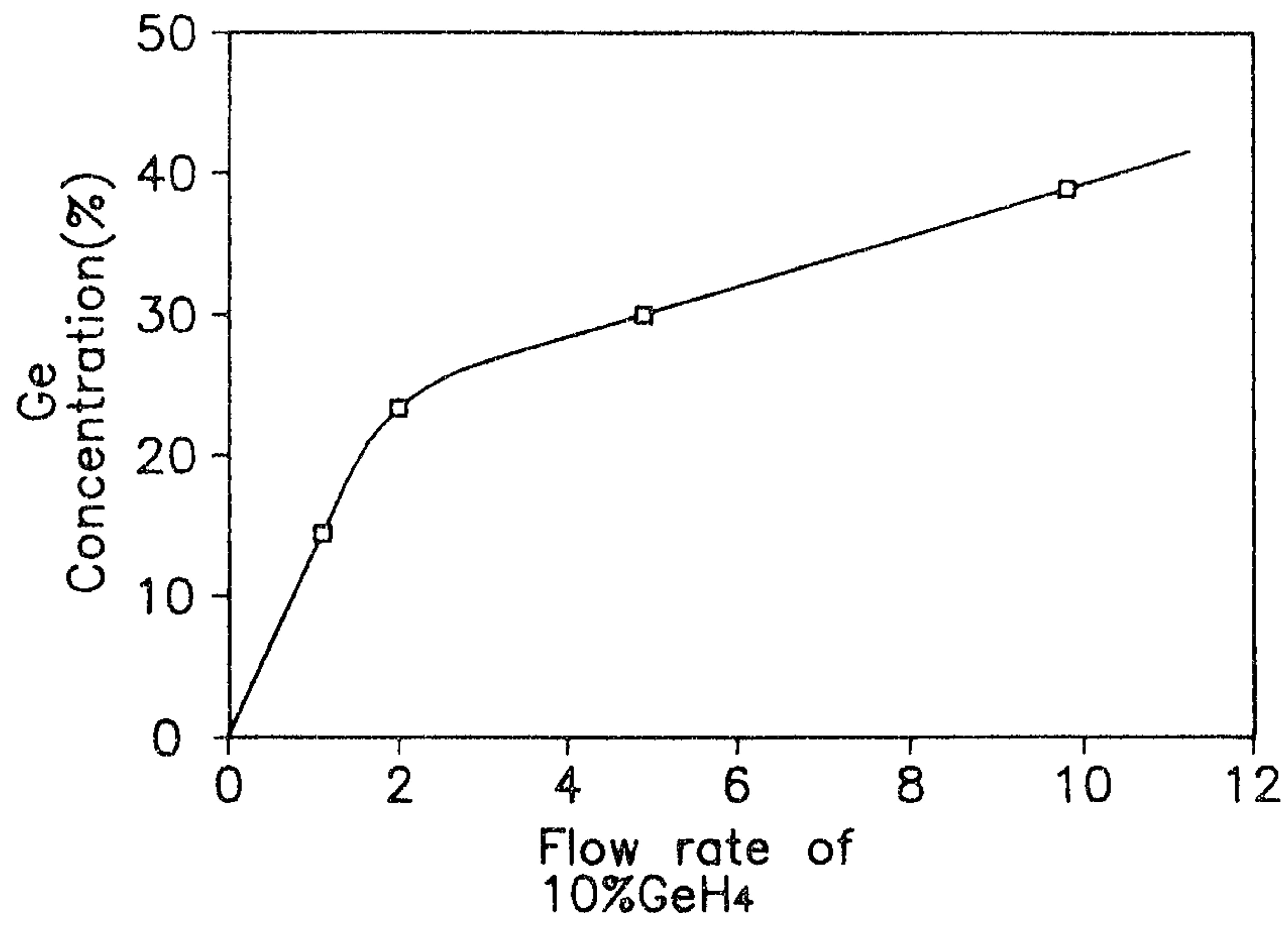
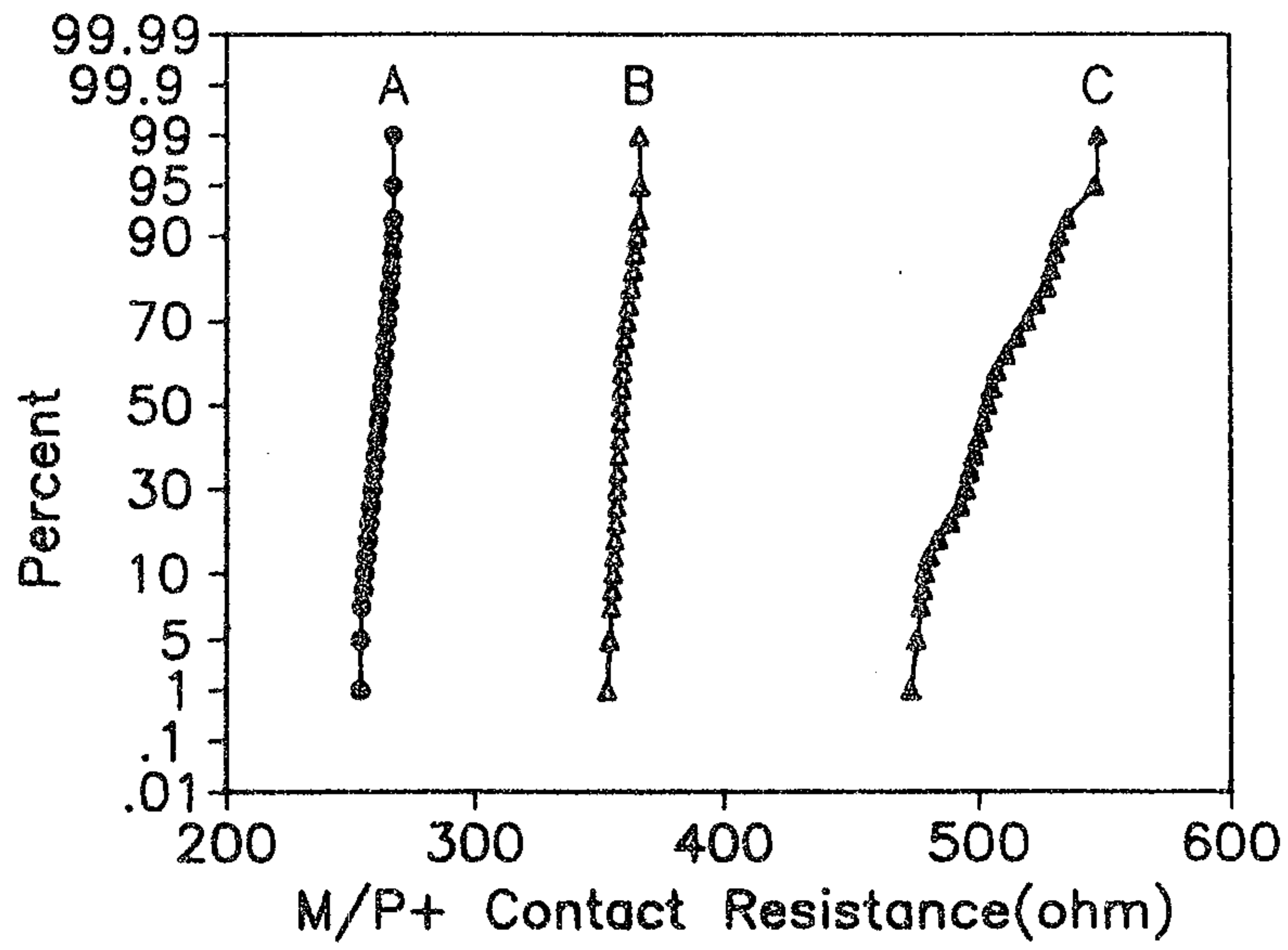
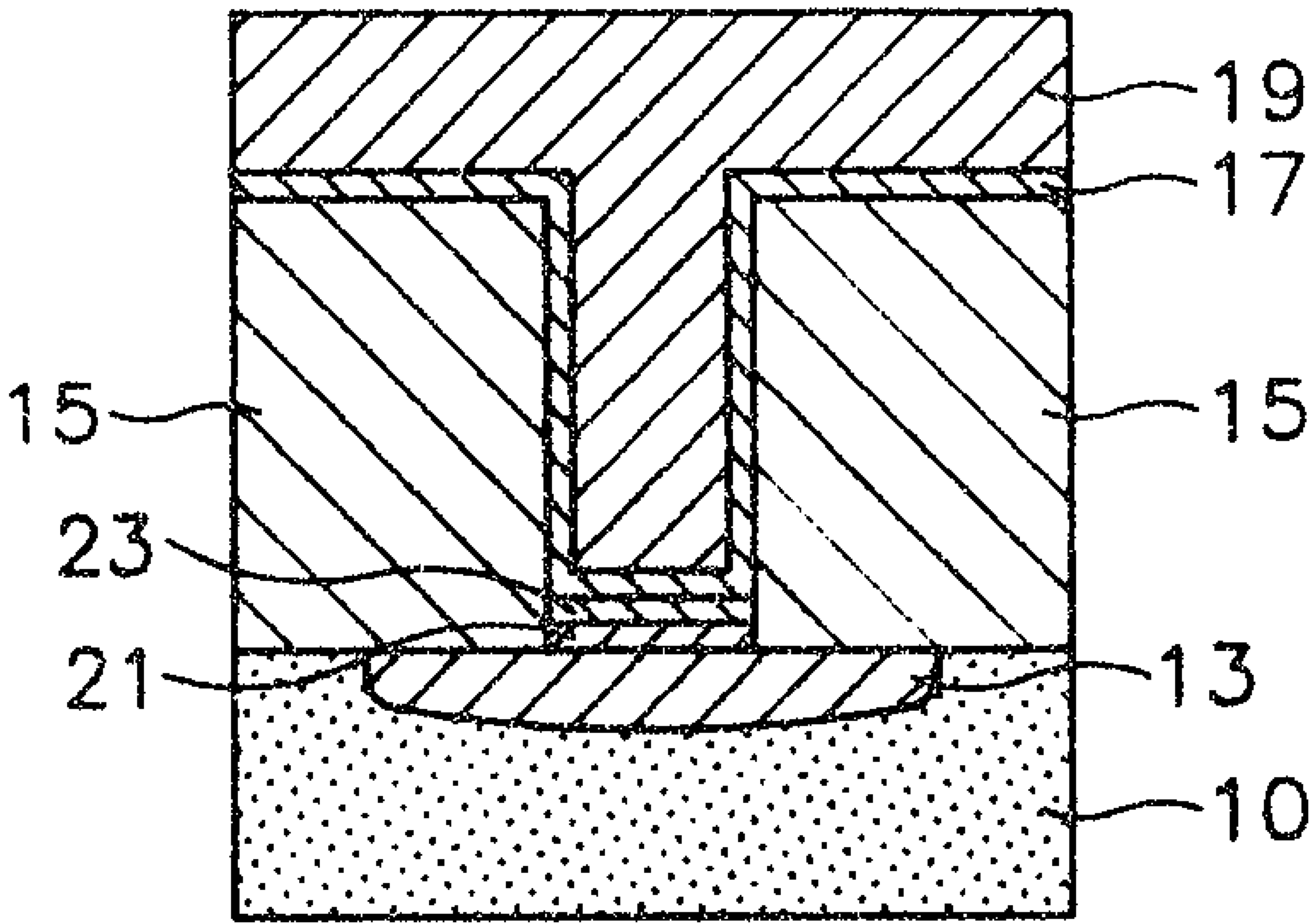


FIG.6

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