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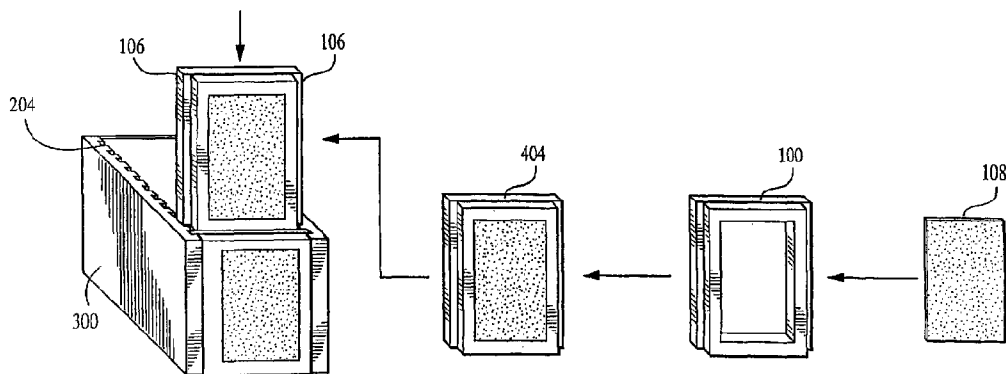
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(54) Title: HIGH DENSITY 3-D INTEGRATED CIRCUIT PACKAGE



(57) Abstract: A slotted file is created by connecting two side walls and a back wall. The side walls have etched grooves facing directly across from each other. The platelet has flanges that fit into the grooves. In one embodiment, a completed cube is formed when the platelets fill the slotted file.

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APPLICATION FOR UNITED STATES PATENT

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Title: **HIGH DENSITY 3-D INTEGRATED CIRCUIT PACKAGE**

15

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High Density 3-D Integrated Circuit Package

GOVERNMENT RIGHTS

The United States Government has acquired certain rights in this invention
5 pursuant to Contract No. DASG60-90-C-0136 awarded by the U.S. Army.

FIELD

The present invention relates generally to circuit packages, and more
particularly, relates to three-dimensional circuit packages that provide stacking for
10 semiconductor platelets.

BACKGROUND

Three-dimensional integrated circuits are employed in applications in which
space is a critical design factor. As the demand for more functionality in less space
15 increases, so does the number of designs using three-dimensional packaging. In
addition to the benefit of reducing space, these designs may also realize higher speeds
because interconnects between circuit components may be shorter.

Memory stacking was the first application of three-dimensional packaging, but
now applications range from stacking memory modules to stacking entire systems.
20 Different layers in the stack may have different functionalities. For example, one layer
may be a memory layer and another may be a logic layer. It is also possible that the
different layers in the stack could have different dimensions.

These applications may require the precise stacking of very thin platelets into
cubes. Platelets may consist of a semiconductor chip placed in a chip carrier. The
25 platelets themselves may be less than 5 mils thick and there may be as many as sixty
platelets stacked in one cube. It is critical that the spacing between the platelets is held
to a very tight tolerance and that the platelets are not damaged during the stacking
procedure.

Typically, the platelets are held in the cubical stack by a very thin layer of epoxy
30 resin between each layer. This epoxy layer may be less than one micron thick. Other
bonding materials, such as silicone rubber or eutectic solder alloy, may also be
employed. The required spacing dimensions may be maintained by using an apparatus

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with a calibrated compression arm that applies pressure to the stack while the epoxy is setting. A typical amount of pressure may be ten Newtons of force. With this arrangement, only the overall cube dimensions can be maintained, and great care must be taken to prevent cracking the delicate platelets by excessive pressure. The critical layer to
5 layer spacing is thus a derived property and is based upon the uniformity of the thickness and pressure-flow characteristics of the adhesive layer.

It would be desirable to provide a stacking method that provides a very tight spacing tolerance between the platelets and that minimizes damage to the platelets during the stacking process. The invention addresses current limitations and makes the critical
10 spacing a directly controlled property resulting in much higher accuracy potential with a relative independence of the adhesive layers.

In one aspect the present invention provides the system for stacking platelets, comprising in combination:

a slotted file;
15 a plurality of platelets which fit into a slotted file, wherein each of the platelets includes a semiconductor chip placed into a chip carrier so that the semiconductor chip contacts a plurality of electrodes located in the chip carrier, and wherein the platelets are stacked in the slotted file; and

epoxy sealing the plurality of platelets into the slotted file to form a three-
20 dimensional integrated circuit package.

In another aspect the present invention provides a method for stacking platelets, comprising in combination:

etching grooves into a wall material, wherein at least two side walls with a plurality of grooves and at least one back wall without the grooves is formed;
25 connecting the at least two side walls and the at least one back wall to form a slotted file;

inserting a plurality of platelets into the slotted file, wherein each of the platelets includes a semiconductor chip placed into a chip carrier so that the semiconductor chip contacts a plurality of electrodes located in the chip carrier; and

30 immersing the slotted file with the inserted platelets in epoxy to form a three-dimensional integrated circuit package.

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SUMMARY

In accordance with an embodiment of the invention the slotted file has at least three walls, typically composed of silicon.

5 The slotted file typically has at least two side walls and at least one back wall. In this case the at least two side walls may be etched with a plurality of grooves. The depth of the plurality of grooves is generally sufficient to hold each of the plurality of platelets. The spacing between the plurality of grooves may be determined based on a platelet thickness or based on a number of platelets in the three-dimensional integrated circuit package or based on an allocated space limitation.

10 In the embodiment described above the at least one back wall may be connected to an end of each of the at least two side walls to form a "U" shape. Here the plurality of grooves on the at least two side walls typically face directly across from each other.

The chip carrier generally has a floor and a frame. The floor and the frame may be composed of a ceramic material. Typically, the floor protrudes past at least two edges of the frame forming flanges. The flanges generally fit into the plurality of grooves in the at least two side walls of the slotted file.

The floor may include the plurality of electrodes referred to above.

The semiconductor chip is usually placed face down on the floor contacting the plurality of electrodes.

20

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments are described below in conjunction with the appended non-limiting drawing figures, wherein like reference numerals refer to like elements in the various figures, and wherein:

25 Fig. 1 is an illustration of an exemplary embodiment of a chip carrier and a semiconductor chip;

Fig. 2 is an illustration of an exemplary embodiment of a slotted file wall;

Fig. 3 is an illustration of an exemplary embodiment of a slotted file;

Fig. 4 is an illustration of the stacking process in an exemplary embodiment; and

30 Fig. 5 is an illustration of an exemplary embodiment of a completed cube.

DETAILED DESCRIPTION

Fig. 1 is an illustration of an exemplary embodiment of a chip carrier 100 and a semiconductor chip 108. The chip carrier 100 is composed of a floor 102 and a frame 104. The chip carrier 100 may be designed to hold the semiconductor chip 108. The floor 102 may be a three-dimensional rectangle having a length, a width, and a thickness. The frame 104 may be a three-dimensional rectangle with a smaller three-dimensional rectangular center removed. The frame 104 has a length, a width, and a thickness. The frame 104 is substantially the same length as the floor 102; however, the frame 104 is not as wide as the floor 102.

The frame 104 is positioned in the center of the floor 102. Because the width of the floor 102 is greater than the width of the frame 104, the floor 102 protrudes past the edges of the frame 104 forming two flanges 106, one on either side of the frame 104.

In an exemplary embodiment both the floor 102 and the frame 104 are formed with ceramic materials, but other materials such as metal and plastic may be used. The floor 102 contains a plurality of electrodes. The frame 104 has interior dimensions slightly larger than those of the semiconductor chip 108. The interior dimensions of the frame 104 may vary to accommodate a variety of different semiconductor chip 108 dimensions. The semiconductor chip 108 may be placed in the frame 104 face down on the floor 102 contacting the plurality of electrodes at the appropriate circuit interfaces to form a platelet 404 (see Fig. 4).

Fig. 2 is an illustration of a slotted file wall 200. A slotted file wall 200 consists of a wall material 202 and may include a plurality of grooves 204. The wall material 202 may be a three-dimensional rectangle having a length, a width, and a thickness. Silicon is the preferred wall material 202 in an exemplary embodiment, but other materials, such as gallium arsenide, may be used.

The wall material 202 may be etched with grooves 204 deep enough to receive the flanges 106 of a chip carrier 100 and less than the thickness of the wall material 202. For example, the depth of the grooves may be less than 10 mils thick. The spacing between the grooves 204 may be selected based on design requirements, such as the thickness of the platelets 404, the number of platelets 404 in a completed cube 500, and an allocated space limitation (see Fig. 5). For example, the allocated space limitation may be the size of an infrared sensor that contains a completed cube 500. Any etching

technique that is compatible with the chosen wall material 202 may be used. A standard wet etch or plasma etch process that can produce a substantially straight wall trench may be suitable for this purpose.

Fig. 3 is an illustration of an exemplary embodiment of a slotted file 300. A
5 slotted file 300 may consist of two side walls 302 and a back wall 304. Other
embodiments may have additional walls. For example, a front wall, a top, or a bottom
may also be part of the slotted file 300. The two side walls 302 may be etched with
grooves 204. The back wall 304 may be a section of the wall material 202 that has not
10 been etched with grooves 204. The dimensions of the slotted file 300 are based on the
size of the platelets 404, the number of platelets 404 that will be placed in the slotted
file 300, and the spacing between the platelets 404 in the slotted file 300 (see Fig. 4).

The back wall 304 may be connected to an end of each of the two side walls 302
to form a "U" shape. The grooves 204 on the two side walls 302 face directly across
from each other. The three walls 302, 304 may be joined together by conventional
15 methods to form a slotted file 300. For example, an etching process in which tabs and
holes are created to join the walls may be employed.

Fig. 4 is an illustration of the stacking process in an exemplary embodiment. The
semiconductor chip 108 is placed into the chip carrier 100 to form a platelet 404. For
example, the platelet 404 may be less than 5 mils thick. Platelets 404 are then fitted into
20 the slotted file 300 by inserting the flanges 106 into the opposing grooves 204. This
may be accomplished by placing the platelet 404 in the vicinity of the opposing grooves
204 and using a shake table to slide the platelet into the opposing grooves 204. The
spacing between the platelets 404 is maintained by the groove interval and no pressure
is required to hold the chips in place because of the rigidity of the slotted file 300.

Fig. 5 illustrates the completed cube 500 after the platelets 404 have been
25 inserted into the slotted file 300. By using a slotted cube arrangement, the platelets 400
are uniformly stacked without damage. There may be, for example, two hundred
platelets 404 in the completed cube 500. The completed cube 500 may be made
permanent by immersing the assembly in epoxy. To enable the epoxy to flow between
30 substantially all the layers, the completed cube 500 may be placed in a vacuum
chamber. Applying a hard vacuum to the chamber may force the epoxy through
substantially all the cracks and layers.

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The reference in this specification to any prior publication (or information derived from it), or to any matter which is known, is not, and should not be taken as an acknowledgment or admission or any form of suggestion that that prior publication (or
5 information derived from it) or known matter forms part of the common general knowledge in the field of endeavour to which this specification relates.

Throughout this specification and the claims which follow, unless the context requires otherwise, the word "comprise", and variations such as "comprises" and "comprising", will be understood to imply the inclusion of a stated integer or step or group
10 of integers or steps but not the exclusion of any other integer or step or group of integers or steps.

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THE CLAIMS DEFINING THE INVENTION ARE AS FOLLOWS:

1. A system for stacking platelets, comprising in combination:
 - a slotted file;
 - a plurality of platelets which fit into the slotted file, wherein each of the platelets
- 5 includes a semiconductor chip placed into a chip carrier so that the semiconductor chip contacts a plurality of electrodes located in the chip carrier, and wherein the platelets are stacked in the slotted file; and
 - epoxy sealing the plurality of platelets into the slotted file to form a three-dimensional integrated circuit package.
- 10
2. The system of claim 1, wherein the slotted file has at least three walls.
3. The system of claim 2, wherein the at least three walls are composed of silicon.
- 15 4. The system of claim 2, wherein the slotted file has at least two side walls and at least one back wall.
5. The system of claim 4, wherein the at least two side walls have been etched with a plurality of grooves.
- 20
6. The system of claim 5, wherein a depth of the plurality of grooves is sufficient to hold each of the plurality of platelets.
7. The system of claim 5, wherein a spacing between the plurality of grooves is
- 25 determined based on a platelet thickness.
8. The system of claim 5, wherein the spacing between the plurality of grooves is determined based on a number platelets in the three-dimensional integrated circuit package.
- 30
9. The system of claim 5, wherein the spacing between the plurality of grooves is determined based on an allocated space limitation.

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10. The system of claim 4, wherein the at least one back wall is connected to an end of each of the at least two side walls to form a "U" shape.
11. The system of claim 10, wherein the plurality of grooves on the at least two side walls face directly across from each other.
12. The system of claim 1, wherein the chip carrier has a floor and a frame.
13. The system of claim 12, wherein the floor and the frame are composed of a ceramic material.
14. The system of claim 12, wherein the floor protrudes past at least two edges of the frame forming flanges.
15. The system of claim 14, wherein the flanges fit into the plurality of grooves in the at least two side walls of the slotted file.
16. The system of claim 12, wherein the floor includes the plurality of electrodes.
17. The system of claim 16, wherein the semiconductor chip is placed face down on the floor contacting the plurality of electrodes.
18. A method for stacking platelets, comprising in combination:
etching grooves into a wall material, wherein at least two side walls with a plurality of grooves and at least one back wall without the grooves is formed;
connecting the at least two side walls and the at least one back wall to form a slotted file;
inserting a plurality of platelets into the slotted file, wherein each of the platelets includes a semiconductor chip placed into a chip carrier so that the semiconductor chip contacts a plurality of electrodes located in the chip carrier; and
immersing the slotted file with the inserted platelets in epoxy to form a three-dimensional integrated circuit package.

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19. The method of claim 18, wherein the wall material is silicon.

20. The method of claim 18, wherein a depth of the plurality of grooves is sufficient to hold each of the plurality of platelets.

5

21. The method of claim 18, wherein a spacing between the plurality of grooves is determined based on a platelet thickness.

22. The method of claim 18, wherein the spacing between the plurality of grooves is
10 determined based on a number of platelets in the completed cube.

23. The method of claim 18, wherein the spacing between the plurality of grooves is determined based on an allocated space limitation.

15 24. The method of claim 18, wherein each of the plurality of platelets has at least two flanges that fit into the plurality of grooves.

25. A system for stacking platelets substantially as hereinbefore described with reference to the Figures.

20

26. A method for stacking platelets substantially as hereinbefore described with reference to the Figures.

DATED this 15th day of June, 2006

25 **Honeywell International, Inc.**

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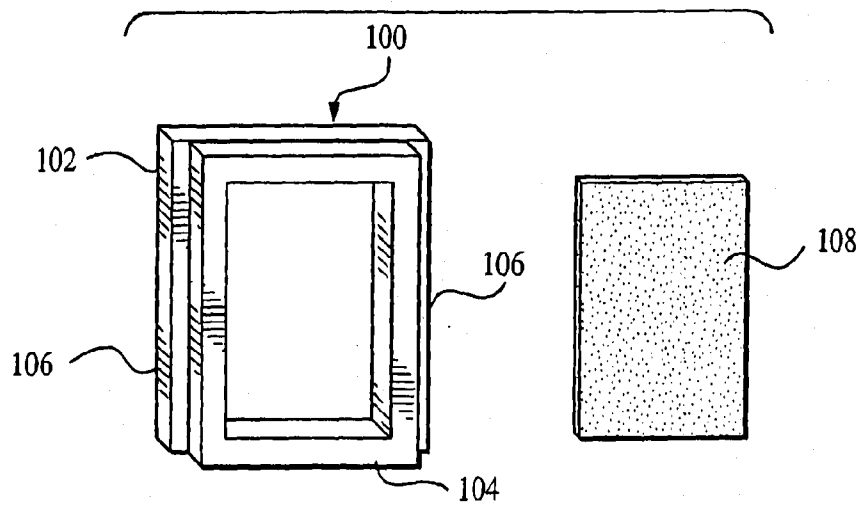


FIG. 1

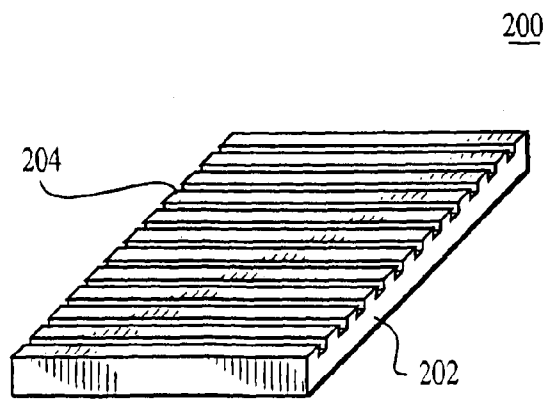


FIG. 2

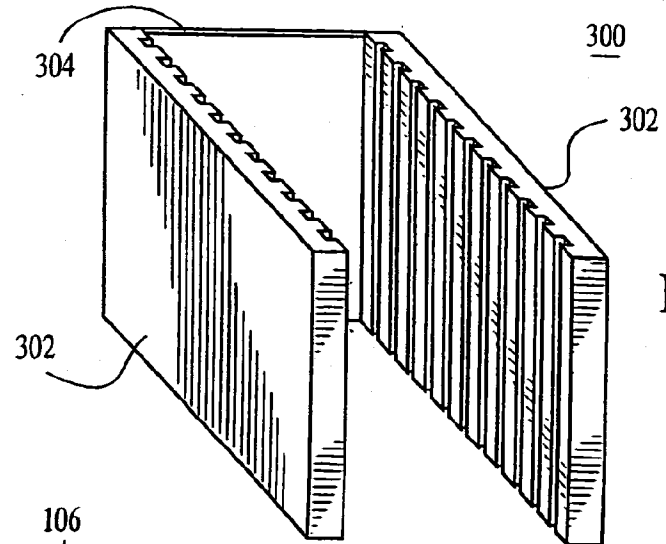


FIG. 3

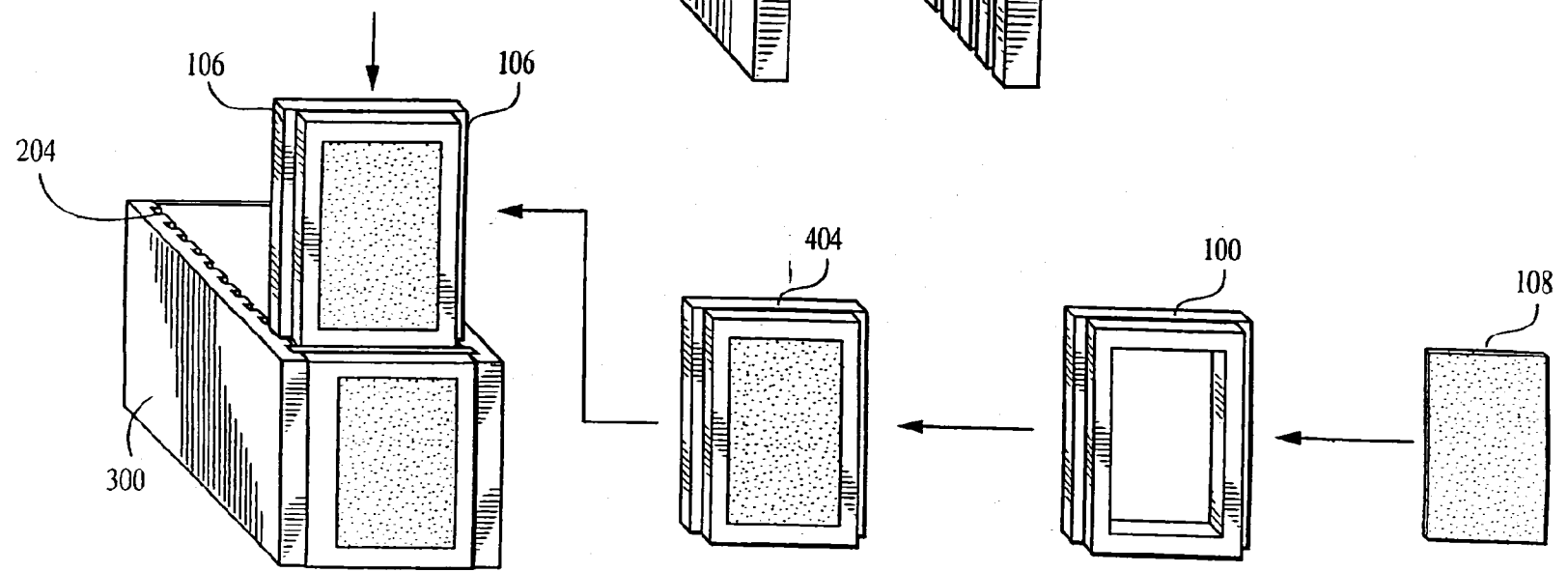


FIG. 4

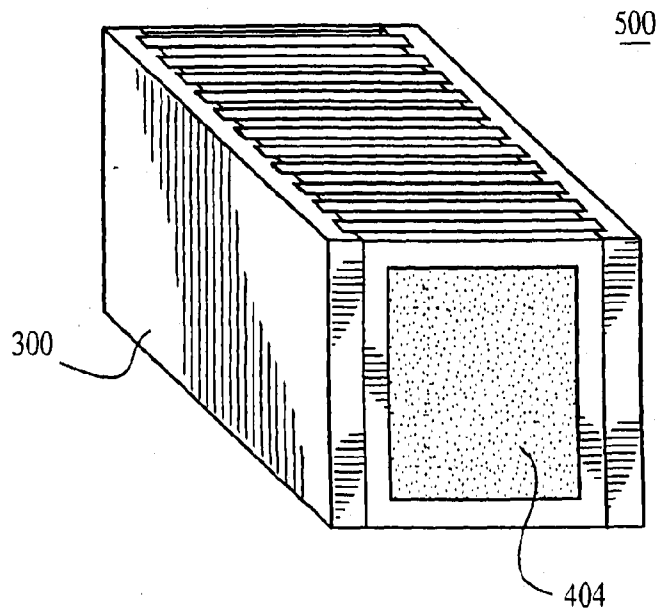


FIG. 5