(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
7 January 2010 (07.01.2010)

PCT

(10) International Publication Number
WO 2010/002516 A2

(51) International Patent Classification:
H01L 21/20 (2006.01)

(21) International Application Number:
PCT/US2009/044825

(22) International Filing Date:
21 May 2009 (21.05.2009)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
0803697 30 June 2008 (30.06.2008) FR
61/093,896 3 September 2008 (03.09.2008) US

(71) Applicant (*for all designated States except US*): **S.O.I.TEC SILICON ON INSULATOR TECHNOLOGIES** [FR/FR]; Parc Technologique des Fontaines, F-38190 Bernin (FR).

(72) Inventors; and
(75) Inventors/Applicants (*for US only*): **NGUYEN, Bich-yen** [US/US]; 110 S. Laurelwood Drive, Austin, TX 78733 (US). **MAZURE, Carlos** [FR/FR]; 143 Chemin du Bas Bernin, Residence Cidex 64a, F-38190 Bernin (FR).

(74) Agents: **FANUCCI, Allan, A.** @ et al.; Winston & Strawn LLP, Patent Department, 1700 K Street, N.W., Washington, DC 20006-3817 (US).

(81) Designated States (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *of inventorship (Rule 4.17(iv))*

Published:
— *without international search report and to be republished upon receipt of that report (Rule 48.2(g))*

(54) **Title**: LOW-COST DOUBLE STRUCTURE SUBSTRATES AND METHODS FOR THEIR MANUFACTURE

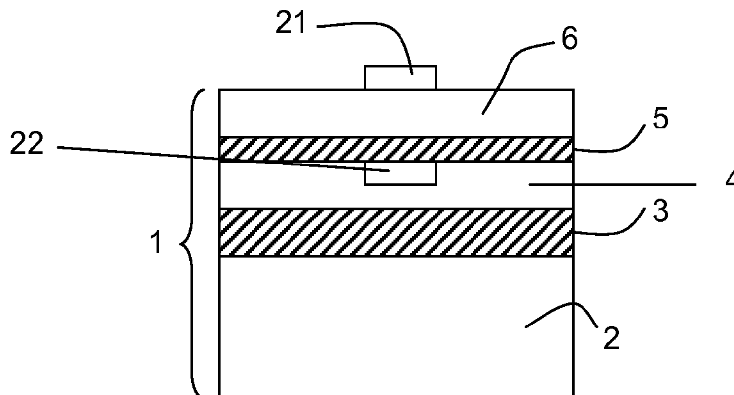


Figure 2

(57) **Abstract**: In preferred embodiments, the invention provides substrates that include a support, a first insulating layer arranged on the support, a non-mono-crystalline semi-conducting layer arranged on the first insulating layer, a second insulating layer arranged on the non-mono-crystalline semi-conducting layer; and top layer disposed on the second insulating layer. Additionally, a first gate electrode can be formed on the top layer and a second gate electrode can be formed in the non-mono-crystalline semi-conducting layer. The invention also provides methods for manufacture of such substrates.

WO 2010/002516 A2

LOW-COST DOUBLE STRUCTURE SUBSTRATES AND METHODS FOR THEIR MANUFACTURE

FIELD OF THE INVENTION

5 The present invention relates to low-cost substrates having a double-structure and to methods of manufacturing such low-cost double-structure substrates.

BACKGROUND OF THE INVENTION

Examples known double-structure substrates are described in Maleville et al., 2000, 10 "Multiple SOI layers by multiple Smart Cut™ transfers", IEEE International SOI Conference, pp 134-135. Double-structure substrates described therein comprise, in succession, a support, a first insulating layer, a first crystalline layer, a second insulating layer and a second crystalline layer.

Such double-structure substrates are useful for the fabrication of microelectronic 15 devices, e.g. certain CMOS transistors, having high-performance but low-power consumption. In particular, multiple gate devices can be fabricated in double-structure substrates, one gate being fabricated in the buried first crystalline layer and a second gate being fabricated on top of the second crystalline layer. In such devices, electrical potentials under the gates sources, drains and channels on the top of the second crystalline layer can be controlled by appropriate 20 operation of gates in the buried first crystalline layer.

Devices fabricated in double-structure substrates achieve high-performance and low-power by reducing the parasitic capacitances between the gates sources and drains and their supports that are typical in traditional single-structure substrates. Such devices cannot be fabricated in traditional single-structure substrates, since they do not have the second 25 insulating layer and the second crystalline layer.

However, the cited document teaches that manufacturing such double-structure substrates is complex, requiring sequentially performing two layer-transfer operations, one layer-transfer to form the first insulating layer and first crystalline layer and the second layer-transfer to form the second insulating layer and top crystalline layer. Although high quality 30 stacks of crystalline layers can be manufactured, their higher costs limit or prevent their economical use in lower-cost, consumer end products mobile phones, PDAs, and the like.

SUMMARY OF THE INVENTION

The present invention provides low-cost double-structure substrates suitable for use in a wide range of applications including microelectronics, optoelectronics, photovoltaic, micro-electro-mechanical devices. The low-cost double-structure substrates of the invention can find particular use in the fabrication of high-performance, low-power devices, e.g., for computing or telecommunication devices that are embedded into mobile consumer devices. The invention also provides devices fabricated from such substrates and methods for manufacture and fabrication of these substrates and devices.

Importantly, instead of the buried mono-crystalline, semi-conducting layers found in double-structure substrates of the prior art, the double-structure substrates of this invention comprise a buried, non-mono-crystalline, semi-conducting layer. This feature, use of a non-mono-crystalline layer instead of a mono-crystalline layer, of the double-structure substrates of this invention simplifies their manufacturing and reduces their cost. The present invention therefore provides a low-cost approach to the problem of providing double-structure substrates that incorporate a non-mono-crystalline semi-conducting layer.

It is also important that the non-crystalline nature of the non-mono-crystalline semi-conducting layer of substrate can be expected to have only minor impacts on the performance and power requirement of the devices that will be formed on and in substrate. This lack of impact is because the so-called “back gate” electrodes are formed in the non-mono-crystalline semi-conducting layer and the operation of such gates do not require high quality mono-crystalline material.

More precisely, the invention provides substrates having a support, a first insulating layer arranged on the support, a non-mono-crystalline semi-conducting layer arranged on the first insulating layer, a second insulating layer arranged on the non-mono-crystalline semi-conducting layer, and a top layer disposed on the second insulating layer.

The invention provides methods of manufacturing such a substrate in which, starting from a support having a first insulating surface layer and a donor substrate having a second insulating surface layer, a non-mono-crystalline semi-conducting layer is formed on the first insulating layer and/or the second insulating layer to obtain a first structure that includes the support and a second structure that includes the donor substrate; then the first structure and the second structure are assembled together; and finally the thickness of the donor substrate of the second structure is reduced to form the final substrate.

The invention provides further methods of manufacturing a substrate in which, starting from an initial substrate, a first insulating layer is placed and/or deposited on the surface of the initial substrate; a non-mono-crystalline semi-conducting layer is placed and/or deposited on the surface of the first insulating layer; and then a second insulating layer is placed and/or deposited on the surface of the non-mono-crystalline semi-conducting layer. The resulting structure is then assembled with an additional substrate such that the first insulating layer, the non-mono-crystalline semi-conducting layer, and the second insulating layer are sandwiched between the initial substrate and the additional substrate. Finally, the thickness of the initial substrate or of the additional substrate is reduced to form the substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the invention will become apparent from the following descriptions that refer to the appended drawings, which illustrate exemplary but non-limiting embodiments of the invention, and in which:

Figure 1 illustrates embodiments of the substrates of the invention;

Figure 2 illustrates embodiments of the substrates of the invention that have been further processed;

Figures 3a1, 3a2, and 3b to 3e illustrate embodiments of the methods of the invention; and

Figures 4a to 4c illustrate further embodiments of the methods of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments and particular examples described herein should be seen as examples of the scope of the invention, but not as limiting the present invention. The scope of the present invention should be determined with reference to the claims.

Figure 1 illustrates double-structure substrate 1 of the invention. Substrate 1 includes support 2, first insulating layer 3 arranged on support 2, non-mono-crystalline semi-conducting layer 4 arranged on first insulating layer 3, second insulating layer 5 arranged on non-mono-crystalline semi-conducting layer 4, and top layer 6 disposed on second insulating layer 5.

Substrate 1 includes support 2 which can be selected from lower-cost materials, e.g., mono-crystalline silicon, or poly-crystalline silicon, or other lower cost materials, as it usually has little or no active role in substrate 1.

Substrate 1 also includes first insulating layer 3 and second insulating layer 5, which can comprise one or more insulating materials, e.g., silicon dioxide, silicon nitride, a low k dielectric i.e. a material with a dielectric constant lower than the dielectric constant of silicon dioxide, a high k dielectric i.e. a material with a dielectric constant higher than the dielectric constant of silicon dioxide, or combinations of these materials. Layers 3 and 5 can be a single layer or can be a stack of sub-layers, the sub-layers being selected from the above insulating materials. In preferred embodiments, first insulating layer 3 and second insulating layer 5 comprise silicon dioxide.

The thicknesses of layers 3 and 5 can be selected as required by the final application of the substrate. In preferred embodiments, the thickness of first insulating layer 3 is more than 50 nm and the thickness of second insulating layer 5 is less than 25 nm, e.g., 10 nm. These thicknesses are particularly advantageous as thicker insulating layer 3 reduces parasitic capacitances whereas thinner insulating layer 5 reduces back gate bias voltages.

Substrate 1 also includes non-mono-crystalline semi-conducting layer 4 having thickness sufficient to form second gate electrode 22. In preferred embodiments, semi-conducting layer 4 comprises silicon or silicon germanium with a thickness between 20 nm and 200 nm. It can be amorphous or polycrystalline, or can have both poly-crystalline regions and amorphous regions.

Substrate 1 includes top layer 6 in which channels of microelectronic devices are usually formed. Therefore, top layer 6 is preferably higher quality and/or mono-crystalline so that device performance and circuit yield are suitable. Top layer 6 can comprise one or more of silicon, strained silicon, germanium, strained germanium, strained silicon germanium, GaAs, GaN, InP, SiC, or other semiconductors. For improved device performance, top layer 6 is preferably thin, e.g., less than 100 nm, or less then 50 nm, or thinner. Microelectronic devices formed in thin top layer 6 are operated in so-called “fully depleted” or “partially depleted” modes in relation to the distribution of the electrical charge flowing in the channel and to reduce junction capacitance so that such devices can have better performance than devices formed in thicker top layers and operated in other modes.

Figure 2 illustrates an exemplary use of substrate 1. First gate electrode and gate dielectric 21 have been formed on top layer 6 in order to control a gate channel (not illustrated in this figure) arranged under the gate dielectric and electrode. Second gate electrode 22 has been formed in non-mono-crystalline e.g., amorphous or poly-crystalline, semi-conducting

layer 4 in order to control and limit parasitic capacitances that usually exist between the source, drain and support.

An exemplary manufacturing process for the device of Figure 2 begins by providing substrate 1, and forming second gate electrode 22 in non-mono-crystalline semi-conducting material layer 4 by, e.g., dopant implantation. Next, gate dielectric and first gate electrode 21 are formed on top layer 6 using known masking, depositing and etching techniques. Alternatively, first gate electrode 21 can be formed before second gate electrode 22, but this alternative is less preferably since it requires that the dopant be implanted through first gate electrode 21.

Figure 3a1, 3a2, and 3b to 3e illustrate an embodiment of processes for manufacturing substrates 1.

Figure 3a1 illustrates support 2 having first insulating layer 3 preferably comprising mono-crystalline silicon.

Figure 3a2 illustrates donor substrate 8 preferably comprising materials suitable for top layer 6, since top layer 6 ultimately derives from donor substrate 8. Accordingly, donor substrate 8 can be mono-crystalline silicon, germanium, strained silicon, or other type of semiconductor material.

First and second insulating layers 3 and 5 can be a single layer or can comprise a stack of sub-layers; the layers and the sub-layers comprise one or more of silicon dioxide, silicon nitride, a low k dielectric material, or a high k dielectric material. In preferred embodiments and where support 2 and donor 8 comprise silicon, first and second insulating layers 3 and 5 can comprise silicon dioxide that is optionally formed by thermally oxidizing silicon support 2 and/or silicon donor substrate 8, respectively.

Figures 3b and 3c illustrate alternatives for depositing and/or placing non-mono-crystalline semi-conducting layer 4 on support 2 or on donor substrate 8 in order to form first structure 8a from support 2 or second structure 9 from donor substrate 7, respectively. Preferably, non-mono-crystalline semi-conducting layer 4 is deposited by chemical vapour deposition or physical vapour deposition of silicon or silicon germanium, in their amorphous or poly-crystalline forms.

Figure 3b illustrates an alternative in which non-mono-crystalline semi-conducting layer 4 is deposited and/or placed on second insulating layer 5.

Figure 3c illustrates an alternative in which non-mono-crystalline semi-conducting layer 4 is deposited and/or placed on first insulating layer 3.

Optionally, prior to the subsequent assembly of support 2 and donor substrate 8, either one or both of the exposed surfaces to be assembled can be polished. Since a poly-crystalline semi conducting layer can present a surface requiring preparation before bonding, optional polishing of such surfaces is particularly advantageous. To the extent that it is easier to obtain an amorphous non-crystalline semi-conducting surface this is ready "as deposited" for bonding, such surfaces are preferred for non-mono-crystalline semi-conducting layer 4. Optionally, prior to assembly and to further facilitate bonding during assembly, non-mono-crystalline semi-conducting layer 4 can be partially oxidized.

Figure 3d illustrates assembling and bonding first structure 8a and second structure 9.

Figure 3e illustrates that, after assembly and bonding, donor substrate 8 as part of second structure 9 is thinned to produce final substrate 1. Known thickness reducing techniques can be used for such thinning, e.g., grind and etch back, Smart Cut® employing ion implantation and layer fracture, and other techniques.

During the steps of assembling and/or reducing the thickness, it can be advantageous to apply thermal treatments. If the non-mono-crystalline semi-conducting layer 4 comprises amorphous material and if the temperature one or more thermal treatments exceeds the amorphous material's deposition temperature, some or all of originally amorphous layer 4 may re-crystallize. In such a case, layer 4 can comprise regions of poly-crystalline nature along with regions of amorphous nature. In any case, the layer remains non-mono-crystalline.

Figure 4a to 4c illustrate another embodiment of processes for manufacturing substrates 1.

Figure 4a illustrates resulting structure 11 and additional substrate 12. Resulting structure 11 can be formed by placing and/or depositing on initial substrate 10 first insulating layer 3, then placing and/or depositing non-mono-crystalline semi-conducting layer 4, and finally placing and/or depositing second insulating layer 5,3. Resulting structure 11, as illustrated, comprises all layers of substrate 1 except top layer 6.

Preferred compositions and thicknesses of layers 3, 4, 5 have been described above and will not be repeated here. First insulating layer 3 can be deposited or formed on initial substrate 10 by thermal oxidation; second insulating layer 5 can also be deposited on the non-mono-crystalline semi-conducting layer 4 or can be formed on layer 4 by oxidation.

Figure 4b illustrates assembly and bonding of resulting structure 11 and additional substrate 12 such that first insulating layer 3, non-mono-crystalline semi-conducting layer 4, and second insulating layer 5 are sandwiched between initial substrate 10 and additional

substrate 12. Bonding of resulting structure 11 and additional substrate 12 can optionally be facilitated by one or more further steps, e.g., additional substrate 12 can be partially oxidized or one or more of additional substrate 12 and first and second insulating layers 5, 3 can be polished.

5 Figure 4c illustrates resulting substrate 1 after initial substrate 10 or additional substrate 12 has been thinned as in the previous embodiment described with respect of Figure 3a to 3e. Since, in different embodiments, top layer 6 can originate from either of initial substrate 10 or additional substrate 12, first and second insulating layers 5, 3 can have different orientations relative to top layer 6 as illustrated in Figure 4c.

THE CLAIMS

What is claimed is:

1. A method of manufacturing a double-structure substrate which comprises:
5 providing a support substrate having a first insulating surface layer;
providing a donor substrate;
forming, in succession, either a non-mono-crystalline, semi-conducting intermediate layer and a second insulating layer on the support substrate, or the second insulating layer and the intermediate layer on the donor substrate;
10 assembling the support substrate with the donor substrate so that the intermediate layer is sandwiched between the first and second insulating layers, and the intermediate layer and the first and second insulating layers are sandwiched between the two substrates;
reducing the thickness of the donor substrate portion of the assembled structure to form the double-structure substrate.

15

2. The method of claim 1 wherein the first insulating layer has a thickness of between 50 nm and 1 micron.

3. The method of claim 1 wherein the intermediate layer is formed to have a
20 thickness between 20 nm and 200 nm.

4. The method of claim 1 wherein the second insulating layer is formed to have a thickness of less than 25 nm.

25 5. The method of claim 1 wherein the remaining portion of the donor substrate is formed to have a thickness of less than 100 nm.

6. The method of claim 1 wherein one or both of the support and donor substrates comprise mono-crystalline silicon.

30

7. The method of claim 1 wherein one or both of the first and second insulating layers comprises silicon dioxide, silicon nitride, low k dielectric material, high k dielectric material, or a combination of these materials.

8. The method of claim 1 wherein the intermediate layer comprises silicon or silicon germanium.

5 9. The method of claim 1 wherein the intermediate layer comprises an amorphous material, or a polycrystalline material, or a combination of these materials.

10. The method of claim 1 further comprising partially oxidising the surface of the non-mono-crystalline semi-conducting layer adjacent to the second insulating layer.

10

11. The method of claim 1 further comprising:

forming a gate dielectric and a first gate electrode on the surface of the remaining portion of the donor substrate; and

forming a second gate electrode in the intermediate layer.

15

12. The method of claim 11 wherein the first gate electrode is formed after the second gate electrode.

13. The method of claim 11 wherein the second gate electrode is formed by

20 implanting dopants into the intermediate layer.

14. A double-structure substrate comprising:

a support substrate;

a first insulating layer arranged on the support and having a thickness between 50 nm

25 and 1 micron;

a non-mono-crystalline semi-conducting intermediate layer arranged on the first insulating layer, having a thickness between 20 nm and 200 nm, and comprising, alone or in combination, an amorphous material or a polycrystalline material;

a second insulating layer arranged on the non-mono-crystalline semi-conducting layer

30 and having a thickness less than 25 nm; and

a semiconductor top layer arranged on the second insulating layer and having a thickness less than 100 nm.

15. The substrate of claim 14 further comprising a gate dielectric and a first gate electrode arranged on the top layer and a second gate electrode arranged in the non-mono-crystalline semi-conducting layer.

5 16. The substrate of claim 14 wherein the support comprises mono-crystalline silicon.

17. The substrate of claim 14 wherein one or both of the first insulating layer and the second insulating layer comprise silicon dioxide, silicon nitride, low k dielectric material,
10 a high k dielectric material, or a combination of these materials.

18. The substrate of claim 14 wherein the intermediate layer comprises silicon or silicon germanium.

15 19. The substrate of claim 14 wherein the top layer comprises one or more of the group consisting of silicon, strained silicon, germanium, strained germanium, strained silicon germanium, GaAs, GaN, InP, and SiC.

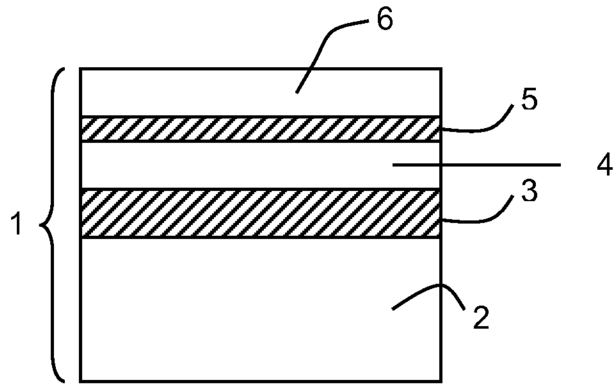


Figure 1

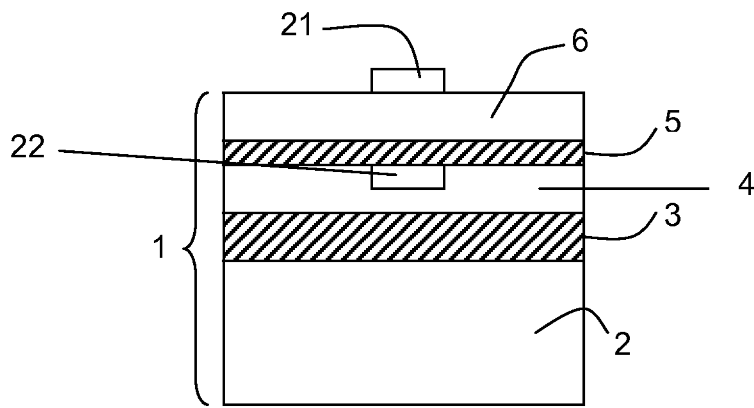


Figure 2

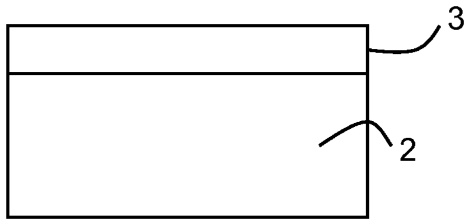


Figure 3a1

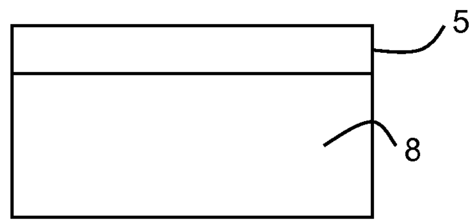
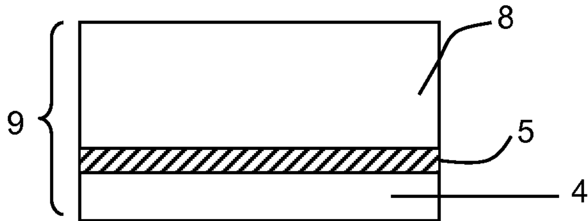


Figure 3a2



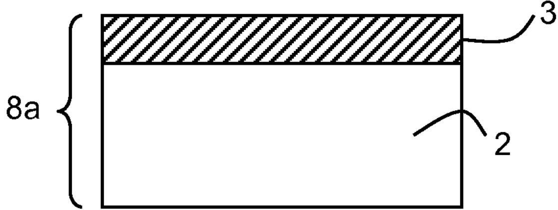
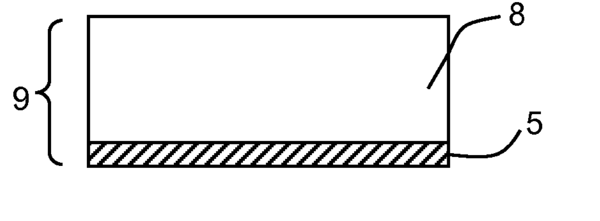


Figure 3b



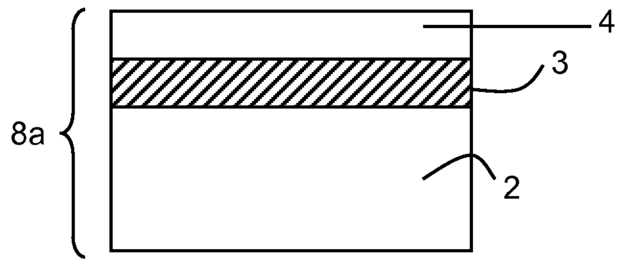


Figure 3c

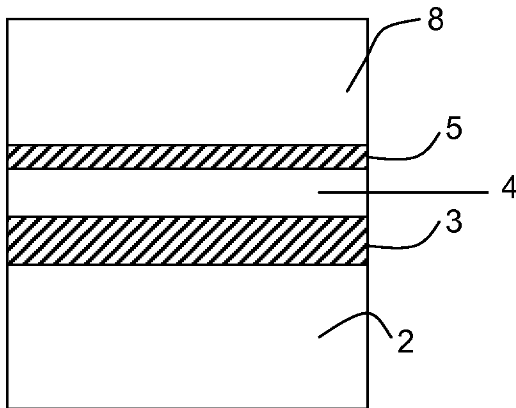


Figure 3d

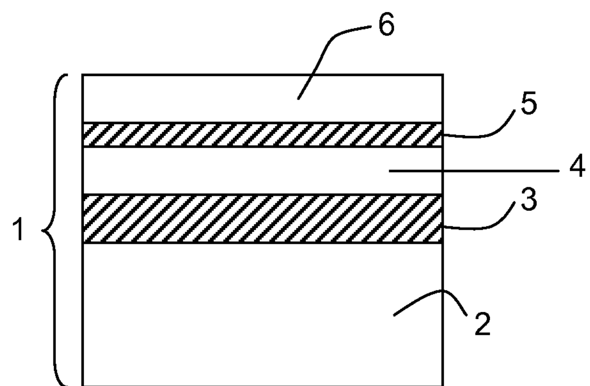


Figure 3e

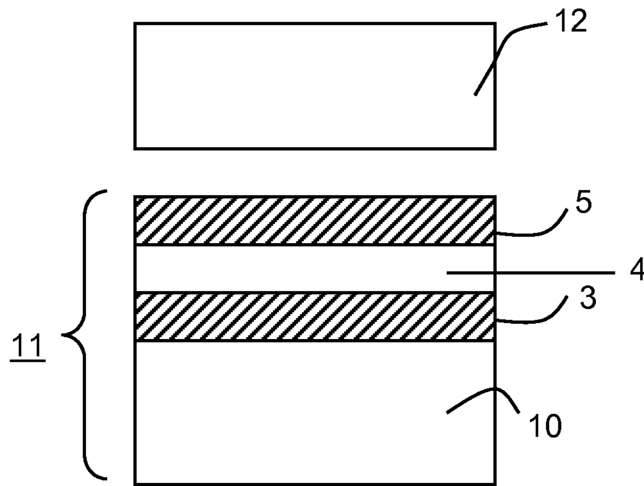


Figure 4a

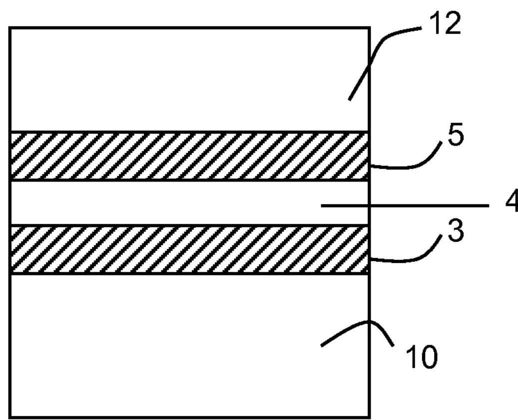


Figure 4b

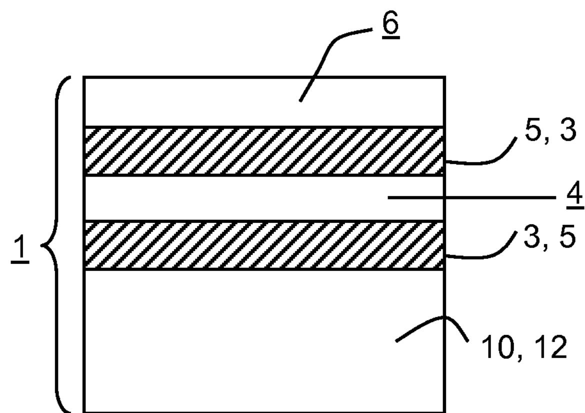


Figure 4c