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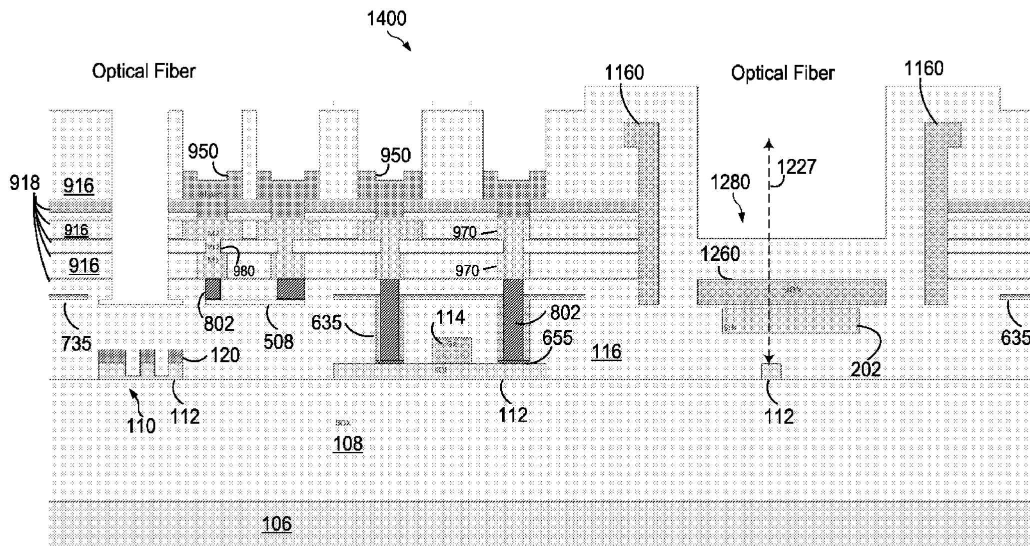

FIG. 14

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(57) Abstract: A process for fabricating a large mode size edge coupler with a dual taper bridge. The fabricating process utilizes a CMOS-compatible hard mask layer, which is easy remove by wet etch, with a high RIE selectivity to ensure there is a uniform layer of dielectric between the Si photonic circuitry in the SOI layer and the waveguide. That is, a thickness of the dielectric layer between the Si photonic circuitry in the SOI layer and the waveguide is suitably controlled using the CMOS-compatible hard mask layer without damaging the dielectric layer during the fabricating process. The hard mask layer also ensures that the thickness of the dielectric above the grating coupling is suitably controlled to provide consistent coupling efficiency. A portion of the hard mask layer may also function as a heating element, which may be beneficially used to change the reflective index of the surrounding dielectric.

[Continued on next page]

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Process Integration Solution For An Optical Component

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This patent application claims the benefit of U.S. Provisional Patent Application No. 63/179851 filed April 26, 2021 by Ge Yi, et al., and titled "Process Integration Solution For An Optical Component," which is hereby incorporated by reference.

TECHNICAL FIELD

[0002] The present disclosure is generally related to the field of a silicon (Si) photonics and, in particular, to an optical component and a process of fabricating the optical component that enables a low loss insertion coupling between the Si photonic circuitry and an optical fiber.

BACKGROUND

[0003] Silicon photonic circuitry made using complementary metal-oxide-semiconductor (CMOS) process technology at the wafer level, and which processes and manipulates information carrying light at the chip level, has an advantage in terms of device reliability and low cost. Due to the high index contrast between the Si core (which is normally built in a silicon on insulator (SOI) layer) and the surrounding cladding layer (e.g., silicon dioxide (SiO_2)), the optical mode is highly confined with a small mode size. Mode size refers to the dimension of a mode in an optical waveguide in a certain direction, for example, the energy distribution in the transverse direction. Mode shape refers to the relative dimension of the mode size in two different directions, for example, a horizontal direction and a vertical direction.

[0004] An optical fiber allows information carrying light to travel distances longer than a few centimeters with a low energy loss. The optical component (e.g., the optical coupler) is used to couple the optical fiber to the Si photonic circuitry. Ordinary optical fiber has a much larger mode size compared to the optical mode size of the Si photonic chip, which leads to a large energy loss or a high insertion loss. That is, due to the small mode size (e.g., sub-micro) of silicon waveguides it is challenging for mode converters to couple light into and/or out of silicon-based photonic devices.

SUMMARY

[0005] The disclosed aspects/embodiments provide a process for fabricating a large mode size edge coupler with a dual taper bridge. The fabricating process utilizes a CMOS-compatible

hard mask layer with a high reactive ion etch (RIE) selectivity to ensure there is a uniform layer of dielectric between the Si photonic circuitry in the SOI layer and the waveguide. That is, a thickness of the dielectric layer between the Si photonic circuitry in the SOI layer and the waveguide is suitably controlled using the CMOS-compatible hard mask layer without fear of damaging the dielectric layer during the fabricating process. The hard mask layer also ensures that the thickness of the dielectric above the grating coupling is suitably controlled to provide consistent coupling efficiency. Moreover, a portion of the hard mask layer may also function as a heating element, which may be beneficially used to change the reflective index of the surrounding dielectric. Changing reflective index of the surrounding dielectric allows the information carrying light to be tuned.

[0006] A first aspect relates to a method of fabricating an optical component, comprising: depositing a hard mask on a dielectric layer supported by a bridge layer of a photonic structure, the photonic structure including a grating coupler and silicon photonic circuitry; performing a first etch to remove portions of the hard mask, the dielectric layer, and the bridge layer, a remaining portion of the bridge layer forming a dual taper bridge; increasing a thickness of a second dielectric layer until the dual taper bridge and a remaining portion of the hard mask are covered by the second dielectric layer, and then removing a portion of the second dielectric layer to expose the hard mask disposed over the dual taper bridge; increasing a thickness of the hard mask over the dual taper bridge to form a first stopping layer and over the grating coupler to form a second stopping layer, and depositing the hard mask to form a heating element; performing a metallization process to electrically couple the silicon photonic circuitry and the heating element to contact pads; exposing the first stopping layer by performing a second etch and removing the first stopping layer by performing a third etch; forming a waveguide over the dual taper bridge after the first stopping layer has been removed, the waveguide, the dual taper bridge, and the silicon photonic circuitry forming an edge coupler; exposing the second stopping layer by performing a fourth etch and removing the second stopping layer by performing a fifth etch; and opening the contact pads to form the optical component.

[0007] Optionally, in any of the preceding aspects, another implementation of the aspect provides that the dielectric layer disposed between the waveguide and the dual taper bridge having a thickness of between about zero nanometers and about fifty nanometers, and a distance between a top surface of the grating coupler and a bottom surface of the second stopping layer is between about four hundred nanometers and about seven hundred nanometers.

[0008] Optionally, in any of the preceding aspects, another implementation of the aspect provides that the hard mask, the first stopping layer, and the second stopping layer being one of aluminum nitride (AlN), titanium nitride (TiN), and tantalum nitride (TaN).

[0009] Optionally, in any of the preceding aspects, another implementation of the aspect provides that one or more of the first etch, the second etch, and the fourth etch being a reactive ion etch (RIE).

[0010] Optionally, in any of the preceding aspects, another implementation of the aspect provides that one or more of the third etch and the fifth etch being a wet etch.

[0011] Optionally, in any of the preceding aspects, another implementation of the aspect provides that the grating coupler comprising a portion of the silicon photonic circuitry and a polysilicon structure.

[0012] Optionally, in any of the preceding aspects, another implementation of the aspect provides forming a germanium (Ge) structure on the silicon photonic circuitry, the silicon photonic circuitry disposed on a buried oxide (BOX) layer, the buried oxide layer disposed on a semiconductor substrate.

[0013] Optionally, in any of the preceding aspects, another implementation of the aspect provides that the dual taper bridge comprising silicon nitride (SiN or Si_3N_4).

[0014] Optionally, in any of the preceding aspects, another implementation of the aspect provides exposing the hard mask disposed over the dual taper bridge by performing chemical mechanical polishing (CMP).

[0015] Optionally, in any of the preceding aspects, another implementation of the aspect provides that the waveguide comprising a silicon oxynitride (SiON).

[0016] Optionally, in any of the preceding aspects, another implementation of the aspect provides that the silicon photonic circuitry, the dual taper bridge, and the waveguide of the edge coupler providing an adiabatic path for light to enter and exit the optical component.

[0017] A second aspect relates to an optical component, comprising: a grating coupler disposed in a dielectric layer of a photonic structure, the grating coupler comprising a layer of polysilicon disposed on silicon photonic circuitry; an edge coupler disposed in the dielectric layer of the photonic structure, the edge coupler comprising a waveguide, a dual taper bridge, and the silicon photonic circuitry; and a heating element in the dielectric layer of the photonic structure, the heating element comprising a hard mask and disposed laterally between the grating coupler and the dual taper bridge.

[0018] Optionally, in any of the preceding aspects, another implementation of the aspect provides that the dielectric layer disposed between the waveguide and the dual taper bridge having a thickness of between about zero nanometers and about fifty nanometers.

[0019] Optionally, in any of the preceding aspects, another implementation of the aspect provides that the dielectric layer disposed above a top surface of the grating coupler having a thickness of between about four hundred nanometers and about seven hundred nanometers.

[0020] Optionally, in any of the preceding aspects, another implementation of the aspect provides that the hard mask one of aluminum nitride (AlN), titanium nitride (TiN), and tantalum nitride (TaN).

[0021] Optionally, in any of the preceding aspects, another implementation of the aspect provides that a portion of the silicon photonic circuitry supporting a germanium (Ge) structure.

[0022] Optionally, in any of the preceding aspects, another implementation of the aspect provides that the dual taper bridge comprising silicon nitride (SiN or Si_3N_4).

[0023] Optionally, in any of the preceding aspects, another implementation of the aspect provides that the waveguide comprising a silicon oxynitride (SiON).

[0024] Optionally, in any of the preceding aspects, another implementation of the aspect provides that the silicon photonic circuitry, the dual taper bridge, and the waveguide of the edge coupler providing an adiabatic path for light to enter and exit the optical component.

[0025] Optionally, in any of the preceding aspects, another implementation of the aspect provides that the photonic structure including a buried oxide (BOX) layer supported by a silicon substrate, and the photonic structure including metallization coupling the heating element and the silicon photonic circuitry to contact pads.

[0026] A third aspect relates to a means for fabricating an optical component, comprising: means for depositing a hard mask on a dielectric layer supported by a bridge layer of a photonic structure, the photonic structure including a grating coupler and silicon photonic circuitry; means for performing a first etch to remove portions of the hard mask, the dielectric layer, and the bridge layer, a remaining portion of the bridge layer forming a dual taper bridge; means for increasing a thickness of a second dielectric layer until the dual taper bridge and a remaining portion of the hard mask are covered by the second dielectric layer and means for removing a portion of the second dielectric layer to expose the hard mask disposed over the dual taper bridge; means for increasing a thickness of the hard mask over the dual taper bridge to form a first stopping layer and over the grating coupler to form a second stopping layer, and means for depositing the hard mask on the second dielectric layer to form a heating element; means for performing a metallization process to electrically couple the silicon photonic circuitry and the heating element

to contact pads; means for exposing the first stopping layer by performing a second etch and removing the first stopping layer by performing a third etch; means for forming a waveguide over the dual taper bridge after the first stopping layer has been removed, the waveguide, the dual taper bridge, and the silicon photonic circuitry forming an edge coupler; means for exposing the second stopping layer by performing a fourth etch and removing the second stopping layer by performing a fifth etch; and means opening the contact pads to form the optical component.

[0027] A fourth aspect relates to a system, comprising: an optical component as disclosed herein, the optical component configured to receive and transmit light; and an optical fiber coupled to the optical component, the optical fiber configured to receive the light from the optical component and to transmit the light to the optical component.

[0028] For the purpose of clarity, any one of the foregoing embodiments may be combined with any one or more of the other foregoing embodiments to create a new embodiment within the scope of the present disclosure.

[0029] These and other features will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] For a more complete understanding of this disclosure, reference is now made to the following brief description, taken in connection with the accompanying drawings and detailed description, wherein like reference numerals represent like parts.

[0031] FIGS. 1-13 illustrate an optical component in various stages of the fabricating process.

[0032] FIG. 14 illustrates an optical component according to an embodiment of the disclosure.

[0033] FIG. 15 illustrates a method of fabricating an optical component.

[0034] FIG. 16 is a schematic diagram of an optical device that may incorporate or include the optical component of FIG. 15.

[0035] FIG. 17 is a schematic diagram of an embodiment of a means for optical processing according to an embodiment of the disclosure.

DETAILED DESCRIPTION

[0036] It should be understood at the outset that although an illustrative implementation of one or more embodiments are provided below, the disclosed systems and/or methods may be implemented using any number of techniques, whether currently known or in existence. The

disclosure should in no way be limited to the illustrative implementations, drawings, and techniques illustrated below, including the exemplary designs and implementations illustrated and described herein, but may be modified within the scope of the appended claims along with their full scope of equivalents.

[0037] In some cases, suspended edge couplers may be used to couple information carrying light between the optical fiber and the Si photonic circuitry. Suspended edge couplers are so named because the Si substrate is etched away to avoid an expended light mode at the end of the edge coupler from being absorbed by the Si substrate, which would result in a substantial optical loss. Unfortunately, the suspended edge coupler is mechanically unstable, especially when an array of edge couplers are used. In addition, suspended edge couplers are difficult to manufacture, which leads to a low-device yield. Moreover, suspended edge couplers suffer performance issues because the light in the suspended edge coupler is not guided far enough away from the Si substrate vertically.

[0038] To enable a good optical coupling between a dual taper bridge (also known in the silicon photonics industry as a silicon nitride (SiN or Si_3N_4) dual taper bridge) and a waveguide such as a silicon oxynitride (SiON) waveguide, the thickness of a dielectric layer such as silicon dioxide (SiO_2) positioned between the dual taper bridge and the waveguide should to be uniformly controlled across the whole wafer. Having a uniform layer of dielectric ensures a consistent mode transition across the wafer, which allows for a high yield and improved reliability. In addition, the thickness of the dielectric above a grating coupling should also be controlled to ensure consistent coupling efficiency.

[0039] Disclosed herein is process for fabricating a large mode size edge coupler with a dual taper bridge. The fabricating process utilizes a CMOS-compatible hard mask layer with a high reactive ion etch (RIE) selectivity to ensure there is a uniform layer of dielectric between the Si photonic circuitry in the SOI layer and the waveguide. That is, a thickness of the dielectric layer between the Si photonic circuitry in the SOI layer and the waveguide is suitably controlled using the CMOS-compatible hard mask layer without fear of damaging the dielectric layer during the fabricating process. The hard mask layer also ensures that the thickness of the dielectric above the grating coupling is suitably controlled to provide consistent coupling efficiency. Moreover, a portion of the hard mask layer may also function as a heating element, which may be beneficially used to change the reflective index of the surrounding dielectric. Changing reflective index of the surrounding dielectric allows the information carrying light to be tuned.

[0040] FIG. 1 illustrates an optical component 100 in an intermediate stage of the fabrication process. As shown, the optical component 100 initially includes a photonic structure 101 that

supports a dielectric layer 102 beneath a hard mask 104. In an embodiment, the photonic structure 101 includes a substrate 106, a buried oxide (BOX) layer 108, a grating coupler 110, silicon photonic circuitry 112, a semiconductor structure 114, a second dielectric layer 116, and a bridge layer 118. In an embodiment, the center portion of the optical component 100 may include one or more active components (e.g., transistors) and, therefore, be referred to as the active device. In an embodiment, portions of the optical component 100 on either side of the active device may be referred to as a coupling structure. The optical component 100 may include additional features in practical applications.

[0041] In an embodiment, the dielectric layer 102 is formed from silicon dioxide (SiO_2) and has a thickness of between about 0 nanometers (nm) and about 50 nanometers. The dielectric layer 102 may be deposited by a thin film deposition process. Examples of such thin film deposition processes include chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), atomic level deposition (ALD), chemical vapor deposition (CVD), and low-pressure chemical vapor deposition (LPCVD). As will be more fully explained below, precisely controlling a thickness of the dielectric layer 102 is desirable and beneficial.

[0042] The substrate 106 is formed from silicon (Si) or a silicon-containing substance. Therefore, the substrate 106 may be referred to as a silicon wafer. The buried oxide layer 108 is disposed on the substrate 106 and permits electrical devices on the substrate 106 to be isolated from each other, as the oxide layer 108 serves as an insulator. In an embodiment, the buried oxide layer 108 is formed from silicon dioxide (SiO_2) or another insulating material and has a thickness of between about one and about four micrometers (μm).

[0043] The grating coupler 110 is formed from a portion of the silicon photonic circuitry 112 and a patterned portion of polysilicon (PolySi) 120. As will be more fully explained below, the grating coupler 110 is able to receive light from outside the optical component 100 and output light from the optical component 100.

[0044] The silicon photonic circuitry 112 comprises a pattern of silicon or silicon-containing material extending through the second dielectric layer 116. When viewed from above, the silicon photonic circuitry 112 may have a pattern similar to the metal traces disposed on a printed circuit board (PCB). Thus, only a few portions of the silicon photonic circuitry 112 are visible in the cross-section of FIG. 1. The pattern allows the silicon photonic circuitry 112 to carry information containing light throughout the optical component. Because the silicon photonic circuitry 112 is seated atop the buried (and insulative) oxide layer 108, the silicon photonic circuitry 112 may be referred to as a silicon on insulator (SOI). In addition, the lateral or horizontal layer of the optical component 100 containing the silicon photonic

circuitry 112 may be referred to as the SOI layer. In an embodiment, the distance between a top surface of the silicon photonic circuitry 112 and a bottom surface of the bridge layer 118 can be in the range of up to several hundred nanometers (nm).

[0045] The semiconductor structure 114 is disposed on the silicon photonic circuitry 112 and is formed from a semiconducting material. For example, the semiconductor structure 114 may be formed from germanium (Ge) or other suitable semiconductor materials. The semiconductor structure 114 may be used to form an optoelectronic component within the optical component.

[0046] In an embodiment, the second dielectric layer 116 is formed from silicon dioxide. That is, in an embodiment the second dielectric layer 116 and the first dielectric layer 102 are formed from the same material. The second dielectric layer 116 may be referred to herein as a cladding layer. The second dielectric layer 116 may be deposited by one of the thin film deposition processes noted above. As shown in FIG. 1, the second dielectric layer 116 is disposed over (or substantially disposed over) the grating coupler 110, the semiconductor structure 114, and the silicon photonic circuitry 112.

[0047] In an embodiment, the bridge layer 118 is disposed immediately beneath the dielectric layer 102. That is, the bridge layer 118 is in direct contact with the dielectric layer 102. The hard mask 104 is disposed over the dielectric layer 102. In an embodiment, the hard mask 104 has been deposited across the entire length of the underlying wafer. In an embodiment, the dielectric layer 102 is disposed immediately beneath the hard mask 104. That is, the dielectric layer 102 is in direct contact with the hard mask 104.

[0048] FIG. 2 illustrates an optical component 200 in an intermediate stage of the fabricating process following that of FIG. 1. As shown in FIG. 2, a patterning and etch has been performed to remove portions of the hard mask 104, the dielectric layer 102, and the bridge layer 118. The etch may also be referred to herein as an etch process, as etching, and so on. In an embodiment, the etch may be an RIE, a wet etch, or another type of etch capable of removing the hard mask 104, the dielectric layer 102, and the bridge layer 118.

[0049] A remaining portion of the bridge layer 118 of FIG. 1 forms a dual taper bridge 202. Thus, in an embodiment the dual taper bridge 202 is formed from silicon nitride. The dual taper bridge 202 may also be referred to as an inverse taper waveguide or other similar designation. In an embodiment, the dual taper bridge 202 has the same or similar shape as the silicon waveguide depicted in U.S. Pat. No. 10,120,135 issued to Futurewei Technologies, Inc., on November 6, 2018 and titled “Inverse Taper Waveguides For Low-Loss Mode Converters.”

In an embodiment, the dual taper bridge 202 may have other shapes or configurations suitable for functioning as a waveguide.

[0050] In an embodiment, precise control of the thickness or depth of the dielectric layer 102 is maintained in the absence of use of the hard mask 104 during the patterning and etch used to form the dual taper bridge 202.

[0051] FIG. 3 illustrates an optical component 300 in an intermediate stage of the fabricating process following that of FIG. 2. In this intermediate stage, the thickness or depth of the second dielectric layer 116 is increased to cover the dual taper bridge 202 and the hard mask 104. Thus, the dielectric layer 102 from FIG. 2 is merged with the second dielectric 116 of FIG. 3. After the thickness or depth of the second dielectric 116 has been increased, a portion of the second dielectric 116 is removed to expose the hard mask 104 (or at least a top surface thereof) disposed over the dual taper bridge 202. In an embodiment, second dielectric 116 is removed by chemical-mechanical polishing (CMP).

[0052] FIG. 4 illustrates an optical component 400 in an intermediate stage of the fabricating process following that of FIG. 3. In this intermediate stage, an etch is performed to remove some of the second dielectric 116 and expose the hard mask 104. In an embodiment, the etch comprises a wet etch

[0053] FIG. 5 illustrates an optical component 500 in an intermediate stage of the fabricating process following that of FIG. 4. In this intermediate stage, a thickness and width of the hard mask 104 is increased over the dual taper bridge 202 to form a first stopping layer 504 and increased over the grating coupler 110 to form a second stopping layer 506. In addition, the hard mask 104 is deposited on the second dielectric layer 116 between the grating coupler 110 and the dual taper bridge 202 to form a heating element 508. In an embodiment, a patterning process is performed to ensure that the hard mask 104 is increased and/or deposited in the desired location on the optical component 500. In an embodiment, the hard mask 104 is increased and/or deposited using one of the thin film deposition processes noted above.

[0054] FIG. 6 illustrates an optical component 600 in an intermediate stage of the fabricating process following that of FIG. 5. In this intermediate stage, openings 645 are formed in the second dielectric layer 116. In an embodiment, the openings 645 are formed (e.g., drilled) down to the silicon photonic circuitry 112. In an embodiment, a silicide at local (SAL) positions process is utilized to form the openings 645. After the openings 645 have been formed, a metal silicide 655 may be deposited or otherwise formed at the bottom of the openings 645. In an embodiment, the metal silicide 655 comprises a cobalt silicide or a nickel silicide. Thereafter, a dielectric layer 635 is deposited. The dielectric layer 635 may be referred to as a barrier layer.

In an embodiment, a patterning process is performed to ensure that the dielectric layer 635 is deposited in the desired location on the optical component 600.

[0055] FIG. 7 illustrates an optical component 700 in an intermediate stage of the fabricating process following that of FIG. 6. In this intermediate stage, additional insulating material is backfilled over the optical component 700. In an embodiment, the additional insulating material is silicon dioxide. Thereafter, a portion of the second dielectric layer 116 is removed by chemical-mechanical polishing (CMP).

[0056] FIG. 8 illustrates an optical component 800 in an intermediate stage of the fabricating process following that of FIG. 7. In this intermediate stage, openings (not shown) are formed in the second dielectric layer 116. In an embodiment, the openings are formed down to the heating element 508 and down to the silicon photonic circuitry 112. As shown in FIG. 8, the openings are filled (or substantially filled) with an electrically conductive material 802. In an embodiment, the electrically conductive material 802 comprises tungsten. Therefore, the structures formed by the electrically conductive material 802 may be referred to as tungsten plugs.

[0057] FIG. 9 illustrates an optical component 900 in an intermediate stage of the fabricating process following that of FIG. 8. In this intermediate stage, a back end of line (BEOL) process is performed to deposit or form alternating dielectric layers 916 and 918. The alternating dielectric layers 916 and 918 may be referred to as passivation layers. In an embodiment, the dielectric layers 916 comprise silicon nitride and the dielectric layers 918 comprise silicon dioxide. The BEOL process also generates various metal layers 970 (e.g., metal layer 1 (M1) and metal layer 2 (M2)) and couples those metal layers 970 to each other with vias 980 (e.g., V12). In an embodiment, the metal layers 970 form a pattern that extends horizontally throughout the insulating layers 916 while the vias 980 extend vertically to connect the metal layers 970 at different levels.

[0058] The BEOL process further generates a contact pad 950, which is coupled to the uppermost metal layer 970. In an embodiment, the metal layers 970 and vias 980 are formed from copper (Cu), aluminum (Al), or another metal and the contact pad 950 is formed from aluminum (Al) or another metal. While FIG. 9 depicts two metal layers (M1 and M2) and a single via (V12) disposed beneath each contact pad 950, additional metal layers 970 and vias 980 may be included in the optical component 900 in practical applications.

[0059] In an embodiment, the various processes depicted in FIGS. 7-9 may be collectively referred to as a metallization process 910. Such metallization process 910 is undertaken to, for example, electrically couple the silicon photonic circuitry 112 and the heating element 508 to the contact pads 950.

[0060] FIG. 10 illustrates an optical component 1000 in an intermediate stage of the fabricating process following that of FIG. 9. In this intermediate stage, the first stopping layer 504 over the dual taper bridge 202 is exposed by performing an etch. In an embodiment, the etch is an RIE. Thereafter, the first stopping layer 504 is removed by performing a subsequent etch. The subsequent etch may be a wet etch or another etch capable of removing the first stopping layer 504.

[0061] FIG. 11 illustrates an optical component 1100 in an intermediate stage of the fabricating process following that of FIG. 10. In this intermediate stage, a waveguide layer 1160 is deposited or formed. In an embodiment, the waveguide layer 1160 is deposited using one of the thin film deposition techniques described above. In an embodiment, the waveguide layer 1160 comprises a silicon oxynitride (SiON).

[0062] FIG. 12 illustrates an optical component 1200 in an intermediate stage of the fabricating process following that of FIG. 11. In this intermediate stage, the waveguide layer 1160 is patterned and partially etched away to form waveguide 1260. As shown, the waveguide 1260 is disposed vertically over the dual taper bridge 202. In an embodiment, the dielectric layer 116 (or the dielectric layer 102 of FIG. 1) disposed between the waveguide 1260 and the dual taper bridge 202 has a thickness (or depth) of between about five nanometers and about fifty nanometers.

[0063] The waveguide 1260, the dual taper bridge 202, and the silicon photonic circuitry 112 collectively form a whole light path with an edge coupler 1280. In an embodiment, the dual taper bridge 202 is formed between the semiconductor structure 114 in the second dielectric layer 116 and the edge coupler 1260 to both lateral and vertically enable the light mode far away from the substrate 106 to avoid absorption of the light by the substrate 106. As used herein, large mode is defined as the physical dimension of the optical mode - the optical energy spread for a guided light. In an embodiment, the edge coupler 1280 is a large mode edge coupler. That is, the normal mode size from a Si taper edge coupler can only expand the mode size to about 3 μm, while an optical fiber's mode size is either about 6-6.5 μm or about 9-9.5 μm. The large mode size edge coupler described herein enables the edge coupler mode size to be greater than about 6 μm to match the mode size in the optical fiber. This results in less light energy loss, and thus causes a lower insert loss.

[0064] Conventional optical component fabrication processes may damage a dielectric layer disposed between a waveguide 1260 and a dual taper bridge 202. Thus, the thickness of the dielectric layer in that location is difficult to precisely control. In contrast, the process described and illustrated herein allows the thickness of the dielectric layer 116 (or the dielectric layer 102

of FIG. 1) between the waveguide 1260 and the dual taper bridge 202 to be precisely controlled. Such precise control ensures consistent coupling efficiency. Indeed, when the dielectric layer 116 between the waveguide 1260 and the dual taper bridge 202 is too thin, light coupling between the edge coupler 1280 and the optical fiber may be lost. When the dielectric layer 116 between the waveguide 1360 and the dual taper bridge 202 is too thick, there is an undesirably high insertion loss.

[0065] In an embodiment, the silicon photonic circuitry 112, the dual taper bridge 202, and the waveguide 1260 of the edge coupler 1280 provide an adiabatic path 1227 for light to enter and exit the optical component 1200. That is, light is able to "jump" from the silicon photonic circuitry 112 to the dual taper bridge 202, from the dual taper bridge 202 to the waveguide 1260, and then exit the optical component 1200 to an optical fiber. Likewise, light from the optical fiber is able to enter the optical component 1300, jump to the waveguide 1260, jump to the dual taper bridge 202, and then jump to the silicon photonic circuitry 112.

[0066] In an embodiment, a distance 1251 between a top surface of the grating coupler 110 and a bottom surface of the second stopping layer 506 is between about 400 nm and about 700 nm.

[0067] Conventional optical component fabrication processes may damage a dielectric layer disposed vertically above a grating coupler. Thus, the amount of dielectric layer above the grating coupler is difficult to precisely control. In contrast, the process described and illustrated herein allows the distance 1251 between the top surface of the grating coupler 110 and the bottom surface of the second stopping layer 506 to be precisely controlled. Such precise control ensures consistent coupling efficiency. Indeed, when the dielectric layer 116 vertically above the grating coupler 110 is too thin, light coupling between the grating coupler 110 and the optical fiber may be lost. When the dielectric layer 116 vertically above the grating coupler 110 is too thick, there is an undesirably high insertion loss.

[0068] FIG. 13 illustrates an optical component 1300 in an intermediate stage of the fabricating process following that of FIG. 12. In this intermediate stage, a patterning and etch is performed to expose the second stopping layer 506 of FIG. 12 over the grating coupler 110. In an embodiment, the etch is an RIE. After the second stopping layer 506 has been exposed, the second stopping layer 506 is removed by a subsequent etch. In an embodiment, the subsequent etch is a wet etch.

[0069] FIG. 14 illustrates an optical component 1400 according to an embodiment of the disclosure. As shown, a patterning and etch has been performed to open the contact pads 950. In an embodiment, the etch is an RIE. A voltage differential may be applied to the contact pads

950 coupled to the heating element 508 to induce a current through the heating element 508. The current passing through the heating element 508 generates heat in the dielectric layer 116 proximate the heating element 508. The applied heat changes the reflective index of the dielectric layer 116 in the area around the heating element 508, which allows for tuning of the light entering or exiting the optical component 1400.

[0070] It should be recognized that other processing steps may be performed on the optical component 1400, both before and after those depicted in FIGS. 1-14, in practical applications. In addition, the optical component 1400 may include other or additional structures, circuitry, or features in practical applications.

[0071] FIG. 15 is a method 1500 of fabricating an optical component (e.g., optical component 1400). The method 1500 may be performed by semiconductor fabricating equipment in, for example, a foundry. In an embodiment, the method 1500 is a CMOS-compatible process. The method 1500 may be performed to precisely control a thickness of a dielectric layer between a waveguide and a dual taper bridge and/or an amount of dielectric layer above a grating coupler.

[0072] In block 1502, a hard mask such as hard mask 104 is deposited on a dielectric layer such as dielectric layer 102)supported by a bridge layer (bridge layer 118) of a photonic structure (photonic structure 101). In an embodiment, the photonic structure includes a grating coupler (grating coupler 110) and silicon photonic circuitry (silicon photonic circuitry 112. In an embodiment, a germanium structure such as structure 114 is formed on the silicon photonic circuitry, which is disposed on a buried oxide supported by a semiconductor substrate.

[0073] In block 1504, a first etch is performed to remove portions of the hard mask (e.g., the hard mask 104), the dielectric layer such as dielectric layer 102, and the bridge layer (e.g., bridge layer 118). A remaining portion of the bridge layer forms a dual taper bridge (e.g., dual taper bridge 202). In an embodiment, the dielectric layer disposed between the waveguide and the dual taper bridge having a thickness of between about zero nanometers and about fifty nanometers. In an embodiment, the first etch is an RIE.

[0074] In block 1506, a thickness of a second dielectric layer (e.g., dielectric layer 116) is increased until the dual taper bridge and a remaining portion of the hard mask are covered, and then a portion of the second dielectric layer is removed to expose the hard mask disposed over the dual taper bridge. In an embodiment, the thickness or depth of the second dielectric layer is increased by backfilling dielectric material. In an embodiment, the backfilled dielectric material is subjected to CMP to expose the hard mask and/or to smooth a top surface of the dielectric material that was deposited.

[0075] In block 1508, a thickness of the hard mask over the dual taper bridge is increased to form a first stopping layer, and the thickness of the hard mask over the grating coupler is increased to form a second stopping layer. In addition, the hard mask is deposited is to form a heating element (e.g., heating element 508). In an embodiment, the hard mask, the first stopping layer, and the second stopping layer are each aluminum nitride, titanium nitride, or tantalum nitride. In an embodiment, the heating element is formed between the grating coupler 110 and the dual taper bridge (202). However, the heating element may be formed in other places in practical applications.

[0076] In block 1510, a metallization process is performed to electrically couple the silicon photonic circuitry and the heating element to contact pads (e.g., contact pads 1050). The metallization process may involve depositing or forming alternating layers of different dielectrics (or insulators), forming different metal layers, coupling the metal layers at different levels with vias, and forming contact pads.

[0077] In block 1512, the first stopping layer is exposed by performing a second etch and removed by performing a third etch. In an embodiment, the second etch is an RIE. In an embodiment, the third etch is a wet etch.

[0078] In block 1514, a waveguide (e.g., waveguide 1260) is formed over the dual taper bridge after the first stopping layer has been removed. The waveguide, the dual taper bridge, and the silicon photonic circuitry form an edge coupler (e.g., edge coupler 1280).

[0079] In block 1516, the second stopping layer is exposed by performing a fourth etch and removed by performing a fifth etch. In an embodiment, the fourth etch is an RIE. In an embodiment, the fifth etch is a wet etch.

[0080] In block 1518, the contact pads are opened to form the optical component. In an embodiment, the contact pads are opened by patterning and performing an etch. In an embodiment, the etch is an RIE. The contact pads are configured to electrically couple with, for example, a ball grid array (BGA) or other electronic structure.

[0081] FIG.16 is a schematic diagram of an optical device 1600 that may incorporate or include the optical component 1400 of FIG. 14. The optical device 1600 comprises ingress ports 1610 and receiver units (Rx) 1620 for receiving data; a processor, logic unit, or central processing unit (CPU) 1630 to process the data; transmitter units (Tx) 1640 and egress ports 16750 for transmitting the data; and a memory 1660 for storing the data. The optical device 1600 may also comprise optical-to-electrical (OE) components and electrical-to-optical (EO) components coupled to the ingress ports 1610, the receiver units 1620, the transmitter units 1640, and the egress ports 1650 for egress or ingress of optical or electrical signals.

[0082] The processor 1630 is implemented by hardware and software. The processor 1630 may be implemented as one or more CPU chips, cores (e.g., as a multi-core processor), field-programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), and digital signal processors (DSPs). The processor 1630 is in communication with the ingress ports 1610, receiver units 1620, transmitter units 1640, egress ports 1650, and memory 1660. The processor 1630 comprises an optical module 1670. The optical module 1670 is able to implement or utilize the optical component 1400. For instance, the optical module 1670 implements, processes, prepares, or provides the various functions of the optical component 1400. The inclusion of the optical module 1670 therefore provides a substantial improvement to the functionality of the optical device 1600 and effects a transformation of the optical device 1600 to a different state. Alternatively, the optical module 1670 is implemented as instructions stored in the memory 1760 and executed by the processor 1630.

[0083] The optical device 1600 may also include input and/or output (I/O) devices 1680 for communicating data to and from a user. The I/O devices 1680 may include output devices such as a display for displaying video data, speakers for outputting audio data, etc. The I/O devices 1780 may also include input devices, such as a keyboard, mouse, trackball, etc., and/or corresponding interfaces for interacting with such output devices.

[0084] The memory 1660 comprises one or more disks, tape drives, and solid-state drives and may be used as an over-flow data storage device, to store programs when such programs are selected for execution, and to store instructions and data that are read during program execution. The memory 1660 may be volatile and/or non-volatile and may be read-only memory (ROM), random access memory (RAM), ternary content-addressable memory (TCAM), and/or static random-access memory (SRAM).

[0085] FIG. 17 is a schematic diagram of an embodiment of a means for optical processing 1700. In an embodiment, the means for optical processing 900 is implemented in an optical device 1702 (e.g., optical device 1600 implementing optical component 1400). The optical device 1702 includes receiving means 1701. The receiving means 1701 is configured to receive an optical signal (e.g., light). The optical device 1702 includes transmission means 1707 coupled to the receiving means 1701. The transmission means 1707 is configured to transmit the optical signal.

[0086] The optical device 1702 includes a storage means 1703. The storage means 1703 is coupled to at least one of the receiving means 1701 or the transmission means 1707. The storage means 1703 is configured to store instructions. The optical device 1702 also includes processing

means 1705. The processing means 1705 is coupled to the storage means 1703. The processing means 1705 is configured to execute the instructions stored in the storage means 1703.

[0087] While several embodiments have been provided in the present disclosure, it may be understood that the disclosed systems and methods might be embodied in many other specific forms without departing from the spirit or scope of the present disclosure. The present examples are to be considered as illustrative and not restrictive, and the intention is not to be limited to the details given herein. For example, the various elements or components may be combined or integrated in another system or certain features may be omitted, or not implemented.

[0088] In addition, techniques, systems, subsystems, and methods described and illustrated in the various embodiments as discrete or separate may be combined or integrated with other systems, components, techniques, or methods without departing from the scope of the present disclosure. Other examples of changes, substitutions, and alterations are ascertainable by one skilled in the art and may be made without departing from the spirit and scope disclosed herein.

CLAIMS

What is claimed is:

1. A method of fabricating an optical component, comprising:

depositing a hard mask on a dielectric layer supported by a bridge layer of a photonic structure, the photonic structure including a grating coupler and silicon photonic circuitry;

performing a first etch to remove portions of the hard mask, the dielectric layer, and the bridge layer, a remaining portion of the bridge layer forming a dual taper bridge;

increasing a thickness of a second dielectric layer until the dual taper bridge and a remaining portion of the hard mask are covered by the second dielectric layer, and then removing a portion of the second dielectric layer to expose the hard mask disposed over the dual taper bridge;

increasing a thickness of the hard mask over the dual taper bridge to form a first stopping layer and over the grating coupler to form a second stopping layer, and depositing the hard mask to form a heating element;

performing a metallization process to electrically couple the silicon photonic circuitry and the heating element to contact pads;

exposing the first stopping layer by performing a second etch and removing the first stopping layer by performing a third etch;

forming a waveguide over the dual taper bridge after the first stopping layer has been removed, the waveguide, the dual taper bridge, and the silicon photonic circuitry forming an edge coupler;

exposing the second stopping layer by performing a fourth etch and removing the second stopping layer by performing a fifth etch; and

opening the contact pads to form the optical component.

2. The method of claim 1, the dielectric layer disposed between the waveguide and the dual taper bridge having a thickness of between about zero nanometers and about fifty nanometers, and a distance between a top surface of the grating coupler and a bottom surface of the second stopping layer is between about four hundred nanometers and about seven hundred nanometers.

3. The method of any of claims 1-2, the hard mask, the first stopping layer, and the second stopping layer being one of aluminum nitride (AlN), titanium nitride (TiN), and tantalum nitride (TaN).

4. The method of any of claims 1-3, one or more of the first etch, the second etch, and the fourth etch being a reactive ion etch (RIE).

5. The method of any of claims 1-4, one or more of the third etch and the fifth etch being a wet etch.

6. The method of any of claims 1-5, the grating coupler comprising a portion of the silicon photonic circuitry and a polysilicon structure.

7. The method of any of claims 1-6, further comprising forming a germanium (Ge) structure on the silicon photonic circuitry, the silicon photonic circuitry disposed on a buried oxide (BOX) layer, the buried oxide layer disposed on a semiconductor substrate.

8. The method of any of claims 1-7, the dual taper bridge comprising silicon nitride (SiN or Si_3N_4).

9. The method of any of claims 1-8, further comprising exposing the hard mask disposed over the dual taper bridge by performing chemical mechanical polishing (CMP).

10. The method of any of claims 1-8, the waveguide comprising a silicon oxynitride (SiON).

11. The method of any of claims 1-9, the silicon photonic circuitry, the dual taper bridge, and the waveguide of the edge coupler providing an adiabatic path for light to enter and exit the optical component.

12. An optical component, comprising:

a grating coupler disposed in a dielectric layer of a photonic structure, the grating coupler comprising a layer of polysilicon disposed on silicon photonic circuitry;

an edge coupler disposed in the dielectric layer of the photonic structure, the edge coupler comprising a waveguide, a dual taper bridge, and the silicon photonic circuitry; and

a heating element in the dielectric layer of the photonic structure, the heating element comprising a hard mask and disposed laterally between the grating coupler and the dual taper bridge.

13. The optical component of claim 12, the dielectric layer disposed between the waveguide and the dual taper bridge having a thickness of between about zero nanometers and about fifty nanometers.

14. The optical component of any of claims 12-13, the dielectric layer disposed above a top surface of the grating coupler having a thickness of between about four hundred nanometers and about seven hundred nanometers.

15. The optical component of any of claims 12-14, the hard mask one of aluminum nitride (AlN), titanium nitride (TiN), and tantalum nitride (TaN).

16. The optical component of any of claims 12-15, a portion of the silicon photonic circuitry supporting a germanium (Ge) structure.

17. The optical component of any of claims 12-16, the dual taper bridge comprising silicon nitride (SiN or Si_3N_4).

18. The optical component of any of claims 12-17, the waveguide comprising a silicon oxynitride (SiON).

19. The optical component of any of claims 12-18, the silicon photonic circuitry, the dual taper bridge, and the waveguide of the edge coupler providing an adiabatic path for light to enter and exit the optical component.

20. The optical component of any of claims 12-19, the photonic structure including a buried oxide (BOX) layer supported by a silicon substrate, and the photonic structure including metallization coupling the heating element and the silicon photonic circuitry to contact pads.

21. A means for fabricating an optical component, comprising:

means for depositing a hard mask on a dielectric layer supported by a bridge layer of a photonic structure, the photonic structure including a grating coupler and silicon photonic circuitry;

means for performing a first etch to remove portions of the hard mask, the dielectric layer, and the bridge layer, a remaining portion of the bridge layer forming a dual taper bridge;

means for increasing a thickness of a second dielectric layer until the dual taper bridge and a remaining portion of the hard mask are covered by the second dielectric layer and means for removing a portion of the second dielectric layer to expose the hard mask disposed over the dual taper bridge;

means for increasing a thickness of the hard mask over the dual taper bridge to form a first stopping layer and over the grating coupler to form a second stopping layer, and means for depositing the hard mask on the second dielectric layer to form a heating element;

means for performing a metallization process to electrically couple the silicon photonic circuitry and the heating element to contact pads;

means for exposing the first stopping layer by performing a second etch and removing the first stopping layer by performing a third etch;

means for forming a waveguide over the dual taper bridge after the first stopping layer has been removed, the waveguide, the dual taper bridge, and the silicon photonic circuitry forming an edge coupler;

means for exposing the second stopping layer by performing a fourth etch and removing the second stopping layer by performing a fifth etch; and

means opening the contact pads to form the optical component.

22. A system, comprising:

an optical component as in any of claims 12-20, the optical component configured to receive and transmit light; and

an optical fiber coupled to the optical component, the optical fiber configured to receive the light from the optical component and to transmit the light to the optical component.

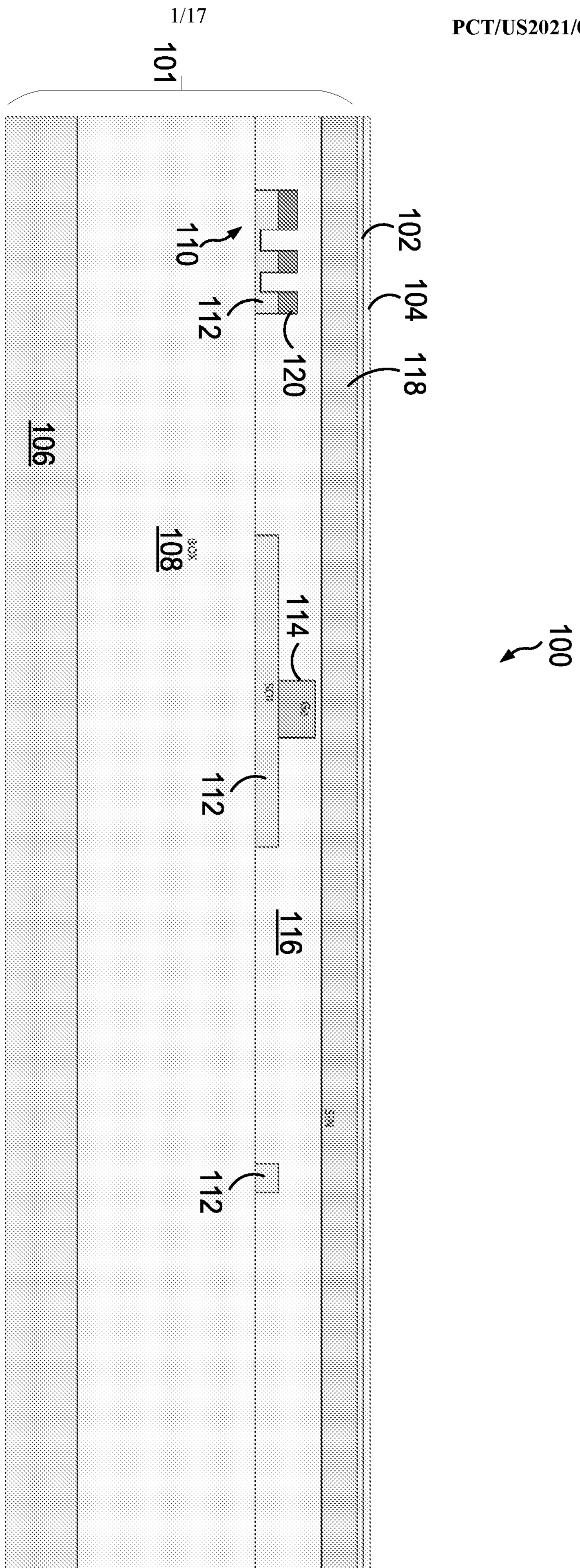

FIG. 1

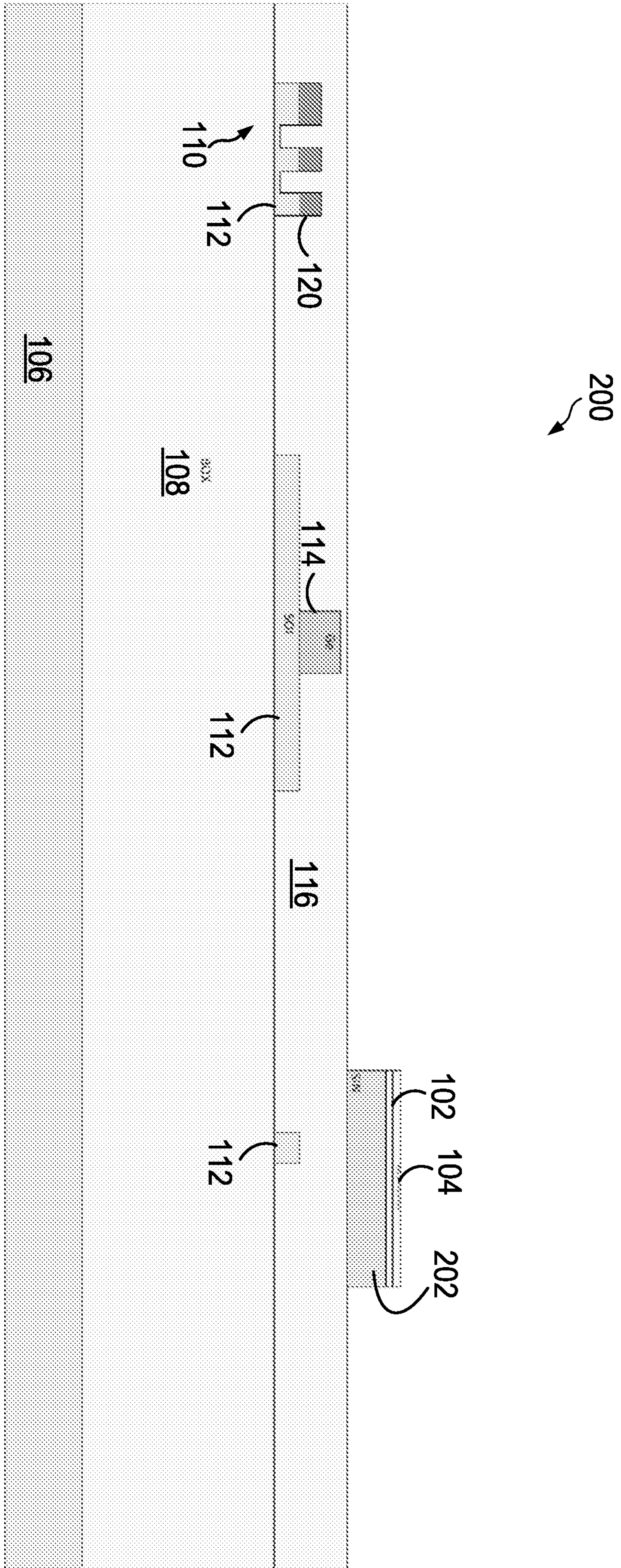

FIG. 2

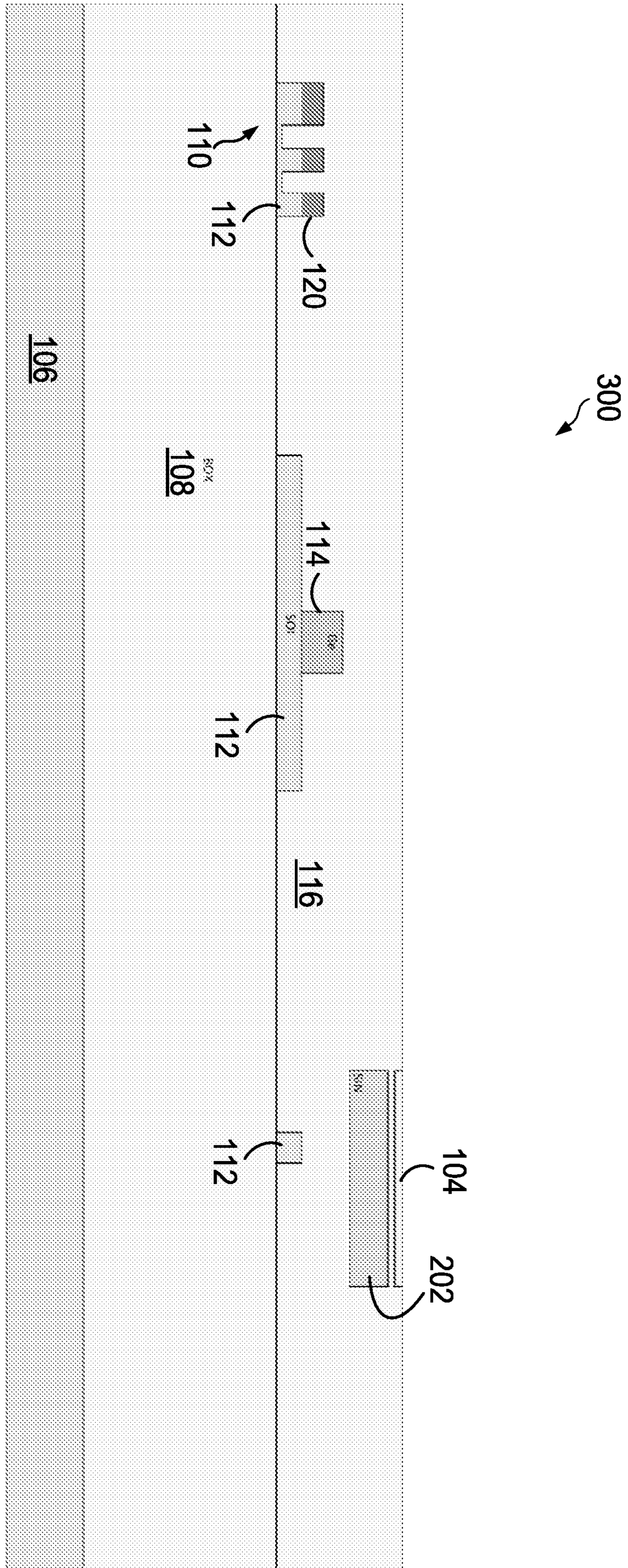

FIG. 3

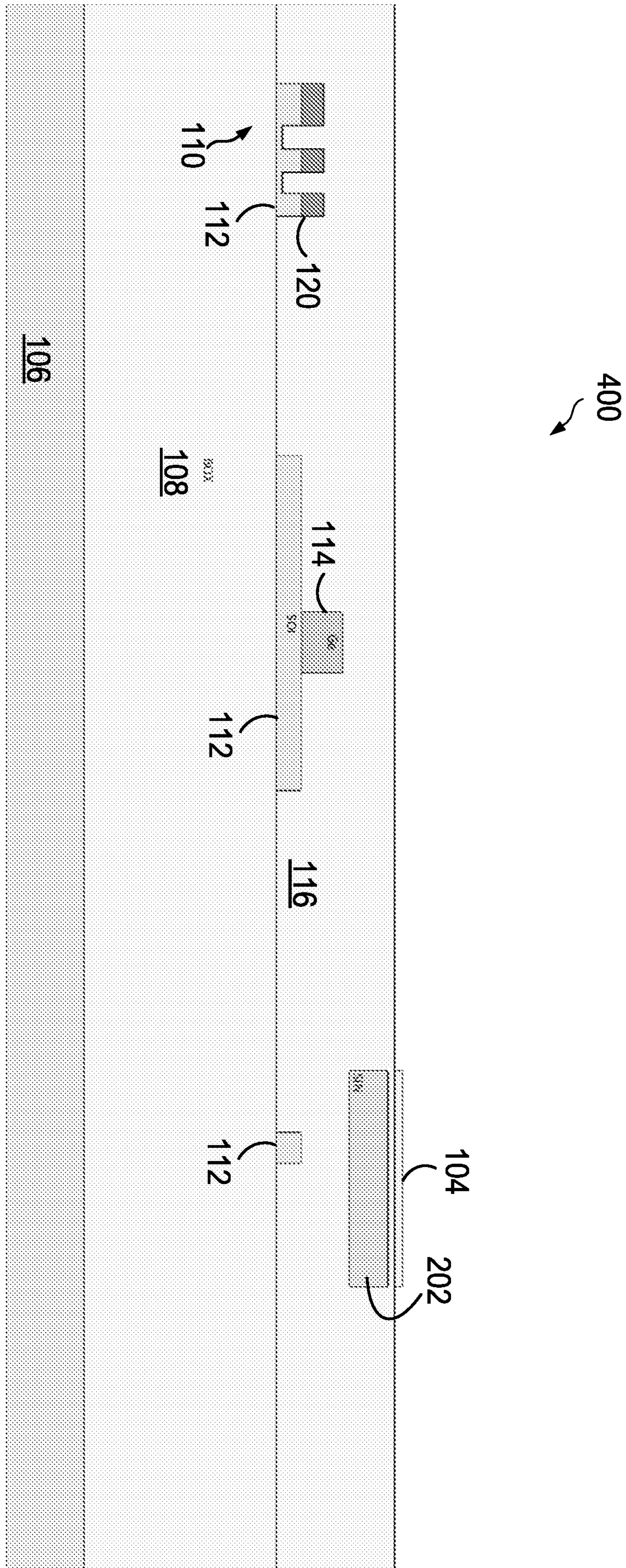

FIG. 4

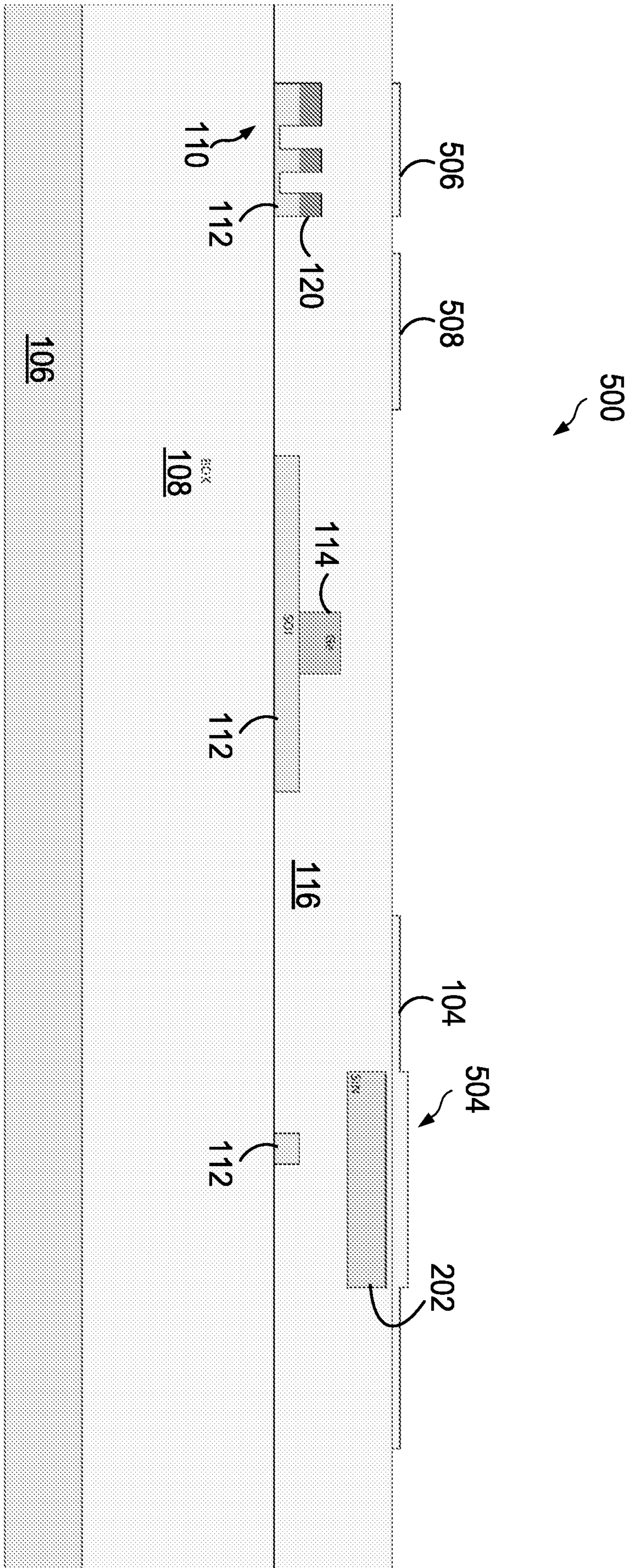

FIG. 5

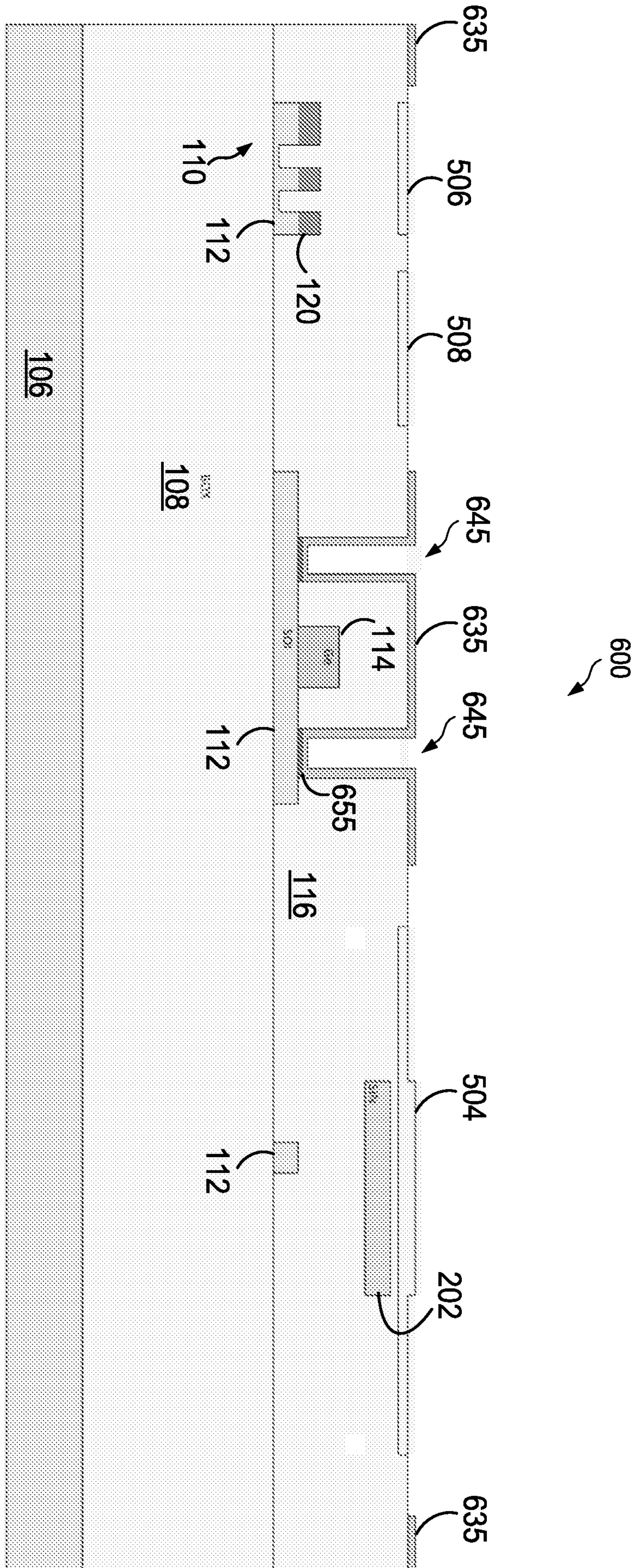

FIG. 6

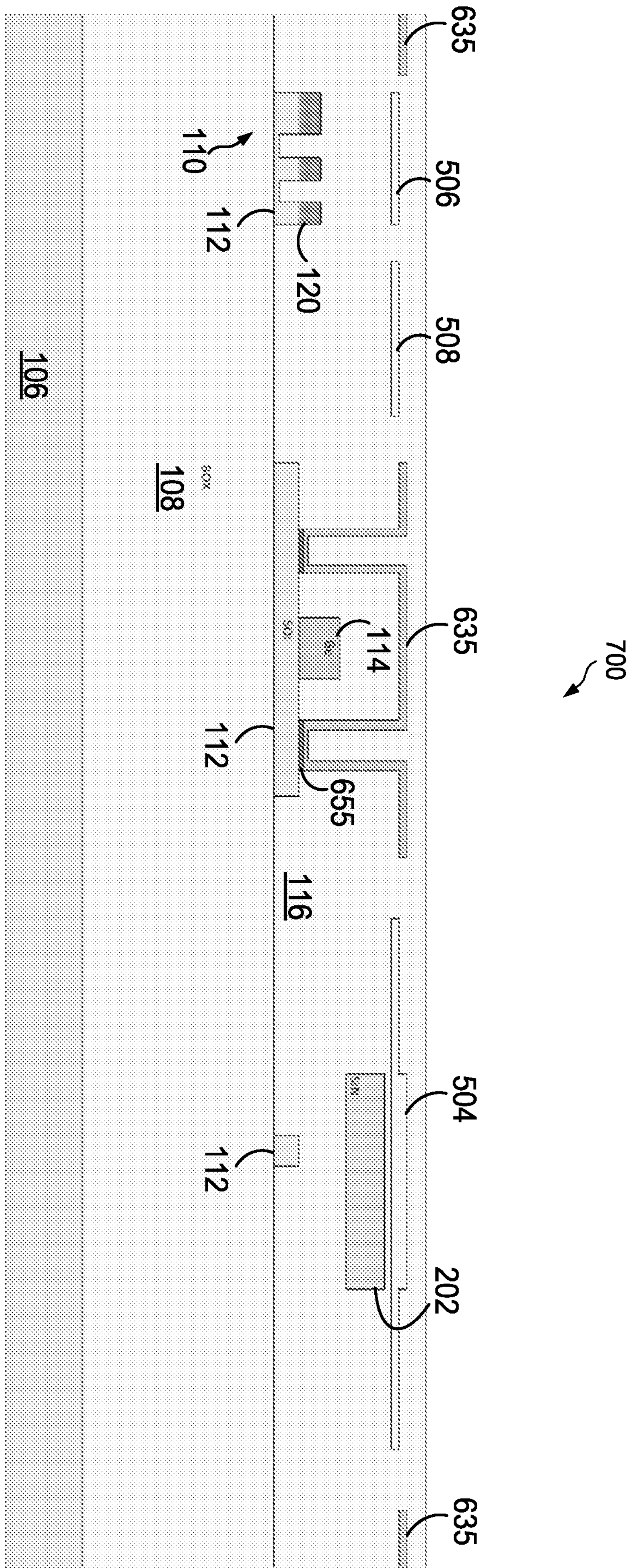

FIG. 7

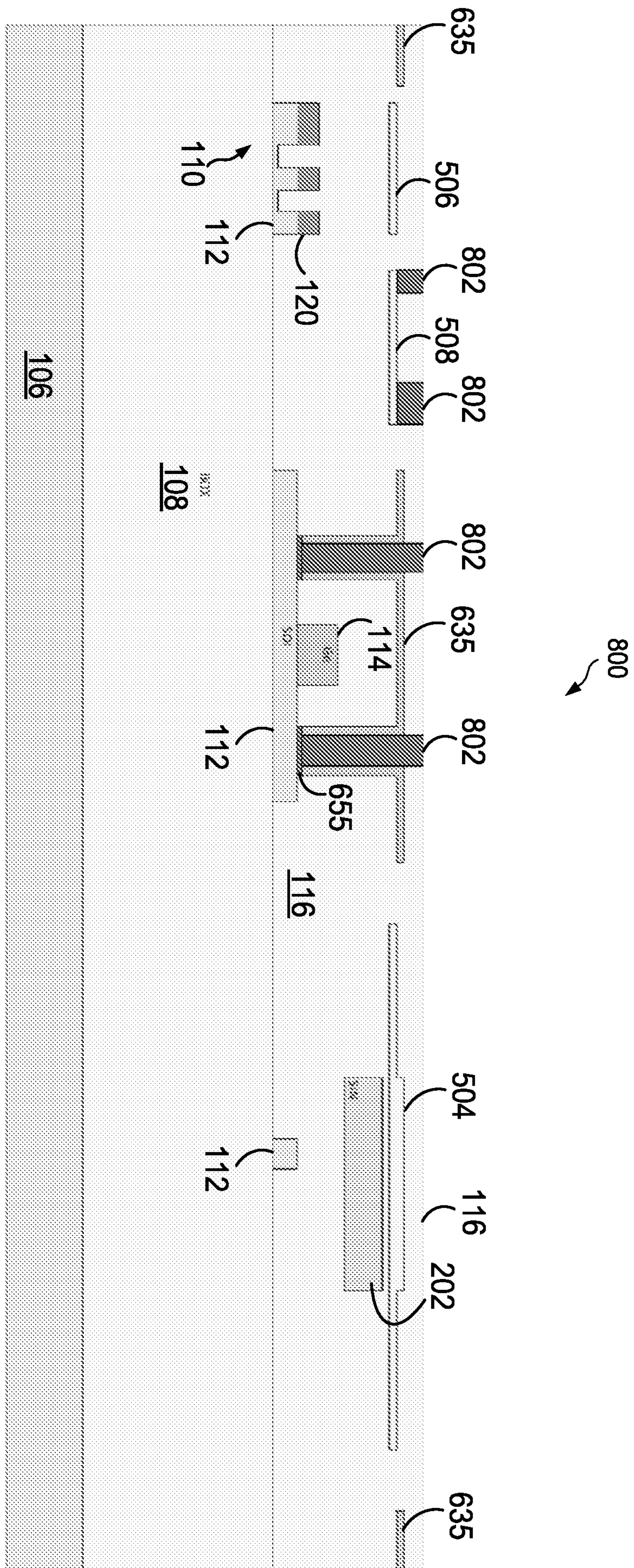

FIG. 8

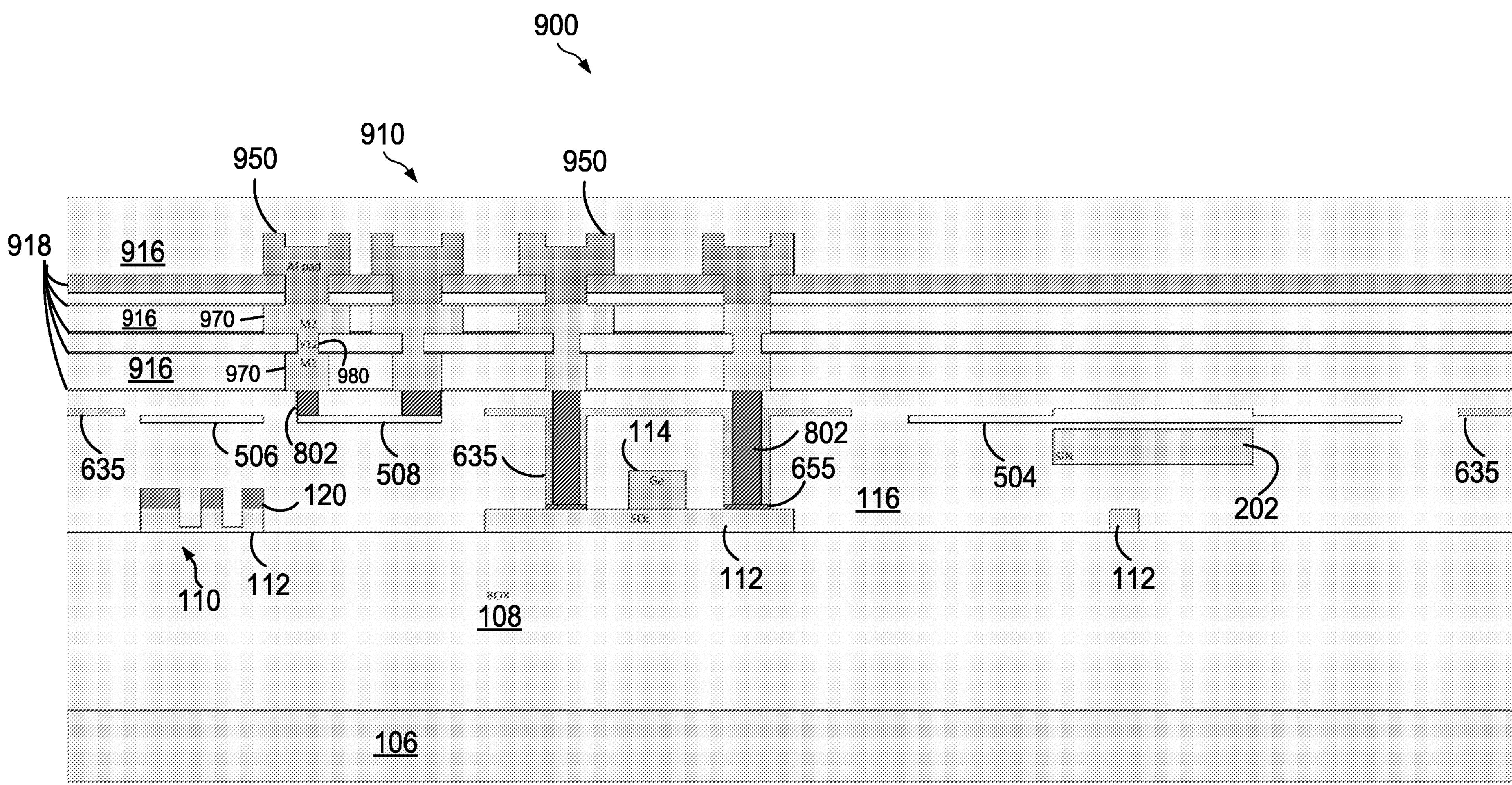

FIG. 9

FIG. 10

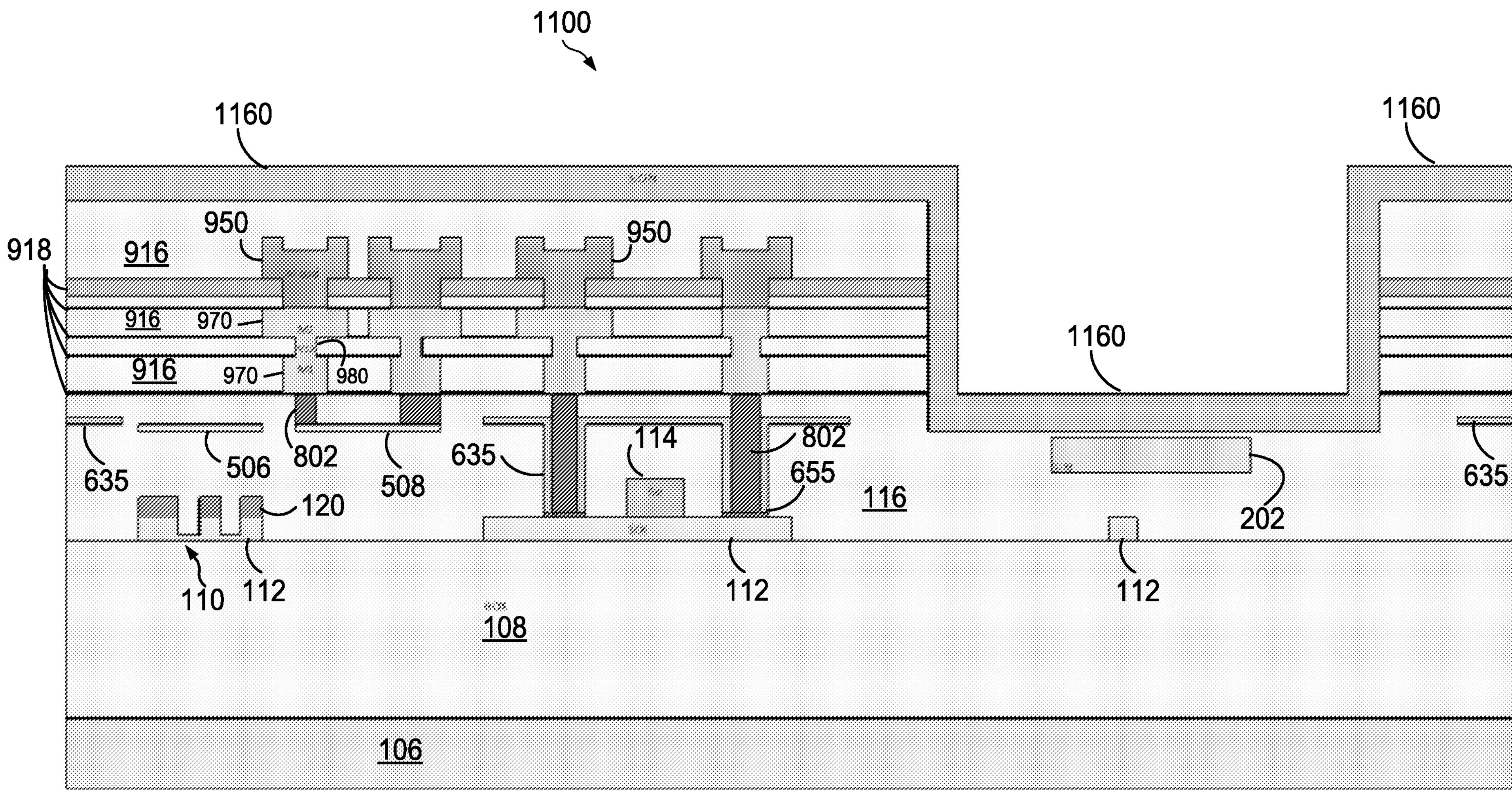

FIG. 11

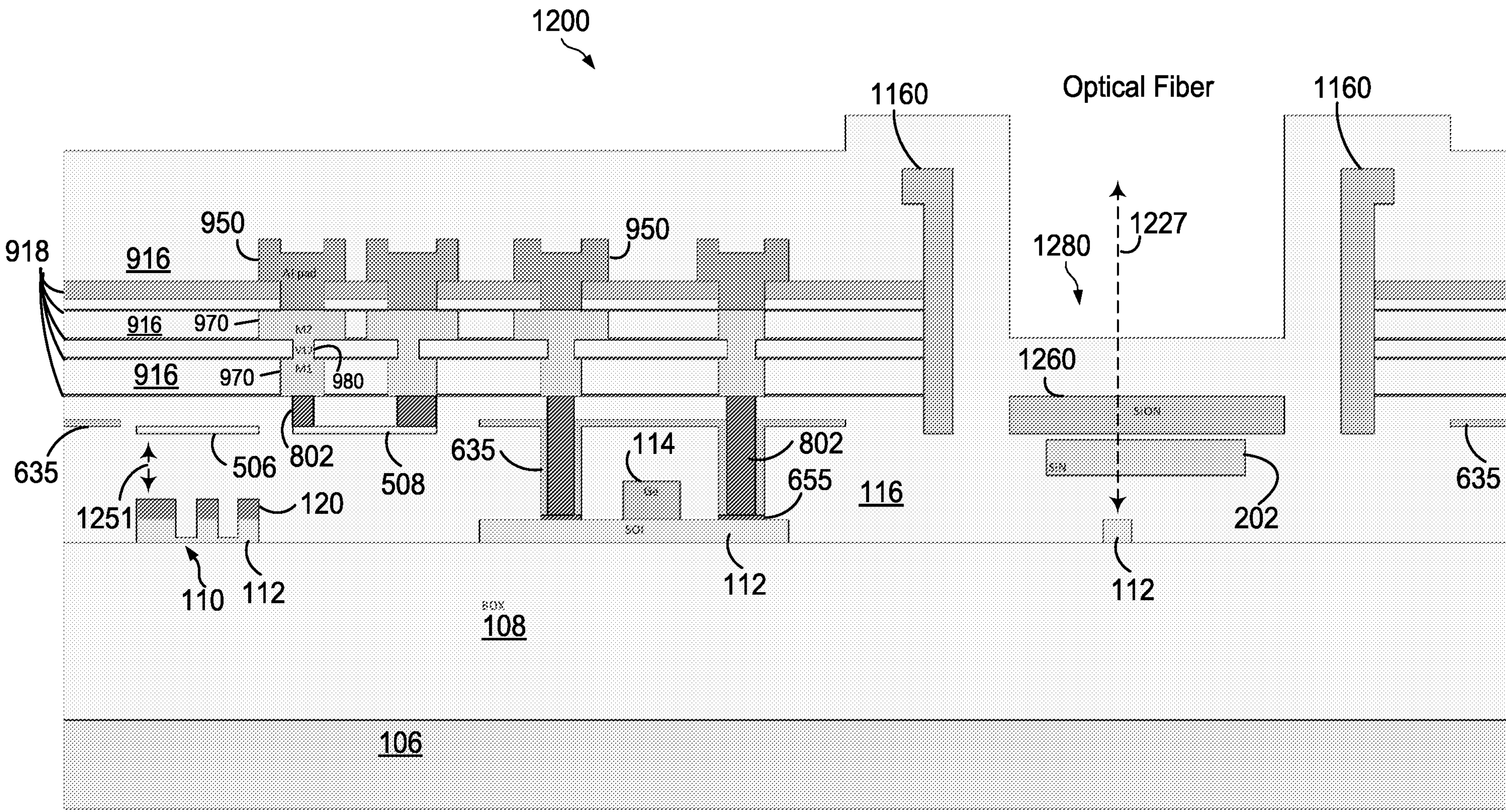

FIG. 12

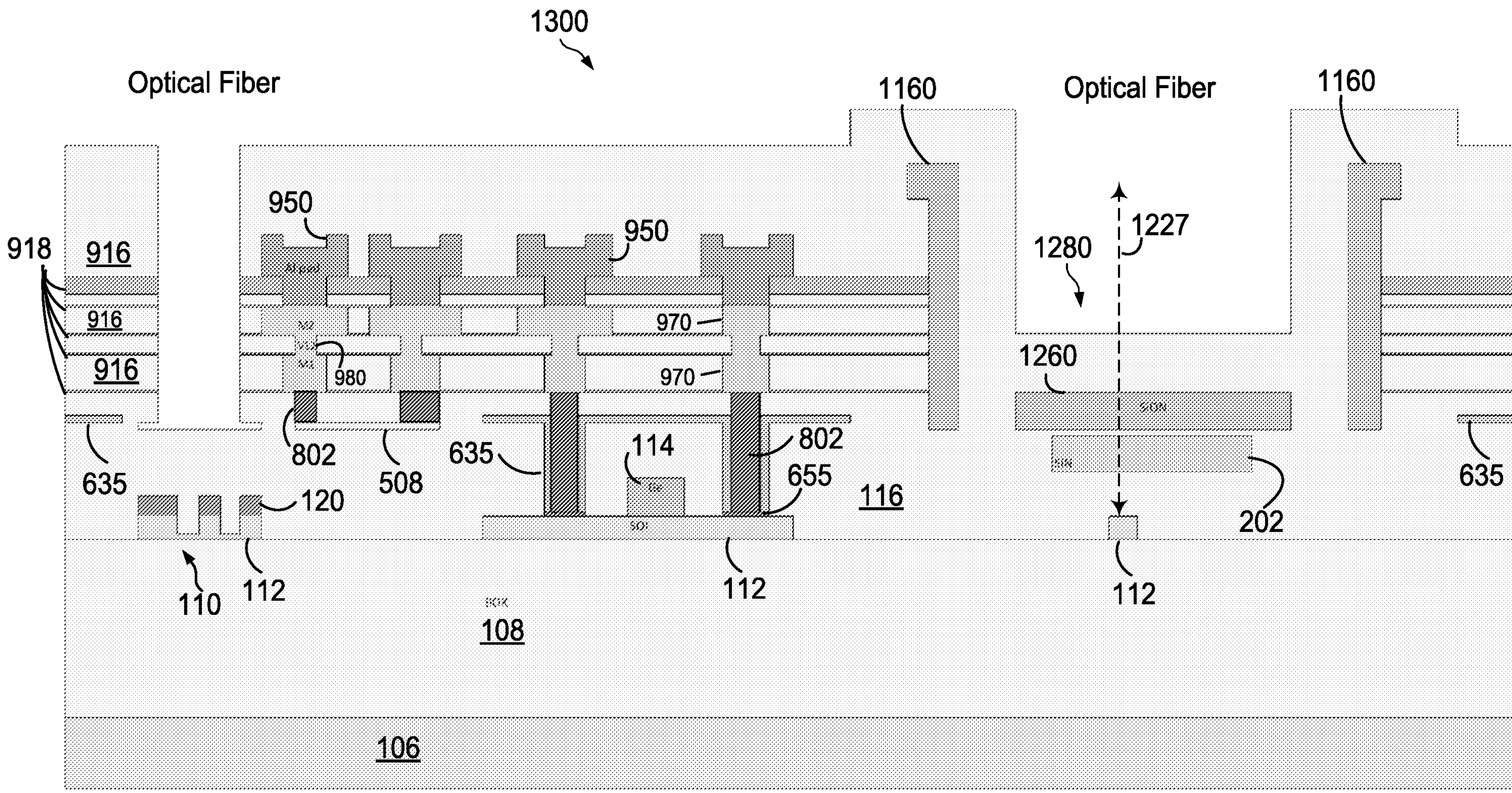

FIG. 13

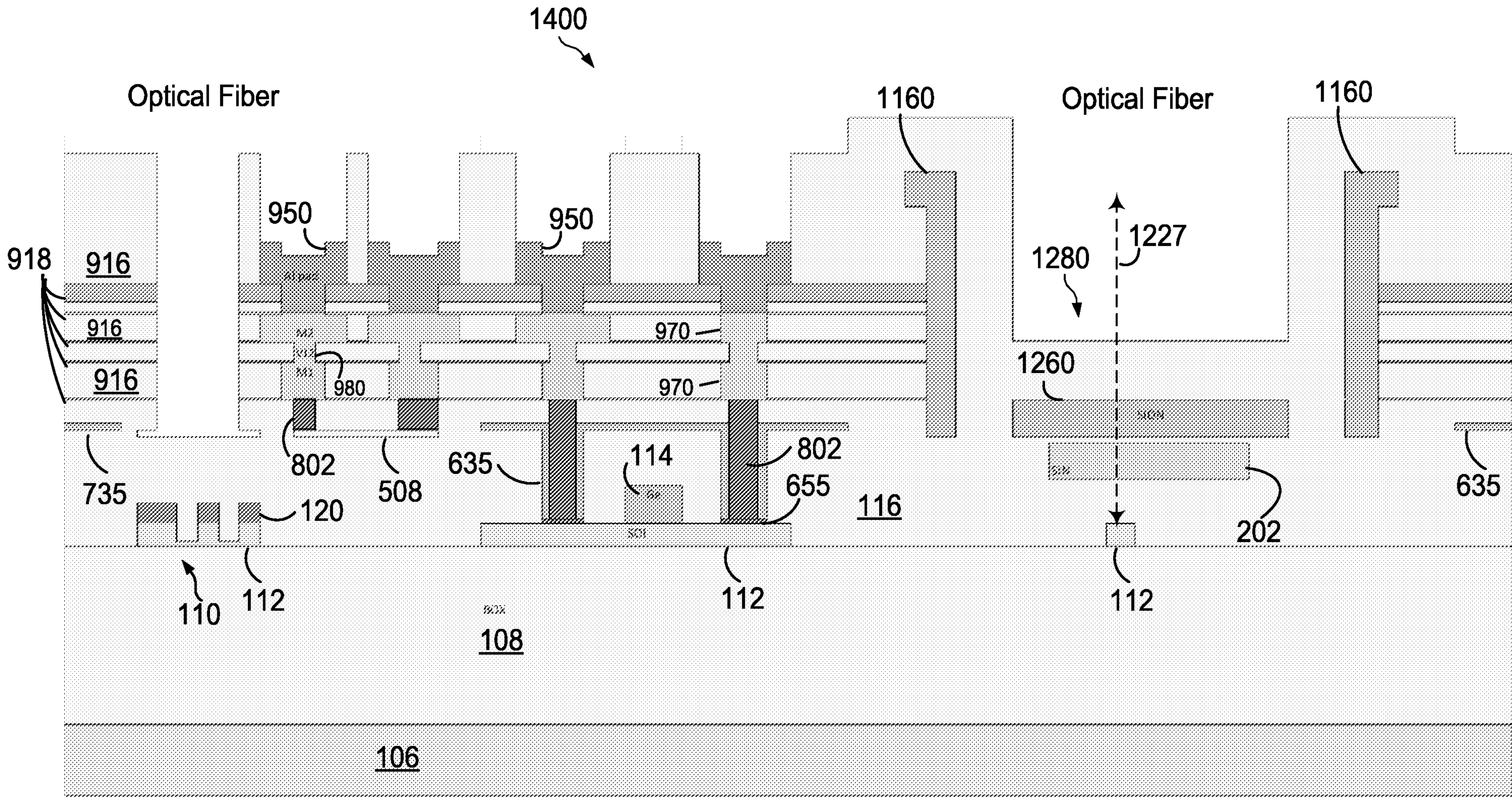

FIG. 14

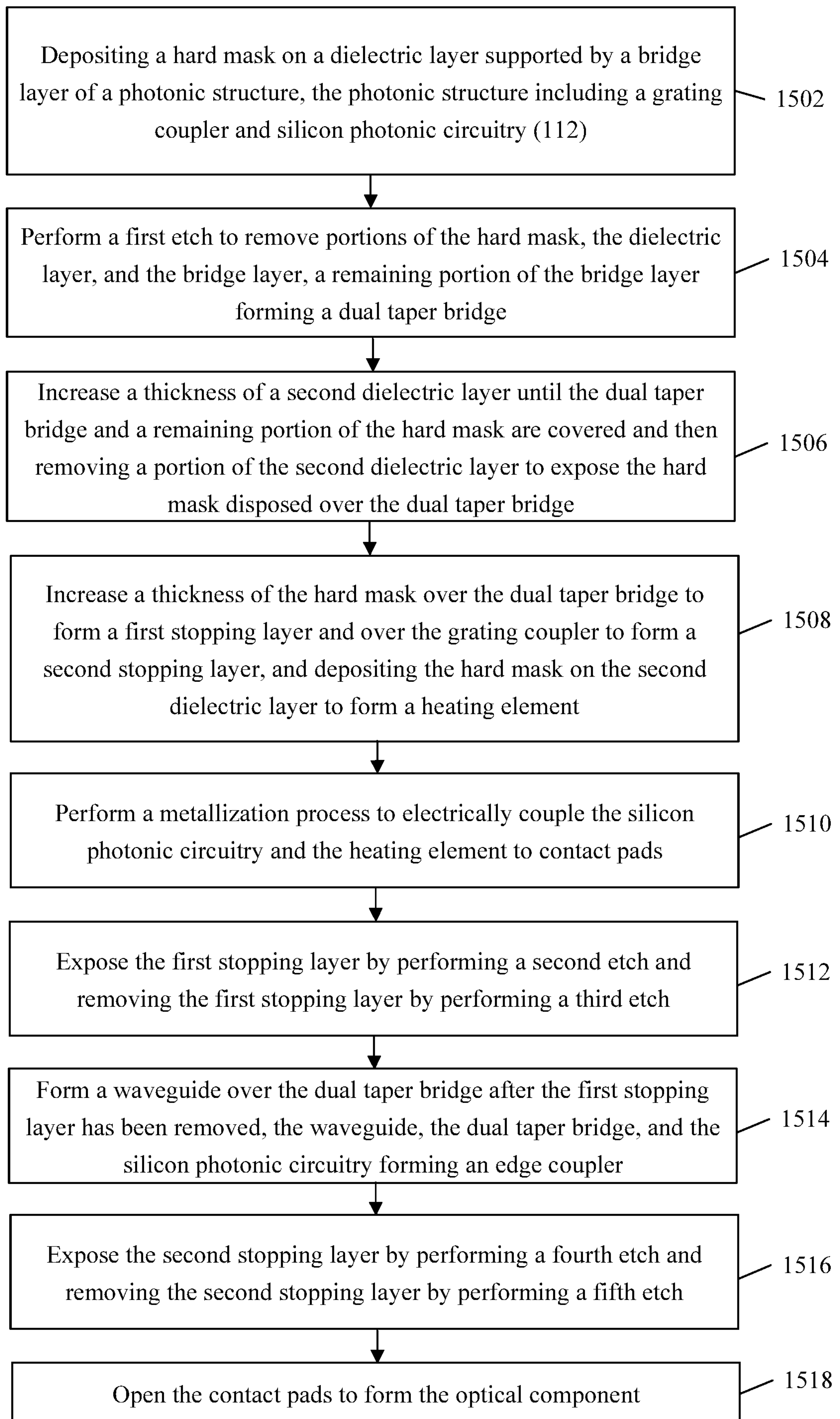

FIG. 15

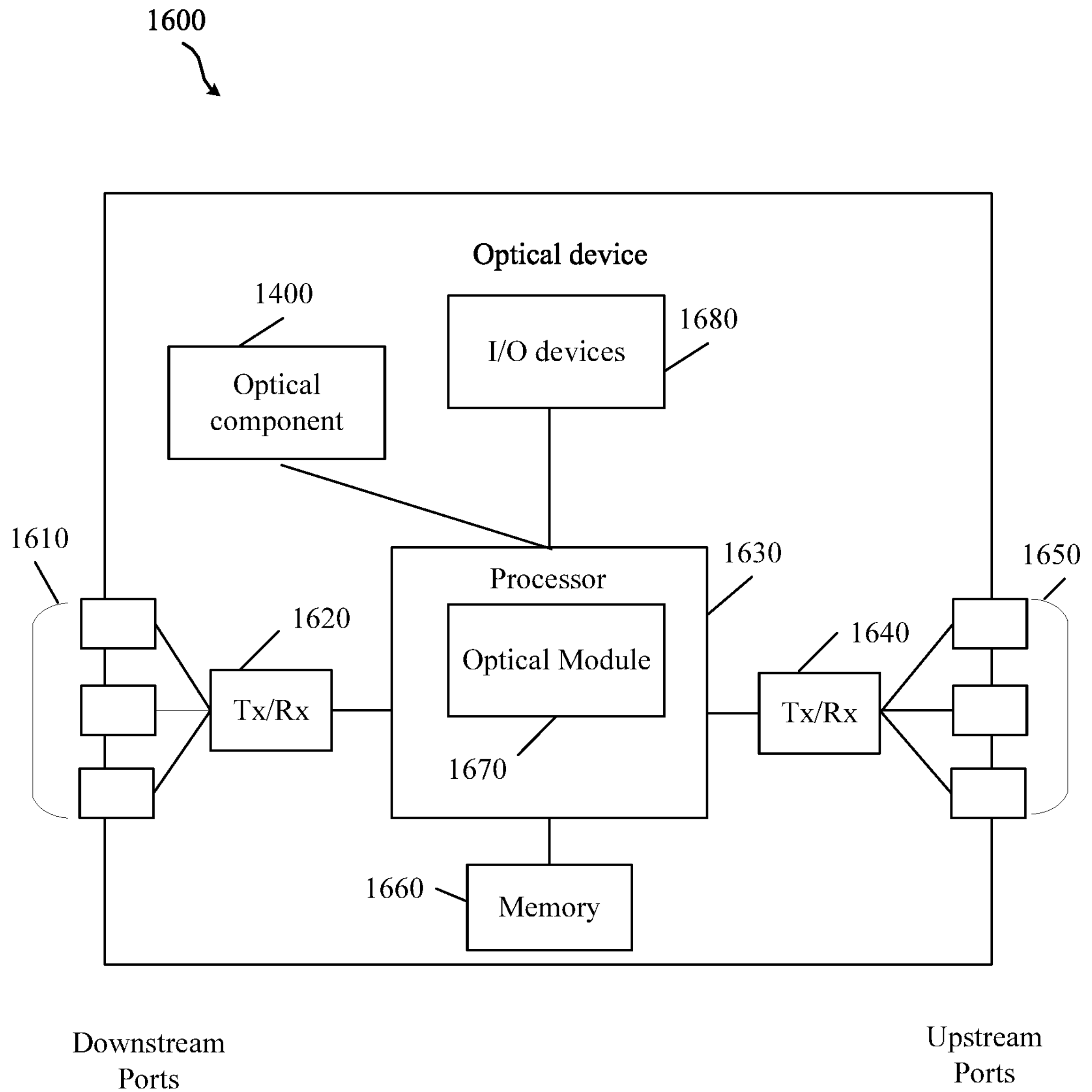

FIG. 16

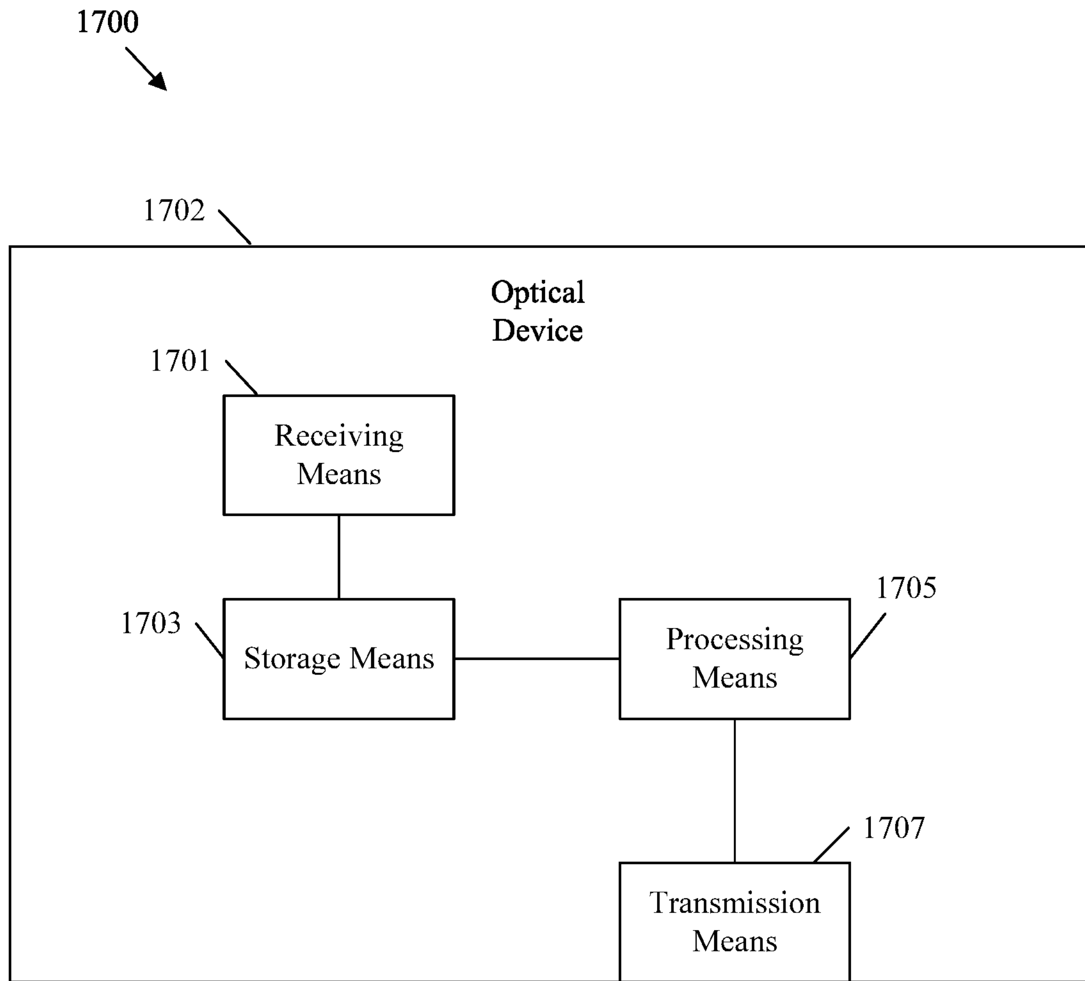

FIG. 17

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2021/042349

A. CLASSIFICATION OF SUBJECT MATTER
INV. G02B6/136
ADD.

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
G02B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EPO-Internal

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	figure 1 figures 2a-d figure 30 section 6.3 -----	1-11

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[x] Further documents are listed in the continuation of Box C.

[x] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance;; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance;; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 January 2022	26/01/2022

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Verbandt, Yves

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Form PCT/ISA/210 (second sheet) (April 2005)

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	WILMART QUENTIN ET AL: "Advanced Si photonics platform for high-speed and energy-efficient optical transceivers for datacom", SPIE PROCEEDINGS; [PROCEEDINGS OF SPIE ISSN 0277-786X], SPIE, US, vol. 11285, 26 February 2020 (2020-02-26), pages 112850B-112850B, XP060129040, DOI: 10.1117/12.2543748 ISBN: 978-1-5106-3673-6 -----	1-22

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2021/042349

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