(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
11 February 2021 (11.02.2021)

(10) International Publication Number
WO 2021/025914 A1

(51) International Patent Classification:
H01L 21/822 (2006.01) *H01L 27/06* (2006.01) *H01L 21/02* (2006.01) *H01L 21/67* (2006.01) *H01L 21/8238* (2006.01)

(21) International Application Number: PCT/US2020/043986

(22) International Filing Date: 29 July 2020 (29.07.2020)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
62/883,192 06 August 2019 (06.08.2019) US
16/705,485 06 December 2019 (06.12.2019) US

(71) Applicant: **TOKYO ELECTRON LIMITED** [JP/JP]; Akasaka Biz Tower, 3-1 Akasaka 5-chome, Minato-ku, Tokyo 107-6325 (JP).

(71) Applicant *(for JP only)*: **TOKYO ELECTRON U.S. HOLDINGS, INC.** [US/US]; 2400 Grove Boulevard, Austin, Texas 78741 (US).

(72) Inventors: **FULFORD, H. Jim**; 2400 Grove Blvd., Austin, Texas 78741 (US). **GARDNER, Mark**; 2400 Grove Blvd., Austin, Texas 78741 (US). **SMITH, Jeffrey**; Suite 214, NanoFab 300 South 255 Fuller Rd., Albany, New York 12203 (US). **LIEBMANN, Lars**; Suite 214, NanoFab 300 South 255 Fuller Rd., Albany, New York 12203 (US). **CHANEMOUGAME, Daniel**; Suite 214, NanoFab 300 South 255 Fuller Rd., Albany, New York 12203 (US).

(54) Title: HIGH DENSITY LOGIC FORMATION USING MULTI-DIMENSIONAL LASER ANNEALING

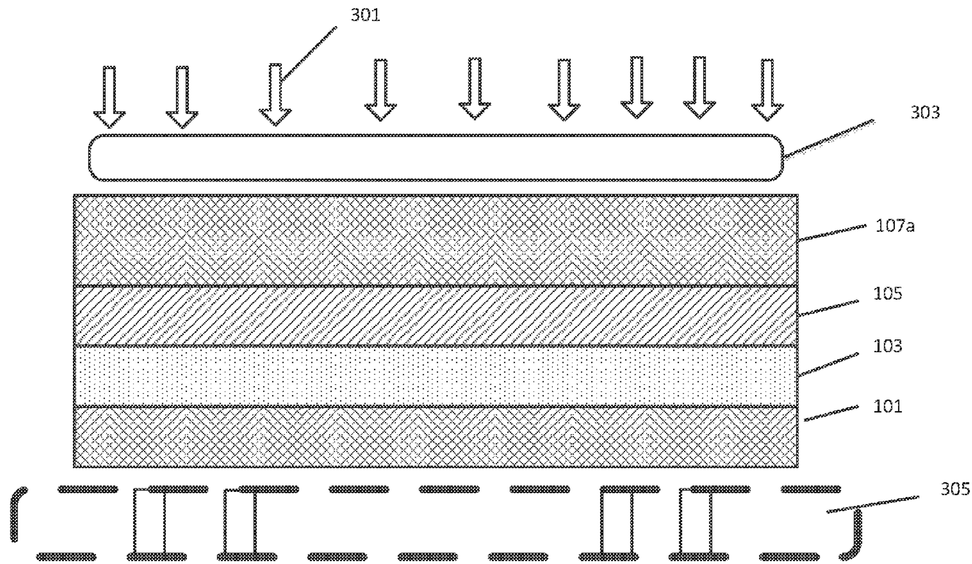

FIG. 3

(57) Abstract: A method of forming transistor devices is described that includes forming a first transistor plane on a substrate, the first transistor plane including at least one layer of epitaxial film adaptable for forming channels of field effect transistors, depositing a first insulator layer on the first transistor plane, depositing a first layer of polycrystalline silicon on the first insulator layer, annealing the first layer of polycrystalline silicon using laser heating. The laser heating increases grain size of the first layer of polycrystalline silicon. The method further includes forming a second transistor plane on the first layer of polycrystalline silicon, the second transistor plane being adaptable for forming channels of field effect transistors, depositing a second insulator layer on the second transistor plane, depositing a second layer of polycrystalline silicon on the second insulator layer, and annealing the second layer of polycrystalline silicon using laser heating.

[Continued on next page]

(74) Agent: MATHER, Joshua D.; Tokyo Electron U.S. Holdings, Inc., 2400 Grove Boulevard, Austin, Texas 78741 (US).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, IT, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Published:

— *with international search report (Art. 21(3))*

HIGH DENSITY LOGIC FORMATION USING MULTI-DIMENSIONAL LASER ANNEALING

CROSS-REFERENCE TO RELATED APPLICATIONS

5 This application claims the benefit of priority to provisional application no. 62/883,192 filed August 6, 2019 and application no. 16//705,485 filed December 6, 2019, the entire contents of which are incorporated herein by reference.

BACKGROUND

10 TECHNICAL FIELD

The present disclosure is directed to microelectronic devices including semiconductor devices, transistors, and integrated circuits, including methods of microfabrication.

DESCRIPTION OF THE RELATED ART

15 The "background" description provided herein is for the purpose of generally presenting the context of the disclosure. Work of the presently named inventors, to the extent it is described in this background section, as well as aspects of the description which may not otherwise qualify as prior art at the time of filing, are neither expressly or impliedly admitted as prior art against the present invention.

20 This disclosure relates to microelectronic devices including semiconductor devices, transistors, and integrated circuits, including methods of microfabrication.

In the manufacture of a semiconductor device (especially on the microscopic scale), various fabrication processes are executed such as film-forming depositions, etch mask creation, patterning, material etching and removal, and doping treatments. These processes

25 are performed repeatedly to form desired semiconductor device elements on a substrate.

Historically, with microfabrication, transistors have been created in one plane, with wiring/metallization formed above the active device plane, and have thus been characterized as two-dimensional (2D) circuits or 2D fabrication. Scaling efforts have greatly increased the number of transistors per unit area in 2D circuits, yet scaling efforts are running into greater challenges as scaling enters single digit nanometer semiconductor device fabrication nodes. Subsequently, while traditional CMOS processes improves signal propagation speed, scaling from current manufacturing and chip-design technologies is becoming more difficult and costly. Semiconductor device fabricators have expressed a desire for three-dimensional (3D) semiconductor circuits in which transistors are stacked on top of each other.

3D integration, i.e. the vertical stacking of multiple devices, aims to overcome scaling limitations experienced in planar devices by increasing transistor density in volume rather than area. Although device stacking has been successfully demonstrated and implemented by the flash memory industry with the adoption of 3D NAND, application to random logic designs is substantially more difficult. 3D integration for logic chips (CPU (central processing unit), GPU (graphics processing unit), FPGA (field programmable gate array, SoC (System on a chip)) is being pursued.

There is a need for 3D logic circuits for future high-density logic circuits for maximum use of silicon base area stacked vertically.

It is one object of the present disclosure to describe a method to form multiple planes of transistors. Other objectives include applying laser annealing to change polycrystalline silicon into single-crystal silicon. The heating amount and duration is targeted to the polysilicon layer so that the underlying layers are not heated above a predetermined temperature.

SUMMARY

In an exemplary embodiment, a method of forming transistor devices is described which includes forming a first transistor plane on a substrate, the first transistor plane including a plurality of field effect transistors, depositing a first insulator layer on the first transistor plane, depositing a first layer of polycrystalline silicon on the first insulator layer; and annealing the first layer of polycrystalline silicon using laser heating, the laser heating increasing grain size of the first layer of polycrystalline silicon.

In another exemplary embodiment, a method of forming transistor devices is described that includes forming a first transistor plane on a substrate, the first transistor plane including at least one layer of epitaxial film adaptable for forming channels of field effect transistors, depositing a first insulator layer on the first transistor plane, depositing a first layer of polycrystalline silicon on the first insulator layer, annealing the first layer of polycrystalline silicon using laser heating, the laser heating increasing grain size of the first layer of polycrystalline silicon, forming a second transistor plane on the first layer of polycrystalline silicon having the increased grain size, the second transistor plane being adaptable for forming channels of field effect transistors, depositing a second insulator layer on the second transistor plane, depositing a second layer of polycrystalline silicon on the second insulator layer, and annealing the second layer of polycrystalline silicon using laser heating, the laser heating increasing grain size of the second layer of polycrystalline silicon.

Note that this summary section does not specify every embodiment and/or incrementally novel aspect of the present disclosure or claimed invention. Instead, this summary only provides a preliminary discussion of different embodiments and corresponding points of novelty over conventional techniques. For additional details and/or possible perspectives of the invention and embodiments, the reader is directed to the Detailed

Description section and corresponding figures of the present disclosure as further discussed below.

BRIEF DESCRIPTION OF THE DRAWINGS

5 A more complete appreciation of this disclosure and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

FIG. 1 is a cross-sectional schematic view of an example substrate segment herein;

10 FIG. 2 illustrates a layer of silicon dioxide is deposited on the first transistor plane;

FIG. 3 illustrates a laser anneal exposure converting the polysilicon to an epitaxial-like silicon after the laser anneal;

FIG. 4 illustrates an example result after polishing the layer of epitaxial-like silicon;

FIG. 5 illustrates a second transistor plane formed on the anneal and polished layer of 15 crystalline silicon;

FIG. 6 illustrates how techniques herein can be repeated for any number of transistor planes; and

FIG. 7 illustrates that with polysilicon converted to epitaxial-like silicon, what is supported is growing a new stack of silicon layers.

20

DETAILED DESCRIPTION

In the drawings, like reference numerals designate identical or corresponding parts throughout the several views. Further, as used herein, the words “a,” “an” and the like generally carry a meaning of “one or more,” unless stated otherwise. The drawings are

generally drawn to scale unless specified otherwise or illustrating schematic structures or flowcharts.

Furthermore, the terms “approximately,” “approximate,” “about,” and similar terms generally refer to ranges that include the identified value within a margin of 20%, 10%, or preferably 5%, and any values therebetween.

Aspects of this disclosure include a method to form multiple planes of transistors. This includes enabling greater than 20 3D nanoplanes of high quality silicon base substrates followed by enabling processing including laser treatment, cleans, CMP (chemical-mechanical polishing), and future epitaxial stacks as several optional embodiments. The multiple transistor planes herein are enabled by laser annealing to change polycrystalline silicon by increasing grain size, making the polycrystalline silicon function more like epitaxial silicon or monocrystalline silicon. This enables growing additional epitaxial layers for more transistor planes including gate-all-around transistor devices. Each transistor plane can contain a film stack for making CFET (nmos over pmos) nanoplane layers. Each additional layer is started by capping with an oxide or other insulator, depositing polycrystalline silicon, using a laser anneal to convert to epitaxial-like silicon, followed by formation of a given transistor plane, which could be logic and/or memory. For purposes of this disclosure, epitaxial-like silicon means a silicon crystal layer on which epitaxial crystal growth can be performed. Epitaxial-like silicon may be any crystalline silicon that can function as epitaxial silicon, including single crystal silicon, which is also referred to as monocrystalline silicon.

Of course, the order of discussion of the different steps as described herein has been presented for clarity sake. In general, these steps can be performed in any suitable order. Additionally, although each of the different features, techniques, configurations, etc. herein may be discussed in different places of this disclosure, it is intended that each of the concepts

can be executed independently of each other or in combination with each other. Accordingly, the present invention can be embodied and viewed in many different ways.

3D integrated circuits address the scaling challenge by stacking 2D dies and connecting them in the 3rd dimension. A common form of 3D integrated circuit design has been wafer bonding. Wafer bonding is a method where several thin-film devices are bonded cumulatively, which allows a large number of device layers. The method involves fabrication of separate devices in separate wafers, reduction in the thickness of the wafers, providing front and back leads, and connecting the thinned die to each other. The method has been used to fabricate 3D integrated circuits with more than three active layers. 3D integrated circuits are currently used for NAND flash memory in mobile devices. However, the demand for smaller packages and the move to multi-dimensional planes of logic as well as memory requires alternative approaches to fabrication.

As one alternative to wafer bonding, monolithic 3D integrated circuits are built in layers on a single semiconductor wafer. With monolithic 3D integrated circuits, there is no need for aligning, thinning, bonding, or through silicon Vias. However, creation of multiple thin layers of defect free silicon requires utilizing low temperature bonding and placing layers on top of active transistor circuitry.

In order to make multi-dimensional planes of logic and memory, a first transistor plane is formed on a substrate. In practice, monocrystalline silicon is produced from a seed crystal, then resulting monocrystalline ingots are sliced into wafers and polished, which is an expensive, time consuming process. The transistor plane is formed through microfabrication processes. It is preferable that this transistor plane be for any type of transistor or logic or memory. After forming the first transistor plane, polycrystalline silicon is deposited on this first transistor plane. However, polysilicon is not desirable as a material for integrated circuits. A single crystal is critical for electronics, since grain boundaries, impurities, and

crystallographic defects can significantly impact the local electronic properties of the material, which in turn affects the functionality, performance, and reliability of the logic devices by interfering with their proper operation.

In 2D semiconductor fabrication, the single crystal substrate is used for epitaxial growth and formation of transistor channels. In particular, semiconductor films are grown epitaxially on semiconductor substrate wafers. For the case of epitaxial growth of a planar film atop a substrate wafer, the epitaxial film's lattice will have a specific orientation relative to the substrate wafer's crystalline lattice such as the [001] Miller index of the film aligning with the [001] index of the substrate.

In order to continue this fabrication process for additional transistor layers, it is necessary to control crystal orientation above a transistor layer. As a solution, a laser annealing process has been developed that enables conversion of polycrystalline silicon into single crystal silicon without impacting the transistor layers below the polycrystalline silicon. In some embodiments, multiple transistor planes disclosed herein are enabled by laser annealing to convert polycrystalline silicon by increasing grain size, making the polycrystalline silicon function more like epitaxial silicon or monocrystalline silicon. This enables growing additional epitaxial layers for more transistor planes including gate-all-around transistor devices.

In one embodiment, a first transistor plane is formed on a substrate in a conventional 2D fabrication process. This transistor plane can be for any type of transistor or logic or memory. After forming the first transistor plane, polycrystalline silicon is deposited on the first transistor plane. The polycrystalline silicon is converted, using a laser anneal process on upper base substrate planes, to be epitaxial-like silicon. Then a subsequent transistor plane can be formed, capped with polycrystalline silicon and converted to epitaxial-like silicon. This process may be repeated for any number of transistor planes.

In an exemplary embodiment, one CFET fabrication process uses a silicon substrate and epitaxial grows alternating layers of SiGe and Si up to 8 to 12 total layers. Limiting the height and/or number of layers in the epitaxial stack can be beneficial for better quality films. Then the SiGe is removed in the stack sandwich such that 4 to 6 layers of transistor planes are available to make logic as gate-all-around (GAA) field effect transistors. Two nanoplanes of transistors can be tied together to make an NMOS or PMOS device. Thus, this fabrication process only allows for a total of three actual transistor planes. In other words, a vertical stack of three FETs is possible while keeping within quality specifications. Three levels of transistors, however, are insufficient to fully enable 3D logic formation for cost effective solutions. For volume scaling, more and more layers of transistors will be required.

Techniques disclosed herein enable 3D planes of transistors to be at least greater than twenty planes or levels of high quality FETs. Each plane of transistors can be used to form any type of transistor including, but not limited to, CFET, planar, FinFET, and memory. Techniques herein can then be expanded as volume scaling increases.

One embodiment will now be described with reference to the figures. FIG. 1 is a cross-sectional schematic view of an exemplary substrate segment herein. A silicon substrate or SOI (silicon-on-insulator) substrate 101 is received. A first transistor plane (circuit plane) 103 is fabricated on the substrate 101. This first plane can include fully-formed field effect transistors through metal layer 1 routing or this transistor plane can include the layer(s) to form channels of transistor devices subsequently. The transistor plane can be CFET devices, FinFet, Memory, Logic or any devices. Optionally, CFET planes are formed prior to etching an entire stack of a given transistor plane or of multiple, separated transistor planes. Accordingly, in a preferred embodiment, there is no restriction on epitaxial stack growth temperature. Each plane of silicon can be used for any type of transistor or memory element without restriction. In one example, forming this first transistor plane can include growing 8

to 12 layer of alternating SiGe/Si using an epitaxial growth process with substantially no temperature limitations.

After forming the first transistor plane 103, an insulator is deposited on the first transistor plane. FIG. 2 illustrates a layer of silicon dioxide 105 is deposited on the first
5 transistor plane 103. Other types of oxides or dielectric films can be selected. For most applications, an insulator is deposited to a preferred thickness of 500 to 3000 Angstroms. Next, polycrystalline silicon (also referred to as polysilicon) is deposited. Deposition temperature is preferably below 580°C. Polysilicon 107 can be deposited using LPCVD (low-pressure chemical vapor deposition), PECVD (plasma-enhanced chemical vapor
10 deposition), sputter deposition, or any polysilicon deposition method (even at room temperature).

At this point, a first transistor plane 103 has been formed and insulated, and polysilicon 107 is now on the working surface of the substrate. Polysilicon, however, is not satisfactory as a material for epitaxial growth and transistor channel materials.
15 Monocrystalline silicon is satisfactory for epitaxial growth. With techniques disclosed herein, a scanning laser crystallization treatment is executed. This laser annealing process increases grain size of the polysilicon so that the resulting layer has sufficiently large grain boundaries that the resulting layer functions essentially like a layer of monocrystalline silicon to support epitaxial growth of additional silicon layers. FIG. 3 illustrates a laser anneal
20 exposure that converts the polysilicon to an epitaxial-like silicon after the laser anneal.

For the scanning laser crystallization treatment, any type of laser can be selected for use. Example wavelengths for silicon treatment are typically 100nm to 800nm. Either the wafer can be held stationary and laser scanned across the wafer, or the laser can be fixed in position while the substrate (wafer) is rotated or moved through the laser. Such scanning
25 motion allows for any type of laser system to be used. As can be appreciated, an amount of

energy delivered, scanning rate, and laser system will depend on a given stack/area to be re-crystallized.

By way of a non-limiting specific example, a laser wavelength (l) and process conditions that rapidly heats silicon or polysilicon is a wavelength of 532 nm, pulse width of 10-15 ns, scanning speed of 14 to 45 cm/s, power 1W to 7W, and beam size of 2 to 3 mm by 40 – 80 um. Scanning time and duration can be adjusted according to a thickness of a given polysilicon film or area to be scanned. The laser is scanning is performed such that just the polysilicon region will receive the energy (heating effect). The laser scanning is performed such that the layers, materials, and devices below the oxide insulator can remain less than 400C. In other words, the heating amount and duration is targeted to the polysilicon layer so that the underlying layers are not heated above a predetermined temperature.

The laser beam 301 melts the polysilicon 107a, which then recrystallizes to a substantially larger grain size. In one embodiment, the grain size increases are 4 to 10 times larger after laser treatment (with typical single crystal grains). Note that with advanced 3D CFET channels being on the order of 5 nm, the laser annealing technique herein has essentially achieved single crystal film properties by reforming grain size to be greater than 100 nanometers. As such, the majority of channels formed with recrystallized polysilicon will not have a single grain boundary. Additionally, with the laser beam 301 being a coherent light source, there is no dispersion or significant spreading of the laser beam or loss of energy. Accordingly for channel scales on the order of single or double digit nanometers, the layer of polysilicon 107a has grain size increased sufficiently to function as single crystal silicon for given channels.

For laser annealing, air can be used as a medium 303 between the laser beam 301 and the polysilicon layer 107a to be annealed. Using air as the medium 303 is convenient for wafer handling considerations. Note, however, that other mediums can be used. For

example, the substrate can use an immersion in water or oil or other fluids because with a coherent laser light source many different mediums are available. In some embodiments, water or chilled water can be used. Using chilled water can be beneficial for substrate cooling because water has a relative high specific heat capacity. The use of other mediums
5 (such as chilled water) can act as a cooling effect for the wafer substrate below the polysilicon. According, such chilling provides two benefits. A chilled medium enables protection of underlying transistor planes, and also serves to further augment grain size increases by enabling higher annealing temperatures.

Another embodiment herein uses cryogenic wafer chuck 305 to obtain a maximum
10 temperature gradient between the laser beam on the polysilicon layer being annealed and the silicon substrate. A wafer chuck is a device for holding the wafer. Wafer chucks are typically round and slightly larger than the wafer size. However, their shape and size may vary depending on the shape and size of the wafer. A wafer chuck may hold a wafer in place by applying a vacuum to the backside of the wafer. Other embodiments use a variable
15 temperature that spans temperatures from 400K (127C) down to 30K (-243K) for a laser anneal system. Example coolants for the laser system can include both liquid nitrogen and liquid helium with two cooling centerpoints (depending on the desired temperature window) thereby enabling effective wafer cycling. Laser scanning can be limited to a particular region of a substrate, or an entire wafer surface.

20 Following laser treatment, a polishing and/or planarization step can optionally be executed. FIG. 4 illustrates an example result after polishing the layer of epitaxial-like silicon. For example, a CMP (chemical-mechanical polishing) step can be executed as one planarization option. A CMP step can modify polysilicon channel regions to modify a now large-grained, relatively thick layer to achieve a relatively thin epitaxial-like silicon channel
25 401. Planarization/polishing are beneficial because surface roughness after laser anneal can

be higher. This roughness can be reduced by an order of magnitude following CMP and cleaning steps, thereby thinning the layer of anneal polysilicon. Example cleaning treatments can include (1) immersing the CMP polished poly-Si film into two mixture solutions (NH4OH: H2O2:H2O=1:4:20 and HCl:H2O2:H2O=1:1:6) at 75°C for 10 minutes to remove
5 most of the residuals from CMP; (2) immersing the substrate into pure H2O2 for 10 minutes to form sacrificial oxide on the poly-Si surface, and (3) removing the sacrificial oxide using dilute HF solution (HF:H2O=1:10) for 5 minutes.

With a first transistor plane 103 formed and insulator 105, and with a polysilicon layer converted to large grain epitaxial-like crystal silicon 401, any number of additional
10 transistor planes can be formed. FIG. 5 shows a second transistor plane 501 formed on the annealed and polished layer of crystalline silicon. Any type of transistors can be formed. For example, a second plane of CFET can be formed. Each transistor plane herein can itself have a stack of transistors. Accordingly, in one example a second set 8 to 12 layers of alternating SiGe/Si can be grown on the substrate. This growth can be executed with current epitaxial
15 growth processes at temperatures as low as about 300 to 400°C. Note that these are the second 12 layers on the substrate, thus a total of 24 nanoplanes exist (12 silicon nanoplanes total, and 12 SiGe nanoplanes total). Thus each transistor plane can have multiple FETs. For example, the first transistor plane 103 can be fabricated to have a vertical stack of four FETs. The second transistor plane 501 can also have a vertical stack of four FETs (or two or six…).
20 Thus, by forming two transistor planes, the substrate can have a total vertical stack of 12 FETs, thereby dramatically increasing transistor count per area (by increasing volume of transistors).

FIG. 6 illustrates how techniques herein can be repeated for any number of transistor planes. Each transistor plane can have a single transistor or a stack of transistors or channels.

With multiple transistors per transistor plane, each additional transistor plane (N+1) 605 can greatly increase a total number of planes or levels of transistors on the substrate.

FIG. 7 illustrates that with polysilicon converted to epitaxial-like silicon 401, what is supported is growing a new stack of silicon layers. For example, epitaxial growth can be
5 executed to form alternating layers of silicon 701b and silicon germanium 701a, being grown from the epitaxial-like silicon 401. After growing this stack of silicon layers, the entire nanoplane stack 701 can be etched to form channels and future source/drain regions. In an example embodiment, the Nano plane stack is grown in one flow with alternating layers of SiGe/Si/SiGe/Si and etched. The channel region is cut in the y direction to form the future
10 source/drain regions. Then the SiGe layers are removed leaving planes of Si. Since adjacent regions of Silicon are open, a 360 degree dielectric (referred to as GAA - gate all around) is formed on each channel region followed by a metal gate electrode designed for NMOS and PMOS devices. Then the source/drain region is at the end side of the channel.

Thus, techniques herein enable multiple transistor planes, which increase density in
15 3D CFET and other advanced logic applications. Techniques herein can be integrated with CFET flows, finFET flows, memory flows, and other flows. With the option to hold a substrate stationary during laser anneal, or to move the substrate through a wafer beam, many types of laser systems can be used for annealing herein. Techniques provide enhanced performance and reliability for microfabrication. Better silicon formation comes from better
20 silicon properties for improved mobility, Idsat, Idoff, Vtc control, and other beneficial properties. Any type of logic, transistor type (including, for example, CFET, PLANER, Finfet) may be fabricated on each new plane of epitaxial-like silicon created by laser anneal. Processes herein can continue to stack vertically to achieve needed 3D Density for N+ 1 transistor/logic/memory planes.

In the preceding description, specific details have been set forth, such as a particular geometry of a processing system and descriptions of various components and processes used therein. It should be understood, however, that techniques herein may be practiced in other embodiments that depart from these specific details, and that such details are for purposes of
5 explanation and not limitation. Embodiments disclosed herein have been described with reference to the accompanying drawings. Similarly, for purposes of explanation, specific numbers, materials, and configurations have been set forth in order to provide a thorough understanding. Nevertheless, embodiments may be practiced without such specific details. Components having substantially the same functional constructions are denoted by like
10 reference characters, and thus any redundant descriptions may be omitted.

Various techniques have been described as multiple discrete operations to assist in understanding the various embodiments. The order of description should not be construed as to imply that these operations are necessarily order dependent. Indeed, these operations need not be performed in the order of presentation. Operations described may be performed in a
15 different order than the described embodiment. Various additional operations may be performed and/or described operations may be omitted in additional embodiments.

"Substrate" or "target substrate" as used herein generically refers to an object being processed in accordance with the invention. The substrate may include any material portion or structure of a device, particularly a semiconductor or other electronics device, and may, for
20 example, be a base substrate structure, such as a semiconductor wafer, reticle, or a layer on or overlying a base substrate structure such as a thin film. Thus, substrate is not limited to any particular base structure, underlying layer or overlying layer, patterned or un-patterned, but rather, is contemplated to include any such layer or base structure, and any combination of layers and/or base structures. The description may reference particular types of substrates,
25 but this is for illustrative purposes only.

Those skilled in the art will also understand that there can be many variations made to the operations of the techniques explained above while still achieving the same objectives of the invention. Such variations are intended to be covered by the scope of this disclosure. As such, the foregoing descriptions of embodiments of the invention are not intended to be 5 limiting. Rather, any limitations to embodiments of the invention are presented in the following claims.

CLAIMS:

1. A method of forming transistor devices, the method comprising:

forming a first transistor plane on a substrate, the first transistor plane including a plurality of field effect transistors;

depositing a first insulator layer on the first transistor plane;

depositing a first layer of polycrystalline silicon on the first insulator layer; and

annealing the first layer of polycrystalline silicon using laser heating, the laser heating increasing grain size of the first layer of polycrystalline silicon.

2. The method of claim 1, further comprising:

forming a second transistor plane on the first layer of polycrystalline silicon, the second transistor plane including the at least one layer of epitaxial film adaptable for forming channels of field effect transistors;

depositing a second insulator layer on the second transistor plane;

depositing a second layer of polycrystalline silicon on the second insulator layer; and

annealing the second layer of polycrystalline silicon using laser heating, the laser heating increasing grain size of the second layer of polycrystalline silicon.

3. The method of claim 1, wherein annealing the first layer of polycrystalline silicon includes increasing a grain size sufficient to convert the first layer of polycrystalline silicon to a monocrystalline silicon film.

4. The method of claim 2, further comprising planarizing the first layer of polycrystalline silicon prior to depositing the second transistor plane.

5. The method of claim 2, where the first transistor plane includes multiple levels of transistors in which one field-effect transistor is positioned directly above a second field effect transistor.

6. The method of claim 1, wherein the annealing the first layer of polycrystalline silicon using laser heating is performed such that the heating amount and duration is targeted to the polycrystalline silicon and the underlying layers are not heated above a predetermined temperature.

7. The method of claim 1, further comprising:

growing alternating SiGe and Si layers on the first layer of polycrystalline silicon converted to epitaxial silicon.

8. The method of claim 1, wherein the annealing the second layer of polycrystalline silicon using laser heating includes laser heating with chilled water as a medium between the laser beam and the polysilicon layer.

9. The method of claim 1, wherein the substrate is held by a wafer chuck, and

wherein the annealing the second layer of polycrystalline silicon using laser heating includes laser heating while the second layer of polycrystalline silicon is in a cryogenic coolant.

10. The method of claim 9, wherein the cryogenic coolant is at a temperature in a range of 400K to 30K.

11. A method of forming transistor devices, the method comprising:

forming a first transistor plane on a substrate, the first transistor plane including at least one layer of epitaxial film adaptable for forming channels of field effect transistors;

depositing a first insulator layer on the first transistor plane;

depositing a first layer of polycrystalline silicon on the first insulator layer;

annealing the first layer of polycrystalline silicon using laser heating, the laser heating increasing grain size of the first layer of polycrystalline silicon;

forming a second transistor plane on the first layer of polycrystalline silicon having the increased grain size, the second transistor plane being adaptable for forming channels of field effect transistors;

depositing a second insulator layer on the second transistor plane;

depositing a second layer of polycrystalline silicon on the second insulator layer; and

annealing the second layer of polycrystalline silicon using laser heating, the laser heating increasing grain size of the second layer of polycrystalline silicon.

12. The method of claim 11, wherein the first transistor plane includes multiple epitaxial films sufficient to form one field-effect transistor positioned directly above a second field effect transistor.

13. The method of claim 11, further comprising, forming a first etch mask on the substrate and using the first etch mask to etch both the first transistor plane and the second transistor plane.

14. The method of claim 11, wherein annealing the first layer of polycrystalline silicon includes increasing a grain size sufficient to convert the first layer of polycrystalline silicon to a monocrystalline silicon film.

15. The method of claim 11, where the second transistor plane includes multiple levels of transistors in which one field-effect transistor is positioned directly above a second field effect transistor.

16. The method of claim 11, wherein the annealing the first layer of polycrystalline silicon using laser heating is performed such that the heating amount and duration is targeted to the polysilicon silicon and the underlying layers are not heated above a predetermined temperature.

17. The method of claim 11, further comprising:

growing alternating SiGe and Si layers on the second layer of polycrystalline silicon converted to epitaxial silicon.

18. The method of claim 11, wherein the annealing the second layer of polycrystalline silicon using laser heating includes laser heating with chilled water as a medium between the laser beam and the polysilicon layer.

19. The method of claim 11, wherein the substrate is held by a wafer chuck, and

wherein the annealing the second layer of polycrystalline silicon using laser heating includes laser heating while the second layer of polycrystalline silicon is in a cryogenic coolant.

20. The method of claim 19, wherein the cryogenic coolant is at a temperature in a range of 400K to 30K.

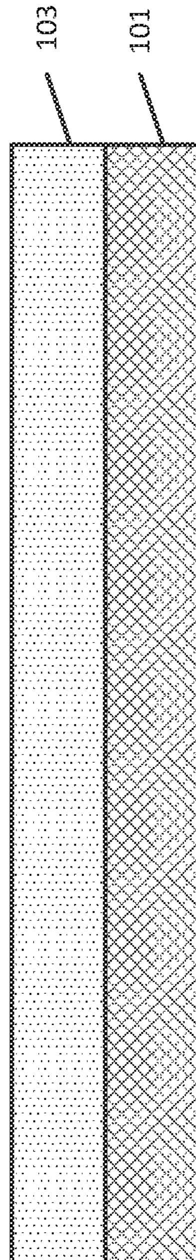

FIG. 1

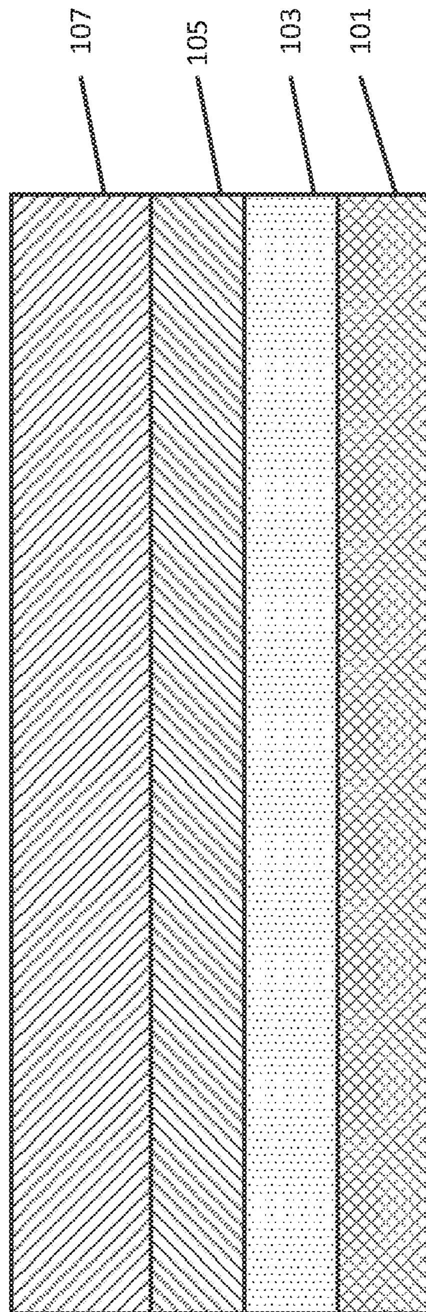

FIG. 2

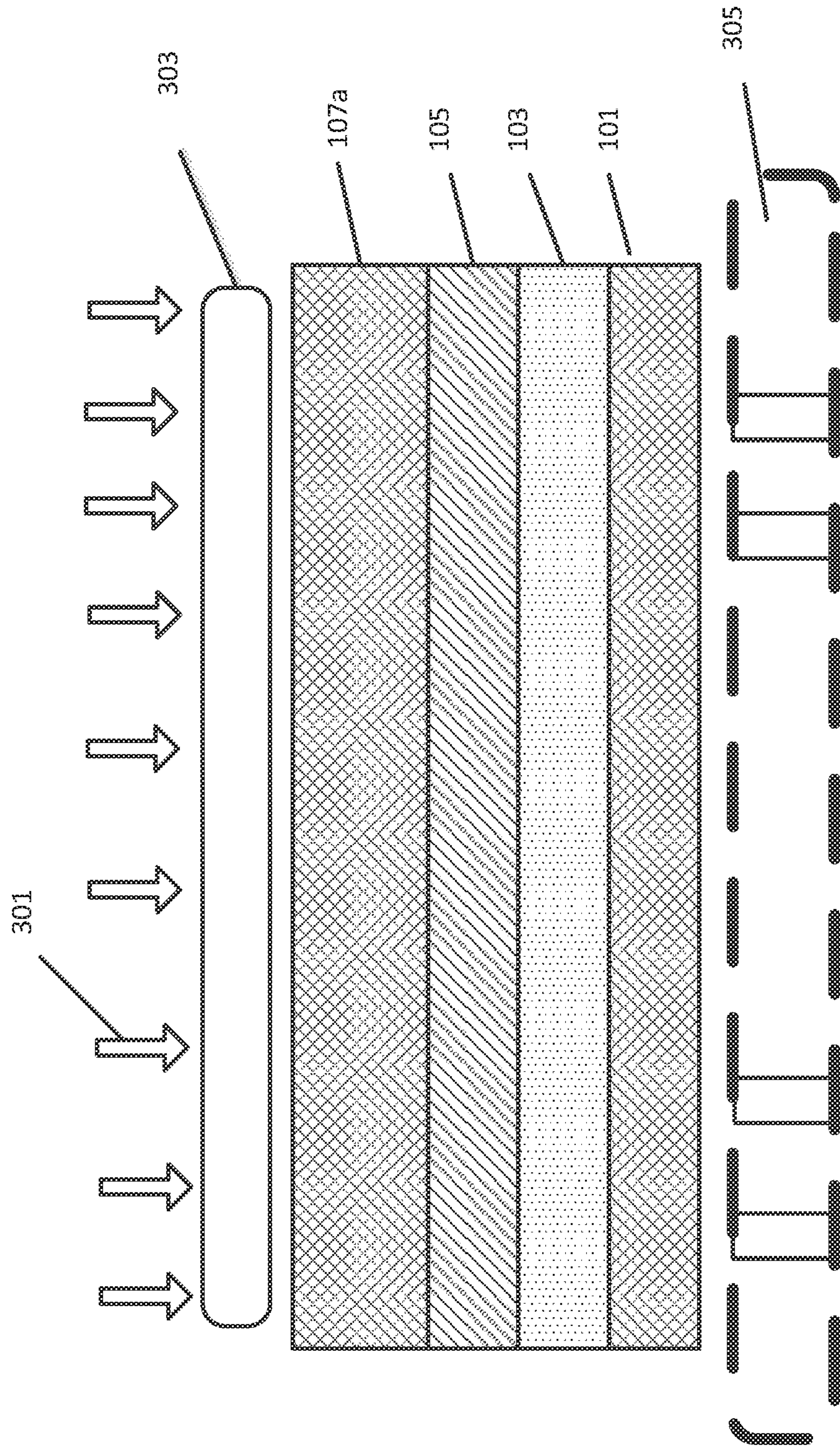

FIG. 3

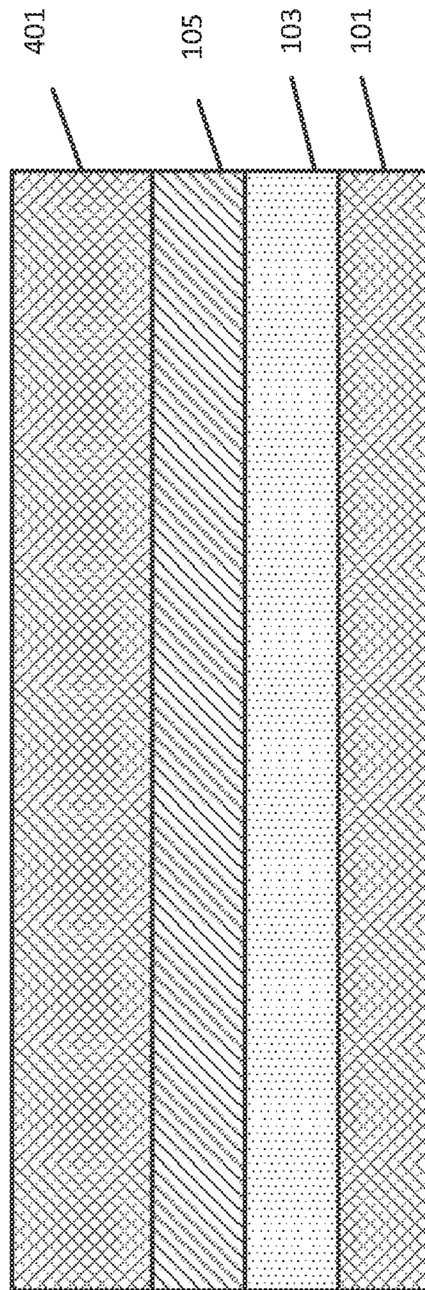

FIG. 4

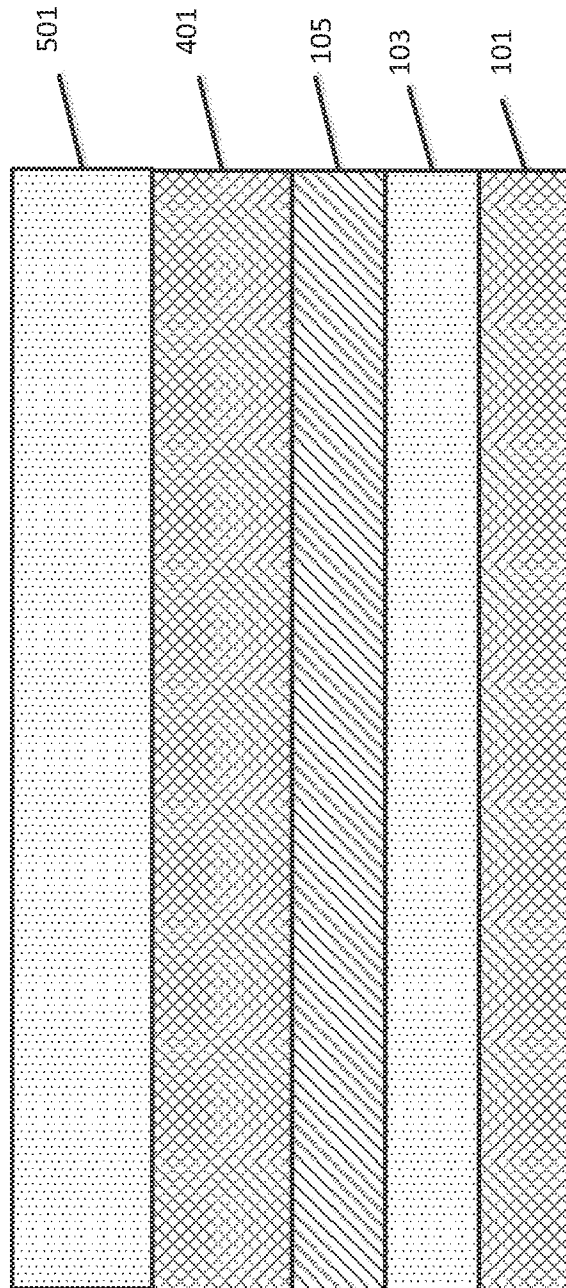

FIG. 5

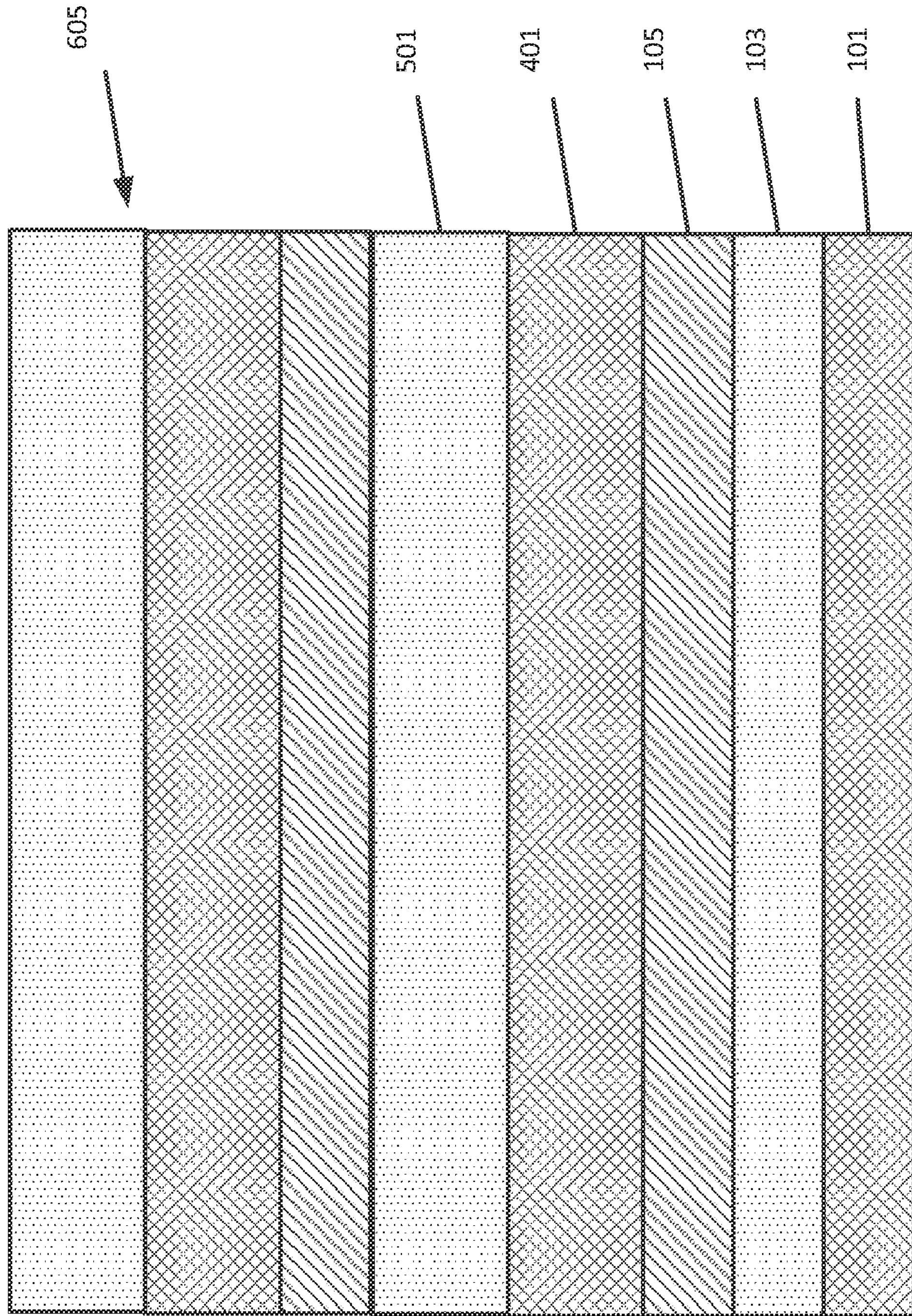

FIG. 6

701

701b

701a

401

105

103

101

FIG. 7

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2020/043986

A. CLASSIFICATION OF SUBJECT MATTER

H01L 21/822(2006.01)i, H01L 21/02(2006.01)i, H01L 21/8238(2006.01)i, H01L 27/06(2006.01)i, H01L 21/67(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L 21/822; H01L 21/02; H01L 21/20; H01L 21/336; H01L 21/8238; H01L 29/45; H01L 29/66; H01L 27/06; H01L 21/67

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Korean utility models and applications for utility models
Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
eKOMPASS(KIPO internal) & Keywords: transistor device, transistor plane, polycrystalline silicon, laser anealing, grain

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	US 2009-0104759 A1 (PIL-KYU KANG et al.) 23 April 2009 See paragraphs [0038]-[0068] and figures 3B-4C.	1,3,6 2,4-5,7-20
Y	US 2019-0214314 A1 (INTERNATIONAL BUSINESS MACHINES CORPORATION) 11 July 2019 See paragraphs [0032]-[0036] and figures 1-2.	2,4-5,7-20
A	US 9087689 B1 (INOSO, LLC) 21 July 2015 See column 5, line 3 - column 8, line 11 and figures 2-10.	1-20
A	KR 10-0714401 B1 (SAMSUNG ELECTRONICS CO., LTD.) 04 May 2007 See paragraphs [0024]-[0049] and figures 2-3f.	1-20
A	US 9613805 B1 (INFINEON TECHNOLOGIES AG) 04 April 2017 See column 13, line 32 - column 16, line 28 and figures 2a-2f.	1-20

☐ Further documents are listed in the continuation of Box C.   ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"D" document cited by the applicant in the international application
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents,such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
13 November 2020 (13.11.2020)	**13 November 2020 (13.11.2020)**

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

KANG MIN JEONG

Telephone No. +82-42-481-8131

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2020/043986

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2009-0104759 A1	23/04/2009	KR 10-1329352 B1	13/11/2013
		KR 10-2009-0038974 A	22/04/2009
		US 8048784 B2	01/11/2011
US 2019-0214314 A1	11/07/2019	US 10325820 B1	18/06/2019
		US 10804165 B2	13/10/2020
		US 2019-0295899 A1	26/09/2019
US 9087689 B1	21/07/2015	US 8916872 B1	23/12/2014
		US 9202756 B1	01/12/2015
KR 10-0714401 B1	04/05/2007	US 2007-0181953 A1	09/08/2007
		US 7741644 B2	22/06/2010
US 9613805 B1	04/04/2017	CN 106876270 A	20/06/2017
		CN 106876270 B	30/06/2020
		DE 102016122787 A1	14/06/2017
		KR 10-1875287 B1	05/07/2018
		KR 10-2017-0074757 A	30/06/2017