United States Patent

[11] 3,593,310

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[54] **DISPLAY SYSTEM**
12 Claims, 14 Drawing Figs.

[52] **U.S. Cl.** ..... **340/172.5,** 340/324 A
[51] **Int. Cl.** **G06f 3/14**
[50] **Field of Search** ..... 340/172.5, 324 A; 235/157

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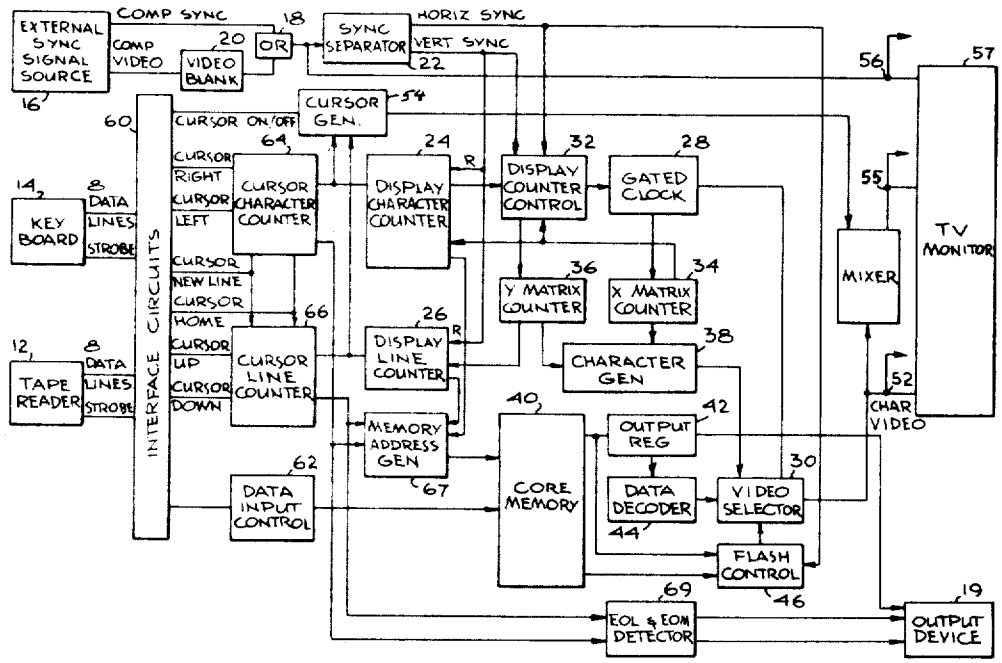
Attorneys—Samuel Lindenberg and Arthur Freilich

ABSTRACT: A system is provided for enabling the information being displayed on a cathode-ray tube of a display system to appear to move upward or downward vertically across the face of the tube.



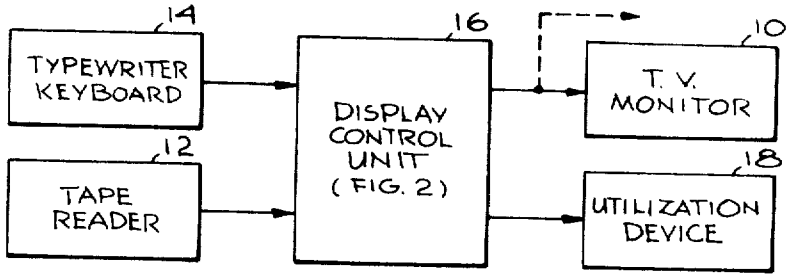


Fig. 1

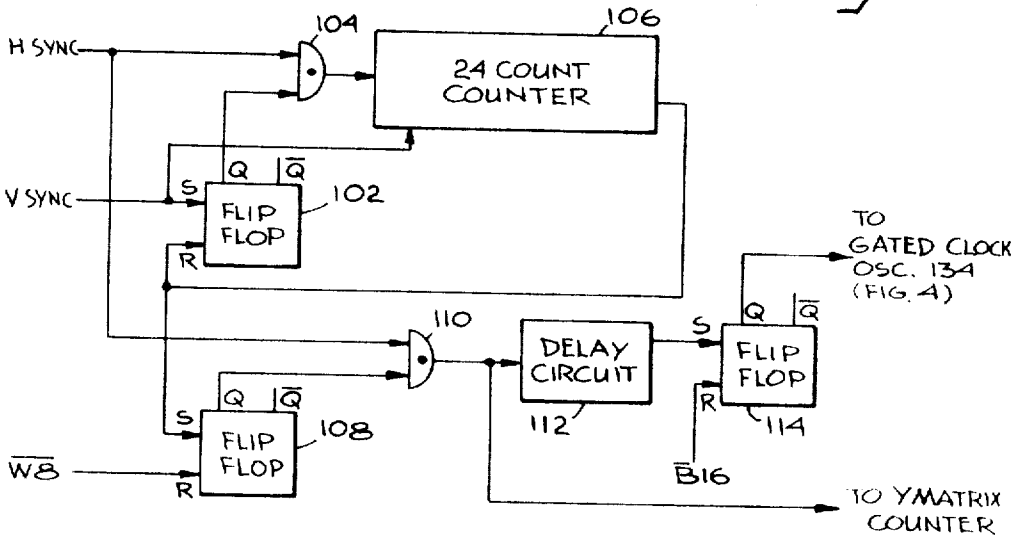


Fig. 3

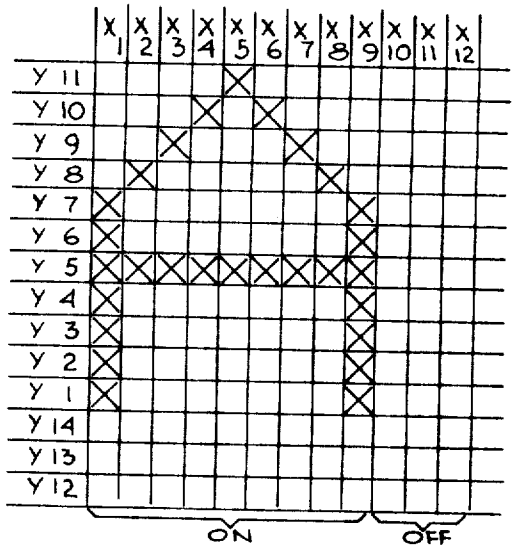


Fig. 5

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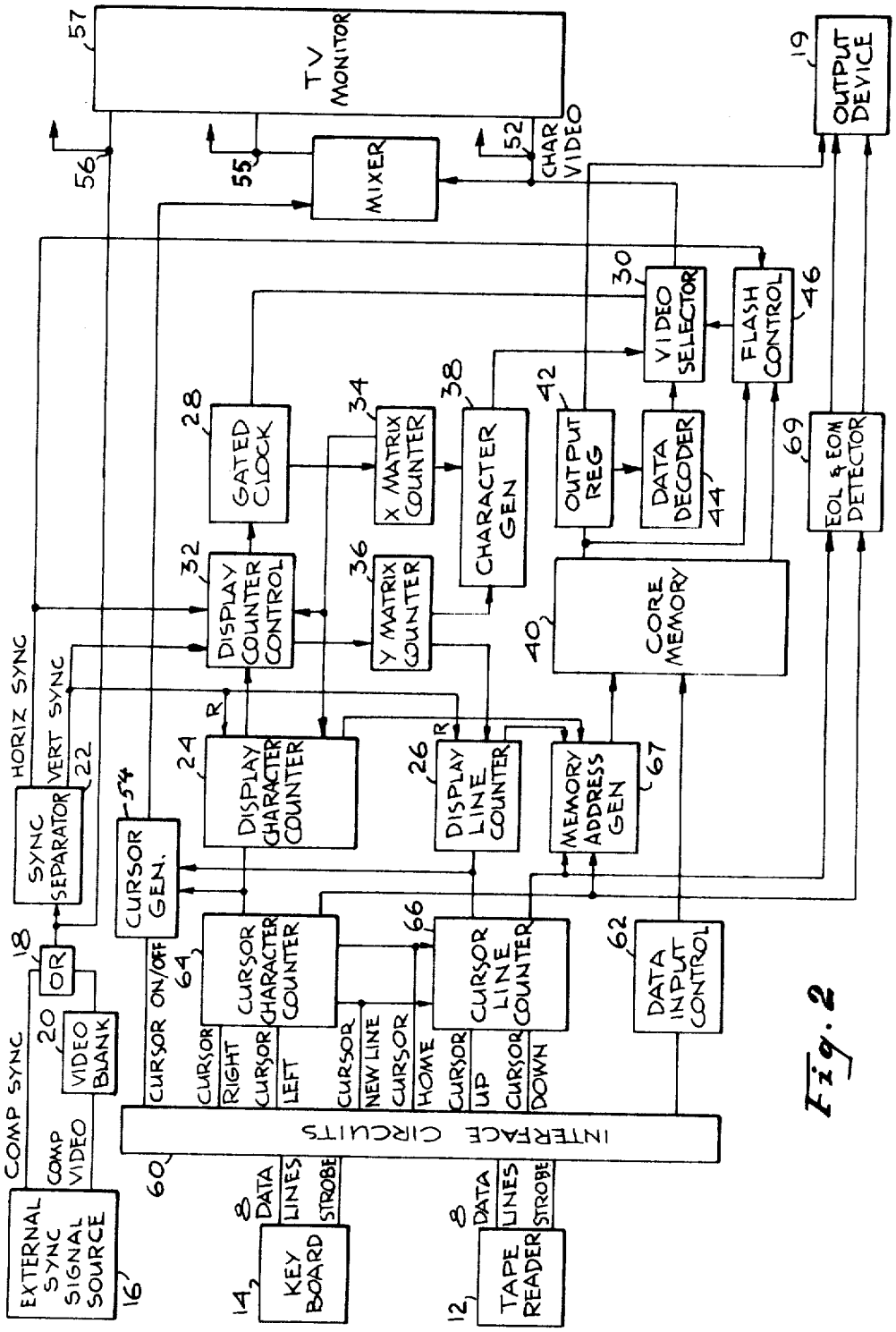

Fig. 2

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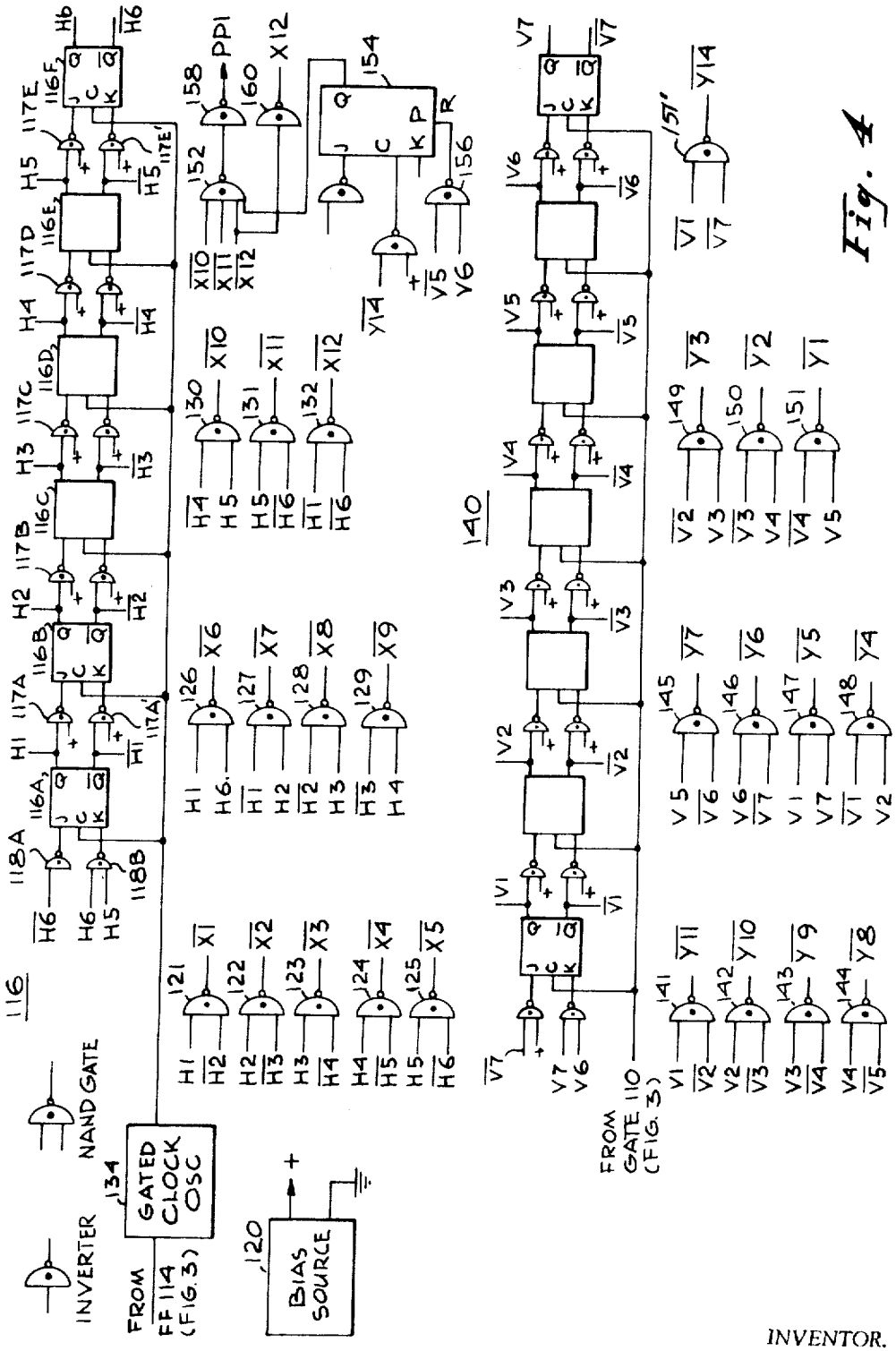

Fig. 4

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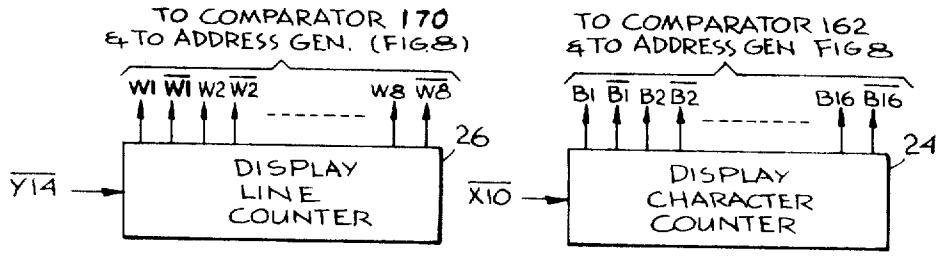

Fig. 6

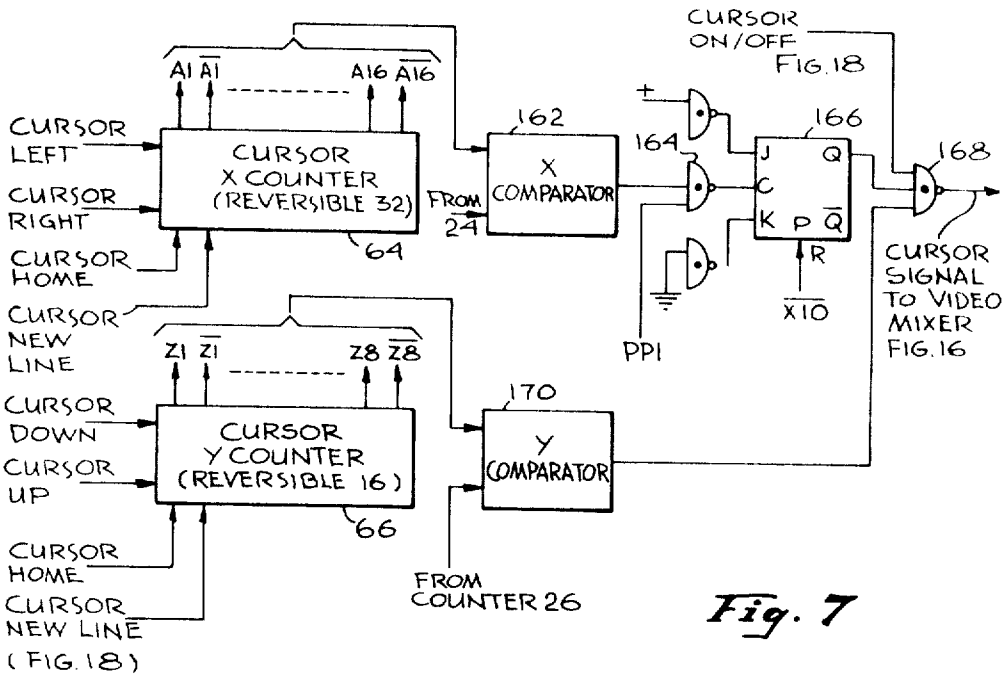

Fig. 7

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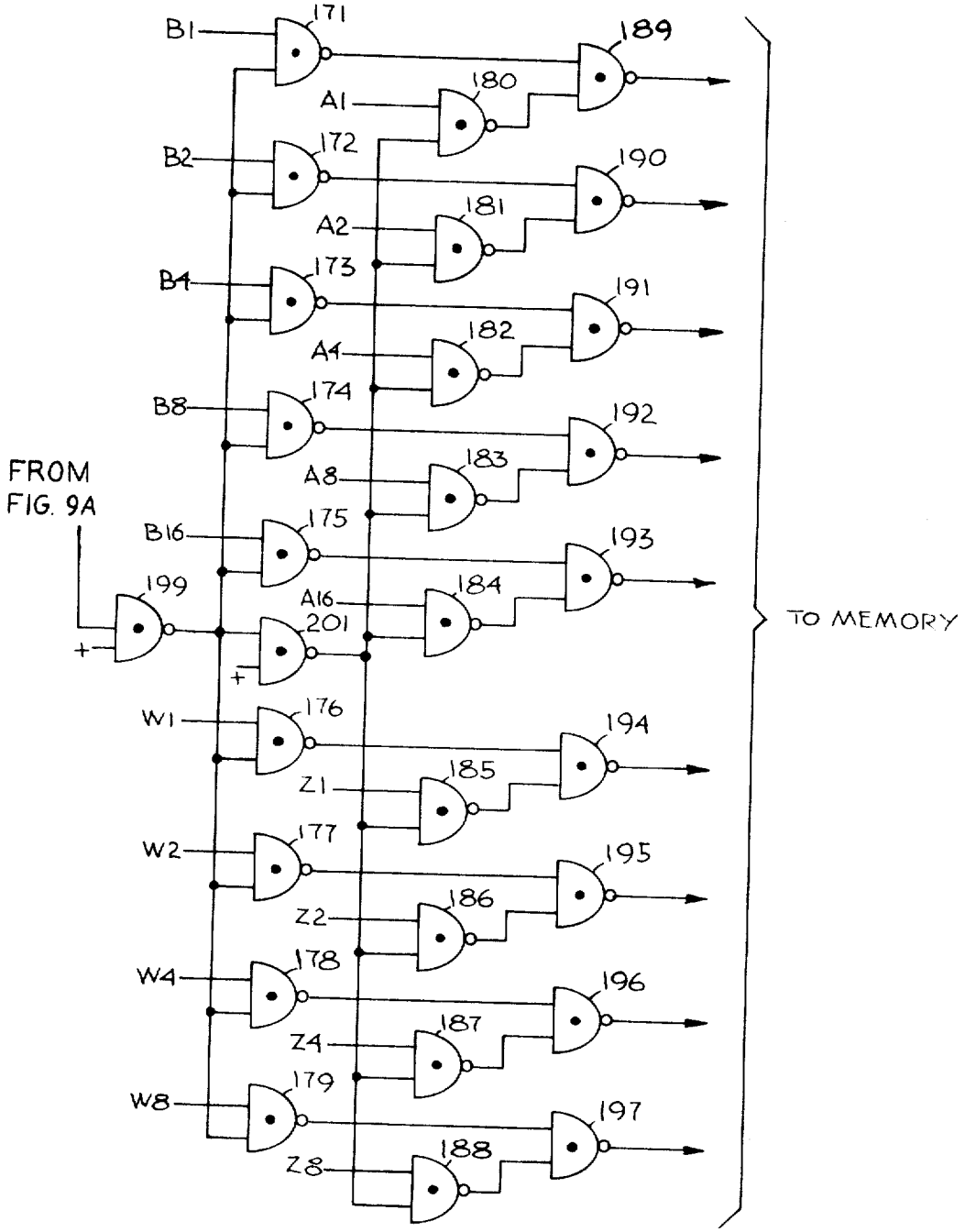

Fig. 8

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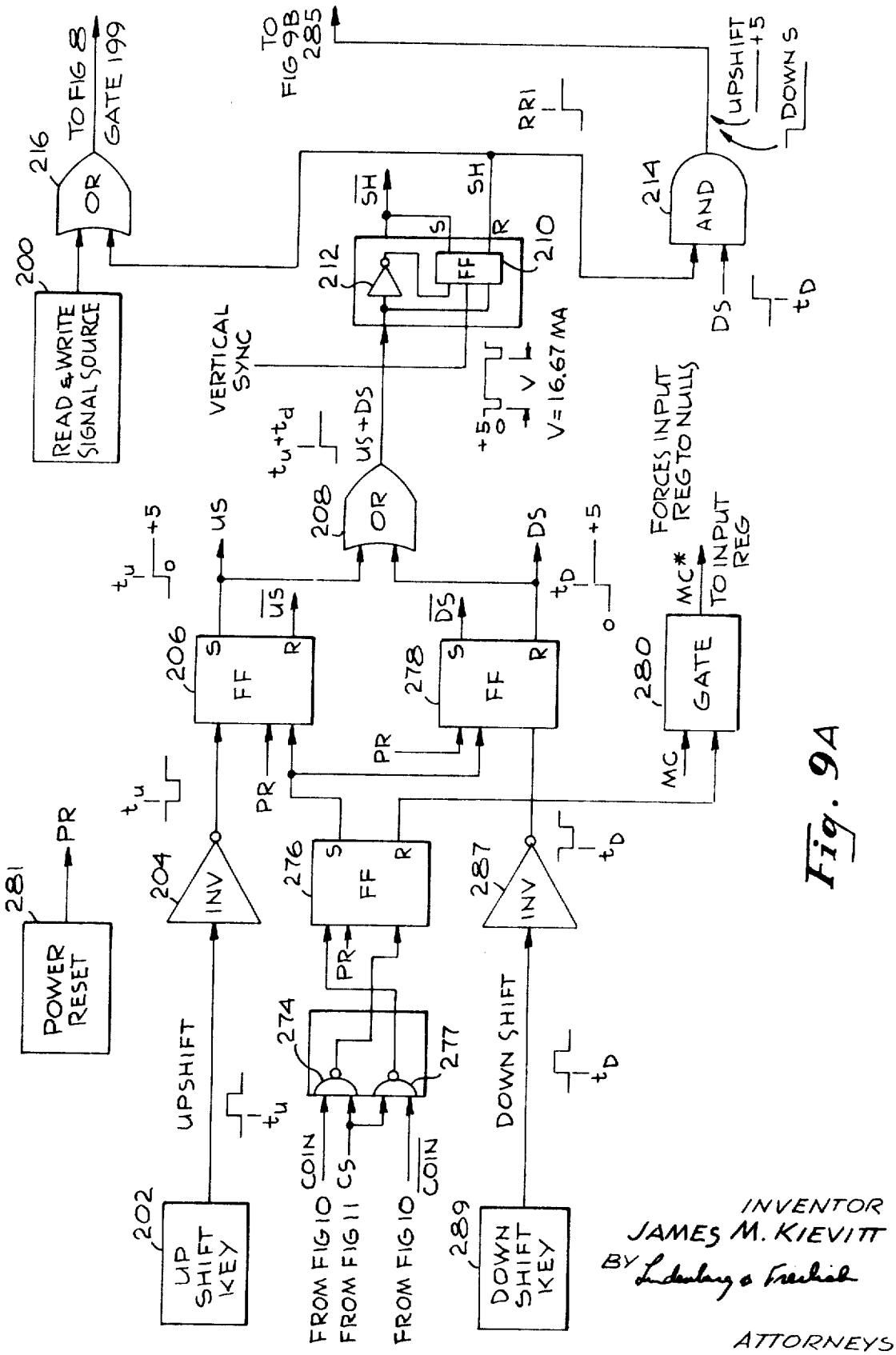

Fig. 9A

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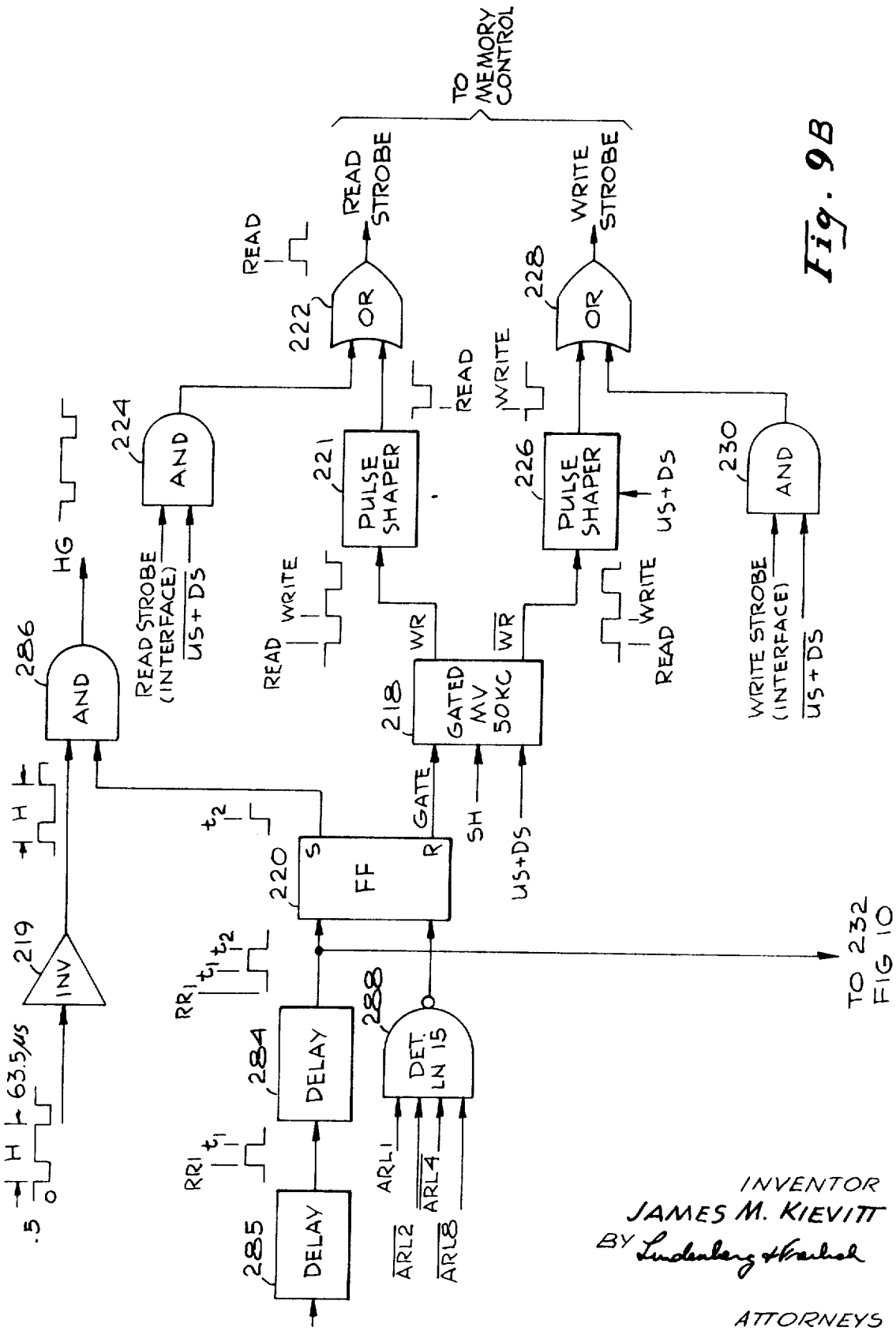

Fig. 9B

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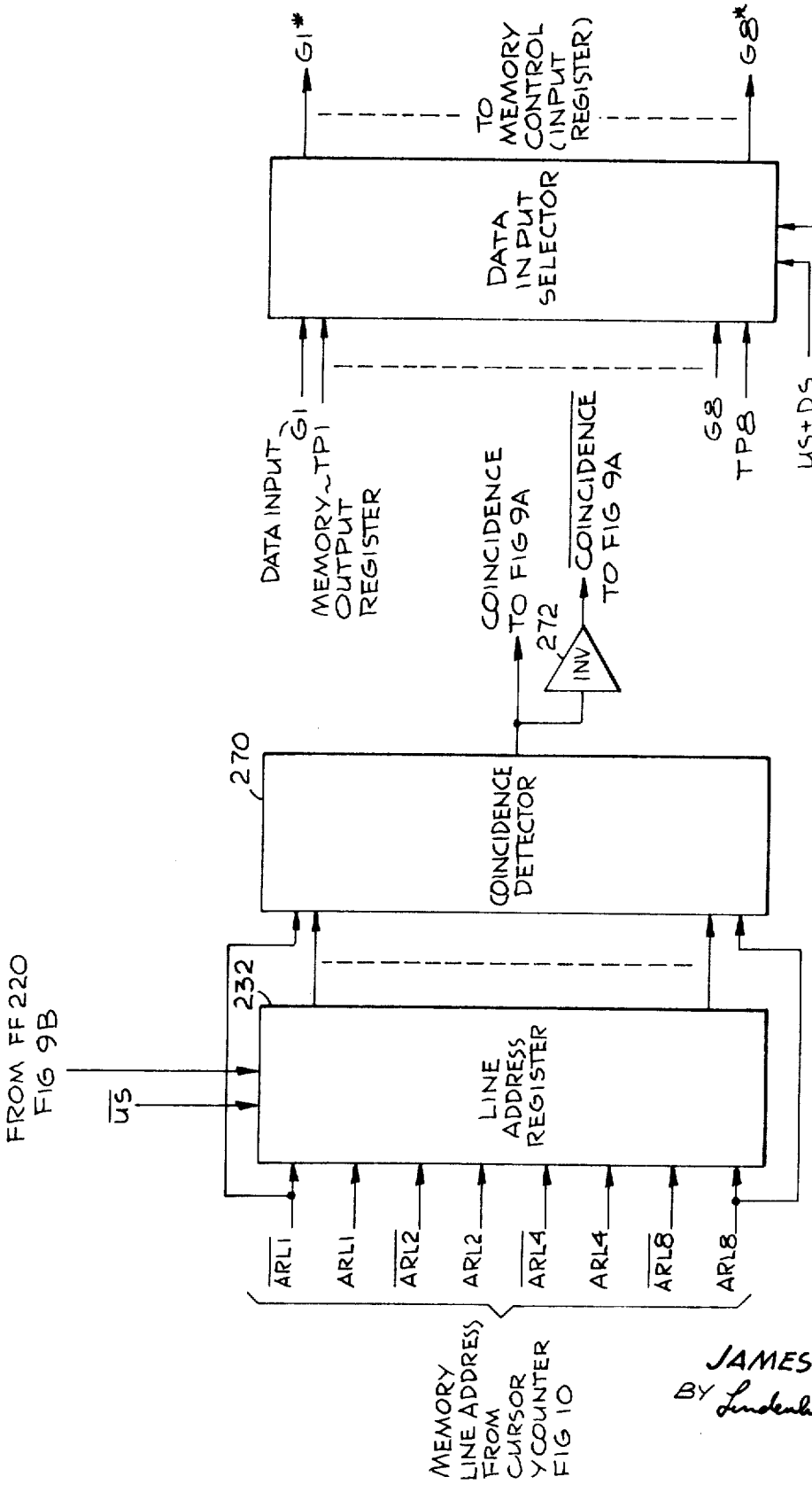

Fig. 10

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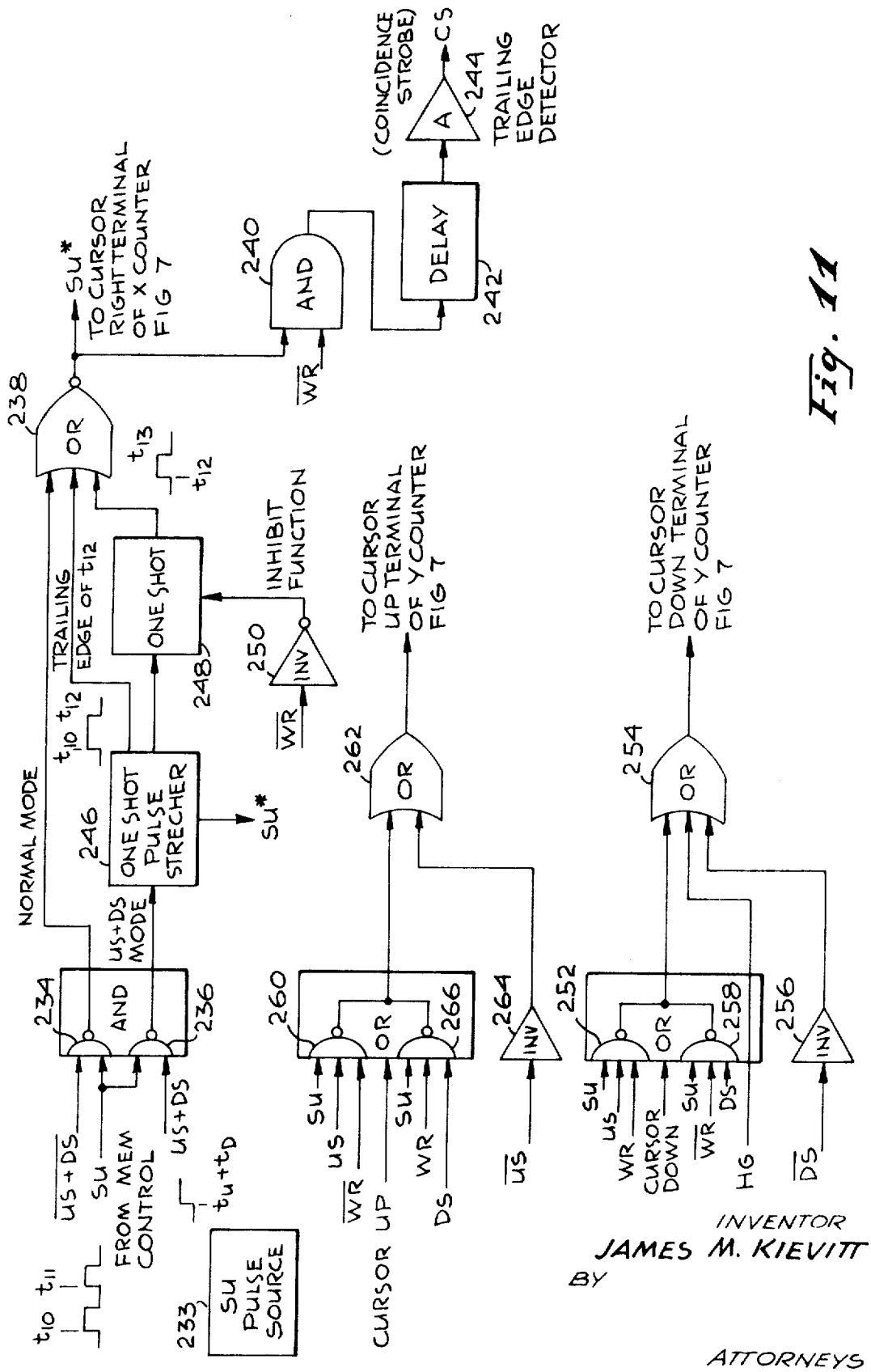

Fig. 11

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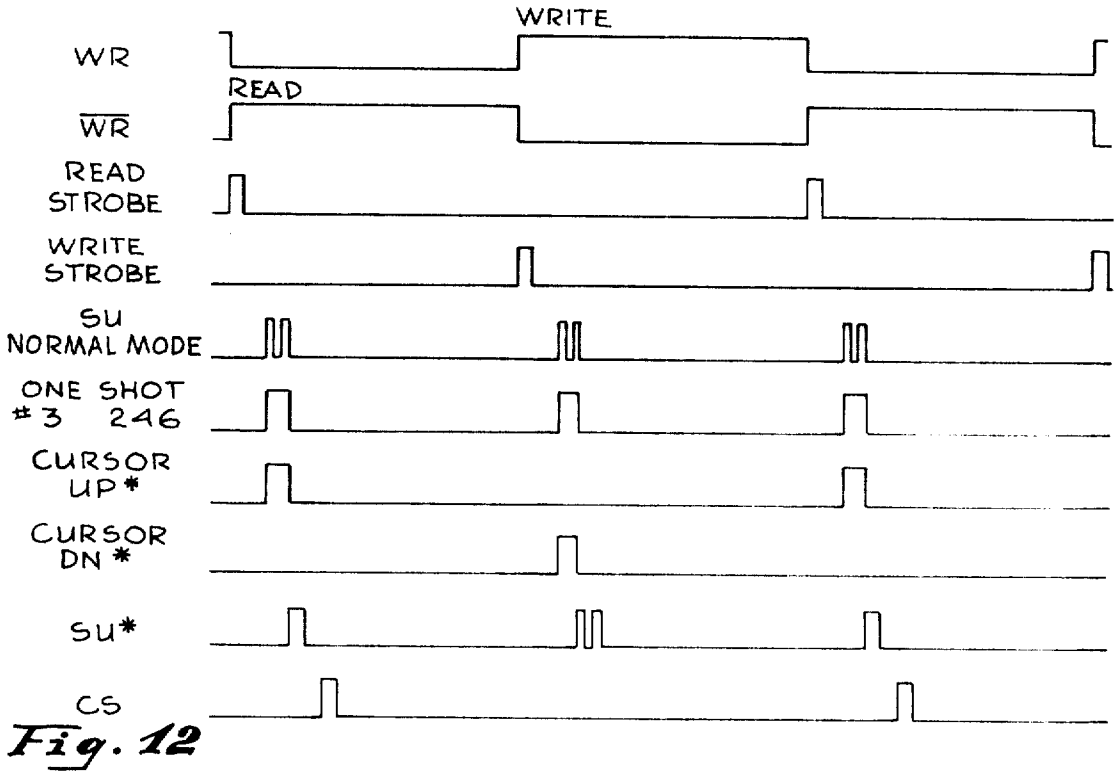

Fig. 12

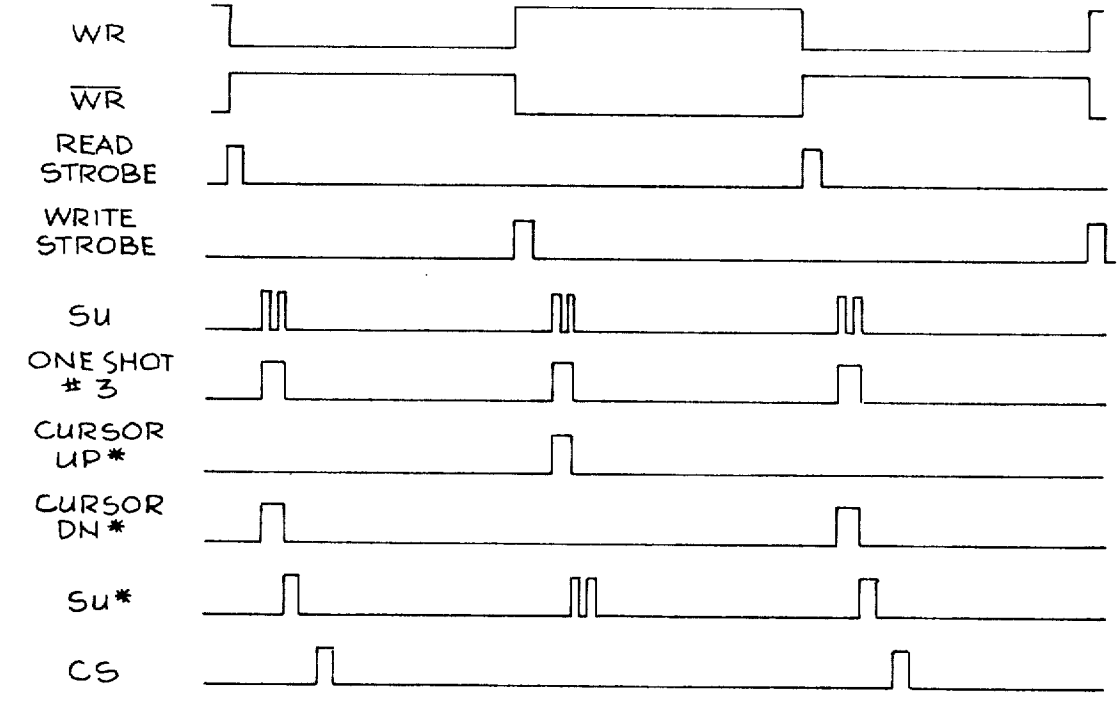

Fig. 13

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DISPLAY SYSTEM

CROSS-REFERENCES TO RELATED APPLICATION

This application is directed to an improvement in an application for a "Display System" by Kite et al., Ser. No. 704,967, filed Jan. 2, 1968, and assigned to a common assignee.

BACKGROUND OF THE INVENTION

This invention relates to display systems which display data on the face of a television monitor, and more particularly to an arrangement for enabling such data to appear to be traveling vertically up or down across the face of the tube.

It is often times desirable to insert a line of information into lines of data being displayed across the face of a cathode ray tube. This requires a means to shift all, or a portion, of the display up or down by an increment of one display line. Up shift deletes the line at the top of the displaced display and by displacing information upward leaves information leaving room at the bottom of the displaced display to insert a line. Downshift deletes a line from the bottom of the display information and by displacing information downward leaves room at the top of the displaced display to insert a line.

OBJECTS AND SUMMARY OF THE INVENTION

The feature of this invention is the provision of an upshift, or downshift arrangement whereby data is stored in the memory of a display system is made to appear to move upward or downward across the face of a display tube.

Another feature of this system is an arrangement whereby information is upshifted or downshifted across the face of a display tube in a display system which operates at commercial television frequencies.

Still another feature of this invention is to provide a means to shift all or a portion of a display up or down an increment of one display line whereby a line is opened up and new information may be inserted therein.

The foregoing and other features of the invention are achieved in an arrangement wherein a display system has a memory having a capacity for storing for each display location on the face of the display tube, a code representing an alphanumeric character. The addresses of the locations in the memory correspond to the addresses of the location on the cathode ray tube face as determined by a character counter, which counts the number of lines of characters displayed on the display tube.

For an upshift operation, means are provided for reading the characters in a line of data out of memory one at a time and rewrite them into memory at an address one line above. Means are provided, when a downshift operation is signalled to go from a given address to the next to the last line of the tube, then to read out characters from a line of memory, and rewrite them in memory one line below. This continues until the given line address is reached.

The novel features of the invention are set forth with particularlity in the appended claims. The invention will best be understood from the following description when read in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating the general layout of a display system in accordance with this invention.

FIG. 2 is a detailed block diagram of a display control unit in accordance with this invention.

FIG. 3 is a block schematic drawing of the display counter control circuit 32.

FIG. 4 is a block schematic drawing of the X and Y matrix counters.

FIG. 5 illustrates a character constructed of selected dots in a dot matrix in accordance with this invention.

FIG. 6 is a block schematic of the display line and character counters.

FIG. 7 is a block schematic diagram of the cursor generator and line and character counters.

FIG. 8 is a block schematic diagram of the memory address generator.

FIGS. 9A, 9B, 10 and 11 are block schematic diagrams of the logic circuits required for upshift and downshift control in accordance with this invention.

FIG. 12 is a timing diagram for the upshift function.

FIG. 13 is a timing diagram for the downshift function.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Since the present invention is an addition to the invention described in the application for "Display System," previously mentioned, in order to understand the operation of this invention, it will be necessary to describe some of the display system. FIG. 1 illustrates a general arrangement of the display system which comprises a standard TV monitor 10, (more than one may be used if required,) which displays human readable data. Digital data may be entered into the system from any data source, illustrative of which there is shown a tape reader 12 and/or a typewriter keyboard 14. This data is fed into a display control unit 16 whose function it is to store the data in a manner so that it may be properly read out for display on the TV monitor or sent to some other utilization device 18, such as Keypunch, a printout device, etc. The display control unit also includes a novel character generator which, in response to the data representative code produces the video signals which are displayed as readable data on the TV monitor 10.

FIG. 2 is a block schematic diagram illustrating details of the display control unit. A tape reader 12 or a typewriter keyboard 14 are well known, and commercially available pieces of hardware. For the purposes of this invention, and in the manner that they function normally, the tape reader produces as an output 8 binary signals together with a strobe pulse, each time a character is read out. Seven of the eight bits represent an alphanumeric character. The eighth bit is parity. The keyboard 14, which can be a facsimile typewriter, also produces at its output 7-bit character signal with an eighth bit having parity significance, together with a strobe pulse. In each of these cases, the signals are produced in parallel on eight data lines and a strobe pulse is produced on a ninth line. The signals are applied to interface circuits 60.

Basic operating synchronization signals for the display control unit may be obtained from an external source of sync signals 16. This external sync signal source may comprise either a television station sync generator, or a composite video signal such as may be obtained from a video tape device. Signals from either of these may be processed to provide horizontal sync signals and vertical sync signals. If composite video is provided, this is applied directly to an OR gate 18 the output of which goes to a sync separator circuit 22. This functions in well-known manner to separate the horizontal sync from the vertical sync. If composite video is provided by the external video signal source, then this is applied to a video blanking circuit 20, which constitutes well-known circuitry for applying a blanking pulse to the composite video during the video interval. This leaves composite sync signals. These are applied to the OR gate 18 and thereafter to the sync separator circuit to be separated into horizontal and vertical sync signals.

The composite sync signals, which are the output of the OR gate 18 are supplied, at the output of the display control unit, to the TV monitor which is used to reproduce the video signals. The vertical sync or vertical drive pulse which is the output of the sync separator 22, is used to reset a display character counter 24, and a display line counter 26, to assure that each field which is to be displayed starts properly. The display character counter has its count advanced by one, for each character being displayed on a line of characters. The display line counter 26 has its count advanced by one for each line of characters which is displayed. Thus, the address of the

last character being displayed is always available from the output of these counters. Actual video display commences after the first 24 horizontal sync pulses which follow the vertical sync pulse and continues until 16 rows of character video are displayed.

There are 32 characters on each line. The first horizontal sync pulse initiates the operation of a display counter control circuit 32. The counter control circuit can start a gated clock circuit 28 where frequency equals the picture element rate of 8 megacycles. The start of the operation of the gated clock is delayed, following the horizontal drive pulse, by approximately 12 microseconds until the first character position in a line of characters is reached. The clock turns on and then continues to operate until the final character in a line is completed. Each character position is defined by a dot matrix in which only those dots are illuminated which form a desired character. Each character used 9 dot positions along a line for the actual character display plus 3 guard band positions. The total number of clock pulses generated per line is therefore 12 times 32 (32 characters per line) or 384 pulses.

The display counter control also receives vertical sync pulses which are used for reset purposes. The gated clock output is used to drive an *x*-matrix counter 34, causing it to count through 12 counts, 9 counts of which correspond to 9 horizontal positions in a character dot matrix starting from left to right, and the three further counts provide for the guard band or character spacing. The *x*-matrix counter 34 therefore goes through a full cycle of operation for each character. Count output signals from XI to XII are derived therefrom. Each time the *x*-matrix counter completes a cycle of 12 counts, it overflows. Its overflow is applied to the display character counter 24 to cause it to advance one count. The display character counter has a count capacity totaling 32, corresponding to the number of characters displayed in each row. Each time the display character counter overflows, it sends the overflow pulse back to the display counter control 32 which in turn uses this overflow pulse to turn off the gated click 28. The gated clock then waits from the next horizontal sync pulse before commencing operation again. The overflow output pulse of the display counter control also enables a *y*-matrix counter 36 to be advanced one count in response to the next horizontal sync pulse.

The *y*-matrix counter has a total count capacity of 14 counts. Eleven of these are used to count the vertical dot matrix locations of a character. Three of these are for a guard band space between lines of characters. Count output s designated from $\overline{Y1}$ to $\overline{Y14}$ are derived therefrom. The overflow output of the *y*-matrix counter 36 is applied to the display line counter 26 to cause it to advance one count. The display line counter has a total count capacity of 16 corresponding to the 16 lines of characters which are displayed in one field of this invention.

A character generator 38 is provided which has applied thereto the count outputs of the *x* and *y* matrix counters. In response to these, the character generator generates video signals representing each one of the alphanumeric characters which the system is capable of displaying. In an embodiment of the invention which has been built and successfully operated, the character generated created 64 alpha numeric characters. The output of the character generator is applied to the video selector 30. This functions to select, in response to a 7-bit alpha-numeric code derived form the core memory 40 of the system, a specific character from all of those being applied to the video selector, which flash is represented by that alphanumeric code. More specifically, the core memory 40 supplies coded signals, one character at a time to an output register 42, which in turn applies them to a data decoder 44 which decodes them successively and enables the video selector to select the proper video character signals. In addition, the video selector 30 is capable of being modulated by a flash control circuit 46. The flash control circuit contains an oscillating circuit that may be turned on by a flash code which is stored in the memory and which is a "nonviewable" character. The flash control 46 remains on until either the next following horizontal drive pulse appears or a space code which separates the following word appears. Operation of the flash control 46 causes all characters of a word that are displayed thereafter to flicker and thus call attention to itself.

After each character is displayed, an unload cycle of the core memory 40 is made to occur to place the alphanumeric signals corresponding to the next character of a row in the output register 42. The address from which the character in core memory is read is provided by the count conditions of the display character counter and display line counter. A specific core memory address is provided for each of the 512 counts which these counters provide. The display character counter 64 and display line counter 66 have their outputs connected to a memory address generator 67, which produces the address information for the core memory 40.

The output of the video selector 30, which comprises the character video signals is applied to a mixer circuit 50 and to an output terminal 52. The mixer circuit combines character video signals with a cursor signal which is provided from a cursor generator 54. The cursor video signal has approximately one-half of the intensity of the character signals. The cursor video signal indicates, on the pattern displayed on the face of the television monitor, the corresponding character signal address in the memory into which the next input character digital signals will be placed when the system is in the write mode. The mixer output is applied to an output terminal 55. In addition, composite sync signals from the output of the OR gate 18 are made available at a terminal 56. These three signals, namely composite sync, character video with cursor, and character video without cursor are thus available at the three output terminals for being applied to a television monitor for display.

The tape reader 12 and the keyboard 14 have their outputs connected to the interface circuitry 60. The interface circuitry serves to check the incoming data lines from either of the two inputs upon receipt of its associated data strobe presented on the strobe lines. If the data is alphanumeric data to be displayed, the input strobe signal triggers a single load cycle of the core memory. This function is provided by the data input control circuit 62. In the load cycle operation, the input character is loaded into the core memory at an address which is determined by the count outputs of the cursor character counter 64 and the cursor line counter 66. The cursor generator 54 detects coincidence between the cursor counters and the display counters and causes the load operation to occur when these counters have the same count. As previously indicated, this occurs at an address in memory corresponding to the position visually indicated by the cursor on the output monitor. Thus, the load operation into the core memory occurs at a location which corresponds to the location of the cursor. From the foregoing it will be appreciated that the memory should provide storage for 512 alpha numeric characters of eight bits per character.

Other signals from the interface circuit are provided in response to the incoming control codes. These specific control codes do not result in a memory load cycle but rather generate signals on appropriate lines out of the interface circuit. These lines perform such functions as cursor on-off, cursor right, cursor left, cursor new line, cursor home, cursor up, cursor down, etc. This will become more clear as this explanation progresses.

During the write mode, as each character is loaded into the core memory, a single pulse advances the cursor character counter by one count. When the cursor character counter overflows, its output advances the cursor line counter. Input load operations therefore, cause the cursor to be advanced character by character and line by line in a manner similar to the typing operation of a typewriter.

The output register 42 may also be used if desired to transmit data which is within the memory to an external utilization device 19 such as tape or a transmitter or an external printer. An "end of line" or "end of message" circuit 69 driven by the

cursor counters, may be used in conjunction with external transmission of data to signal their occurrences to external equipment.

DISPLAY COUNTER CONTROL CIRCUIT 32

FIG. 3

FIG. 3 is a block schematic diagram of the display counter control circuit. This circuit arrangement functions to initiate operation of the gated clock oscillator at the proper time so that the subsequent matrix and display counters may commence to operate at the proper time and in the proper time sequence. In a television type display both a top margin as well as a left side margin must be provided for. Essentially the display counter control circuit provides for these delays. The first vertical sync pulse which is delivered by the output of the sync separator 22 is applied to a flip-flop 102 to drive it to its set state. This causes the Q output of the flip-flop to become high. The Q output of the flip-flop enables an AND gate 104 whereby it can pass horizontal sync pulses which are received from the sync separator. These are applied to drive a 24 count counter 106. This counter provides a top margin delay. The 24th count of the counter is used to reset the flip-flop 102 and sets a flip-flop 108. The next vertical sync pulse enables flip-flop 102 again and simultaneously resets the 24 count counter so it can begin counting again.

The Q output of flip-flop 108 enables an AND gate 110 to pass horizontal sync pulses. The output of the AND gate 110 is applied to a delay circuit 112. The delay circuit provides a delay whose duration is determined by the size of the desired left-hand margin on the display tube. The output of the delay circuit 112 sets a flip-flop 114. The Q output of the flip-flop 114, which is high in response to its set input being enabled, is applied to the gated clock oscillator to cause it to commence to produce clock pulses.

Flip-flop 114 is reset by a $\overline{B16}$ output, which is received from the display character counter which counts the number of characters displayed on a line. After the last character has been displayed flip-flop 114 is reset so that at the commencement of the next line, signaled by the appearance of another horizontal sync pulse, a delay is provided on the left-hand side of the display tube. The flip-flop 108 is reset by a $\overline{W8}$ signal which is provided by the display line counter. This signal occurs after the last character on the last line has been displayed. Accordingly, flip-flop 108 cannot be set again until the counter 106 has counted through its next 24 counts to provide the top magin delay.

FIG. 4

FIG. 4 is a block schematic diagram of the *x* and *y* dot matrix counters. A character, in accordance with this invention, is made by illuminating selected dots in a dot matrix that extends nine dots in a horizontal direction and 11 dots in a vertical direction. There are five dot spaces allowed between characters on a line to serve as a guard band, and three dot spaces between lines of characters, also to serve as a guard band. Thus, the counter that counts for the horizontal dot placement will have a count capacity of 14 and the counter that counts for the vertical dot placement will have a count capacity of 14.

In FIG. 4, there is shown a horizontal counter 116 which is made up of six flip-flops, respectively 116A through 116F. Each one of these flip-flops is of the type known as "JK" flip-flop. It is well known and commercially purchasable.

Each flip-flop has J, K and C inputs, and Q and $\overline{Q}$ outputs. When a clock pulse is applied to its C input the flip-flop will transfer to its outputs the state of its J and K inputs. Thus, if the J input is high and the K input is low when a C or clock pulse is applied to the C input, the Q output will be high and the $\overline{Q}$ output will be low. The J and K inputs are applied to the respective flip-flops from the Q and $\overline{Q}$ outputs of the respective flip-flops through NAND gates. A NAND gate behaves like an AND gate followed by an inverter. Accordingly, when the two inputs to the NAND gate are high, its output is low and when the inputs to the NAND gate are low, its output is high. When one of the inputs is high and the other is low, the NAND gate output is high.

The counter 116 has the Q and $\overline{Q}$ outputs of the respective flip-flops 116A through 116E respectively connected to the J and K inputs of the immediately following flip-flops through the respective NAND gates 117A and 117A' through 117E and 117E'. NAND gates 118A and 118A' are connected to the respective J and K inputs of flip-flop 116A. The NAND gate 118A has one input connected to the $\overline{Q}$ output of flip-flop 116F which is designated as $\overline{H6}$. The NAND gate 118A has its inputs respectively connected to the Q outputs of respective flip-flops 116E and 116F. These Q outputs are respectively designated as H5 and H6.

It should be noted that whenever a designation is shown for only one NAND gate input, the other input of the NAND gate is connected to a bias source 120. As the result, a one input NAND gate acts as an inverter to invert the input.

The respective Q and $\overline{Q}$ outputs of flip-flops 116A and 116F are respectively designated as H1 through H6 and $\overline{H1}$ through $\overline{H6}$. These are collected by the 12 NAND gates respectively 121, through 135 to provide 14 output count indications in their not form. These are designated by $\overline{X1}$ through $\overline{X14}$. Thus, upon the occurrence of an H1 and $\overline{H2}$ input to NAND gate 121, it will produce an output designated as $\overline{X1}$, which is the first output count of the counter. H6 and $\overline{H7}$ occurring at the input of NAND gate 126 produce an $\overline{X6}$ output, $\overline{H5}$ and H6 occurring simultaneously at the input of NAND gate 132 produces an $\overline{X12}$ output or a not 12 count output.

The manner in which the counter 116 functions is for each one of the flip-flops to successively assume its one state or state with its Q output high and thereafter each flip-flop successively returns to the state with its $\overline{Q}$ output high. The counter is cyclic and will repeat this operation in response to successive applications or clock pulses from the gated clock oscillator 134. This oscillator comprises a circuit which, in the presence of an enabling input from flip-flop 114 in FIG. 3, provides successive clock pulses, to the counter 116.

To illustrate how the counter works, assume initially that all the flip-flop stages are in their zero state. The $\overline{Q}$ output of flip-flop 116F is high. Upon the occurrence of the first clock pulse from the gated clock oscillator 134, flip-flop 116A will be driven to its one state with its Q output high, since its J input is now high and its K input is low. Upon the occurrence of the next clock pulse, flip-flop 116B assumes a one state. This progresses with successive clock pulses until flip-flop 116F assumes its one state. Since, the K input to flip-flop 116A is driven to its high state in response to H6 and H5 which are connected to the NAND gate 118A being high, flip-flop 116A is driven to its zero state with its $\overline{Q}$ output high. This zero state of the counter 116A is successively passed with the occurrence of each clock pulse to all of the flip-flops in the counter. From an understanding of the operation of this counter, it should now be understood how the inputs to the NAND gates 121 through 132 operate to produce the indicated count outputs.

Counter 140 is identical in construction with counter 116. Accordingly, it can produce 14 count outputs. It advances in respect to pulses obtained from the output of gate 110 in FIG. 3. These are essentially horizontal sync pulses. The NAND gates 141 through 150 are connected to the flip-flop outputs for the purpose of deriving the respective counts 1 through 14 which are in their "not" form. The Q and $\overline{Q}$ outputs of the respective flip-flops of the counter 140 are respectively designated from V1 through V7 and from $\overline{V1}$ to $\overline{V7}$. The counter 140, which counts for the vertical dot positions is given a count capacity of 14 counts. Since it is customary to reference the bottom line of a character as a first position and the top of a character as the last position, assuming each location or position of a line were given a number, the bottom of a character would be considered in the Y1 location and the top would be considered in the Y11 location. Therefore, while the present invention displays a character in television raster

form, where the top of the character appears first and the bottom last, the count output of the Y matrix counter is given a reverse count designation. That is, the first count of the counter is designated as $\overline{Y11}$ the eleven count of the counter is designated as $\overline{Y1}$, $\overline{V1}$ and $\overline{V7}$, which are generated when all of the stages of the counter are in their zero state, are combined to produce a Y14 count. The reasoning for this arrangement will become more clear with a description of FIG. 5.

FIG. 4 shows how pulse signals $\overline{X1}$ through $\overline{X14}$ and $\overline{Y1}$ through $\overline{Y11}$ and $\overline{Y14}$ are generated. In addition to these signals, other logic signals are required for the operation of this invention. Thus, in FIG. 4, a NAND gate 152 is used to collect $\overline{X10}$, $\overline{X11}$, $\overline{X12}$, $\overline{X13}$ and $\overline{X14}$ together with the Q output of a flip-flop 154. The Q output of the flip-flop 154 is enabled when a $\overline{Y14}$ signal is applied to its clock input. The flip-flop remains set until the occurrence of a $\overline{Y12}$ signal (Y5 and Y6). This is produced when counter 140 provides a $\overline{V5}$ and $\overline{V6}$ output to a NAND gate 156. Thus, flip-flop 154 is set at the end of a counting cycle of counter 140 and is reset upon the occurrence of the twelfth count output of the flip-flop 140. The output of NAND gate 152 is inverted by NAND gate 158 to produce a signal designated as PP1. The $\overline{X12}$ of "not 12" count of the counter 116 is inverted by a NAND gate 160 to produce an X12 count.

EXAMPLE OF A DOT MATRIX CHARACTER

FIG. 5

FIG. 5 shows the appearance of a character, "A," constructed of selected dots in a dot matrix in accordance with this invention, with the appropriate designations applied to the possible dot locations which may be used for representing a character. There may be as many as 32 of these characters displayed in a line across the face of the display tube. There may be as many as 16 of these lines displayed vertically. These values are given by way of illustration of an operative embodiment of the invention which has been built, and are not to be construed as a limitation upon the invention.

DISPLAY LINE COUNTER AND DISPLAY CHARACTER COUNTER

FIG. 6

The display line counter and the display character counter respectively 26 and 24 are each the usual binary counters with respective count capacities of 16 and 32. Each time an $\overline{X10}$ signal is generated by the X matrix counter 34, the display character counter is advanced one count. Each time a $\overline{Y14}$ signal is generated by the Y matrix counter 36, the display line counter is advanced one count. The display character counter has its respective outputs designated B1, $\overline{B1}$, B2, $\overline{B2}$, . . . through B16, $\overline{B16}$. The display line counter has its outputs designated as W1, $\overline{W1}$, W2, $\overline{W2}$, . . . W8, $\overline{W8}$. The character counter is the one which keeps track of the number of characters on a line, for which 32 are allowed. The $\overline{B16}$ output of the character counter, referring back to FIG. 3, is the output which turns off the gated clock oscillator. This occurs when the last character in a line has been displayed. The last output of the display line counter, which is designated as $\overline{W8}$ is the one which turns off flip-flop 108 in FIG. 3. This occurs at the end of the last line which is displayed.

CURSOR GENERATOR 54 AND COUNTERS 64, 66

FIG. 7

The cursor X counter 64 as shown in FIG. 7, is a reversible counter having any of the well-known reversible counter constructions. Its 32 outputs are respectively designated at A1, $\overline{A1}$ through A16, $\overline{A16}$. This counter is advanced by receiving a signal from whatever external data input device is employed. A signal for advancing the counter is supplied with each character when the display control is in its "write" mode. Such a signal is supplied from the typewriter to the "cursor right" input of the counter. The counter may be made to count in reverse by receiving an input signal on its "cursor left" terminal, from the typewriter keyboard. The cursor signal, which by way of example has been indicated as a background display of half intensity for a character, will occur at the proper time, at a location along a line determined by the count output or by the address represented by the count output of counter 64.

A cursor Y counter, which is similar in construction and operation to the cursor X counter, has a 16 count capacity and is also reversible. This counter is advanced by signals from the keyboard applied to its "cursor down" terminal and is caused to count backwards in response to pulses received which are applied to its "cursor up" terminal. This counter establishes, by its output, the line address on which the cursor signal is displayed. The output of this counter is designated by Z1, $\overline{Z1}$ to Z8, $\overline{Z8}$, with the Z8 signal being the 16the or highest count output of the counter.

The cursor is displayed only when there is a concurrence in the address indicated by the cursor counters and the display counters. To achieve this operation, a comparator circuit 162 compares the address outputs of the counter 64 and the counter 24, shown in FIG. 6, and when there is an identity it provides an output signal to a NAND gate 164. Another input to this NAND gate is the PP1 signal which is generated by the logic shown in FIG. 4. This PP1 signal, in view of the presence of the inverter 158, (in FIG. 4), is present from $\overline{X1}$ through $\overline{X9}$ time. From $\overline{X10}$ through $\overline{X12}$ time, the PP1 signal is not present and no output is obtained from NAND gate 164. Upon the occurrence of a comparator signal and a PP1 signal, a JK flip-flop 166 is driven so that its Q output is high. This flip-flop is reset upon the occurrence of an $\overline{X10}$ signal.

The occurrence of the cursor on a particular line is determined by the output of a comparator 170. This comparator compares the addresses provided by the output counts of the cursor counter 66 and the display line counter 26. The output of the y comparator 170 is applied to the NAND gate 168. The typewriter keyboard 14 will have a key which can be operated to actuate a circuit which can provide a voltage to a third input to the NAND gate 168 designated as the "cursor on-off" input. When this voltage is not present, no cursor is provided. This circuit is shown subsequently herein in FIG. 18.

Therefore, NAND gate 168 functions to provide a cursor signal output when there is a concurrence in the addresses at the outputs of the cursor *x* and *y* counters and the display character and line counters. Since the display counters are sequenced continuously through their count states, there will be concurrence of cursor and character counters only at one location over the entire face of the display tube. Accordingly, the cursor will be displayed at one character location only.

The memory storage device which is employed with this embodiment of the invention should be able to store, for readout onto the face of a display tube, as many characters as will be displayed across the face of the tube. The example given by way of illustration herein is 32 times 16 or 512 characters, or more correctly the code bits to represent 512 characters. Thus a total of at least 8×512 or 4,096 bits is required. There should be a character location in the memory which corresponds to the location on the display tube face at which that character is to be displayed. The memory must be addressed successively for the purpose of successively reading out the characters for display. The successive addressing of the memory is a function of the display counters.

The address of a location in the memory into which data is to be entered or read out (output data not display) is indicated by the address of the cursor. This address can be changed by applying signals to the cursor counters which establish the line and the location along the line desired for the cursor, and thereby the location in the memory into which data will be introduced. The cursor counters may be advanced by actuation of the typewriter keyboard in a normal manner for the purpose of writing character by character into the memory. Provision may also be made for advancing the cursor counters when input of characters is from a tape reader or any other source.

MEMORY ADDRESS GENERATOR 67

FIG. 8

FIG. 8 is a schematic representation of a memory address generator. By way of illustration, and not to serve as a limitation, a magnetic core memory was employed with an embodiment of this invention which was built and operated.

The memory address generator addresses the memory for the purpose of reading out the data stored therein which is converted into video signals and then displayed. The address generator also provides the address of the locations into which incoming data or readout data is stored. The display character and line counters provide the address information for instructing the memory as to the location from which display readout is to occur. The cursor X and Y counters provide the address information for instructing the memory as to the location at which data is to be entered.

As may be seen in FIG. 6, the memory address generator merely comprises a number of gates which are connected to the outputs of the respective display and cursor counters. The set of gates connected to the display counters are enabled during the process of display readout whereby the address presented to the memory is that indicated by the display counters. Alternatively, the gates connected to the cursor counter are enabled when write or readout operation for this invention is desired. The outputs from the flip-flops making up the display character counter 24 are respectively applied to each one of the NAND gates 171 through 175. It should be remembered that the counter 24 is a binary counter and its output presents a binary code pattern representative of one of its 32 counts. The inputs to these NAND gates are designated by the terminology B1, B2, B4, B8 and B16, which corresponds to the outputs shown for the counter 24 in FIG. 6. Similarly, the W1, W2, W4 and W8 outputs of the line counter 26 are respectively applied to the NAND gates 176, 177, 178 and 179.

The five outputs of the cursor character counter 64 are respectively applied to the respective counter 26 are respectively applied to the NAND gates 176, 177, 178 and 179.

The five outputs of the cursor character counter 64 are respectively applied to the respective NAND gates 180, 181, 182, 183 and 184. The outputs of the cursor line counter 66 are respectively applied to the respective NAND gates 185, 186, 187 and 188. NAND gate 189 receives the output of NAND gates 171 and 180. NAND gate 190 receives the output of NAND gates 172 and 181. NAND gate 191 receives the output of NAND gates 173, 182. NAND gate 192 receives the outputs of NAND gates 174 and 183. NAND gate 193 receives the outputs of NAND gates 175 and 184. NAND gate 194 has applied to it the outputs of NAND gates 176 and 185. NAND gate 195 receives the outputs of NAND gates 177 and 186. NAND gate 196 receives the outputs of NAND gates 178 and 187. NAND gate 197 receives the outputs of NAND gates 179 and 188.

An inverter 199 receives a signal from a read-write signal source 200, shown on FIGS. 9A, 9B, which is actuated by the typewriter keyboard or other input data source, when in the write mode. Otherwise, and normally, a low signal is received from the read-write signal source. Accordingly, the output of inverter 199 is high when in the read mode and is low when in the write mode. The output of inverter 199 is applied to an inverter 201 as well as to all of the NAND gates 171 through 179. The output of inverter 201 is applied to all of the NAND gates 180 through 188.

In the read mode, the output of inverter 199 is high whereby the NAND gates 171 through 179 are all enabled. The high input to inverter 201 results in a low output whereby NAND gates 180 through 188 are not enabled. Thus, the outputs of NAND gates 189 through 197 will be the outputs of NAND gates 171 through 179 or the address data from the display counters. In the readout or WRITE mode of operation, a high signal is applied to the input of inverter 199. This is inverted thus holding NAND gates 171 through 179 disabled. However, the inverter 201 will provide a high or enabling input to the NAND gates 180 through 188. As a result the NAND gates 189 through 197 will provide an address to the memory which constitutes the count outputs of the two cursor counters.

The memory which is to be employed with this invention may be any digital storage type memory. One that is preferred is the well-known magnetic core memory. The operations of addressing such a memory, entering data for storage and addressing such memory for writing and reading out the stored data are well known and accordingly need not be discussed here.

SUMMARY

As described thus far the display character counter 24 and the display line counter 26 provide an address which is used as the address of a character in memory as well as the location that that character is displayed on the face of the cathode-ray tube. The character read out of the core memory is entered into a display register where it is held for the purpose of being decoded and then applied to a video selector which selects the one of the video signals generated by a character generator, which corresponds to the character read from the memory. The output of the video selector is applied to a mixer circuit, if it is also desired to display the cursor on the CRT face. Otherwise the video selector output may be directly applied to the face of the CRT.

The timing problem is solved by the manner in which the display and matrix counters are driven. The display character counter has its count advanced once for every character to be displayed. The X matrix counter has its count advanced 12 times for every character to be displayed. The display line counter has its count advanced once for every line of characters which are displayed. The Y matrix counter has its count advanced 14 times corresponding to 14 video lines for each line of characters to be displayed. Logic gates select from the X and Y matrix counters the addresses within a dot matrix which are to be illuminated whereby a character is displayed. The character displayed is the one selected by the address represented by the count outputs of the display character and line counters.

The description given thus far is from the application for Display Device filed for Martin Kite et al., as previously indicated. The description of the present invention follows.

SUMMARY OF UPSHIFT AND DOWNSHIFT OPERATION

A brief description of the upshift operation is as follows. The cursor is placed by means of the keyboard control, at a location at which it is desired that an upshift operation commence. Thereafter, the upshift key is depressed at the keyboard. The address of the readout from the memory is then no longer under the control of the character and line counter, but is completely under the control of the cursor character and cursor line counter. The logic provided reads the character from memory moves the cursor location from the one indicative of the character to be read out from memory to a location on the line immediately above the one where the character read out from memory would have been otherwise displayed. The character is written back into memory at this location. The cursor character counter is then incremented by one, causing the cursor to move one character position to the right, and the cursor line counter is then incremented by one causing the cursor line position to drop down one line. The memory is then addressed again by the cursor counters and the cycle just described is repeated. When the cursor reaches the end of the line, it is transferred to the beginning of the next line which is the address of the next line of characters to be read out from memory.

The upshift operation continues until the end of line 16 has been read out and rewritten in line 15. At this time, the infor-

mation stored for line 16 which has just been written on line 15, is erased from line 16, and the cursor is transferred to the beginning of line 16 to await the entry of new information from the keyboard.

On the downshift operation, an address at which downshift operation should terminate is stored. Upon application of the downshift signal, the cursor is stepped down until it reaches the line 15 address position. Readout of characters then commences in a manner somewhat similar to the upshift manner of character readout. The data stored in line 15 is written on line 16. The data stored in line 15 is written on line 16. The data stored on line 14 is written on line 15, etc. This operation continues until the cursor reaches the stored address, when the operation terminates after erasing one line.

UPSHIFT OPERATION DETAIL

Reference will now be made to FIGS. 9A, 9B, 10, and 11 and timing diagram 12. FIGS. 9A, 9B, 10 and 11 are a block schematic diagram of the logical circuitry employed for the upshift operation.

An upshift key 202, which is on the input typewriter keyboard or other input device, is actuated when the upshift operation is desired. This applies a positive pulse signal to an inverter 204, whose output is applied to a flip-flop 206. The flip-flop is set in response to its input providing a US signal at its set output and a $\overline{US}$ signal at its reset output. The US signal from flip-flop 206 is applied to an OR gate 208. The output of the OR gate 208 is applied directly to the reset input of a flip-flop 210, and through an inverter 212 to the set input of the flip-flop 210. This flip-flop is of the JK variety, and requires a clock pulse in order to assume the state established by its inputs. The clock pulse for this flip-flop is provided by the system vertical sync signals. In the presence of a US signal and upon the occurrence of the next vertical sync pulse, flip-flop 210 is driven to its reset state or state where one of its outputs designated as SH is high and the other of its outputs designated as $\overline{SH}$ is low. The SH output is applied to an AND gate 214. This AND gate requires, as its second input, a DS or downshift signal. This signal is not present at this time, therefore no output is obtained from the AND gate 214.

The SH output is applied to an OR gate 216. The other input to this OR gate is the keyboard read/write signal source 200. That is, these are the read/write memory address control signals which are generated in the normal mode of operation of the system which instructs the memory to display from the address provided by the character counters and to write or readout in the address provided by the cursor counter. The output of the OR gate 216 is applied to the inverter 199 in FIG. 8 to thereby cause the memory to be addressed for both read and write operations by the address in the cursor line and character counters.

The gated multivibrator 218, is gated on in the presence of three signals. These are the reset output of flip-flop 220, and an SH signal, or a US or DS signal. Since flip-flop 220 is in its reset state and SH and US signals are present, the multivibrator commences oscillating and provides as its output alternatively WR and $\overline{WR}$ pulses. The WR pulse is applied to a pulse shaper 220 to be squared, and then is applied to an OR gate 222. The output of the OR gate is a read strobe signal, which is applied to the memory to cause it to read out a character from the address indicated by the memory address gates. The address in this instance would be that indicated by the cursor X and Y counters. When the display device is not in upshift or downshift mode, the normally generated read strobe signal is applied to an AND gate 224, whose other input is a $\overline{US+DS}$ signal. An output of the AND gate 224 is applied to OR gate 222 when the normal addressing operation of the memory is to take place.

The $\overline{WR}$ output of the multivibrator 218 is applied to a pulse shaper 226, whose output is thereafter applied to an OR gate 228. The output of the OR gate 228 is the write strobe signal for the memory to instruct it to write back into the memory a character which has just been read out.

For normal writing operation, an AND gate 230 has its output connected to the OR gate 228. The two required inputs to this AND gate are the $\overline{US+DS}$ signal and the normal write strobe signal.

To summarize the operations achieved thus far, upon actuation of the upshift key, after the next vertical sync signal, the memory read/write addressing operation is now directed solely by the address displayed by the cursor line and character counters. Alternate reading and writing strobe signals for causing the memory to read and write in response thereto are initiated.

In FIG. 10 there is shown a line address register 232. Upon the occurrence of the $\overline{US}$ signal, all 1's are directly entered into this register representing the cursor line address in the last line of the display, or the 16th line.

Referring now to FIG. 11, at the beginning of each memory operation, (comprising either readout of a character or a write in of that character), a double pulse, as shown in FIG. 12, which is designated as SU is generated by an SU pulse source is applied to two NAND gates respectively 234, 236. The other input to the NAND gate 234 is a $\overline{US+DS}$ signal. The second input to the NAND gate 236 is a US+DS signal. In the normal mode of operation of the display system, the double SU pulses can pass through the AND gate 234 to an OR gate 238. The output of this OR gate is applied to the cursor right terminal of the cursor X counter 64 shown in FIG. 7. The output of OR gate 238 is also applied to an AND gate 240, whose other required input in the $\overline{WR}$ signal. This effectively corresponds to the write strobe signal. Accordingly, no output is derived from AND gate 240 except when the display device is operating in either the upshift or downshift mode.

In the upshift or downshift mode of operation, an AND gate 240 output is achieved in the presence of the $\overline{WR}$ signal. This signal is slightly delayed by a delay network 242, and then applied to a trailing edge detector 244. The output of the trailing edge detector is a coincidence strobe signal hereafter designated at CS.

The output of the NAND gate 236, which only occurs when the display system is operating in either the upshift or downshift mode, is a double pulse (corresponding to the SU double pulse). This is applied to a one shot pulse stretcher 246. This circuit operates to convert the double pulse into a single pulse. The output of the one shot pulse stretcher is a single broad pulse designated as SU. The trailing edge of this output is applied to the NOR gate 238, and the actual broad pulse is applied to the one shot 248. The one shot 248 is inhibited in the presence of a WR signal, which is applied to the one shot 248. The one shot 248 is inhibited in the presence of a $\overline{WR}$ signal, which is applied to the inverter 250 whose output serves to inhibit the one shot. Accordingly, in the absence of ea $\overline{WR}$ signal the output of the NOR gate 238 again consists of two narrow SU* pulses. In the presence of a $\overline{WR}$ signal the output consists of a single SU* signal. The timing of these signals as well as their waveforms may be seen in FIG. 12. Since a character is displayed in the next character time after the one during which it is read out of memory, the memory address is ordinarily stepped back one count before a readout or write operation and the two SU pulses after that restore the addressing counters to their correct address for cursor display.

In response to the SU* pulse train after a read operation the cursor character counter is advanced only one count, which compensates for the one count reverse which occurs in response to the read operation of the memory. The character cursor address is unchanged after the read cycle. The two SU* pulses which are applied after the writing operation, advances the count of the X counter by two counts, thus leaving it on the address of the next character to be read.

In order to advance the cursor line counter or Y counter, the circuitry shown in FIG. 11 is employed. A NAND gate 252 receives as a required input the SU signals, the US signal and the WR signal. In the presence of these signals an output is provided to an OR gate 254. The output of the OR gate 254 as indicated, is connected to the cursor down terminal of the Y counter, which is shown in FIG. 7. The OR gate 254 will pro-

vide an output also when in normal operation a cursor down signal is applied from the keyboard. Another input to the OR gate **254** which can cause the cursor line counter to increase its count may be obtained from another NAND gate **258**. Its output is applied to the OR gate **254**. NAND gate **258** produces an output in the presence of a $\overline{WR}$ signal, a DS signal, or an HG signal. The derivation of the HG signal will be shown subsequently herein. It is sufficient to know however that it is obtained from horizontal sync signals. The derivation of the DS and the $\overline{DS}$ signal will also be indicated in the description of the downshift mode of operation.

For moving the display of the character up one line, a cursor up signal is generated. This is provided by a NAND gate **260**, which requires as its input an *SU* signal, a US signal and a $\overline{WR}$ signal. Its output is applied to a NOR gate **262**. The output of the OR gate is applied to the cursor up terminal of the Y counter as shown in FIG. **7**.

At the end of an upshift sequence, which occurs with the cursor in line **1** address, it is necessary to reposition the cursor to the first character position of line **16** after information has been erased. This function is carried out by the signal received when flip-flop **206** is reset whereby $\overline{US}$ signal is applied to an inverter **264**, whose output is applied to the OR gate **262**. This returns the cursor to the beginning of a line that becomes erased at the end of the upshift sequence.

The input to the OR gate **262** from NAND gate **266** is employed during the downshift sequence. This output is achieved in the presence of an SU signal, a DS signal and a WR signal.

In summary of the foregoing therefore, upon the application of an upshift signal, the logic provided waits for the next vertical sync pulse. A line address register has the address of the last line of the display tube inserted therein. Thereafter a character is read from memory. The cursor line counter count is reduced by one count causing the cursor to be displaced upward by one line. This occurs because at the time of the read operation, the $\overline{WR}$ signal is high. This, as may be seen from FIG. **11**, causes an output from the OR gate **262** which causes the cursor line counter to decrease one count.

A WR signal is generated which causes the write strobe signal to occur. This is followed by the application of a count signal (an increase in the count of the counter) to the Y counter of the cursor also immediately followed by the cursor being shifted one character to the right. The next readout cycle occurs from that address.

It should be noted that the character which is read out from a line, is written back into the memory at an address which is on the line immediately above the one from which it was read out.

The address in the line address register **232** is compared with the address in the Y cursor counter by a coincidence detector **270** in the presence of a CS pulse. When these addresses are identical, which happens when the downshift operation brings the cursor line counter down to the beginning of the bottom line, the coincidence detector provides a "coincidence" output. An inverter **272**, in well known fashion provides a $\overline{\text{coincidence}}$ output. The $\overline{\text{coincidence}}$ and CS signals are applied to a NAND gate **274**. It should be noted that the CS signal appears only before a write strobe. AND gate **274** applies its output to set a flip-flop **276**. Since the cursor address is set to line **16** each time just before the read signal, the CS and coincidence signals are obtained while the entire line **1** is being written on line **16**. Simultaneously AND gate **280** is enabled by set output of flip-flop **276** to insert null representative signals (MC) into the input register of the memory. These are in place of the characters which would otherwise be written back into memory. Accordingly, the line **16** or last line location of the memory is emptied.

After line **16** is completed, i.e. erased, the cursor line counter contains the address of line **1**, immediately preceding a write strobe. At this time, the $\overline{\text{coincidence}}$ signal is generated and in the presence of CS resets flip-flop **276**, which, in turn, results in the termination of the operation of the gated multivibrator **218**, which generated the read/write strobes. At this time, the upshift cycle ends and flip-flop **210** is reset by the next vertical sync pulse.

From the point where upshift started all the information which remains in the memory has been shifted up by one line. The bottom line is available for entry of data thereinto. A power reset signal **281** is generated by power turn on to initialize the system by applying a PR pulse to all flip-flops.

DOWNSHIFT OPERATION

In order to enable downshift operation to occur, a downshift key **280** on the typewriter keyboard is actuated. This applies a pulse to an inverter **282**, the output of which causes flip-flop **278** to assume its reset position. This provides a DS signal from the reset output of the flip-flop and a $\overline{DS}$ signal from the set output of the flip-flop. The DS signal is applied through OR gate **208** to the flip-flop **210**. As before, upon the occurrence of the vertical sync pulse, flip-flop **210** assumes its reset state where upon there is an SH and $\overline{SH}$ output. Cursor control of the addressing for write in and read out is provided in response to the output of the OR gate **216**.

AND gate **214**, in view of the presence of the DS and SH signals applies an output signal to a first delay circuit **282**. The output of the first delay circuit is applied to a second delay circuit **284**. The reason for using these two delay circuits is to insure that the address lines from the output of the cursor X and Y counters are stabilized. The output of the delay circuit **284** is used both to set a flip-flop **286**, and also to strobe into the line address register **232**, the address which is in the cursor Y counter at this time. The set output of flip-flop **220** is applied to an AND gate **286**. The other input to this AND gate comprises horizontal sync pulses which are applied therethrough an inverter **288**. The output of the AND gate **286** comprises the HG pulses which have horizontal sync frequency.

The HG pulses are applied to the OR gate **254** in FIG. **11**. The OR gate **254** applies these pulses to the cursor down terminal of the Y counter.

As a result, the cursor is moved successively down each line until it reaches line **15**. The output of the cursor line counter is applied to a line **15** detector **288**, which simply comprises a set of gates which are enabled when the line counter obtains the count of **15**. The output of these gates is applied to flip-flop **220** to cause it to be reset. This terminates the HG pulse train and enables the gated multivibrator **218** to commence generating WR and $\overline{WR}$ pulses.

The first character to be read out of memory is the first character on the 15th display line. This is written in the first character position of the 16th display line. The timing sequence for downshift is very similar to upshift with the exception that cursor down operation follows read strobe and cursor up operation follows a write strobe. This may be seen by the timing diagram shown in FIG. **13**. The result of this is that the end of a display line is gone through immediately after a cursor up signal. The downshift sequence works its way from left to right on the screen and from bottom to top, as the cursor line counter is incremented in an up direction.

The logic circuits which have been described in connection with the upshift operation, operate to provide the *SU*, SU* signal, the CS signal, the WR and $\overline{WR}$ signals, and the cursor counter signals to cause them to advance the display in the manner described. When the cursor line counter is advanced to the line at which the coincidence detector **270** detects coincidence between the line address entered into the register **232** at the beginning of the operation at the present line address, then a coincidence output signal is derived. Coincidence is now detected immediately preceding the write strobe, between the line address of the cursor counter and the line address contained at the beginning of the operation. At this time, flip-flop **276** is set, as it was in the case of upshift. Then, the MC* null signals are directed into the input register for the line on which the cursor started out. Finally, when the next line to be written yields a noncoincidence condition, flip-flop **274** is reset, which in turn leads to setting flip-flop **278**, and

flip-flop 210 is reset on the next vertical sync pulse. The downshift cycle is now completed. The result of a downshift cycle operation from the point where the cursor started is to cause all of the date in memory to be downshifted one line leaving the line at which the downshift operation terminated blank, for entry of data thereinto.

There has been accordingly described and shown herein a novel, and useful system for enabling the operation of a display system to provide a display of data downshifted one line from the position it normally would occupy, or upshifted one line from the position it normally would occupy, leaving provision for entering data into the top or bottom of the display or any line in-between after the completion of the downshift or upshift operation.

I claim:

1. In a continuous display system of the type wherein a memory stores data in the form of characters in predetermined lines of characters and said data is read out of said memory to be displayed on the face of a display tube at line locations corresponding to the line locations of said memory, means for altering the display location of said data by a line comprising;

means for establishing the address of the last line location at which it is desired to terminate the alteration operation,

address means for establishing a character address in memory from which readout of said character is to occur,

means for incrementing the address of said address means to sequence through the addresses of successive characters and successive lines of characters,

means for successively reading data character by character from one line of memory whose address is provided by said address means and for writing it back into memory at another line,

detecting means for recognizing coincidence between the address established by said means for establishing and the address reached by said address means and producing a coincidence signal responsive thereto,

means responsive to said coincidence signal for writing zeros into the last line location of memory from which readout occurs, and

means responsive to said coincidence signal and the completion of the writing of zeros in the last line for terminating operation of said previously recited means whereby said data upon subsequent readout is displayed, displaced by a line.

2. In a continuous display system as recited in claim 1 wherein said address means includes:

a first counter means for indicating the line address of a character and a second counter means for indicating the address of the character along a line,

said means for successively reading data includes means for generating alternate read strobe and write strobe signals,

memory control means responsive to a read strobe signal and the address indicated by said first and second counters to read a character out of said memory from said address and responsive to a write strobe signal and the address indicated by said first and second counters to write the character read out of said memory back into memory at the address indicated by said first and second counters,

first address change means responsive to said read strobe signal to alter the count of said first counter means before the occurrence of the succeeding write strobe signal, and

second address change means responsive to said write strobe signal to alter the count of said second counter means before the occurrence of the succeeding read strobe signal.

3. In a continuous display system as recited in claim 2 wherein said first address change means includes means for increasing the count of said first counter means, and said second address change means includes means for decreasing the count of said second counter means.

4. In a continuous display system as recited in claim 2 wherein said first address change means includes means for decreasing the count of said first counter means, and said second address change means includes means for increasing the count of said second counter means.

5. In a display system wherein characters of data are stored in a memory at address locations, each of which corresponds to an address location on the face of a display tube upon which the data will be displayed, each character of said data having an address location in the form of a horizontal position along a line designated by X*a* where "*a*" is a number indicating the position along a line and a vertical position designated by "Y*b*"where "*b*" is a number indicating the vertical position of said line, there being a cursor address means for providing addresses for write into memory, a display address means for providing addresses for readout of memory for display, and a memory address means for addressing said memory for write in responsive to said cursor address means or read out responsive to said display address means, means for altering the address of said data in said memory by a line and for enabling data display at said new line address comprising;

means for applying only said cursor address means output to said memory address means for readout as well as write in,

means for alternately ordering a readout of a character from memory and a write back of said character in memory,

means responsive to said means for alternately ordering for changing said cursor address means in sequence after a read out from X*a*, Y*b* to X*a*, Y*b*−1; and then after a write in to X*a*+1, Y*b*, then after a readout to X*a*+1, Y*b*−1, then after a write in to X*a*+2, Y*b*, . . . until the address X*a*+*n*, Y*b*−*n* has been reached, where X*a*,+*n*is the X address of the last character in memory and Y*b*−*n* is the Y address of the last character in memory, .

means for sensing when the address of a last line of characters in said memory is reached,

means responsive to the output of the means for sensing for erasing said last line of characters after it has been read, and

means responsive to the erasure of said last line of characters for terminating the operation of all of said aforesaid means.

6. In a display system wherein characters of data are stored in a memory at address locations, each of which corresponds to an address location on the face of a display tube upon which the data will be displayed, each character of said data having an address location in the form of a horizontal position along a line designated by X*a* where "*a*" is a number indicating the position along a line and a vertical position designated by Y*b* where "*b*" is a number indicating the vertical position of said line, there being a cursor address means for providing addresses for write into memory, a display address means for providing addresses for readout of memory for display, and a memory address means for addressing said memory for write in responsive to said cursor address means or read out responsive to said display address means,

means for altering the address of said data in said memory by a line and for enabling data display at said new line address comprising;

means for applying only said cursor address means output to said memory address means for read out as well as write in,

means for alternately ordering a read out of a character from memory and a write back of said character in memory,

means responsive to said means for alternately ordering for changing the address of said cursor address means in sequence after readout from X*a*, Y*b* to X*a*, Y*b*+1, then after a write in to X*a*+1, Y*b* then after a readout to X*a*+1, Y*b*+1, then after a write in to X*a*+2,Y*b*, . . . until the address X*a*+*n*, Y*b*+*n*, has been reached where X*a*+*n*, Y*b*30 *n* is the X, Y address of the character in memory at which it is desired to terminate the operation,

means for sensing when the address of a last line of characters in said memory is reached,

means responsive to the output of the means for sensing for erasing said last line of characters after it has been read, and

means responsive to the erasure of the last line of characters for terminating the operation of all of said aforesaid means.

7. In a continuous display system of the type wherein a memory stores data in the form of characters in predetermined lines of characters, and said data is read out of said memory to be displayed on the face of a display tube at line locations corresponding to the line location addresses in said memory, means for shifting said data downward by a line comprising:

means for establishing an address corresponding to a location on said display tube at which it is desired to terminate a downshift operation,

means for reading data from said memory commencing with the address of data stored in the next to the last line in memory, reading each line of data above the next to the last line out of said memory and writing each line of data back into the line location immediately below the line from which readout has occurred,

coincidence detecting means for detecting when the address of the line which is read from memory is the same as the address which was established and producing a signal,

means for erasing the line of data which is stored at the address for terminating said downshift operation responsive to said coincidence detecting means signal, and

means rendered operative when said line of data has been erased for terminating further operation of all of the aforesaid means to terminate said downshift operation.

8. In a continuous display system for successively reading data out of memory and displaying it, wherein a memory stores data in the form of characters in predetermined lines of characters and said data is read out of said memory to be displayed on the face of a display tube at line locations corresponding to the line location addresses in memory,

means for shifting said data upward by a line comprising:

means for storing an address corresponding to the location of the last line of data displayed on said display tube,

means for reading data from said memory commencing with a desired line address and successively reading each line of data below said desired line address and writing each line of data back in said memory at a line address above the location address from which a line of data is read out,

coincidence detecting means for detecting when the address of the line which is read from memory is the same as the address which is stored,

means for erasing the line of data which is stored at the address of the last line of data in said memory responsive to said coincidence detecting means signal, and

means for terminating further operation of all of the foregoing means after said line of data is erased to terminate said upshift operation.

9. In a continuous display system for successively reading data out of memory and displaying it wherein a memory stores data in the form of characters at addresses established by line and position along a line, said memory being addressed for write in and read out by a line counter means and a character counter means, and data read out of said memory is displayed on the face of a display tube at line locations and locations along a line corresponding to the line location addresses in said memory, means for shifting said data display and storage downward by a line comprising:

means for establishing the address at which it is desired to terminate,

means for causing said line counter means to increase its count until it indicates the address of the next to the last line in said memory,

means for reading out of memory a character at the address indicated by said line and character counter means,

means for increasing the count of said line counter means by one count,

means for writing said readout character back in memory at the new address established by said line and character counter means,

means for decreasing the count of said line counter by one count and for increasing the count of said character counter means by one count,

means for detecting when the address of the data being read out of said memory corresponds to said established address and producing a coincidence signal output,

means responsive to said coincidence signal for erasing the line of data from memory at said established address, and

means responsive to a termination of said coincidence signal to terminate the operation of all of said foregoing means to terminate said downshift operation.

10. In a continuous display system for successively reading data out of memory and displaying it wherein a memory stores data in the form of characters at addresses established by line and position along a line, said memory being addressed for write in and read out by a line counter means and a character counter means, and data read out of said memory is displayed on the face of a display tube at line locations and locations along a line corresponding to the line location addresses in said memory, means for shifting said data display and storage upward by a line comprising:

means for reading out of memory a character at the address indicated by said line and character at the address indicated by said line and character counter means, to be displayed on said display tube,

means for decreasing the count of said line counter means by one count,

means for writing said displayed character back in memory at the new address established by said line and character counter means,

means for increasing the count of said line counter and of said character counter by one count,

means for detecting when the address of data being read out of said memory has reached the last line in said memory and producing a coincidence output signal,

means responsive to said coincidence signal for erasing the last line of data from said memory, and

means responsive to a termination of said coincidence signal to terminate the operation of all of the aforesaid means to terminate said downshift operation.

11. In a continuous display system of the type wherein a memory stores data in the form of characters in predetermined lines of characters, and said data is read out of said memory to be displayed on the face of a display tube at line locations corresponding to the line locations in said memory,

the steps of downshifting said data downward by a line comprising:

storing the address of a location on said display tube at which it is desired to terminate a downshift operation,

reading character by character from memory commencing with the next to the last line in memory and successively for each line of data above the next to the last line, reading a line of data out of said memory, writing each character read from memory back into memory on the line below the line from which data has been read out,

detecting when the address of the line which is displayed is the same as the address which was stored and producing a coincidence signal,

erasing the line of data which is stored at the address for terminating said downshift operation responsive to said coincidence signal, and

terminating further downshift operation at the termination of said coincidence signal.

12. In a display system of the type wherein a memory stores data in the form of characters in predetermined lines of characters, and said data is read out of said memory to be displayed on the face of a display tube at line locations corresponding to the line locations in said memory,

means for shifting said data downward by a line comprising:

means for storing the address of a location at which it is desired to terminate a downshift operation,

means, commencing with the next to the last line in memory, and successively for each line of data above the next to the last line, reading a line of data out of said memory and writing it back into the line location immediately below the line from which readout has occurred,

coincidence detecting means for detecting when the address of the line which is being written is the same as the address which was stored,

means for erasing the line of data which is stored at that address responsive to said coincidence detecting means signal, and

means for terminating further downshift operation when said line of data has been erased.