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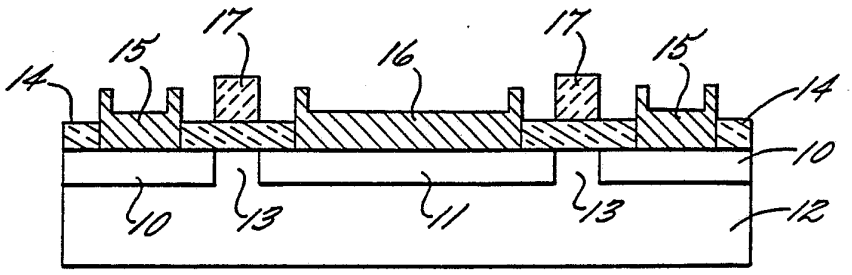

(57) Abstract

The present invention comprises a metal-oxide-semiconductor field-effect transistor (MOSFET) formed in silicon carbide (12). The doped source (10) and doped drain (11) are formed by high temperature ion implantation of dopant ions into the silicon carbide (12).

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MOSFET IN SILICON CARBIDE

Field of the Invention

The present invention relates to metal oxide semiconductor field effect transistors (MOSFETs), and in particular to such transistors formed in silicon carbide.

Background of the Invention

The growth in the use of semiconductor devices for electrical applications has resulted in a number of different devices which have particular application in the creation of circuits and electrical components. One type of device is known as a metal-oxide-semiconductor field-effect transistor (MOSFET) which is named after its three main components. In broader terms, such a device can be referred to as a metal-insulator-semiconductor field-effect transistor (MISFET), but as the most common applications use an oxide as the insulating layer, the oxide designation will be used primarily throughout this application. It will be understood, however, that other insulating materials can be appropriately used and referred to.

A field effect transistor differs somewhat from a junction transistor. Junction transistors, which historically were the first developed, are formed when two p-n junctions are placed in close proximity with one another and share a small portion of the semiconductor material known as the base. A junction transistor controls the flow of current from a portion of semiconductor material adjacent

from a portion of semiconductor material adjacent one of the junctions (the collector) through the base and then to and out from the semiconductor portion adjacent the other junction (the emitter) by controlling the applied voltage on the base.

A field effect transistor works on a somewhat different principle. Typically, current enters a field effect transistor through a region of semiconductor material known as the source, and exits the semiconductor material from another region of semiconductor material known as the drain. The source and drain are separated from each other by yet another region of semiconductor material which is known as the gate. When an appropriate voltage of either positive or negative bias (depending upon the type of transistor) is applied to the active region through the gate, current can be controlled. In particular, if the semiconductor material in the gate is an n-type material through which current would normally flow, applying a negative bias to the gate depletes electrons from the active region, making the conducting channel smaller and thereby hindering the flow of electrons from the source to the drain. Such a device is referred to as a depletion mode MOSFET. Alternatively, where the semiconductor material in the gate is a p-type material which is normally nonconductive, applying a positive bias voltage to the gate depletes holes from the region, making it more conductive from the resulting excess of electron carriers.

In order to passivate the surface of the source and the drain and isolate the gate contact from the gate semiconductor portion, an insulator material is positioned between these respective portions. Because silicon is presently the semiconductor material most commonly used in MOSFETs, the insulating portion most commonly is

formed from silicon dioxide. The gate contact, which can be a metal or other conductive material, the insulator (usually silicon dioxide), the semiconductor material and the device's method of operation give the MOSFET its name.

The MOSFET has gained wide acceptance as an appropriate device since its introduction. As is the with all other semiconductor devices, however, some of the characteristics of a MOSFET will be limited by the characteristics of the semiconductor material from which it is formed. Because silicon has some inherent limitations for certain applications, corresponding MOSFETs formed from silicon will also have inherent limitations.

Accordingly, it has long been recognized that one method of improving the performance of devices is to attempt to form them on materials having superior characteristics. One such material having a number of superior characteristics is silicon carbide (SiC). Silicon carbide has some excellent semiconductor properties: a wide bandgap, a high thermal conductivity, a high melting point, a high breakdown electric field strength and a high saturated electron drift velocity. The wide bandgap gives silicon carbide advantages over semiconductor materials with narrower bandgaps. Additionally, its high thermal conductivity and better temperature stability mean that devices made from silicon carbide can be packed more closely together without risk of destroying each other from dissipated heat energy, and devices made from silicon carbide can operate at significantly higher temperatures than can those devices made from narrower bandgap semiconductors.

Accordingly, a number of attempts have been made to form devices, and specifically MOSFETs, on silicon carbide. Silicon carbide is, however, a

successful production of crystalline silicon carbide of an appropriate chemical purity and low defect level has remained a somewhat elusive goal, and the growth of single crystal thin films and large crystals have heretofore been difficult to accomplish. Additionally, successful introduction and activation of the necessary dopant ions into silicon carbide for device manufacture has likewise proved difficult.

These problems have recently been successfully addressed as described in several co-pending United States patent applications assigned to the assignee of the present invention, the contents of which are incorporated herein by reference. These include "Growth of Beta-SiC Thin Films and Semiconductor Devices Fabricated Thereon," Serial No. 113,921, Filed October 26, 1987; "Homoepitaxial Growth of Alpha-SiC Thin Films and Semiconductor Devices Fabricated Thereon," Serial No. 113,573, Filed October 26, 1987; and "Implantation and Electrical Activation of Dopants into Monocrystalline Silicon Carbide," Serial No. 113,561, Filed October 26, 1987. The advances in forming silicon carbide thin films, silicon carbide single crystals, and in successfully doping silicon carbide according to these methods have rekindled interest in producing commercial-quality devices from silicon carbide, including transistors.

A number of attempts have been made to produce various junctions, diodes, rectifiers and other contacts on silicon carbide. More specifically, however, in the patent literature, Wallace No. 3,254,280 discusses a method of forming a junction transistor in silicon carbide. According to Wallace, the appropriate necessary single crystals of silicon carbide can be "grown in accordance with any suitable procedure known to

accordance with any suitable procedure known to those skilled in the art," and doping can take place using "any . . . method known in the art." Although the production of doped single crystal silicon carbide is rather easily dismissed in Wallace's discussion, in practice forming doped single crystals of appropriate purity and defect level is quite difficult and commercial devices based on Wallace's teaching have not been observed.

Hall No. 2,918,396 also discusses a method of forming a junction type transistor in silicon carbide in which the primary technique suggested by the disclosure is that of placing an alloy formed of silicon along with an "activator" (dopant) on the surface of a single crystal of silicon carbide, raising the silicon carbide to a temperature below its melting point but sufficient to cause the alloy to melt and dissolve a surface portion of the silicon carbide. When the materials are cooled, a p-n junction hopefully results. According to Hall, appropriate crystals can be prepared using the Lely technique. As is known to those familiar with silicon carbide technology, however, the Lely process represents an unseeded sublimation technique which has generally failed to overcome the inherent difficulties in producing device quality single crystals of silicon carbide.

Other researchers have made specific attempts to produce workable MOSFETs on silicon carbide. For example, in Inversion-Type MOS Field Effect Transistors Using CVD Grown Cubic SiC on Si, Jap. J. Appl. Phys. 23, L862 (1984), Shibahara et al. discuss their attempts to produce an inversion type, n-channel MOSFET on cubic silicon carbide grown on the (100) face of silicon by chemical vapor deposition (CVD). Shibahara's work is also discussed in Novel Refractory Semiconductors,

Materials Research Society Symposium Proceedings, edited by T. Aselage, D. Emin, and C. Wood (Materials Research Society, Pittsburgh, PA, 1987), Vol. 97, p. 247.

In spite of these described methods, the devices fabricated by Shibahara et al. have never been demonstrated to have successfully operated above room temperature. As discussed earlier, operation of devices at very high temperatures is one of the particular reasons for seeking to form devices on silicon carbide. Devices formed on silicon carbide which cannot operate at temperatures different from those upon which devices formed on silicon can operate offer no particular advantage.

Kondo et al. also describe an experimental MOSFET produced on beta silicon carbide in Experimental 3C-SiC MOSFET, IEEE Electron. Device Lett., EDL-7, 404 (1986). According to this discussion, Kondo first grew beta silicon carbide film epitaxially on a p-type silicon (100) substrate using CVD. Kondo fabricated a depletion mode MOSFET; nevertheless, the resulting device showed no current saturation, no threshold cutoff, and no high temperature capability. Therefore, the techniques disclosed in Kondo's study must be deemed unsuccessful.

Accordingly, it is an object of this invention to produce a metal-oxide-semiconductor field-effect transistor (MOSFET), fabricated from silicon carbide.

It is another object of the invention to provide both inversion mode and depletion mode MOSFETs fabricated from silicon carbide.

It is a further object of this invention to provide a MOSFET formed on silicon carbide which can operate at temperatures as high as 650° centigrade.

It is another object of the invention to provide a method of forming a metal-oxide-semiconductor field-effect transistor suitable for operation at temperatures of at least 650° centigrade and high radiation densities by oxidizing a silicon carbide substrate having a first conductivity type to form a silicon dioxide surface layer, selectively applying gate contact material to the silicon dioxide surface layer, forming a doped source and a doped drain of a desired conductivity type by high temperature implantation of doping ions, and applying the source and drain contacts.

It is a further object of this invention to provide a method of forming an inversion mode metal-insulator-semiconductor field-effect transistor suitable for operation at temperatures of at least 650° centigrade and high radiation densities, by forming a doped source and a doped drain having a first conductivity type in a doped portion of silicon carbide having a second conductivity type by high temperature implantation of source and drain with doping ions.

It is yet another object of the invention to provide a method of forming a depletion mode metal-insulator-semiconductor field-effect transistor suitable for operation at temperatures of at least 650° centigrade and high radiation densities, by forming a more heavily doped source and a more heavily doped drain in a silicon carbide semiconductor portion having the same conductivity type as the doped source and doped drain by high temperature implantation of source and drain with doping ions.

Other objects and advantages of the invention and the manner in which the same are accomplished will be set forth in the accompanying detailed description which illustrates exemplary and

preferred embodiments, and in the following drawings in which:

Description of the Drawings

Figures 1-5 illustrate several of the steps and the resulting structure of an n-channel inversion mode metal-insulator-semiconductor field-effect transistor formed according to the present invention;

Figure 6 is a cross-sectional view of an n-channel depletion mode metal-insulator-semiconductor field-effect transistor according to the present invention;

Figure 7 is a plot of drain current versus drain voltage at a temperature of 296K for an n-channel depletion mode MOSFET according to the present invention;

Figure 8 is another plot of drain current versus drain voltage at a temperature of 573K for the same MOSFET as Figure 7 according to the present invention; and

Figure 9 is yet another plot of drain current versus drain voltage at a temperature of 923K for the same MOSFET as Figures 7 and 8 according to the present invention.

Summary of the Invention

The invention is a method of forming a metal-oxide-semiconductor field-effect transistor suitable for operation at temperatures of at least 650° centigrade, and at high radiation densities and at high power levels. The method comprises oxidizing a silicon carbide substrate having a first conductivity type to form a silicon dioxide surface layer, then selectively applying gate contact material to the silicon dioxide surface layer. A doped source and a doped drain of a desired conductivity type are formed by high temperature

implantation of doping ions, following which source and drain contacts are applied.

As an example of the invention, depletion mode n-channel metal-oxide-semiconductor field-effect transistors were fabricated on n-type beta silicon carbide (111) thin films epitaxially grown by chemical vapor deposition on the (0001) face of 6H alpha silicon carbide single crystals. The gate oxide was thermally grown on the silicon carbide, the source and drain were doped n^+ by nitrogen ion implantation at 823K. Stable saturation and subthreshold current was achieved at drain voltages (V_{DS}) exceeding 25 volts. Transconductances as high as 11.9 mS/mm were achieved. Stable transistor action was observed at temperatures as high as 923K, the highest temperature reported to date for a transistor in any material.

Detailed Description

Historically, research on electrical devices formed on silicon carbide has been rather limited, mainly because of the difficulty in obtaining high quality silicon carbide films. Recently, however, and as described in the co-pending patent applications to the same assignee described earlier, success in growing both alpha and beta silicon carbide thin films on silicon carbide substrates, as well as success in growing large single crystals of silicon carbide, have provided a better foundation for device research than has previously ever existed. The MOSFET devices described herein were formed using some of these successful new techniques.

Additionally, and as also referred to earlier, a novel and successful method of adding dopant ions to silicon carbide has also been recently developed. As therein, it has been

discovered that attempts to dope silicon carbide with ion implantation techniques at both room temperature (e.g. 298K) and low temperatures (e.g. 77K) have been unsuccessful, even following annealing. When, as discussed in the above application, the implantation is carried out at relatively high temperatures (e.g. 623K, 823K, 1023K), however, initial damage to the lattice is minimized and an annealing step at a more moderate temperature (1200°C) than is usually necessary sufficiently activates the dopant ions.

Figures 1-5 show some of the steps used in forming an n-channel inversion mode MOSFET according to the present invention and its resulting structure. Figure 5 is a cross-sectional view of the finished device which has a concentric ring structure which will be described further herein. In Figure 5, the source is indicated at 10 and is n-type. The drain is indicated at 11 and is also n-type, both formed by high temperature implantation in a p-type silicon carbide substrate 12. The gate is indicated at 13. The insulating layer of silicon dioxide is indicated at 14, the source contacts at 15, and the drain contacts at 16, with both source and drain contacts being formed of tantalum silicide ($TaSi_2$), which is a novel use of this material. As set forth earlier, the gate 13 has a gate contact 17 formed of polysilicon. In a preferred embodiment of the invention, the concentric gate ring had a 20 micrometer (um) wide connecting strip which extended to a 100 um X 100 um contact pad. The source contact 15 is an outer concentric semicircle that surrounds the gate ring 13 and the gate contact except for the gate's connection strip. The source ring also has a connecting strip to the 100 micrometer diameter contact pad 15.

Figure 1 illustrates some of the initial steps in forming a MOSFET according to the present invention. The silicon dioxide layer 14 is added through normal oxidation procedures to the p-type substrate of silicon carbide 12. A layer of phosphorous doped polysilicon 17 is deposited over the oxide layer 14. A photoresist material 20 is applied and patterned as shown. After the exposed polysilicon is etched away and the photoresist removed, the substrate 12 and oxide layer 14 have the appearance shown in Figure 2 in which the only remaining polysilicon is that which will form the gate contacts 17. Nitrogen is added by high temperature ion implantation (823K) through the oxide layer 14 into the p-type silicon carbide 12 to form n-type wells for the source 10 and the drain 11.

In Figure 3, additional photoresist 20 has been added and patterned in order to etch windows in the exposed oxide layer 14 above the source and drain. In Figure 4, tantalum silicide has been sputter deposited over the photoresist and over the exposed silicon carbide surface exposed by the openings in the oxide. When the photoresist 20 is lifted off, the only tantalum silicide which remains is that on the previously exposed silicon carbide surfaces adjacent the source and drain (Figure 5).

Figure 6 shows a depletion mode MOSFET formed according to the present invention. In Figure 6, a p-type alpha silicon carbide substrate is shown at 21 which carries a p-type beta silicon carbide layer 22 and an n-type beta silicon carbide layer 23. A more heavily n-doped source 24 and drain 25 are also illustrated along with the gate 26, Figure 6 being a cross-sectional view as discussed earlier. As in the inversion mode MOSFET described earlier, source and drain contacts 27 and

30 are formed of tantalum silicide while the gate contacts 31 are formed of polysilicon and are superimposed on the oxide layer 32.

In particular embodiments, the silicon carbide films were first polished using 0.1 um diamond paste, oxidized to remove polishing damage and etched in hydrofluoric acid (HF) to remove the oxide film. The gate oxide was subsequently grown, preceded by a three-step cleaning process using hot sulfuric acid (H_2SO_4) for five minutes, a one-to-one mixture of hot ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2) for five minutes, and HF for one minute, followed by a rinse with deionized water.

A 500 nm thick film of polysilicon was deposited on the prepared oxide via low pressure chemical vapor deposition at 893K which was degenerately doped by phosphorous (P) diffusion at 1173K for five minutes, then patterned as shown in the drawings to form the gate contacts.

The n-type doped source and drain areas were then formed by high temperature ion implantation of nitrogen through the oxide. The implantation was carried out at 773K, 70 keV at a dosage of 5.0×10^{14} cm^{-2}.

Figure 7 shows the drain current versus drain voltage characteristics measured at a temperature of 296K for a MOSFET formed according to the present invention in beta silicon carbide. The particular device upon which the measurements were made had a gate length of 7.2 um and a gate width of 390 um, with a source to drain contact distance of 24 um. As indicated in Figure 7, this device showed very stable drain current saturation out to a drain source voltage of 25 volts. This trend actually continued to a source drain voltage of 30 volts at which point the oxides began to break down.

Accordingly, this is the first time stable saturation has been reported for drain source voltages of greater than 5 volts for any field effect transistor formed in beta silicon carbide.

The threshold voltage was a gate voltage (V_G) of -12.9 V, as determined from a plot of the square root of the drain-source current versus V_G. The leakage current at a V_{DS} of 25 volts in this device was 3.75 microamps (uA) in the off-state (V_G = -15V). The transconductance of this device at room temperature with V_{DS} fixed at 20V was 5.32 mS/mm at V_G = 2.5V.

Figure 8 is another plot of drain current versus drain voltage for the same device, but with the device heated to 573K and allowed to stablize for 15 minutes at that temperature. Despite the increase in temperature, the drain current saturation was still very stable up to 25 volts. The leakage current at a drain source voltage of 25 volts and a gate voltage of -15 volts increased to 22 uA and the threshold voltage shifted negatively to V_G = -13.3V.

Figure 9 is yet another plot of drain current versus drain voltage for the same device, but measured at a temperature of 923K. The transconductance decreased with this further increase in temperature. The lower transconductance of the device as measured in Figure 9 at 923K is demonstrated by the lower current at a zero gate voltage as compared with Figure 7 and Figure 8. Although the transconductance at 923K became erratic above a gate voltage of 1 volt, it reached a maximum of about 4.8 mS/mm at a gate voltage of 8 volts and a drain source voltage of 20 volts. This decrease in transconductance at higher temperatures is due to increasing lattice scattering at the higher temperatures.

In Figure 9, the threshold voltage again shifted negatively to a gate voltage of -14.8 volts at 923K. The leakage current increased to 128 uA at a gate voltage of -15 volts and a drain source voltage of 25 volts. At 973K, the device showed similar current saturation but the gate oxide experienced breakdown. Therefore, the current was being injected at the gate and the device could not be cut off.

In the description and drawings, there have been set forth preferred and exemplary embodiments of the invention which have been set forth by way of example and not of limitation, the scope of the invention being that set forth in the following claims.

That which is claimed is:

1. The method comprising a metal-oxide-semiconductor field-effect transistor suitable for operation at temperatures of at least 650° centigrade and high radiation densities, the method comprising:

a) oxidizing a silicon carbide substrate having a first conductivity type to form a silicon dioxide surface layer;

b) selectively applying gate contact material to the silicon dioxide surface layer;

c) forming a doped source and a doped drain of a desired conductivity type by high temperature implantation of doping ions; and

d) applying source and drain contacts.

2. A method according to Claim 1 further comprising preparing the surface for oxidation by:

polishing the silicon carbide substrate;

oxidizing the portion of the substrate damaged by the polishing; and

removing the oxidized damaged portion prior to oxidizing the resulting substrate surface to form the silicon dioxide surface layer.

3. A method according to Claim 1 wherein the step of applying gate contact material comprises adding a conductive polysilicon gate contact material to the silicon dioxide surface layer.

4. A method according to Claim 1 wherein the step of applying source and drain contacts comprises applying tantalum silicide source and drain contacts.

5. A method according to Claim 1 wherein the step of forming a doped source and a doped drain comprises:

directing an ion beam of dopant ions onto the silicon carbide substrate in which the silicon carbide substrate is maintained at a temperature of between about 600K and about 1100K.

6. A method of forming an inversion mode metal-insulator-semiconductor field-effect transistor suitable for operation at temperatures of at least 650° centigrade and high radiation densities, the method comprising:

forming a doped source and a doped drain having a first conductivity type in a doped portion of silicon carbide having an opposite conductivity type by high temperature implantation of source and drain with doping ions into the silicon carbide portion.

7. A method according to Claim 6 wherein the step of forming a doped source and a doped drain comprises forming an n-doped source and an n-doped drain in a p-doped portion of silicon carbide.

8. A method according to Claim 6 wherein the step of forming a doped source and a doped drain comprises forming a p-doped source and a p-doped drain in an n-doped portion of silicon carbide.

9. A method of forming a depletion mode metal-insulator-semiconductor field-effect transistor suitable for operation at temperatures of at least 650° centigrade and high radiation densities, the method comprising:

forming a doped source and a doped drain in a silicon carbide semiconductor portion having

the same conductivity type as the doped source and doped drain by high temperature implantation of the source and drain portions with doping ions into the silicon carbide portion.

10. A method according to Claim 9 wherein the step of forming a doped source and a doped drain comprises forming a more heavily n-type doped source and a more heavily doped n-type drain in an n-type silicon carbide semiconductor portion.

11. A method according to Claim 9 wherein the step of forming a doped source and a doped drain comprises forming a more heavily p-type doped source and a more heavily doped p-type drain in a p-type silicon carbide semiconductor portion.

12. An inversion mode metal-oxide-semiconductor field-effect transistor comprising:

a p-type silicon carbide substrate;

a source formed of n-type silicon carbide;

a drain formed of n-type silicon carbide;

a p-type silicon carbide gate; and

source and drain contacts formed of tantalum silicide.

13. An inversion mode metal-oxide-semiconductor field-effect transistor according to Claim 12 further comprising gate contacts formed of conductive polycrystalline silicon.

14. An inversion mode metal-oxide-semiconductor field-effect transistor according to Claim 12 wherein said drain is surrounded by said gate and said gate is surrounded by said source.

15. An inversion mode metal-oxide-semiconductor field-effect transistor according to Claim 14 wherein said source and said gate form concentric circles surrounding said drain.

16. A depletion mode metal-oxide-semiconductor field-effect transistor comprising:

a p-type alpha silicon carbide substrate;

a p-type beta silicon carbide layer upon the p-type alpha silicon carbide layer for electronically bordering the depletion region;

an active layer of n-type beta silicon carbide upon the p-type beta silicon carbide layer;

a more heavily doped n-type source region in the active layer of n-type beta silicon carbide;

a more heavily doped n-type drain region in the active layer of n-type beta silicon carbide; and

a gate region in the active layer of n-type beta silicon carbide and defined by the portion of the active layer which is positioned between the more heavily doped source and drain regions.

17. A depletion mode metal-oxide-semiconductor field-effect transistor according to Claim 16 further comprising gate contacts formed of conductive polysilicon.

18. A depletion mode metal-oxide-semiconductor field-effect transistor according to Claim 16 wherein said drain region is surrounded by said gate region and said gate region is surrounded by said source region.

19. A depletion mode metal-oxide-semiconductor field-effect transistor according to Claim 18 wherein said source region and said gate region form concentric circles surrounding said drain.

20. A depletion mode metal-oxide-semiconductor field-effect transistor comprising:

an n-type beta silicon carbide gate and depletion region;

an n-type beta silicon carbide source;

an n-type beta silicon carbide drain; and

said transistor having the following operational characteristics at temperatures of about 296K:

stable drain-current saturation at drain-source voltages of at least 25 volts and a gate voltage of -15 volts;

a leakage current of less than 4 microamps at drain source voltages of up to 25 volts; and

a transconductance of at least 5.32 mS/mm at a gate voltage of 2.5 volts and a drain-source voltage of 20 volts.

21. A depletion mode metal-oxide-semiconductor field-effect transistor comprising:

an n-type beta silicon carbide gate and depletion region;

an n-type beta silicon carbide source;

an n-type beta silicon carbide drain; and

said transistor having the following operational characteristics at temperatures of about 573K:

stable drain-current saturation at drain-source voltages of at least 25 volts and a gate voltage of -15 volts;

a leakage current of less than 23 microamps at drain source voltages of up to 25 volts; and

a transconductance of at least 6.00 mS/mm at a gate voltage of 5.5 volts and a drain-source voltage of 20 volts.

22. A depletion mode metal-oxide-semiconductor field-effect transistor comprising:

an n-type beta silicon carbide gate and depletion region;

an n-type beta silicon carbide source;

an n-type beta silicon carbide drain; and

said transistor having the following operational characteristics at temperatures of about 923K:

stable drain-current saturation at drain-source voltages of at least 25 volts and a gate voltage of -15 volts;

a leakage current of less than 130 microamps at drain source voltages of up to 25 volts; and

a transconductance of at least 4.8 mS/mm at a gate voltage of 8 volts and a drain-source voltage of 20 volts.

23. A method of forming a metal-oxide-semiconductor field-effect transistor suitable for operation at temperatures of at least 650° centigrade and high radiation densities, the method comprising:

a) forming an insulating surface layer upon a silicon carbide substrate;

b) selectively applying gate contact material to the insulating surface layer;

c) forming a doped source and a doped drain of a desired conductivity type in the silicon

carbide substrate by high temperature implantation of doping ions; and

d) applying source and drain contacts.

24. A method according to Claim 23 wherein the step of forming an insulating surface comprises forming a layer of silicon nitride upon the silicon carbide substrate.

25. A method according to Claim 23 wherein the step of forming an insulating layer comprises forming a silicon dioxide surface layer upon the silicon carbide substrate.

Fig. 1.

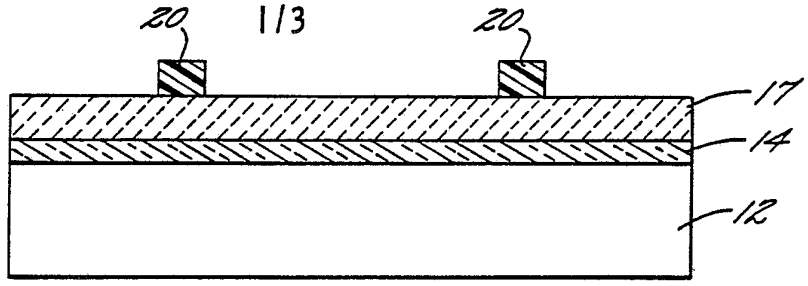


Fig. 2.

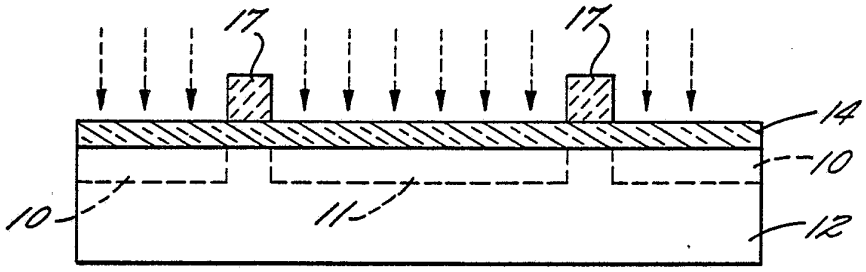


Fig. 3.

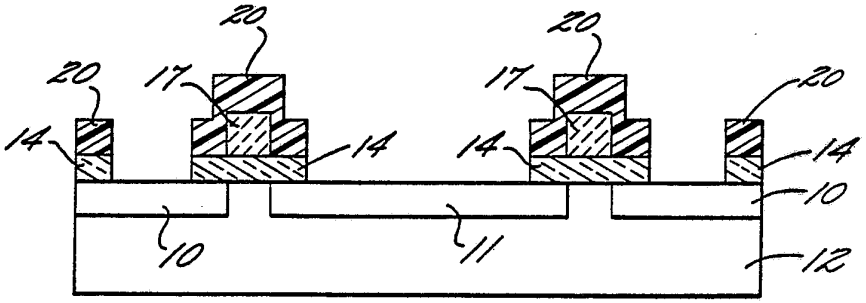


Fig. 4.

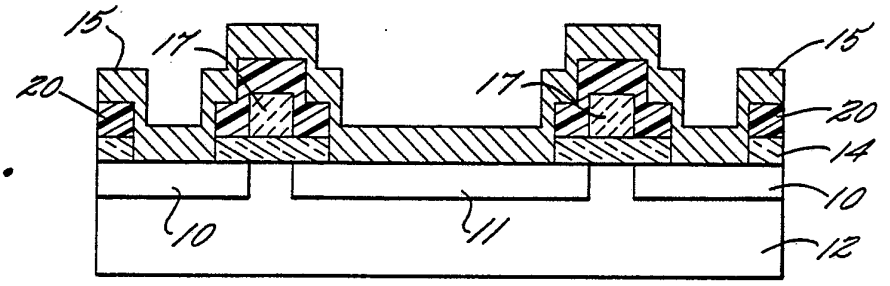
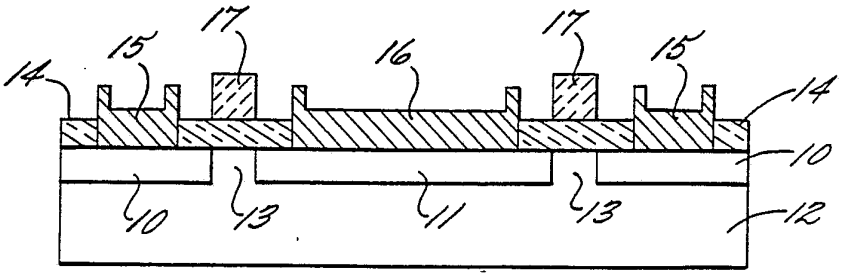


Fig. 5.



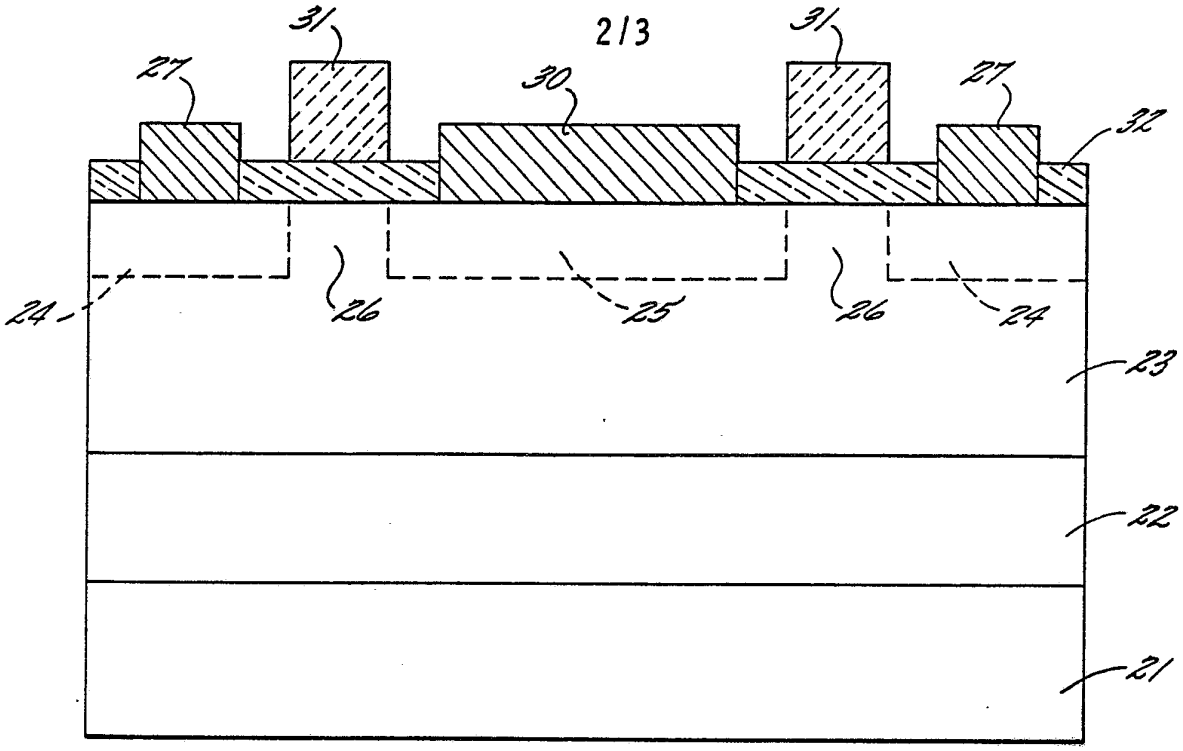

31
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Fig. 6.

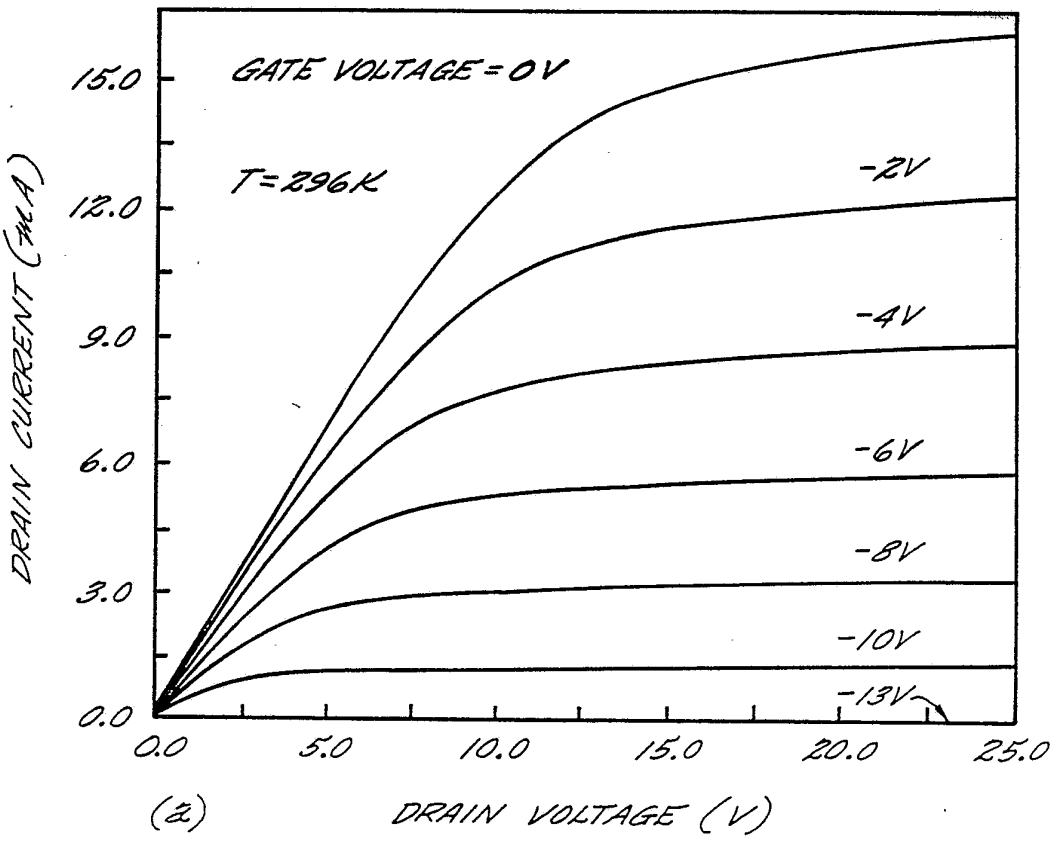
GATE VOLTAGE = 0V
T = 296K
-2V
-4V
-6V
-8V
-10V
-13V
15.0
12.0
9.0
6.0
3.0
0.0
0.0
5.0
10.0
15.0
20.0
25.0
DRAIN CURRENT (mA)
(2)
DRAIN VOLTAGE (V)

Fig. 7.

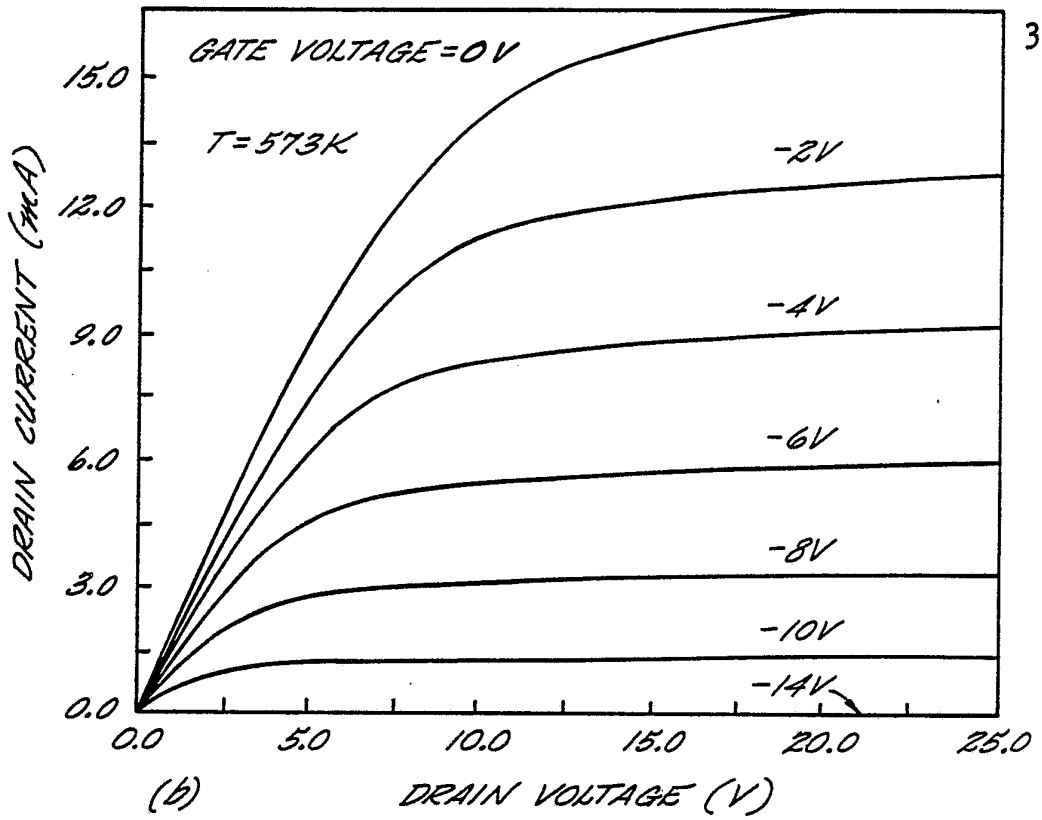

Fig. 8.

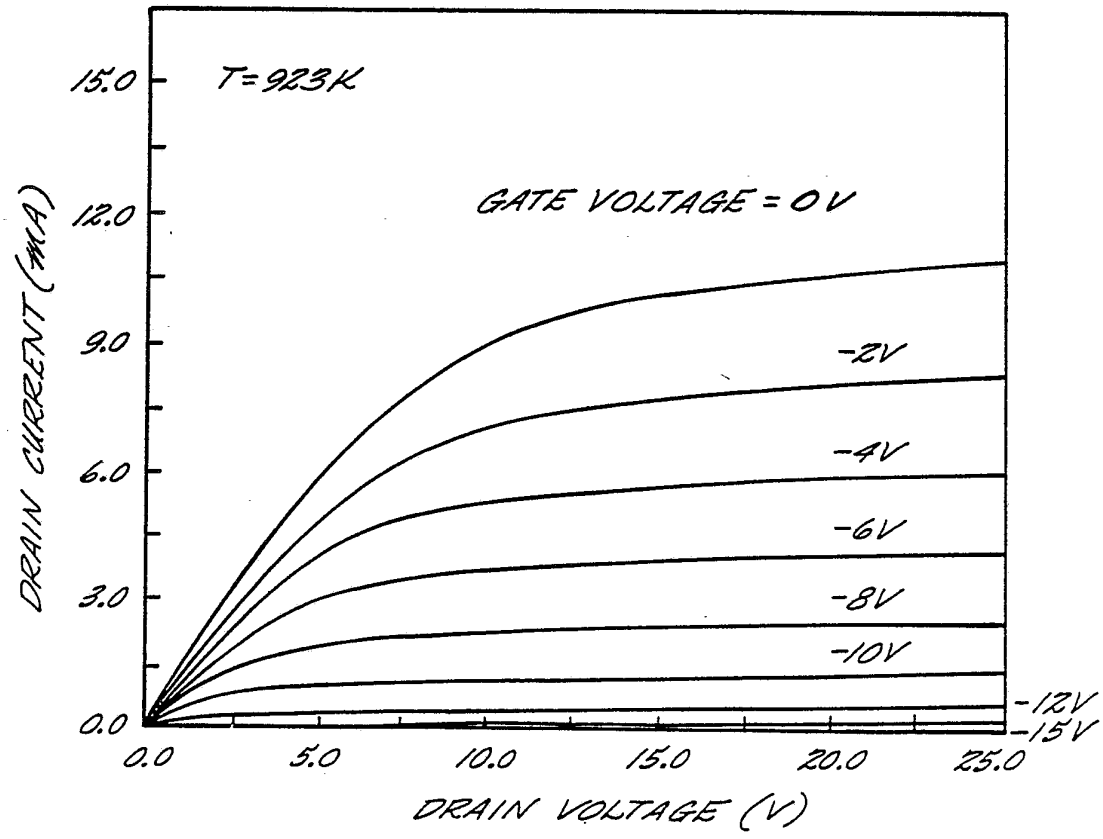

Fig. 9.

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US 88/03793

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC(4) H01L: 21/265, 29/78, 29/167
U.S. CL. 357/23.12, 63 59G, 61, 23.2, 23.1; 437/41, 100, 946

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
U.S.	357/23.12, 63, 59G, 61, 23.1, 23.2; 437/41, 100, 946

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
A	U.S., A, 2,918,396 (HALL) 22 December 1959	1-25
X	U.S., A 3,254,280 (WALLACE) 31 May 1966, see Fig.'s 1 to 6 and columns 1 to 4.	1,2,5-11,23
Y	U.S., A, 3,577,285 (RUTZ)04 May 1971, see columns 1 to 3.	1-11&23-25
Y	U.S., A, 3,662,458 (FORMIGONI ET AL) 16 May 1972, see Abstract.	4
Y	U.S., A, 4,028,149 (DEINES ET AL.)07 June 1977, see Fig.'s 1 to 15 and columns 2 to 4.	1-11&23-25
A	U.S., A, 4,032,961 (BALIGA ET AL.) 28 June 1977	1-25
A	U.S., A, 4,068,134 (TOBEY, JR ET AL.) 10 January 1978	1-25
A	U.S., A, 4,531,142 (WEYRICH ET AL.) 23 July 1985	1-25
Y	U.S., A, 4,582,561 (IOKU) 15 April 1986, see columns 1-3.	1-11&23-25

(continued on extra sheet)

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
12 January 1989	08 MAR 1989
International Searching Authority	**Signature of Authorized Officer**
ISA/US	William A. Mintel

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
Y, P	US, A, 4,757,028 (KONDOH ET AL.) 12 July 1988, see Fig.'s 1 to 6 and columns 1 to 3.	2,3,24,25
Y	JP.,A 56-7479 (KURAMOTO) 26 January 1981, see Fig. 5.	14-15
Y	IBM Technical Disclosure Bulletin, Volume 21, No. 9, issued 1979 February (Armonk, New York), V.L. Rideout, "Polysilicon-Gate Field-Effect Transistors with Self-Registering Metal Contacts to both Polysilicon and Diffused Silicon Regions", see pages 3833 to 3835.	13
Y	IBM Technical Disclosure Bulletin, Volume 28, No. 7, issued 1985 December (Armonk, New York), No Author, "Dual Silicides for Gate Channel Definition", see pages 2901 to 2902.	12-22
Y	IBM Technical Disclosure Bulletin, Volume 27, No. 10A, issued 1985 March (Armonk, New York), No Author, "Selective Oxidation of Titanium While Forming Titanium Silicide At Polysilicon and Diffusions", see pages 5870 to 5875.	4,12-22
Y	IEEE Electron Device Letters, Volume EDL-7, No. 7, 1986 July, Y Kondo, "Experimental 3C-SiC MOSFET", see pages 404 to 405.	16,20-22
A	IEEE Electon Device Letters, Volume EDL-8, No. 2, 1987 February, K. Furukawa, "Insulated-Gate and Junction-Gate FET's of CVD-Grown Beta-SiC".	1-25
Y	Japanese Journal of Applied Physics, Volume 23, issued 1984, K. Shibahara, "Inversion-Type MOS Field Effect Transistors using CVD grown cubic SiC on Si", see pages L862 to L867.	12-22
Y	Radiation Effects, Volume 6, issued 1970, O.J. Marsh, "Ion-Implanted Junctions and Conducting Layers in SiC", see Abstract.	16,20-22