(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
8 February 2007 (08.02.2007)

PCT

(10) International Publication Number
WO 2007/015930 A1

(51) International Patent Classification:
H01L 21/336 (2006.01)

(21) International Application Number:
PCT/US2006/028171

(22) International Filing Date: 20 July 2006 (20.07.2006)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
11/191,684 27 July 2005 (27.07.2005) US

(71) Applicant *(for all designated States except US)*: **ADVANCED MICRO DEVICES, INC.** [US/US]; ONE AMD PLACE, MAIL STOP 68, P.O. Box 3453, Sunnyvale, CA 94088-3453 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **PEIDOUS, Igor** [RU/US]; 1j Mountain View Knolls, Fishkill, XX 12524 (US). **SULTAN, Akif** [IN/US]; 6504 Skinner Cove, Austin, TX 78759 (US). **PELELLA, Mario, M.** [US/US]; 1876 Miramonte Avenue, Mountain View, CA 94040 (US).

(74) Agent: **DRAKE, Paul, S.**; ADVANCED MICRO DEVICES, INC., 5204 EAST BEN WHITE BOULEVARD, Mail Stop 562, Austin, TX 78741 (US).

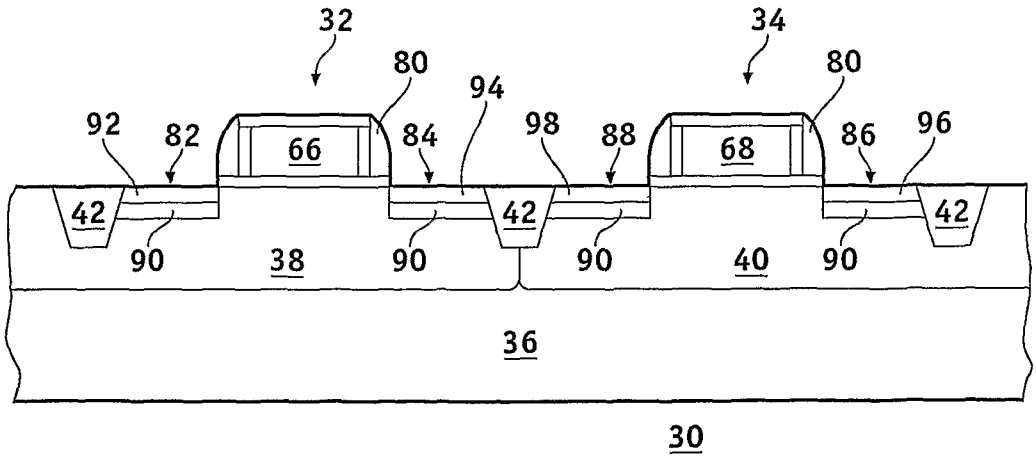
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) **Title:** METHODS FOR FABRICATING A STRESSED MOS DEVICE



(57) **Abstract:** Methods are provided for fabricating a stressed MOS device [30]. The method comprises the steps of forming a plurality of parallel MOS transistors in and on a semiconductor substrate [36]. The parallel MOS transistors having a common source [92] region, a common drain [94] region, and a common gate electrode [66]. A first trench [82] is etched into the substrate in the common source [92] region and a second trench [84] is etched into the substrate in the common drain [94] region. A stress inducing semiconductor material [90] that has a crystal lattice mismatched with the semiconductor substrate is selectively grown in the first [82] and second [84] trenches. The growth of the stress inducing material [90] creates both compressive longitudinal and tensile transverse stresses in the MOS device channel [50] that enhance the drive current of P-channel MOS transistors. The decrease in drive current of N-channel MOS transistors caused by the compressive stress component is offset by the tensile stress component.

WO 2007/015930 A1

METHODS FOR FABRICATING A STRESSED MOS DEVICE

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention generally relates to methods for fabricating semiconductor devices, and more particularly relates to methods for fabricating stressed MOS devices.

BACKGROUND OF THE INVENTION

[0002] The majority of present day integrated circuits (ICs) are implemented by using a plurality of interconnected field effect transistors (FETs), also called metal oxide semiconductor field effect transistors (MOSFETs), or simply MOS transistors. An MOS transistor includes a gate electrode as a control electrode and spaced apart source and drain electrodes between which a current can flow. A control voltage applied to the gate electrode controls the flow of current through a channel between the source and drain electrodes.

[0003] MOS transistors, in contrast to bipolar transistor, are majority carrier devices. The gain of an MOS transistor, usually defined by the transconductance (g_m), is proportional to the mobility of the majority carrier in the transistor channel. The current carrying capability of an MOS transistor is proportional to the mobility times the width of the channel divided by the length of the channel (g_mW/l). MOS transistors are usually fabricated on silicon substrates with the crystallographic surface orientation (100), which is conventional for silicon technology. For this and many other orientations, the mobility of holes, the majority carrier in a P-channel MOS transistor, can be increased by applying a compressive longitudinal stress to the channel. Such a compressive longitudinal stress, however, decreases the mobility of electrons, the majority carriers in N-channel MOS transistors. A compressive longitudinal stress can be applied to the channel of an MOS transistor by embedding an expanding material such as pseudomorphic SiGe in the silicon substrate at the ends of the transistor channel [For example, see IEEE Electron Device Letters v. 25, No 4, p. 191, 2004]. A SiGe crystal has greater lattice constant than the lattice constant of a Si crystal, and consequently the presence of embedded SiGe causes a deformation of the Si matrix. Unfortunately, present techniques for increasing carrier mobility by embedding an expanding material cannot be applied in the same way to both P-channel and N-channel MOS transistors because the compressive longitudinal stress that improves hole mobility is detrimental to electron mobility. Also, the present techniques exploit only phenomenon of carrier mobility enhancement by the longitudinal stress, neglecting the transverse stress that also influences the mobility.

[0004] Accordingly, it is desirable to provide methods for fabricating stressed MOS devices that utilize both longitudinal and transverse stresses. In addition, it is desirable to provide methods for fabricating stressed MOS devices that improve the carrier mobility of both N-channel and P-channel devices. Furthermore, other desirable features and characteristics of the present invention will become apparent from the subsequent detailed description and the appended claims, taken in conjunction with the accompanying drawings and the foregoing technical field and background.

BRIEF SUMMARY O F THE INVENTION

[0005] Methods are provided for fabricating a stressed MOS device in and on a semiconductor substrate. The method comprises the steps of forming a plurality of parallel MOS transistors in and on the semiconductor substrate, the plurality of parallel MOS transistors having combined source region, combined drain region, and a common gate electrode. A first recess is etched into the semiconductor substrate in the combined source region and a second recess is etched into the semiconductor substrate in the combined drain region. A stress inducing semiconductor material having a lattice constant greater than the lattice constant of the semiconductor substrate is selectively grown in the first trench and the second trench.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] The present invention will hereinafter be described in conjunction with the following drawing figures, wherein like numerals denote like elements, and wherein

[0007] FIGS. 1, and 4-8 illustrate, in cross section, a stressed MOS device and methods for its fabrication in accordance with various embodiments of the invention; and

[0008] FIGS. 2 and 3 illustrate schematically, in plan view, a portion of a stressed MOS device at a stage of its fabrication.

DETAILED DESCRIPTION OF THE INVENTION

[0009] The following detailed description is merely exemplary in nature and is not intended to limit the invention or the application and uses of the invention. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, brief summary or the following detailed description.

[0010] In a typical complementary MOS (CMOS) integrated circuits, high performance P-channel MOS transistors N-channel MOS transistors each have a relatively wide channel width to provide sufficient drive current. The channel width of such transistors is on the order of 1 μm while the channel length and the depth of the source and drain regions are less than about 0.1 μm. If stress inducing material having a thickness of the same order of magnitude as the source and drain regions is embedded at the ends of the channel, such stress inducing materials can apply a longitudinal stress along the channel, but are relatively ineffective in applying a transverse stress to the channel. Notable transverse stresses are induced only at the edges of the channel, and such stresses propagate within the channel to a distance only of the same order of magnitude as the thickness of the stress inducing material. As a result, high transverse stresses are induced only in a small portion of the channel and have little effect on device performance. In accordance with an embodiment of the invention, this problem is overcome by replacing wide channel MOS transistors with a plurality of narrow channel MOS transistors coupled in parallel. A narrow channel transistor having a stress inducing material embedded at the ends of the channel experiences both a compressive longitudinal stress and a tensile transverse stress across the whole channel region. The compressive longitudinal stress increases the hole mobility and decreases the electron

mobility in the channel while the tensile transverse stress increases both the hole mobility and the electron mobility in the channel.

[0011] FIGS. 1-8 illustrate a stressed MOS device 30 and method steps for manufacturing such an MOS device in accordance with various embodiments of the invention. In this illustrative embodiment the only portion of stressed MOS device 30 that is illustrated is a single P-channel MOS transistor 32 and a single N-channel MOS transistor 34. An integrated circuit formed from stressed MOS devices such as device 30 can include a large number of such transistors. Although complementary MOS transistors are illustrated, the invention is also applicable to devices that include only P-channel MOS transistors.

[0012] Various steps in the manufacture of MOS transistors are well known and so, in the interest of brevity, many conventional steps will only be mentioned briefly herein or will be omitted entirely without providing the well known process details. Although the term "MOS device" properly refers to a device having a metal gate electrode and an oxide gate insulator, that term will be used throughout to refer to any semiconductor device that includes a conductive gate electrode (whether metal or other conductive material) that is positioned over a gate insulator (whether oxide or other insulator) which, in turn, is positioned over a semiconductor substrate.

[0013] As illustrated in FIG. 1, the fabrication of a stressed MOS device 30 in accordance with an embodiment of the invention begins with providing a semiconductor substrate 36. The semiconductor substrate is preferably a monocrystalline silicon substrate wherein the term "silicon substrate" is used herein to encompass the relatively pure silicon materials typically used in the semiconductor industry. Silicon substrate 36 may be a bulk silicon wafer or a thin layer of silicon on an insulating layer (commonly know as silicon-on-insulator or SOI) that, in turn, is supported by a silicon carrier wafer, but is here illustrated, without limitation, as a bulk silicon wafer. Preferably the silicon wafer has either a (100) or (110) orientation. One portion 38 of the silicon wafer is doped with N-type impurity dopants (an N-well) and another portion 40 is doped with P-type impurity dopants (a P-well). The N-well and P-well can be doped to the appropriate conductivity, for example, by ion implantation. Shallow trench isolation (STI) 42 is formed to electrically isolate between the N-well and P-well and to isolate around individual devices that must be electrically isolated. The STI defines an active area 44 for the formation of P-channel MOS transistor 32 and an active area 46 for the formation of N-channel MOS transistor 34. As is well known, there are many processes that can be used to form the STI, so the process need not be described here in detail. In general, STI includes a shallow trench that is etched into the surface of the semiconductor substrate and that is subsequently filled with an insulating material. After the trench is filled with the insulating material, the surface is usually planarized, for example by chemical mechanical planarization (CMP). The two wells and the STI are illustrated in cross section in FIG. 1 and in top view in FIG. 2.

[0014] In accordance with an embodiment of the invention P-channel transistor 32 and N-channel transistor 34 are both wide channel MOS transistors and are both implemented as a plurality of narrow channel MOS transistors coupled in parallel. As will be explained more fully below, P-channel MOS transistor 32 and N-channel MOS transistor 34 each includes a common source, a common drain, a common gate, and a plurality of parallel channels extending from the source to the drain beneath the common gate. As illustrated in FIG. 3, the plurality of parallel channels 50 of P-channel MOS transistor 32 are defined by a plurality of STI regions 52 that are formed in the surface of active area 44. As also illustrated in FIG. 3, the plurality of parallel channels 54 of

N-channel MOS transistor 34 are defined by a plurality of STI regions 56 that are formed in the surface of active area 46. The STI regions can be formed at the same time as STI region 42 or can be formed separately. FIG. 3, like FIG. 2, illustrates stressed MOS device 30 in top view. The plurality of parallel channels preferably each have a width of about 0.1μm. Although only three parallel channels are shown for each of the transistors, the total number of parallel channels for each of P-channel MOS transistor 32 and for N-channel transistor 34 are selected to provide the equivalent channel width of the single wide channel transistor each is designed to replace. Preferably the channels are oriented along the <110> crystalline direction.

[0015] A layer of gate insulator 60 is formed on the surface of silicon substrate 36, including on the surface of active areas 44 and 46 as illustrated in FIG. 4. The gate insulator may be a thermally grown silicon dioxide layer formed by heating the silicon substrate in an oxidizing ambient, or may be a deposited insulator such as a silicon oxide, silicon nitride, a high dielectric constant insulator such as HfSiO, or the like. Deposited insulators can be deposited by chemical vapor deposition (CVD), low pressure chemical vapor deposition (LPCVD), or plasma enhanced chemical vapor deposition (PECVD). In the illustrated embodiment the layer of gate insulator is a deposited insulator that deposits equally on the STI and on the silicon substrate. The gate insulator material is typically 1-10 nanometers (nm) in thickness. In accordance with one embodiment of the invention a layer of polycrystalline silicon 62 is deposited onto the layer of gate insulator. The layer of polycrystalline silicon is preferably deposited as undoped polycrystalline silicon and is subsequently impurity doped by ion implantation. A layer 64 of hard mask material such as silicon oxide, silicon nitride, or silicon oxynitride can be deposited onto the surface of the polycrystalline silicon. The polycrystalline material can be deposited to a thickness of about 100 nm by LPCVD by the hydrogen reduction of silane. The hard mask material can be deposited to a thickness of about 50 nm, also by LPCVD.

[0016] Hard mask layer 64 and underlying layer of polycrystalline silicon 62 are photolithographically patterned to form a P-channel MOS transistor gate electrode 66 overlying active area 44 and an N-channel MOS transistor gate electrode 68 overlying active area 46 as illustrated in FIG. 5. Gate electrode 66 overlies the plurality of parallel channels 50 of P-channel MOS transistor 32 and gate electrode 68 overlies the plurality of parallel channels 54 of N-channel MOS transistor 34. Gate electrodes 66 and 68 are also illustrated by dashed lines in FIG. 3. The polycrystalline silicon can be etched in the desired pattern by, for example, plasma etching in a Cl or HBr/O_2 chemistry and the hard mask can be etched, for example, by plasma etching in a CHF_3, CF_4, or SF_6 chemistry. Following the patterning of the gate electrode, in accordance with one embodiment of the invention, a thin layer 70 of silicon oxide is thermally grown on the opposing sidewalls 72 of gate electrode 66 and a thin layer 74 of silicon oxide is thermally grown on the opposing sidewalls 76 of gate electrode 68 by heating the polycrystalline silicon in an oxidizing ambient. Layers 70 and 74 can be grown to a thickness of about 2-5 nm. Gate electrodes 66 and 68 and layers 70 and 74 can be used as an ion implantation mask to form source and drain extensions (not illustrated) on either or both of the MOS transistors. The possible need for and method of forming multiple source and drain regions are well known, but are not germane to this invention and hence need not be explained herein.

[0017] In accordance with one embodiment of the invention, as illustrated in FIG. 6, sidewall spacers 80 are formed on the opposing sidewalls 72 and 76 of gate electrodes 66 and 68, respectively. The sidewall spacers can be formed of silicon nitride, silicon oxide, or the like by depositing a layer of the spacer material over the gate

electrodes and subsequently anisotropically etching the layer, for example by reactive ion etching. Sidewall spacers 80, gate electrodes 66 and 68, the hard mask on the top of the gate electrodes, and STI 42 are used as an etch mask to etch trenches 82 and 84 in the silicon substrate in spaced apart self alignment with P-channel gate electrode 66 and to etch trenches 86 and 88 in spaced apart self alignment with N-channel gate electrode 68. The trenches intersect the ends of the narrow parallel channels 50 and 54. The trenches can be etched, for example, by plasma etching using HBr/O_2 and Cl chemistry. Preferably each of the trenches has a depth that is the same order of magnitude as the width of the narrow parallel channels 50 and 54.

[0018] As illustrated in FIG. 7, the trenches are filled with a layer of stress inducing material 90. The stress inducing material can be any pseudomorphic material that can be grown on the silicon substrate with a different lattice constant than the lattice constant of silicon. The difference in lattice constant of the two juxtaposed materials creates a stress in the host material. The stress inducing material can be, for example, monocrystalline silicon germanium (SiGe) having about 10-30 atomic percent germanium. Preferably the stress inducing material is epitaxially grown by a selective growth process to a thickness that is the same order of magnitude as the width of the narrow parallel channels 50 and 54. Methods for epitaxially growing these materials on a silicon host in a selective manner are will known and need not be described herein. In the case of SiGe, for example, the SiGe has a greater lattice constant than silicon and a compressive longitudinal stress in the transistor channel. By itself, the compressive longitudinal stress increases the mobility of holes in the channel and hence improves the performance of a P-channel MOS transistor. The compressive longitudinal stress, however, decreases the mobility of electrons in the channel of an N-channel MOS transistor. By decreasing the width of the channel of both P-channel MOS transistor 32 and N-channel transistor 34, in accordance with an embodiment of the invention, a transverse tensile stress is applied to the channel of the transistors, and such a stress increases the mobility of both holes and electrons. For the P-channel MOS transistor the tensile transverse stress increases the mobility of the majority carrier holes in addition to the increased hole mobility caused by the compressive longitudinal stresses. For the N-channel MOS transistor the increase in electron mobility caused by the transverse tensile stress helps to offset the decrease in electron mobility caused by the compressive longitudinal stress. Because of the improvement in electron mobility caused by the tensile stress, which, in turn, is caused by the embedded stress inducing material, the same processing can be applied to both the P-channel transistor and to the N-channel transistor. Because the same processing can be applied to both transistors, the N-channel transistor does not have to be masked during the etching and selective growth steps and the total process is therefore made simpler, more reliable, and hence less expensive.

[0019] Source and drain regions of the MOS transistors can be partially or completely in-situ doped with conductivity determining impurities during the process of selective epitaxial growth. Otherwise, following the growth of the stress inducing material in trenches 82, 84, 86, and 88, P-type conductivity determining ions are implanted into the stress inducing material in trenches 82 and 84 to form a source region 92 and a drain region 94 of P-channel MOS transistor 32 as illustrated in FIG. 8. Similarly, N- type conductivity determining ions are implanted into the stress inducing material in trenches 86 and 88 to form a source region 96 and a drain region 98 of N-channel MOS transistor 34.

[0020] Stressed MOS device 30 can be completed by well known steps (not illustrated) such as depositing a layer of dielectric material, etching opening through the dielectric material to expose portions of the source and

drain regions, and forming metallization that extends through the openings to electrically contact the source and drain regions. Further layers of interlayer dielectric material, additional layers of interconnect metallization, and the like may also be applied and patterned to achiever the proper circuit function of the integrated circuit being implemented.

[0021] While at least one exemplary embodiment has been presented in the foregoing detailed description, it should be appreciated that a vast number of variations exist. It should also be appreciated that the exemplary embodiment or exemplary embodiments are only examples, and are not intended to limit the scope, applicability, or configuration of the invention in any way. Rather, the foregoing detailed description will provide those skilled in the art with a convenient road map for implementing the exemplary embodiment or exemplary embodiments. It should be understood that various changes can be made in the function and arrangement of elements without departing from the scope of the invention as set forth in the appended claims and the legal equivalents thereof.

CLAIMS

What is claimed is:

1. A method for fabricating a stressed MOS device [30] in and on a silicon substrate [36] comprising the steps of:

forming a gate insulator layer [60] on the silicon substrate [36];

depositing a layer of gate electrode material [62] overlying the gate insulator layer [60] and patterning the layer of gate electrode [66] material to form a gate electrode having opposing side surfaces [72];

etching a first trench [82] and a second trench [84] in the silicon substrate, the first trench and the second trench spaced apart and self aligned to the opposing sides surfaces of the gate electrode;

selectively growing a layer of stress inducing material [90] in the first trench [82] and in the second trench [84];

ion implanting conductivity determining impurity ions into the stress inducing material [90] in the first trench [82] to form a source region [92] and into the stress inducing material [90] in the second trench [84] to form a drain region [94]; and

defining a plurality of parallel channel regions [50] in the silicon substrate extending between the source region [92] and the drain region [94] beneath the gate electrode [66].

2. The method of claim 1 wherein the step of selectively growing comprises the step of epitaxially growing a layer comprising a semiconductor material having a lattice constant greater than the lattice constant of silicon.

3. The method of claim 1 wherein the step of defining a plurality of parallel channel regions [50] comprises the step of forming a plurality of spaced apart shallow trench isolation regions [52] extending from the source region [92] to the drain region [94].

4. A method for fabricating a stressed MOS device [30] in and on a silicon substrate [36] comprising the steps of:

forming an isolation structure [42] in the silicon substrate to define a first region [44] and a second region [46];

forming a first plurality of parallel isolation structures [52] in the silicon substrate in the first region [44] to define a plurality of P-channels [50];

forming a second plurality of parallel isolation structures [56] in the silicon substrate in the second region [46] to define a plurality of N-channels [54];

forming a first gate electrode [66] having first opposing sides [72] overlying the plurality of P-channels and a second gate electrode [68] having second opposing sides [96] overlying the second plurality of N-channels;

etching first [82] and second [84] trenches into the silicon surface spaced apart from the first opposing sides [72] of the first gate electrode [66], the first and second trenches intersecting the plurality of P-channels [50];

etching third [86] and fourth [88] trenches into the silicon surface spaced apart from the second opposing sides [76] of the second gate electrode [68], the third and fourth trenches intersecting the plurality of N-channels [54];

selectively growing a stress inducing material [90] in the first [82] and second [84] trenches and in the third [86] and fourth [88] trenches;

ion implanting P-type conductivity determining impurity ions into the stress inducing material [90] in the first trench [82] to form a P-type source region [92] and into the stress inducing material [90] in the second trench [84] to form a P-type drain region [94]; and

ion implanting N-type conductivity determining impurity ions into the stress inducing material [90] in the third trench [86] to form an N-type source region [96] and into the stress inducing material in the fourth trench [88] to form an N-type drain region [98].

5. The method of claim 4 wherein the step of selectively growing a stress inducing material [90] comprises the step of epitaxially growing a SiGe layer.

6. A method for fabricating a stressed MOS device [30] in and on a semiconductor substrate [36] comprising the steps of:

forming a plurality of parallel MOS transistors in and on the semiconductor substrate, the plurality of parallel MOS transistors having a common source [92] region, a common drain region [94], and a common gate electrode [66];

etching a first trench [82] in the semiconductor substrate in the common source region [92] and a second trench [84] in the common drain region [94]; and

selectively growing a stress inducing semiconductor material [90] lattice mismatched with the semiconductor substrate in the first trench and in the second trench.

7. The method of claim 6 wherein the step of forming a plurality of parallel MOS transistors comprises the step of forming a plurality of parallel MOS transistor each having a channel [50] of predetermined width.

8. The method of claim 7 wherein the step of selectively growing comprises the step of selectively growing a layer of semiconductor material [90] having a thickness of the same order of magnitude as the predetermined width.

9. The method of claim 6 wherein the step of selectively growing comprises the step of epitaxially growing a layer comprising SiGe.

10. The method of claim 6 wherein the step of forming a plurality of parallel MOS transistors comprises the steps of:

forming a shallow trench isolation structure [42] to define an active area [44]; and

dividing the active area [44] into a common source region [82], a common drain region [84], and a plurality of parallel channel regions [50].

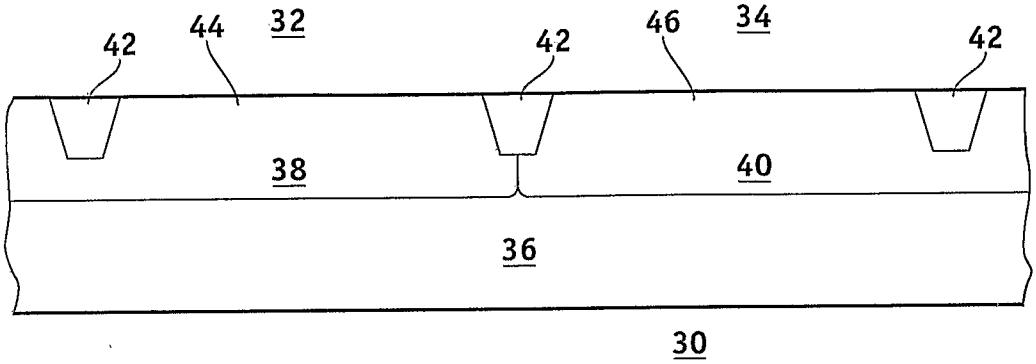


FIG. 1

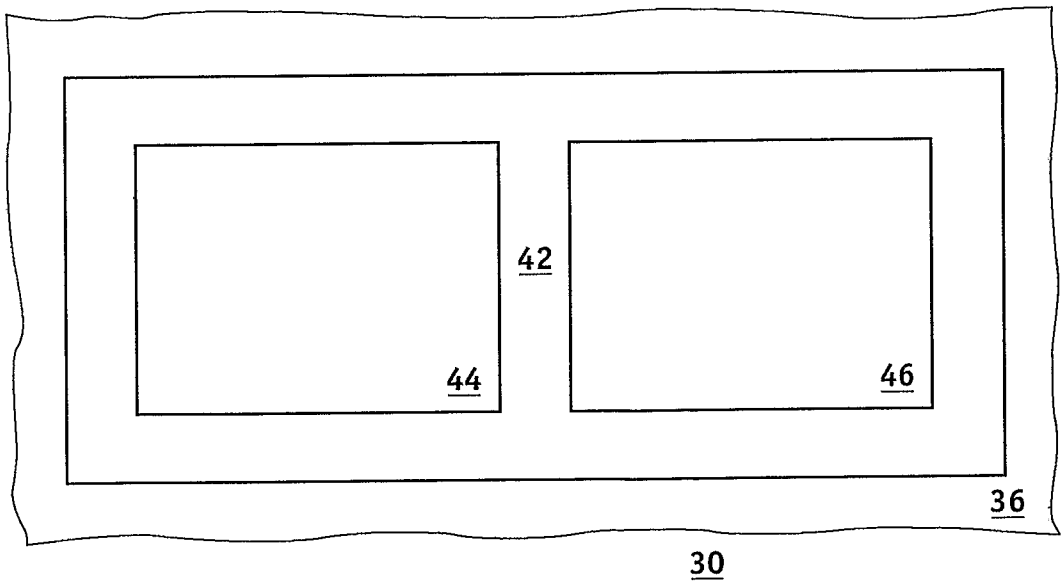


FIG. 2

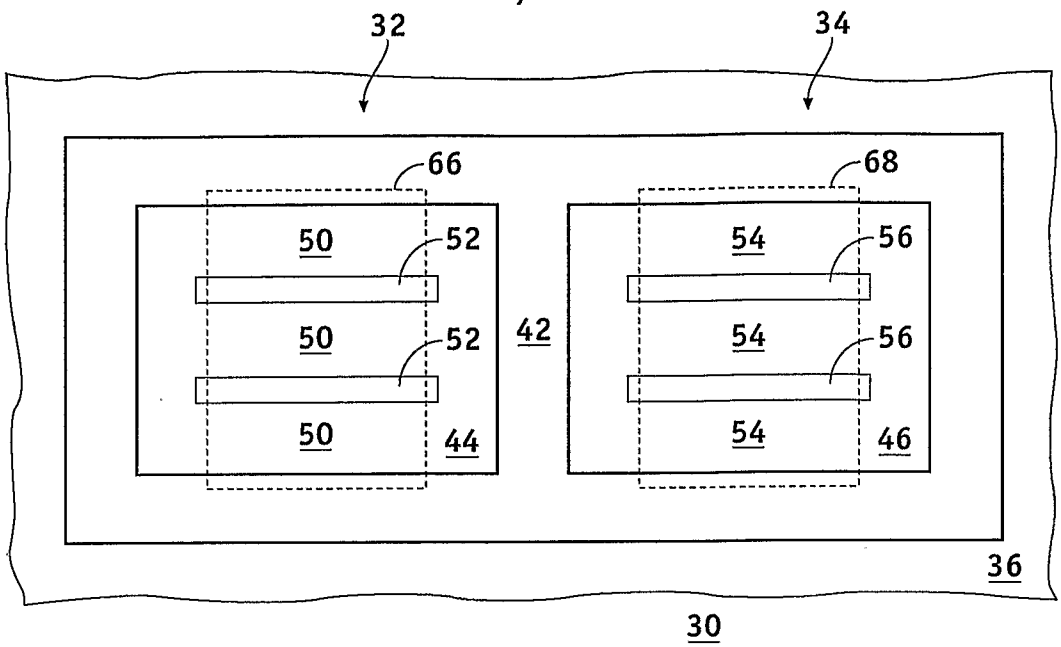


FIG. 3

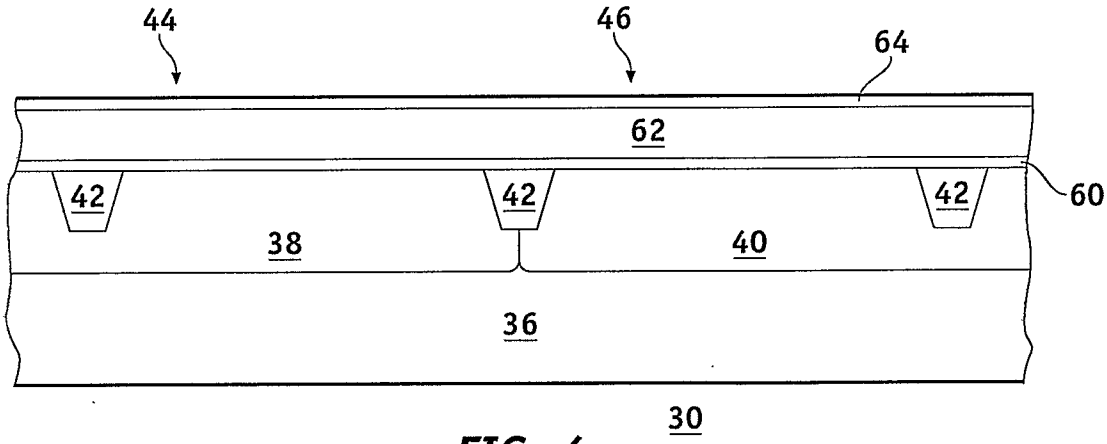


FIG. 4

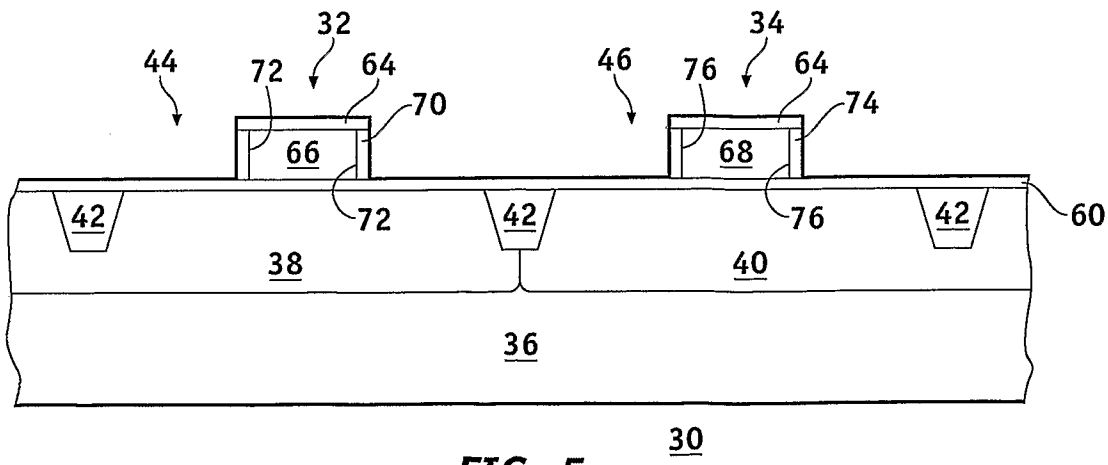


FIG. 5

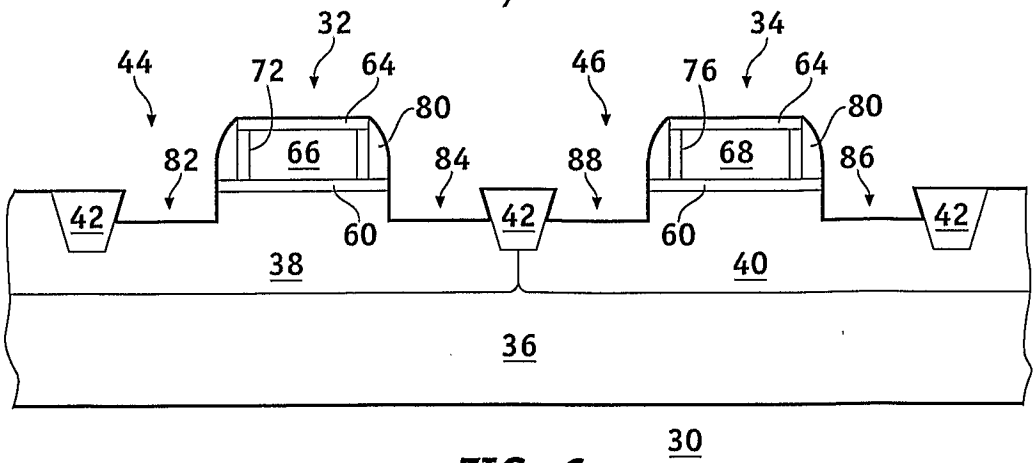


FIG. 6

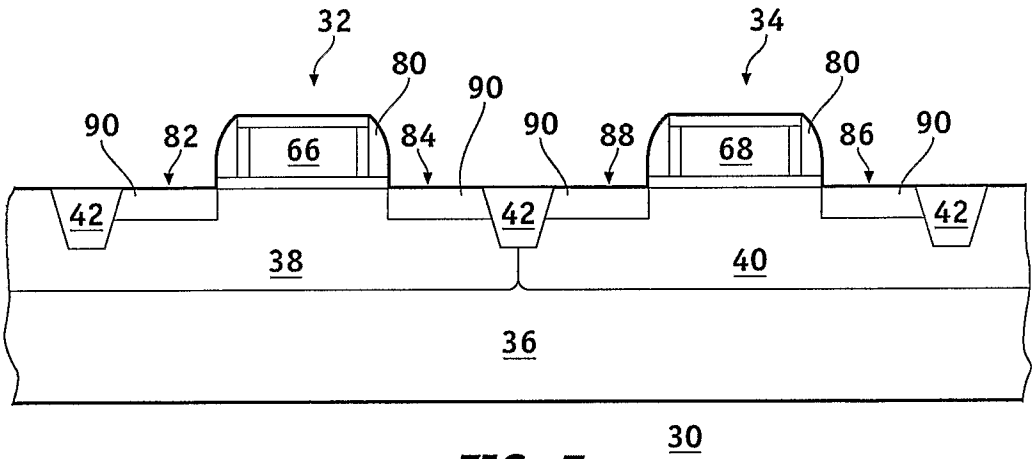


FIG. 7

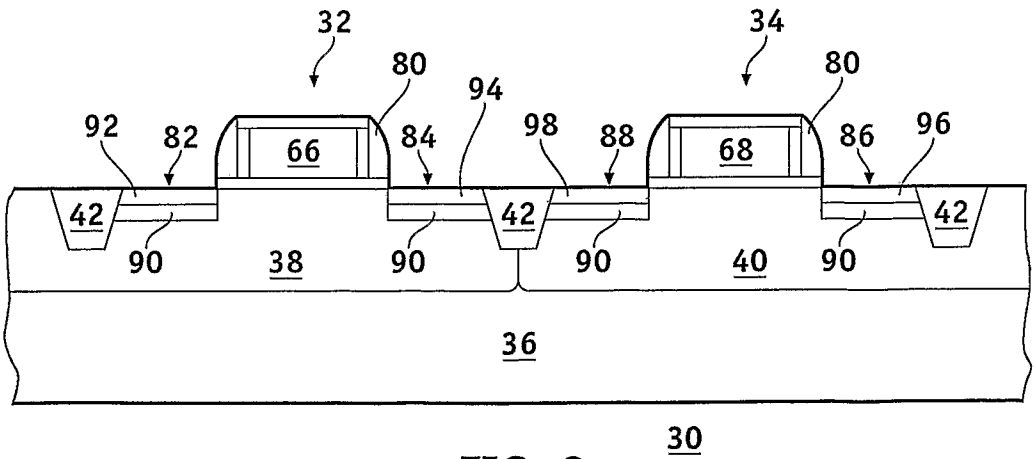


FIG. 8

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/028171

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L21/336

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2001/005022 A1 (OGURA TAKASHI [JP]) 28 June 2001 (2001-06-28) paragraph [0044] - paragraph [0080]; figures 1-3	1-10
Y	NOURI F ET AL: "A systematic study of trade-offs in engineering a locally strained pMOSFET" IEEE INTERNATIONAL ELECTRON DEVICES MEETING, 2004. IEDM TECHNICAL DIGEST. SAN FRANCISCO, CA, USA, DEC. 13-15, 2004, 13 December 2004 (2004-12-13), pages 1055-1058, XP010788995 PISCATAWAY, NJ, USA, IEEE ISBN: 0-7803-8684-1 the whole document	1-10

-/--

[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
17 November 2006	06/12/2006

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31–70) 340–2040, Tx. 31 651 epo nl, Fax: (+31–70) 340–3016	Götz, Andreas

INTERNATIONAL SEARCH REPORT

International application No
PCT/US2006/028171

C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	KRIVOKAPIC Z ET AL: "Locally Strained Ultra-Thin Channel 25nm Narrow FDSOI Devices with Metal Gate and Mesa Isolation" INTERNATIONAL ELECTRON DEVICES MEETING 2003. IEDM. TECHNICAL DIGEST. WASHINGTON, DC, DEC 8 - 10, 2003, 8 December 2003 (2003-12-08), pages 445-448, XP010684048 NEW YORK, NY : IEEE, US ISBN: 0-7803-7872-5 the whole document	1-10
A	US 2004/227187 A1 (CHENG ZHIYUAN [US] ET AL) 18 November 2004 (2004-11-18) figure 8A	1-10

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/US2006/028171

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2001005022 A1	28-06-2001	JP 2001185721 A	06-07-2001
US 2004227187 A1	18-11-2004	US 2005202604 A1	15-09-2005