(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

PCT

(43) International Publication Date
23 June 2011 (23.06.2011)

(10) International Publication Number
WO 2011/073886 A1

(51) International Patent Classification:
H01L 33/00 (2010.01) *H01L 33/48* (2010.01)
H01L 33/62 (2010.01)

(21) International Application Number:
PCT/IB2010/055783

(22) International Filing Date:
13 December 2010 (13.12.2010)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09306264.4 18 December 2009 (18.12.2009) EP

(71) Applicants *(for all designated States except US)*: **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL). **PHILIPS LUMILEDS LIGHTING COMPANY, LLC** [US/US]; 370 West Trimble Road MS 91/MG, San Jose, California 95131 (US).

(72) Inventor; and
(75) Inventor/Applicant *(for US only)*: **LETERTRE, Fabrice Jerome** [FR/US]; P.O. Box 3001, 345 Scarborough Road, Briarcliff Manor, NY 10510-8001 (US).

(74) Agent: **DAMEN, Daniel, M.**; Philips Intellectual Property & Standards, High Tech Campus 44, P.O. Box 220, NL-5600 AE Eindhoven (NL).

(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PE, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LR, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:
— *with international search report (Art. 21(3))*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

(54) **Title**: SUBSTRATE FOR A SEMICONDUCTOR LIGHT EMITTING DEVICE

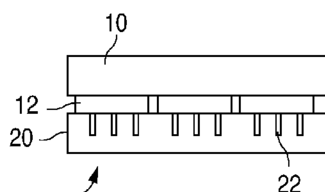

FIG. 2

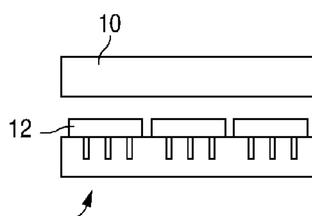

FIG. 3

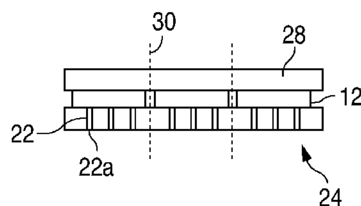

FIG. 4

(57) **Abstract**: A semiconductor structure (12) comprising a light emitting layer (44) disposed between an n-type region (42) and a p-type region (46) is grown on a first substrate (10). The semiconductor structure (12) is attached to a top surface of a second substrate (24). The second substrate (24) includes a body (20) with a plurality of holes (22) filled with a conductive material. After attaching the semiconductor structure (12) to the second substrate (24), the body (20) is thinned from the bottom surface of the second substrate (24), such that a bottom surface of the holes (22) is exposed.

SUBSTRATE FOR A SEMICONDUCTOR LIGHT EMITTING DEVICE

BACKGROUND

FIELD OF INVENTION

[0001] The present invention is directed to methods of attaching a light emitting device to a substrate then processing the substrate.

DESCRIPTION OF RELATED ART

[0002] Semiconductor light-emitting devices including light emitting diodes (LEDs), resonant cavity light emitting diodes (RCLEDs), vertical cavity laser diodes (VCSELs), and edge emitting lasers are among the most efficient light sources currently available. Materials systems currently of interest in the manufacture of high-brightness light emitting devices capable of operation across the visible spectrum include Group III-V semiconductors, particularly binary, ternary, and quaternary alloys of gallium, aluminum, indium, and nitrogen, also referred to as III-nitride materials. Typically, III-nitride light emitting devices are fabricated by epitaxially growing a stack of semiconductor layers of different compositions and dopant concentrations on a sapphire, silicon carbide, III-nitride, or other suitable substrate by metal-organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), or other epitaxial techniques. The stack often includes one or more n-type layers doped with, for example, Si, formed over the substrate, one or more light emitting layers in an active region formed over the n-type layer or layers, and one or more p-type layers doped with, for example, Mg, formed over the active region. Electrical contacts are formed on the n- and p-type regions.

[0003] US 7,256,483 teaches “it is sometimes desirable to remove the growth substrate to, for example, improve the optical properties of the LED or to gain electrical access to the LED layers. In the case of a sapphire substrate, removal may be by means of laser melting a GaN/sapphire interface. In the case of Si or GaAs substrates, more conventional selective wet etches may be utilized to remove the substrate.

[0004] “Since the LED epitaxial layers are extremely thin (e.g., less than 10 microns) and delicate, before removing the growth substrate, the LED wafer must first be attached to a support substrate so that the LED layers are sandwiched between the growth substrate and the support substrate. The support substrate has the desired optical, electrical, and thermal characteristics for a particular application of the LED. The growth substrate is then removed by known processes. The resulting wafer with the support substrate and LED layers is then diced, and the LED dice are then mounted in packages.

[0005] “A package typically includes a thermally conductive plate with electrical conductors running from the die attach region to the package terminals. The p and n layers of the LED are electrically connected to the package conductors. In the case of a vertical injection device, the support substrate is metal bonded to the package, providing a current path to the n or p-type LED layers adjacent to the support substrate, and the opposite conductivity type layers are connected via a wire (e.g., a wire ribbon) to a package contact pad. In the case of a flip-chip LED (n and p-type layers exposed on the same side), both n and p-connections are formed by die attaching to multiple contact pads patterned to mate to the n and p-contact metallizations on the die. No wires are required.

[0006] Needed in the art are substrates to which light emitting devices may be connected which are simple to handle and which efficiently conduct heat away from the light emitting device.

SUMMARY

[0007] In embodiments of the invention, a semiconductor structure comprising a light emitting layer disposed between an n-type region and a p-type region is grown on a first substrate. The semiconductor structure is attached to a top surface of a second substrate. The second substrate includes a body with a plurality of holes filled with a conductive material. After attaching the semiconductor structure to the second substrate, the body is thinned from the bottom surface of the second substrate, such that a bottom surface of the holes is exposed.

[0008] In some embodiments, attaching the semiconductor structure to a substrate with conductive vias permits wafer-level processing of the semiconductor structure and the substrate.

Heat may be conducted away from the semiconductor structure by the conductive vias.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Fig. 1 illustrates LEDs grown on a growth substrate.

[0010] Fig. 2 illustrates the LEDs of Fig. 1 attached to a substrate with conductive vias.

[0011] Fig. 3 illustrates removing the growth substrate from the structure of Fig. 2.

[0012] Fig. 4 illustrates thinning the substrate of Fig. 3 to expose the bottom of the conductive vias.

[0013] Fig. 5 illustrates an LED and substrate attached to a mount.

[0014] Fig. 6 illustrates an LED, substrate with through vias, and substrate with integrated circuitry attached to a mount.

DETAILED DESCRIPTION

[0015] In embodiments of the invention, a semiconductor light emitting device is bonded to a substrate with conductive through-vias. The substrate supports the semiconductor light emitting device to prevent breakage during wafer-level processing. The through-vias may conduct heat away from the light emitting device during operation.

[0016] Fig. 1 illustrates a III-nitride device 12 and portions of two other devices grown on a growth substrate 10. Only a portion of the growth substrate 10 is shown. Multiple LEDs are grown on a single growth substrate. A growth substrate may be, for example, on the order of centimeters in diameter. Each LED may be, for example, about 1 mm long. Growth substrate 10 may be, for example, a sapphire, SiC, Si, composite, or any other suitable substrate. Composite substrates are described in more detail in US 2007/0072324, which is incorporated herein by reference.

[0017] The semiconductor structure of the device includes an n-type region 42, a light emitting or active region 44, and a p-type region 46. An n-type region 42 is grown first on

substrate 10. The n-type region may include multiple layers of different compositions and dopant concentration including, for example, preparation layers such as buffer layers or nucleation layers, which may be n-type or not intentionally doped, release layers designed to facilitate later release of the growth substrate or thinning of the semiconductor structure after substrate removal, and n- or even p-type device layers designed for particular optical or electrical properties desirable for the light emitting region to efficiently emit light.

[0018] A light emitting or active region 44 is grown over the n-type region 42. Examples of suitable light emitting regions include a single thick or thin light emitting layer, or a multiple quantum well light emitting region including multiple thin or thick quantum well light emitting layers separated by barrier layers.

[0019] A p-type region 46 is grown over the light emitting region 44. Like the n-type region, the p-type region may include multiple layers of different composition, thickness, and dopant concentration, including layers that are not intentionally doped, or n-type layers.

[0020] A metal p-contact 50 is formed on the p-type region. P-contact 50 may include one or more metal layers such as, for example, a reflective layer, such as silver, an ohmic contact layer, and a guard layer. Portions of the p-contact 50, the p-type region 46, and the light emitting region 44 of the semiconductor structure are etched away to expose portions of the n-type region. N-contacts 52 are formed on the exposed portions of the n-type region. The n- and p-contacts 52 and 50 may be separated by a gap 54, which may be filled with an insulating material such as a suitable dielectric.

[0021] In some embodiments, instead of both p- and n-contacts formed on the same surface of the semiconductor structure, as illustrated in Fig. 1, a single large p-contact may be formed on the top surface of the semiconductor structure in the orientation illustrated in Fig. 1. A contact to the n-type region is formed on a surface of the n-type region exposed after removing the growth substrate, as described below in reference to Fig. 3.

[0022] Trenches 48 may be formed between individual devices 12. Metal bond pads, not shown in Fig. 1, may be formed over n- and p-contacts 52 and 50. In some embodiments, one or both of p-contacts 50 and n-contacts 52 are reflective, and light is extracted from the device

through the surface of the semiconductor opposite the contacts, the bottom surface of the semiconductor structure illustrated in Fig. 1.

[0023] In Fig. 2, the wafer of LEDs illustrated in Fig. 1 is flipped over and attached to a substrate 24. Substrate 24 may include vias or holes 22 filled with a conductive material such as metal formed in a non-metallic body 20. The material of body 20 may be selected for ease of forming vias and ease of thinning, as described below. Examples of suitable materials include silicon and ceramics such as AlN. Vias 22 in a silicon substrate 20 may be formed by conventional techniques such as laser drilling or deep reactive ion etching. One suitable deep reactive ion etching process is described in more detail in US Patent 5,501,893, which is incorporated herein by reference. Vias 22 may be, for example, between 10 and 100 microns deep in some embodiments, between 30 and 70 microns deep in some embodiments, and 50 microns deep in some embodiments. Vias 22 may be filled with any suitable conductive material formed by any suitable technique. In some embodiments, copper is electroplated into the vias.

[0024] LEDs 12 are attached to substrate 24 by, for example, a metallic bond or any other suitable bonding technique. For example, copper bond pads may be formed on LEDs 12 and substrate 24 then directly bonded pad to pad. Dielectric regions which insulate the n- and p-type pads may be formed between the copper bonds pads. In some embodiments, there is no air gap between the bonded pads. In other embodiments, LEDs 12 are attached to substrate 24 by solder or other metal interconnects, which may include multiple layers of materials. In some embodiments, interconnects between LEDs 12 and substrate 24 include at least one gold layer and the bond between the LEDs 12 and the substrate 24 is formed by ultrasonic bonding, or molecular bonding between mating surfaces. LEDs 12 are aligned on substrate 24 such that vias 22 are electrically connected to n- and p-contacts 52 and 50, shown in Fig. 1.

[0025] After bonding LEDs 12 to substrate 24, all or part of the growth substrate 10 may be removed by a technique appropriate to the growth substrate, as illustrated in Fig. 3. For example, a sapphire growth substrate may be removed by laser lift off, which may permit reuse of the growth substrate. A silicon substrate may be removed by grinding, etching, polishing or a combination of these techniques. A transparent substrate may remain part of the device. After removing the substrate, additional LED processing may be performed, such as surface etching,

cleaning, or deposition of dielectric layers, for example. In some embodiments, the semiconductor structure remaining after removing the host substrate is thinned, for example by photoelectrochemical etching. The semiconductor surface may be roughened or patterned, for example with a photonic crystal structure. Since the entire wafer of LEDs 12 is connected to substrate 24, conventional wafer-scale tools may be used for processing after the growth substrate is removed.

[0026] After optional post-growth-substrate-removal processing and optional testing, the top surface of the wafer of LEDs 12 may be attached to handling tape 28, as is known in the art of semiconductor processing. The substrate 24 may be thinned by conventional techniques such as etching, grinding, or polishing, which remove material from the bottom surface of the substrate. Substrate 24 is thinned to a thickness suitable for mechanical handling, and at least until the bottoms 22a of vias 22 are exposed.

[0027] The use of substrate 24 permits wafer-level processing on both the front side (for example, removing the LED growth substrate and thinning the LED semiconductor structure) and back side (for example, thinning the substrate 24 to expose the vias) of the structure.

[0028] After thinning, the substrate 24 may be diced at locations 30 between individual LEDs 12.

[0029] An individual LED 12 and its substrate 24 may then be attached to a mount 34 by conventional pick and place techniques. Mount 34 may be, for example, a silicon, ceramic, or AlN mount, a silicon mount with through vias as described above, a printed circuit board, or any other structure on which LED 12 and substrate 24 may be mounted. Conductive vias 22 in substrate 24 may align with vias 32 in mount 34. Vias 32 in mount 34 may be formed in, for example, a silicon structure 30.

[0030] In some embodiments, integrated circuits such as those required for, for example, efficient driving, feedback control, and electrostatic discharge protection, are formed in a substrate with conductive through-vias, as illustrated in Fig. 6. In a substrate 36, integrated circuitry 40 may be formed in a silicon body before or after vias 38 are formed.

[0031] In some embodiments, a wavelength converting material, which absorbs light emitted by the light emitting region and emits light of one or more different peak wavelengths, may be disposed over the LED 12 illustrated in Figs. 5 and 6. In some embodiments, polarizers, dichroic filters or other optics known in the art are formed over the LED or over the wavelength converting material.

[0032] Having described the invention in detail, those skilled in the art will appreciate that, given the present disclosure, modifications may be made to the invention without departing from the spirit of the inventive concept described herein. For example, though the above examples refer to III-nitride light emitting devices, other devices such as other III-V devices, III-phosphide, III-arsenide, or II-VI devices, may be used with the above-described substrates. Therefore, it is not intended that the scope of the invention be limited to the specific embodiments illustrated and described.

CLAIMS

What is being claimed is:

1. A method comprising:

providing a semiconductor structure grown on a first substrate, the semiconductor structure comprising a light emitting layer disposed between an n-type region and a p-type region;

attaching the semiconductor structure to a top surface of a second substrate, the second substrate comprising a body with a plurality of holes, wherein the plurality of holes are filled with a conductive material; and

after attaching the semiconductor structure, thinning the body from the bottom surface of the second substrate, such that a bottom surface of the holes is exposed.

2. The method of claim 1 wherein the body is silicon.

3. The method of claim 1 further comprising:

forming holes in the body by one of laser drilling and deep reactive ion etching; and

filling the holes with a conductive material.

4. The method of claim 1 further comprising removing the first substrate.

5. The method of claim 4 further comprising:

processing the semiconductor structure after removing the first substrate; and

dicing the semiconductor structure after processing the semiconductor structure.

6. The method of claim 1 further comprising aligning the plurality of holes with n- and p-contacts disposed on the semiconductor structure.

7. The method of claim 1 further comprising attaching the second substrate to a mount.

8. The method of claim 7 further comprising disposing a third substrate between the second substrate and the mount, the third substrate comprising an integrated circuit.

9. The method of claim 8 further comprising aligning the holes in the second substrate with holes filled with conductive material in the third substrate.

10. The method of claim 1 wherein the conductive material is copper.

11. The method of claim 1 further comprising dicing the semiconductor structure after thinning the body from the bottom surface of the second substrate.

12. A method comprising:

attaching a semiconductor structure to a substrate, the semiconductor structure comprising a III-nitride light emitting layer disposed between an n-type region and a p-type region, the substrate comprising a silicon body with a plurality of holes filled with a metal; and

after attaching the semiconductor structure, thinning the silicon body from the bottom surface to expose the metal filling the plurality of holes.

13. The method of claim 12 wherein the semiconductor structure comprises a wafer of light emitting devices, the method further comprising dicing the semiconductor structure and the substrate into individual light emitting devices after thinning the silicon body.

14. The method of claim 12 wherein the semiconductor structure comprises a wafer of light emitting devices, the method further comprising:

processing a surface of the semiconductor structure after attaching the semiconductor structure to the substrate; and

dicing the semiconductor structure and the substrate into individual light emitting devices after processing the surface of the semiconductor structure.

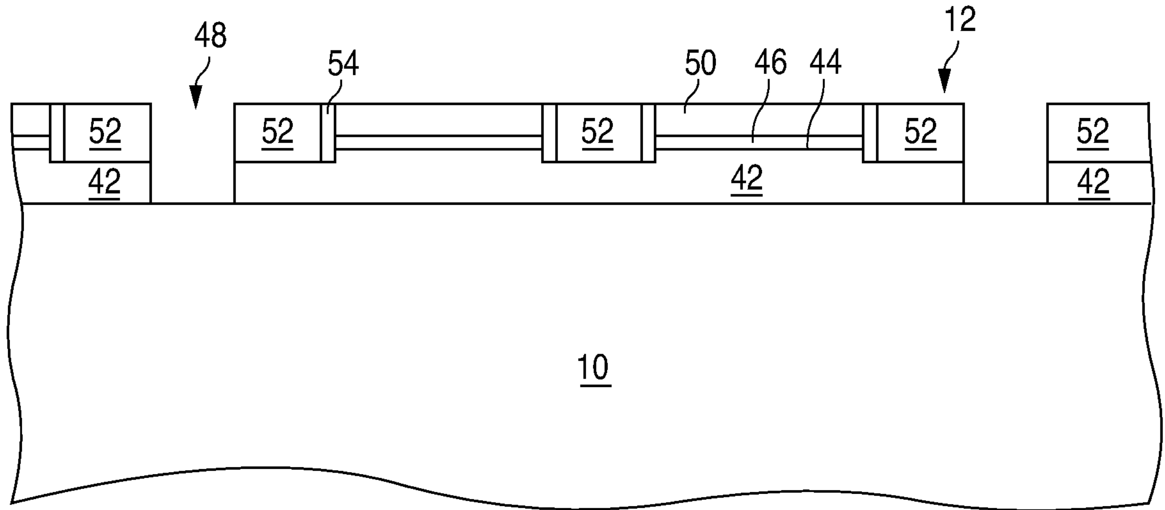

FIG. 1

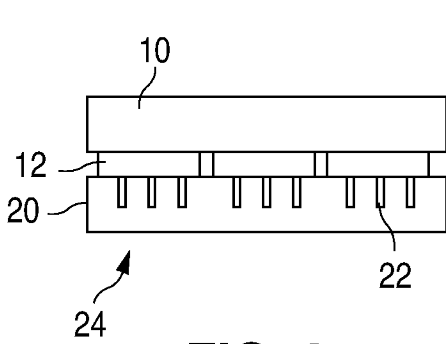

FIG. 2

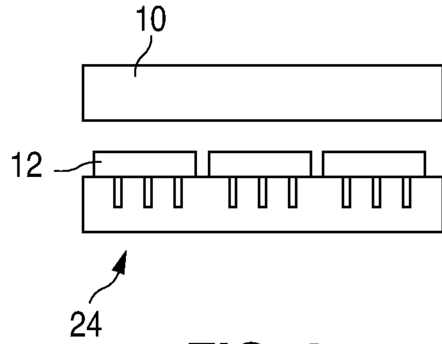

FIG. 3

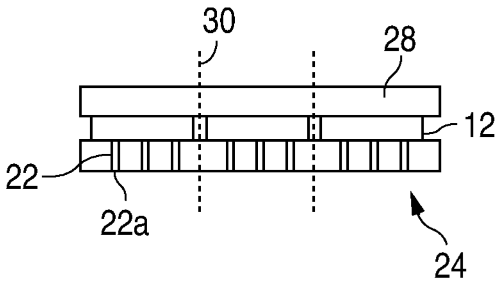

FIG. 4

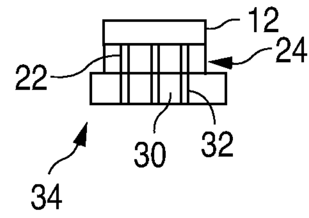

FIG. 5

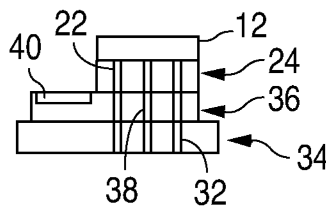

FIG. 6

INTERNATIONAL SEARCH REPORT

International application No
PCT/IB2010/055783

A. CLASSIFICATION OF SUBJECT MATTER
INV. H01L33/00 H01L33/62
ADD. H01L33/48

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L H01S

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, INSPEC, COMPENDEX

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2005/091388 A1 (MATSUSHITA ELECTRIC IND CO LTD [JP]; NAGAI HIDEO) 29 September 2005 (2005-09-29) page 30, line 12 - page 43, line 25 page 46, line 26 - page 54, line 7 figures 8A-17, 20-24	1-14
X,P	WO 2010/111821 A1 (HK APPLIED SCIENCE & TECH RES [CN]; LIN LIMIN [CN]; XIE BIN [CN]; YUAN) 7 October 2010 (2010-10-07) page 5, paragraph [0031] - page 8, paragraph [0040] figures 1-12	1,2,4, 10,12

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[X] Further documents are listed in the continuation of Box C.

[X] See patent family annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

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Date of the actual completion of the international search	Date of mailing of the international search report
21 April 2011	10/05/2011

Name and mailing address of the ISA/	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Fax: (+31-70) 340-3016	Sauerer, Christof

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C(Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	DE 10 2006 043843 A1 (SAMSUNG ELECTRO MECH [KR]) 19 April 2007 (2007-04-19) page 4/14, paragraph [0026] - page 5/14, paragraph [0041] figures 2-8 -----	1-14
A	US 2008/029761 A1 (PENG YI FANG [CN]) 7 February 2008 (2008-02-07) the whole document -----	1-14
A	US 2008/296627 A1 (WATANABE KENTARO [JP] ET AL) 4 December 2008 (2008-12-04) figure 6 page 5, paragraph [0074] - page 6, paragraph [0079] -----	1-14

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No
PCT/IB2010/055783

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