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(54) Title: PHOTON COUNTING AND INTEGRATING PIXEL READOUT ARCHITECTURE WITH DYNAMIC SWITCHING OPERATION

(57) Abrégé/Abstract:
A new pixel readout architecture is presented for direct conversion radiation detectors (for example, amorphous selenium). Photon-counting operation provides excellent sensitivity to low radiation doses but saturates the system at medium to high doses due to the poor charge transport properties of a-Se. Thus, we present a photon counting readout circuit design that is also capable of dynamically operating in integrating mode to enable the detection of high-dose radiation. This extends the resolvable dynamic range of the imaging system from very low gamma-ray count rates to very high flux x-ray radiations. The readout architecture thus is promising for applications such as mammography tomosynthesis and fluoroscopy, and its benefits can be extended to other radiation detectors as well. We also show spectroscopy results with a-Se and show the circuit's simulated behaviour of dynamically switching between counting mode and integrating mode to show the wide resolvable operating range.

Abstract

A new pixel readout architecture is presented for direct conversion radiation detectors (for example, amorphous selenium). Photon-counting operation provides excellent sensitivity to low radiation doses but saturates the system at medium to high doses due to the poor charge transport properties of a-Se. Thus, we present a photon counting readout circuit design that is also capable of dynamically operating in integrating mode to enable the detection of high-dose radiation. This extends the resolvable dynamic range of the imaging system from very low gamma-ray count rates to very high flux x-ray radiations. The readout architecture thus is promising for applications such as mammography tomosynthesis and fluoroscopy, and its benefits can be extended to other radiation detectors as well. We also show spectroscopy results with a-Se and show the circuit's simulated behaviour of dynamically switching between counting mode and integrating mode to show the wide resolvable operating range.

PHOTON COUNTING AND INTEGRATING PIXEL READOUT ARCHITECTURE WITH DYNAMIC SWITCHING OPERATION

FIELD OF THE INVENTION

The invention generally relates to method and apparatus for detecting, counting, and integrating photons of varying energies.

BACKGROUND

The field of medical imaging has seen many advances over the past two decades with the advent of digital imaging systems using electronic readout mechanisms. The majority of commercial systems use flat-panel arrays coated with direct conversion radiation detection materials such as amorphous selenium[1]. The traditional readout mechanism employed for each pixel in the array has been an integrating system (also referred to as current mode) where the charge created by the radiation incident upon the detector is integrated over a timeframe. But this technique can be susceptible to noise and results in the charge created by radiation to be proportional to the energy of the photons[2]. This effect limits the system's operation at low doses of radiation energy[3,4].

Another readout mechanism that deals with the problems present in the integrating scheme is the photon-counting system. In such a system each incident photon within a certain threshold window is given equal weight, regardless of its energy (i.e., the amount of charge it creates in the detector) such that the intensity at a pixel is measured simply by the number of photons within the threshold that have struck it, as opposed to the total charge buildup. This gives photon-counting systems the advantage of allowing for better operation in low-dose, low-noise applications with good resolution[5]. However counting systems have their own inherent drawback, as they are vulnerable to a pile-up effect at higher radiation doses, where the count saturates, rendering them incapable of distinguishing different doses of radiation past a certain point.

Amorphous selenium (a-Se) is the prevailing detector used in commercial x-ray imaging systems mainly due to its ease of deposition over a large area via vacuum evaporation[6]. This is despite the fact that a-Se exhibits poorer charge transport properties than competing detectors like crystalline cadmium-zinc-telleride

(CdZnTe). The charge transport properties of a-Se are apparent in its charge yield from x-ray radiation being an order of magnitude less than CdZnTe and its slow carrier mobility resulting in recombination of carriers in the detector even at high-bias operating fields[7]. This fundamentally limits the applications of a selenium-based photon-counting system, as the charge transport properties of the detector limit the readout system's maximum count rate, since all generated carriers should be collected by the readout system. Selenium is still appealing as a detector for photon-counting applications though, primarily because of its high resistivity and low leakage currents at high-bias operating fields. Leakage compensation techniques are typically necessary in detector readout circuits in order to distinguish the signal charge at the detector from charge as a result of leakage[8], but a-Se's high resistivity and low leakage currents allow for it to be direct coupled to the readout circuitry without the need for leakage compensation.

Dose-limited medical imaging applications such as mammography tomosynthesis and fluoroscopy where the amount of radiation given to the patient is capped can benefit from a system that combines the two readout schemes. Such a system would also allow a-Se's strengths as a detector with integrating mode readout to be complemented with the benefits of photon-counting mode at low doses to provide an excellent contrast and signal-to-noise ratio. Thus a new selenium-based counting-integrating pixel circuit architecture, which is capable of operating in both low-dose counting mode and high-dose integrating mode without *a priori* knowledge of dose intensity, is presented. Other hybrid counting-integrating circuit designs have been proposed but have the two different pixel architectures implemented using different circuitry operating simultaneously to show the benefits of having both modes of operation, and without showing a direct circuit readout capability[9]. Conversely, the architecture presented here is novel and significant because using a single readout circuit each pixel can dynamically adapt to the radiation dose it receives and seamlessly switch from counting mode to integrating mode if the dose is too high, thus providing a simple "smart pixel" solution that greatly extends the resolvable range of the imaging system while conserving processing time, power, and die area.

DETAILED DESCRIPTION OF THE INVENTION

1.1. Introduction

Thanks to considerable developments in medical imaging, doctors today have a considerably improved arsenal with which to diagnose their patients than ever before. Applications such as mammography tomosynthesis, where a series of images are taken from different angles around a women's breast have

allowed for easier diagnosis and better and more accurate identification of potentially cancerous cells[10,11]. Tomosynthesis has also made the process of getting a mammogram less obtrusive for the patient due to the lessened need for compressions of the breast compared to traditional single-image mammography, while also providing better image detail with the series of image slices[11].

The total radiation used in mammography tomosynthesis is required to be the same as one mammogram to make sure the radiation dose is still suitable for the patient, which means if a tomosynthesis system takes 60 images the total radiation dosage used in static mammography is divided by that factor for each image. Hence, a typical exposure range for such a tomosynthesis system with a 150μm pixel pitch taking 60 images per second is 6μR to 4mR[4,11]. In procedures such as angiography, however, dynamic imaging occurs in real time via digital fluoroscopy. The harmful effects of prolonged exposure of the patient to radiation during the operation means the dosages for fluoroscopy applications have to be rather low, orders of magnitude less than static imaging applications like mammography[12]. A typical range for fluoroscopy exposure is 0.1μR to 10μR using a pixel size of 150μm and a frame rate of 30 images per second[4,13-15].

Given the large exposure range with applications like tomosynthesis and fluoroscopy, a photon-counting architecture would be ideal for providing a high signal-to-noise ratio at the lower doses; however, the maximum count rate for the photon-counting circuit is limited by the transit time of electrons in a-Se, which are the slower charge carrier in selenium[16]. From this we can define the maximum pulse count rate (PCR_{max}) for a selenium photon-counting circuit using a semi-Gaussian pulse shaper, which has a shaping time (τ_s) of half of the maximum transit time of electrons[17] (τ_e). The semi-Gaussian profile causes the peak time (τ_g) to occur at $2.2\tau_s$, but the overall pulse width is still $5\tau_s$ wide, which defines the delay until the next pulse can be counted. Thus, the maximum pulse count rate for a pixel is given by the following equation[18,19]:

$$PCR_{\max} = \frac{1}{5\tau_s} = \frac{2}{5\tau_e} = \frac{2\mu_e F}{5d_{Se}} \tag{1}$$

where τ_s is the pulse shaping time, τ_e is the maximum transit time of electrons, d_{Se} is the thickness of the amorphous selenium film, μ_e is the mobility of electrons, and F is the electric field bias. Using the values summarized in Table 1, PCR_{max} for this pixel architecture is 8000 photon counts per second.

We now show what the count rate per pixel will be for the exposure range specified for the applications to see how it compares to the count rate calculated above. The minimum dose is 0.1μR, while the maximum is

240μR. The number of x-ray photons incident is related to the radiation dose and photon energy by the following formula, which expresses the photon fluence ς in photons per mm^2 per mR of radiation as a function of photon energy[20]:

$$\zeta(E) = \frac{5.43 \times 10^5}{(\mu_{en}(E)/\rho)_{air} E} \quad [\frac{photons}{mm^2 mR}] \tag{2}$$

where E is the photon energy in eV and $(\mu_{en}(E)/\rho)_{air}$ is the mass energy absorption coefficient of air, which is itself also dependent on the photon energy.

Calculating the maximum count rate that the range of radiation fluxes for these applications could provide gives pixel counts as high as over 1 million. This count rate, even though it is likely an underestimation, still far exceeds the maximum count a selenium-based counting circuit can handle, which we calculated earlier to be 8000 counts per second per pixel. This is the reason why the pixel architecture needs to switch to integrating mode, which can handle radiation doses as high as 4mR. It is this very concept upon which the counting-integrating circuit's intelligence is based – if a count rate for a pixel beyond the maximum set value is detected, the operation of that particular pixel's readout circuit will switch to integrating mode as will be shown in the next section's in-depth explanation of the circuit's operation.

1.2 Pixel Architecture

The block diagram of the hybrid CMOS readout pixel designed to operate with the direct-converting a-Se detector is shown in Figure 1. The pixel is comprised of a radiation detector (a-Se), a charge sensitive amplifier (CSA), a pulse shaper, two comparators, a decision unit, and a pseudorandom counter. The device can operate in low radiation photon-counting mode and dynamically switch to integrating mode when it detects high-dose radiation. Following detection, the circuit can also be in operated at a high clock rate in readout mode to serially read out the value of the pixel counter. A pseudorandom counter is used to record the pixel count because it can operate at very fast readout rates and has a simple design of cascaded registers taking up minimal die size and allowing for serial readout. With *m* registers a pseudorandom counter can hold up to a maximum pixel count of 2^m-1.

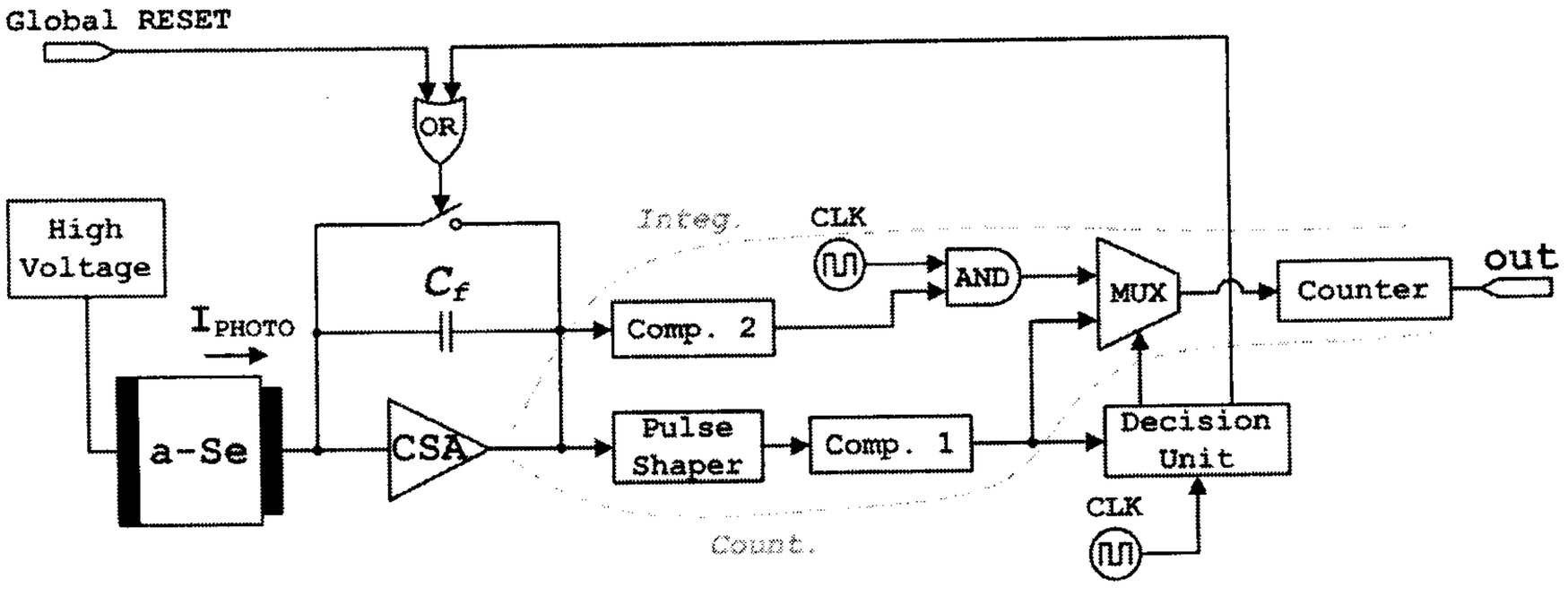


Figure 1: The block diagram of the hybrid CMOS readout pixel operated with amorphous selenium in low-flux counting mode and high-flux integrating mode.

A more detailed look at the operation of the counting-integrating circuit pixel architecture is shown in the complete schematic in Figure 2. The photon-induced charge from the a-Se detector is collected at the input of the CSA. The CSA integrates this charge to provide a voltage ramp at its output whose slope is proportional to the amount of collected input charge. The low-noise amplification of the charge signal by the CSA increases the detector's sensitivity.

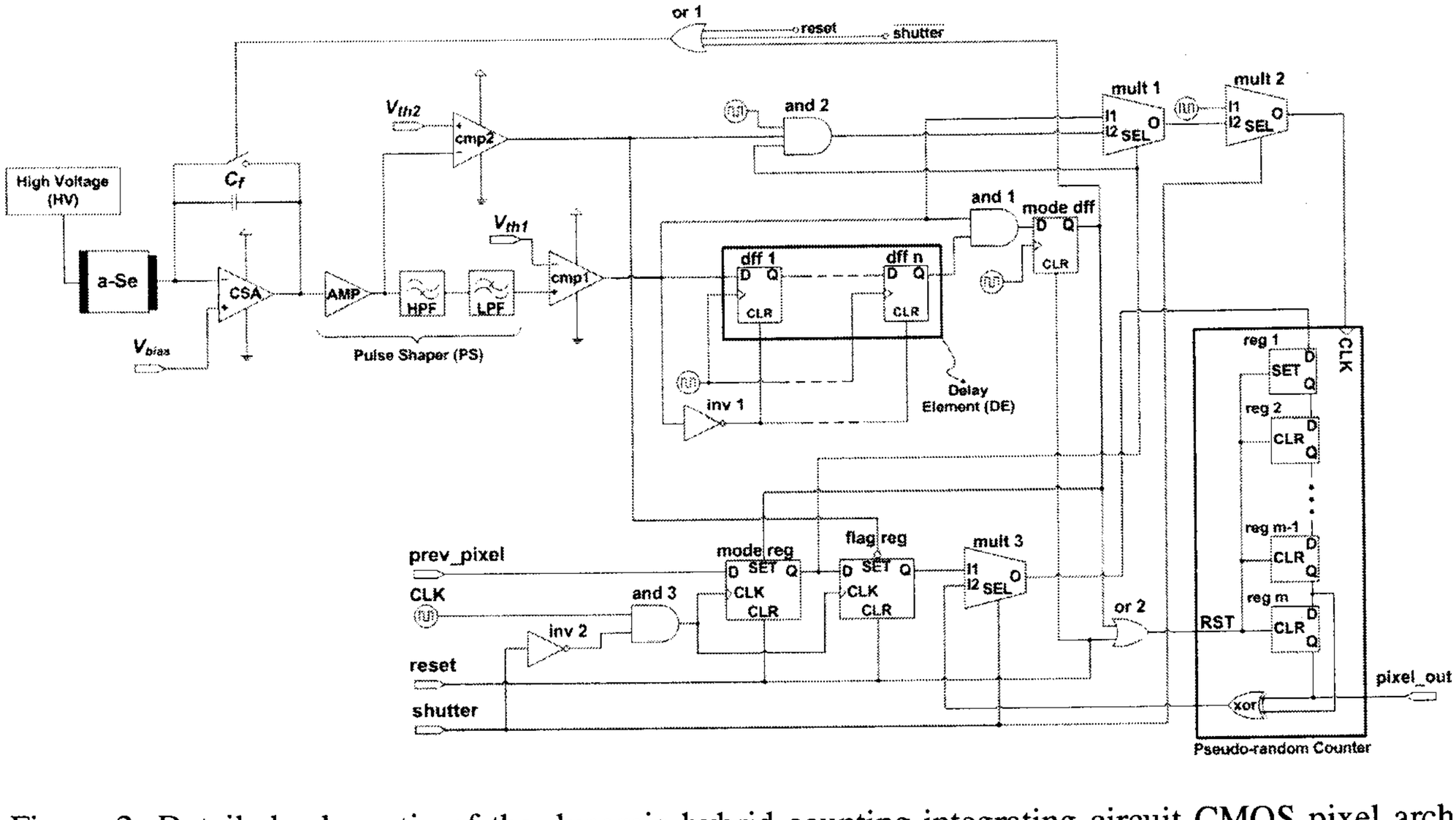


Figure 2: Detailed schematic of the dynamic hybrid counting-integrating circuit CMOS pixel architecture with amorphous selenium detector.

1.2.1 Counting Mode Operation

The output of the CSA across is fed to a semi-Gaussian pulse shaper with a baseline restorer. A pulse shaper is a circuit that provides amplification and filtering of the signal. A unipolar semi-Gaussian implementation is used in this architecture because it can maximize count rate and minimized pulse width compared to other implementations[18]. It contains a differentiator and three integrators providing a total nominal gain A_0 at the center frequency of the inverse of the shaping time τ_s radians per second. Its transfer function is given by the following equation[19]:

$$H_{PS}(s) = A_0 \frac{s\tau_s}{(1+s\tau_s)^4} \tag{3}$$

The pulse shaper amplifies the signal independent of its rise time and shortens the circuit's response time, while filtering low- and high-frequency noise. Its magnitude frequency response is shown by the Bode plot in Figure 3. The semi-Gaussian pulse shaper used in the counting-integrating circuit also employs a baseline restorer such that the output pulse does not display an undershoot upon settling, so as not to distort the next output pulse, thus allowing for the fastest possible operation at the given shaping time[18]. The pulse-shaper's transient response is shown in Figure 4, which displays its output decaying to zero without an undershoot.

Energy windowing is not required in a selenium-based counting system since the photon energy resolution of a-Se is poor, as indicated by its spectrum showing a full-width at half-maximum of 50% of the full spectrum[17]. Thus, accurate energy discrimination of photons cannot be reliably achieved, and a single-threshold comparator is sufficient to indicate the arrival of photons. The output of the pulse shaper is fed to this single-threshold comparator (cmp1) with the threshold V_{th1}, which is set to the minimum voltage level for photon detection above noise to eliminate false counts. The a-Se detector exhibits low leakage and the CSA does not need leakage compensation, but the pixel architecture presented here can easily be used with other radiation detectors by using a CSA with leakage compensation circuitry.

In the case of low radiation doses, the continuous arrival of single photons results in the integrated output of the CSA constantly increasing in small ramp steps due to the added charge from the arrival of the photons. The pulse shaper converts each added step on the CSA output to a semi-Gaussian pulse shown by the solid line pulse in Figure 4. So the output of cmp1 stays high for the period of time during which this pulse is above V_{th1} as indicated, and this pulse goes through the two multiplexers mult1 (SEL=0, since at the start of each frame the mode register is reset) and mult2 (SEL=1, since during detection shutter is high) and thus a

count is recorded in the pseudorandom counter for each single-photon pulse. The operation of the counter will be covered in a following section.

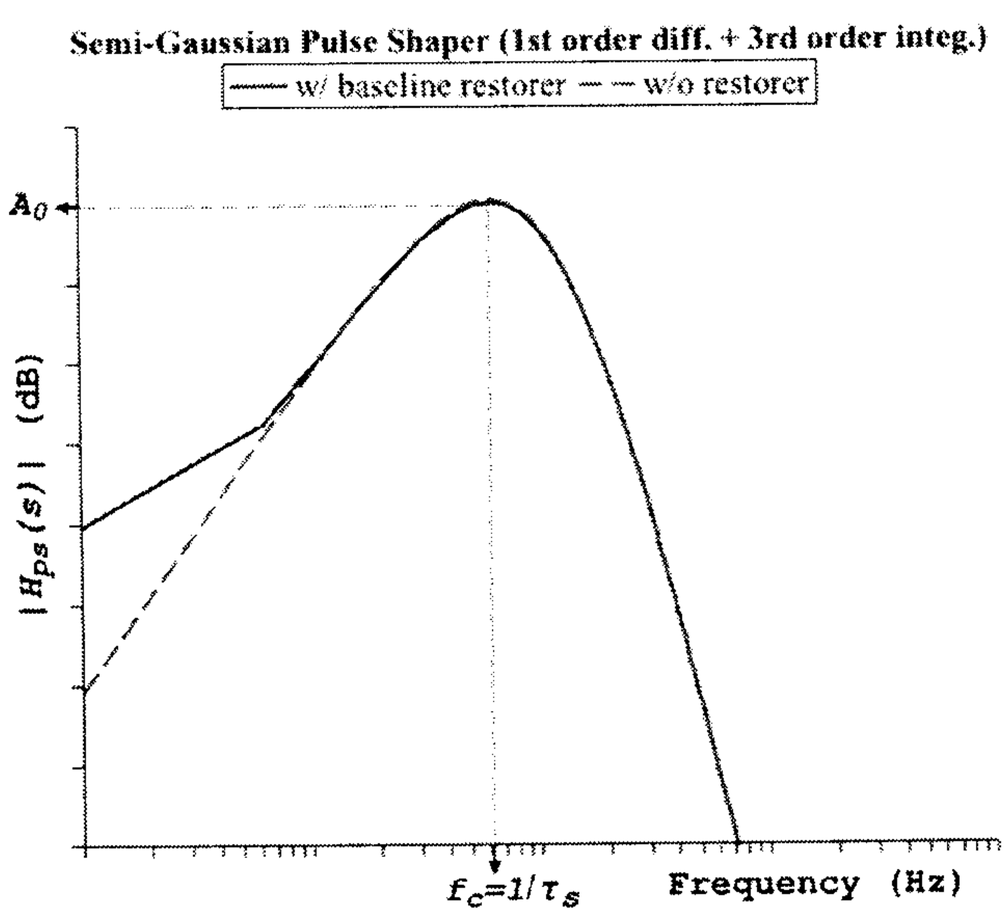


Figure 3: Frequency response of a semi-Gaussian pulse shaper with and without the baseline restorer.

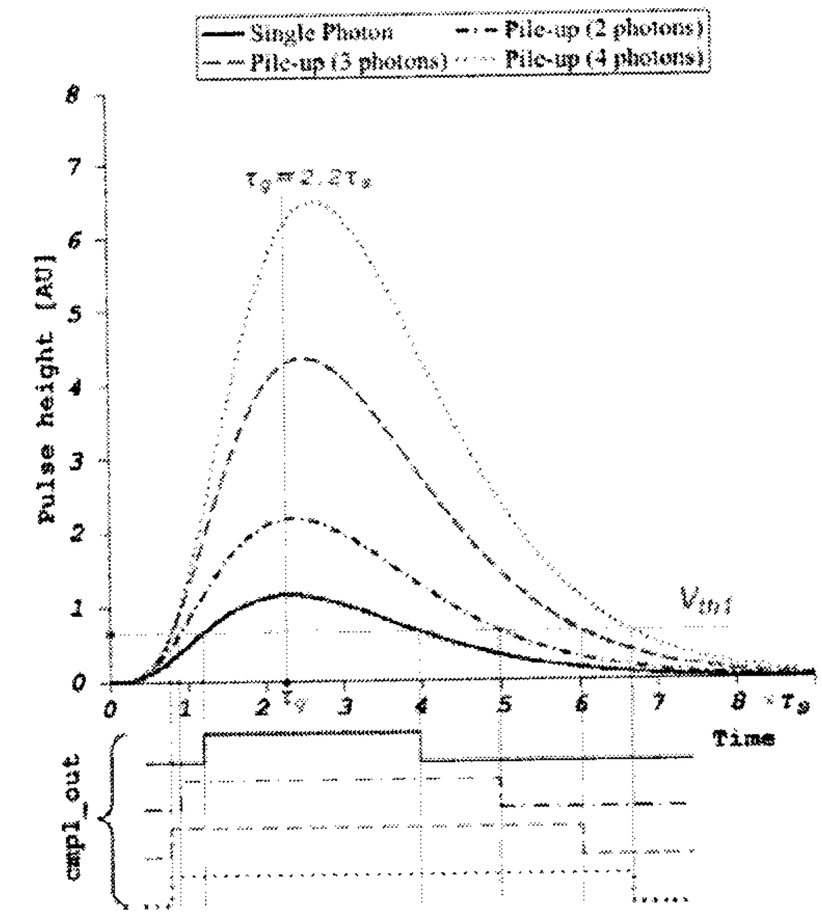


Figure 4: Outputs of pulse shaper with baseline restorer and counting threshold comparator for different scenarios of photon arrival, showing the effect of pile-up.

The number of photon counts in counting mode (C_C) can be represented by the following equation relating it to the photon count rate and detection time:

$$C_C = PCR \cdot t_{int} \text{ [photons/pixel]} \tag{4}$$

It can be shown that for the maximum photon count rate in a selenium-based system, the output of the CSA will not saturate. The output of the CSA is based on the charge at its input, with a gain equal to $1/C_f$, where C_f is the feedback capacitor. But this output voltage is made up of not just the charge generated by the photons, but also the charge due to the slight leakage current in the a-Se detector. So we can represent the CSA output voltage in counting mode with the following expression:

$$(V_{CSA})_C = V_{counts} + V_L = (C_C)\cdot\left(\frac{E}{W_{\pm}(E,F)}\right)\cdot\left(\frac{q}{C_f}\right) + \frac{I_L(F)\cdot t_{det}}{\cdot C_f} \text{ [V]} \tag{5}$$

where V_{counts} represents the voltage built up due to the charge created by the photons and V_L represents the voltage due to the leakage current, and where C_C is the number of photon counts per pixel as defined in equation 4, E is the photon energy in eV, $W_{\pm}(E,F)$ is the energy in eV required per electron-hole pair freed

in a-Se (a function of the electric field bias and photon energy), q is the charge of a single electron in Coulombs, C_f is the CSA feedback capacitor in Farads, $I_L(F)$ is the leakage current as a function of the electric field bias, and t_{det} is the time during detection in one frame.

The CSA output voltage is the sum of two terms, where the second term V_L represents the leakage current's additive voltage contribution during detection. The first term V_{counts}, which is a product of three different terms, represents the photon count's output contribution: The first term is the number of photons counted in one frame, the second term provides the number of electron-hole pairs freed per photon, and the third term provides the charge gain. Using a set of typical values and using the maximum C_C to find the largest CSA output voltage, the output is still well below the saturation limit of the CSA. It can also be shown that the maximum photon count rate does not exceed the maximum that the pseudorandom counter can hold, which is 2^m-1. Using typical values with a 12-bit counter, with the minimum frame rate of 5 used by some tomosynthesis systems[10], the maximum photons per frame is still far less than 2^{12}-1, or 4095.

1.2.2 Pile-up Detection and Dynamic Switching to Integrating Mode Operation

The comparator cmp1's output, which only remains high while the pulse shaper output is above the single-photon threshold voltage V_{th1}, is *and*ed with a delayed version of itself via a delay element (DE) made up of n flops; the calculation for the number of flops required is shown later in this section. It is the output of this *and1* gate that dictates the mode of operation by setting the mode register. For low-radiation doses, the pulse shaper output has a small width and so the comparator's pulse output is short compared to the total delay in the DE, resulting in *and2* to output 0 and the mode register to stay at its mode value of 0 (counting mode). It should also be noted that the inverter *inv* is necessary to clear the output of the flops in the delay element when the output of the comparator is low – that is, when the comparator signal is low, the flops are reset, and the only way a 1 can begin at the comparator output and propagate through all of the flops to reach the *and* gate is with a wide pulse.

The delay element is an integral part of how the circuit dynamically adapts to the input radiation and detects pile-up. In the case of higher radiation doses, pile-up occurs as shown in the transient response of the pulse shaper in Figure 4; as a result the pulse shaper output is wider and remains above V_{th1} for a longer amount of time. This means that the comparator cmp1's output pulse is high for a longer amount of time, channeling through the DE and resulting in the *and1* output to switch to 1 before eventually becoming 0 again. The

pulse at the output of *and1* indicates that pile-up has been detected and there needs to be a change in operating mode. The pulse sets the mode register output to 1, which also controls the SEL input of multiplexer mult1. This triggers mult1 to change to its other input I2, which is the integrating mode path, bypassing the pulse shaper. The pulse at the output of *and1* also resets the pseudorandom counter (through *or2*) so that it can begin recording the clock pulse count during the integration phase.

The integrating mode of operation uses the concept of slope detection to quantify the analog signal in digital terms and enable low-noise readout at high radiation fluxes. The output of the CSA increases linearly with a buildup in charge at the input. For proper slope detection the output of the CSA is amplified by a factor A_{amp} and fed to the comparator cmp2 where it is compared to the threshold voltage V_{th2}, and while the latter remains below the V_{th2} the comparator output stays high. The comparator output is *and*ed with the mode bit (now 1, as described earlier) and the clock, and so during this time the output of *and2* is simply the clock. This is routed through mult1 and mult2 to record counts in the pseudorandom counter.

To conserve power during integrating mode, the counting mode comparator cmp1 as well as the filters inside the pulse shaper are turned off. Also, it should be noted that the alternative to having a second comparator for the integrating path is to use the same comparator used in counting mode for pile-up detection along with a series of analog switches to change the inputs and decouple the output, reducing die area.

The routing of the clock through the two multipliers to the counter continues until the amplified CSA output ramp exceeds V_{th2}, causing the comparator output to go low, which in turn causes *and2* to output a 0. Thus, clock edges are counted during the integration ramp until the threshold V_{th2} is reached as shown in Figure 5.

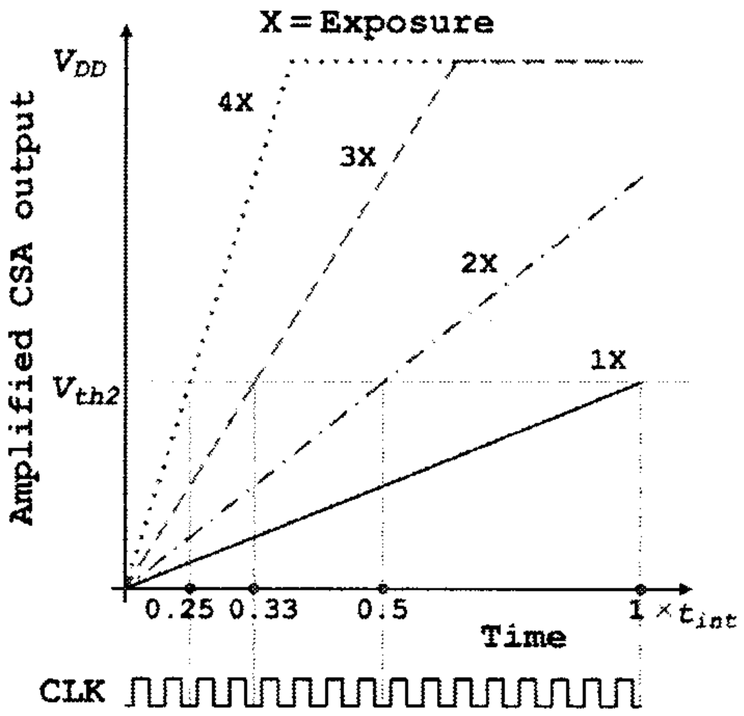


Figure 5: Hybrid circuit operation in integrating mode, where the number of clock edges counted during detection time until threshold is reached is proportional to the radiation exposure.

We can represent the CSA output voltage during integrating mode with the following equation:

$$(V_{CSA})_I = V_{sig} + V_L = \zeta(\mathrm{E}) \cdot X \cdot A \cdot (\frac{\mathrm{E}}{\mathrm{W}_{\pm}(\mathrm{E},F)}) \cdot (\frac{q}{C_f}) + \frac{I_L(F) \cdot t_{\mathrm{det}}}{C_f} \text{ [V]} \qquad (6)$$

where V_{sig} represents the voltage due to the integrated charge signal which is proportional to radiation flux, and V_L represents the constant additive voltage term due to leakage (the same as it was in equation 5), and where ζ is the photon fluence (from equation 2) in photons per mm^2 per mR, X is the radiation in mR, A is the pixel area in mm^2, E is the photon energy in eV, $W_{\pm}(E,F)$ is the energy required in eV per electron-hole pair freed in a-Se, which is a function of the electric field bias and photon energy, and q is the charge of a single electron in Coulombs.

Since the slope of the CSA output is proportional to the dose of radiation incident on the detector, fewer number of counts recorded means higher radiation. Once the CSA's amplified output exceeds V_{th2}, the comparator cmp2's output goes low, causing the output of *and2* to go low, which causes clock pulse counts to stop being recorded in the counter.

It was explained earlier that the output of the CSA is amplified before being fed to the comparator. This helps to improve the signal-to-noise ratio, but more importantly, it is due to the fact that larger analog signals can much more easily and accurately be compared with comparator. So, the actual comparison being made by cmp2 is between V_{th2} and the amplified CSA output, or $A_{amp}(V_{CSA})_I$, but for analysis purposes we will talk about the comparison being made between $(V_{CSA})_I$ and the raw threshold voltage V_{th20}, such that

V_{th2} is equal to $A_{amp}V_{th20}$. We showed earlier that the CSA output does not saturate in counting mode for the highest photon count rate at the lowest frame rate. Radiations any higher than the maximum single photon count rate are expected to be handled by the hybrid circuit in integrating mode; as such, the raw threshold voltage V_{th20} is set to the highest voltage that the output of the CSA can reach during the detection time t_{det} in counting mode, which was defined by equation 5.

Hence, we can write the following equation that expresses the relationship between V_{th20} and t_{det} to quantify the time it takes for the amplified CSA output to reach V_{th20} (denoted as t_{th}). If we then assume that the additive leakage term is negligible and substitute equation 5 for V_{th20} and equation 6 for $(V_{CSA})_I$ we can get an equation for t_{th} as follows:

$$\frac{(V_{CSA})_I}{t_{det}} = \frac{V_{th2_0}}{t_{th}} \longrightarrow \therefore \; t_{th} = \frac{V_{th2_0}}{(V_{CSA})_I} t_{det} = \frac{PCR \cdot t_{det}^{\,2}}{\zeta(E) \cdot X \cdot A} \tag{7}$$

As shown in Figure 5, we can see that when t_{th} is equal to t_{det}, that represents the lowest dose of radiation the integrating mode operation can detect. Since the number of clock pulse counts during t_{th} is the recorded count in integration mode (C_I), we can use equation 7 to define a direct relationship between C_I:

$$C_I = \frac{t_{th}}{T_{CLK}} = \frac{PCR \cdot t_{det}^{\,2}}{\zeta(E) \cdot X \cdot A \cdot T_{CLK}} \tag{8}$$

As expected, the number of counts is inversely proportional to the radiation incident on the detector. Also to note is that for the same radiation, using a lower clock period gives a higher number of counts; the importance of this fact will be shown in the next section dealing with the error.

If we assume that pile-up occurs and is detected by the circuit via the pulse shaper and delay element soon after the arrival of the first photon, then the switch to integrating mode occurs almost immediately and the voltage ramp begins building up so that C_I provides a reliable representation of the radiation. However, if pile-up is not detected until later on during the frame, there is a chance that the integration ramp after amplification does not reach the specified V_{th2} value before the end of detection time during the frame, since the switch to integrating mode will have come later during the frame and the feedback capacitor discharged at that time. This would mean that the number of clock pulse counts recorded during integration only represent a part of the frame time, resulting in a smaller C_I value which could be interpreted as a high radiation dose, when in fact that is not the case. In order to compensate for this when the output of *and2*

drops back low to indicate that the threshold V_{th2} has been reached, the flag register is set high to indicate that the count is reliable and equation 8 holds, because the integrated signal reached the integration threshold within the time of detection. If, after readout, the flag is not set but the mode register indicates the circuit was operating in integrating mode, the radiation detected at the pixel would have to be interpreted as occurring in the counting-integrating switching threshold and analyzed as such.

It is now appropriate to discuss the clock period T_{CLK}. Clearly, operating at a higher clock frequency, which has a smaller clock period, allows for higher resolution since more counts can be stored. But the pseudorandom counter used has a maximum storage capability of 2^m-1 as described earlier. So the clock frequency has to be picked such that the maximum number of edges recorded during integration time does not exceed this value. Since the maximum number of edges occurs if t_{th} is equal to the detection time (the lowest dose of radiation in integrating mode), we can write:

$$2^m - 1 \geq \frac{t_{\det}}{T_{CLK}} \tag{9}$$

Having clearly defined the clock period, we can return to the issue of the delay element and its n flops which are responsible for detecting wide pulses to indicate pile-up has occurred and the pixel needs to switch to integrating mode. The output of *and1* will only be high if both of its inputs – the pulse shaper comparator cmp1 signal and a delayed version of that same signal – are high. This will only happen if the signal remains high for n clock cycles while the delayed version of itself propagates to *and1*'s other input. As such, we can define an expression for the number of flops required as a function of the minimum signal pulse width (PW) and clock period (T_{CLK}):

$$n = \frac{PW}{T_{CLK}} \tag{10}$$

From Figure 3, it can be seen that for pile-up to have been detected, the signal needs to remain high for $3\tau_s$, where τ_s is the shaping time of the pulse shaper. Hence, setting PW to 3τs and dividing it by the clock period as shown by equation 10 gives the appropriate number of flops in the delay element.

1.2.3 Readout Mode Operation

Readout from the pseudorandom counter is done serially by driving the shutter signal low and operating the decision unit clock at a high rate, which is no longer constrained by the limitations on T_{CLK} during the detection modes. The bits are read out from the least significant to the most on the pixel_out line, with each clock edge pushing through the next bit. The *m+1*st bit read out will be the output of mult3, which is the flag bit stored in the flag register, followed by the mode bit stored in the mode register. Thus, the most significant bit of each pixel value, *m+2* bits wide, indicates whether the pixel value was operating in counting mode (0) or integrating mode (1), while the second most significant bit, which is only relevant if the pixel was in integrating mode, is the flag bit indicating whether the integrating mode count is valid or whether the pixel was operating in the counting-integrating threshold.

The following *m* bits provide the pixel count value – the number of photons counted in the frame for counting mode (C_C as given by equation 4), and the number of clock edges until the integrated signal reaches the set threshold for integrating mode (C_I as given by equation 7). The prev_pixel input allows for the pixel architecture to be cascaded in a row, with each previous pixel's pixel_out line connecting to the next one's prev_pixel input. The pixel values for the entire row can then be serially read out.

RESULTS AND DISCUSSION

2.1 Spectroscopy Results with Amorphous Selenium

In order to characterize the operation of the a-Se detector for use with the photon-counting readout circuit, spectroscopy tests were conducted to attain the results that are outlined below. The a-Se detector was DC coupled to the setup with no leakage compensation. A 150μm-thick sample of a-Se was used, though it should be noted that the sample was about 20 years old and degraded in quality due to crystallization over time. As such, the carrier mobility was greatly reduced and the maximum transit time of electrons was increased quite considerably. In fact it was found that a shaping time (τ_s) of 60μs needed to be used for the semi-Gaussian pulse shaping in the spectroscopy setup to ensure complete charge collection and avoid ballistic deficit, which occurs when some carriers formed in the detector due to the incident radiation are not collected due to fast processing time or short shaping time. The spectroscopy results are shown in Figure 6 below.

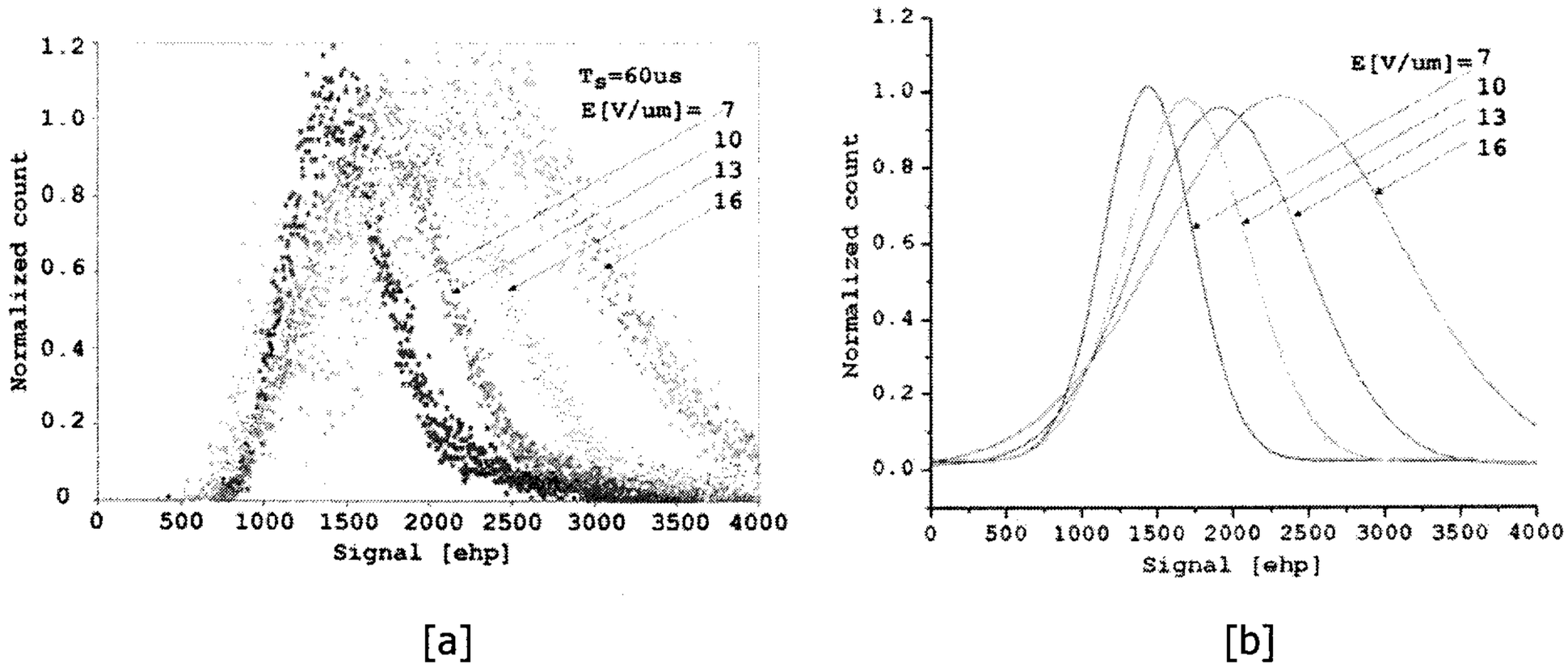


Figure 6: Spectroscopy results using 150μm-thick a-Se sample at varying bias voltages; [b] shows the Gaussian fitted curves of the results from [a].

Figure 6 [a] shows that as the electric field across the detector was increased, a wider spectrum was observed, which can be seen more clearly in the Gaussian fitted curves in Figure 6 [b]. The mean shifted slightly each time but the standard deviation of the curves steadily increased by a larger amount as the bias voltage was increased, which means that there was more noise in the circuit at the higher electric field biases. This is due to the fact the higher fields induced larger leakage currents, which in turn means greater shot noise in the circuit's operation. The reasons for the higher leakage are two-fold. There was greater charge injection at the selenium contacts with the higher bias voltages, since blocking layers were not used at the contacts. Also, the crystallization present in the 20-year-old selenium sample means it has a higher conductivity, helping drive up the leakage current.

Figure 7 below shows the relationship between the electric field bias and charge collection. As shown with the fitted line showing the mean of the Gaussian fitted curves from Figure 6[b], there is a linear relationship between charge collection and electric field, as the signal goes up with an increased electric field because more carriers are generated. However, the full-width at half-maximum (FWHM) values, which represent the noise in the circuit, do not follow the linear progression. Indeed, at the higher two bias voltages, the FWHM values increase much sharper than the linear progression of the lower two, which confirms the fact that there is an increase in noise with large bias voltages.

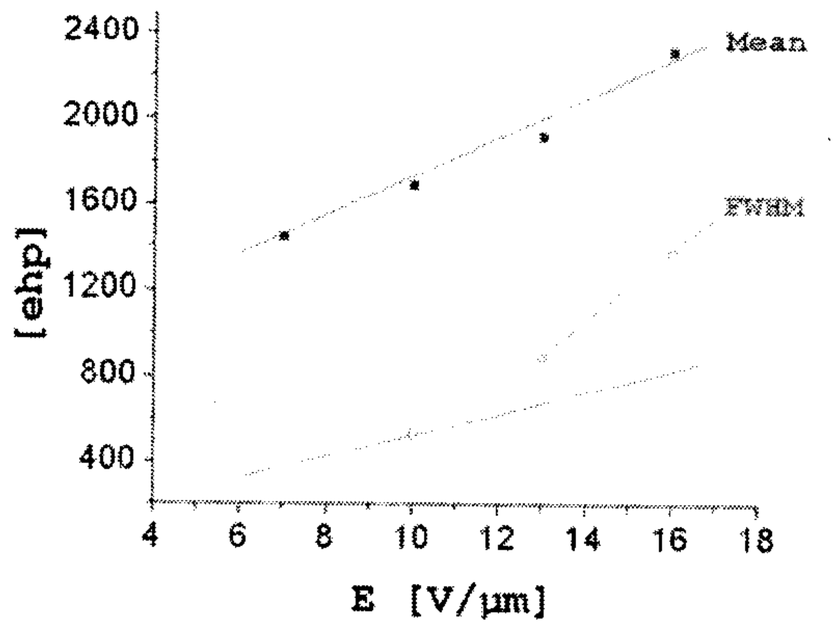


Figure 7: Electric field bias and charge collection have a linear relationship as shown by the line connecting the Mean data from Figure 6[b]. At large electric field biases (larger than 10V/μm), the circuit noise is increased due to greater leakage, shown by the FWHM data from Figure 6[b] displaying a non-linear relationship at the higher fields.

To show the effect of shaping time on the capability of the detector as described in section 1, spectroscopy tests were done with a shorter shaping time while keeping the electric field bias constant. The results are shown in Figure 8 below.

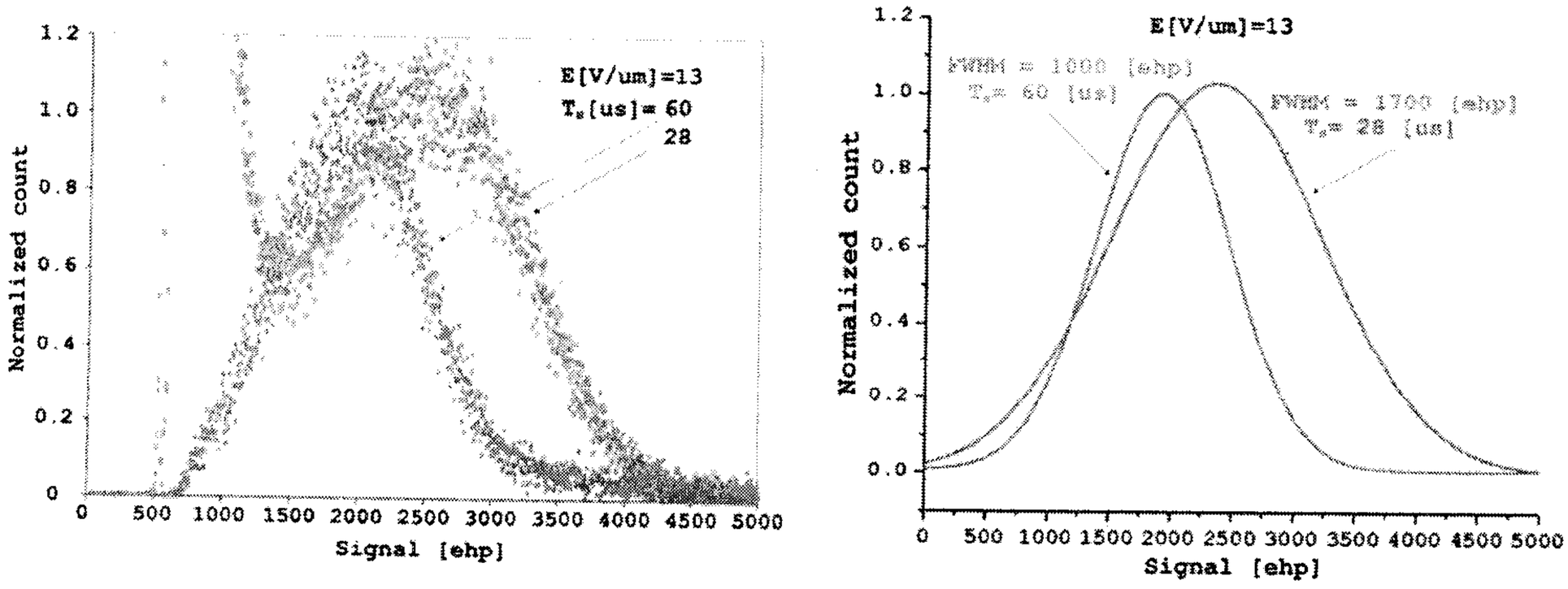


Figure 8: Spectroscopy results showing the effect of varying shaping time on charge collection, using 150μm-thick a-Se as the detector; [b] shows the Gaussian fitted curves of the results from [a].

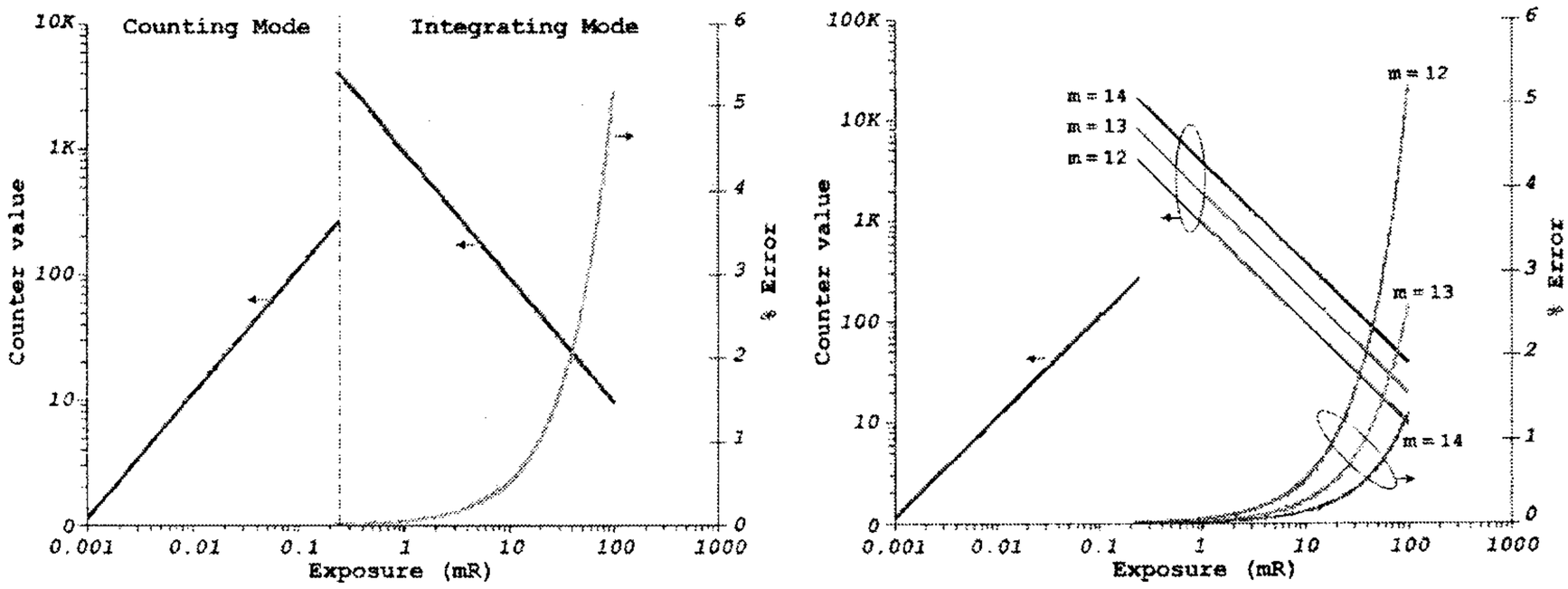
The shorter shaping time of 28μs had a detrimental effect on the spectroscopy results, as expected. Looking at Figure 8[b], the Gaussian fitted curves of the spectroscopy results, the curve for the shorter shaping time is wider and the full-width at half maximum is nearly twice that of the longer shaping time. This illustrates the fact that the noise in the readout circuit has been increased due to the fact that the short shaping time does not allow for complete charge collection, causing the ballistic deficit displayed. Furthermore, Figure 8[a] shows that at lower signal energies, the shorter shaping time causes a large amount of noise due to the electronic noise having gone up.

3.2 Simulation Results and Maximum Error

It is important to analyze the accuracy of the count provided by the integrating mode operation of the circuit, since it is based on digitizing an analog signal. The count obtained after readout with integrating operation provides a maximum digitized error of one count, since the last clock edge could arrive up to one clock cycle before the amplified CSA output hits the threshold value. This is due to the fact that the output of the *and1* gate is flopped and thus the recording of pulses begins at the same time as the feedback capacitor gets discharged and reset for integrating to begin. If the operation here were asynchronous, the uncertainty of one clock cycle would exist at the beginning of the integrating period as well, causing the maximum error in the count to be 2.

For this reason we take the readout value to be the mean value it could represent; for example the time the threshold is hit for a recorded count of 22 pulses could be anywhere from 22 to 22.9 times the clock period, so we should interpret it as 22.5 times the clock period. This allows the error to be plus or minus half of one count (+/- 0.5 counts). It is thus apparent that a higher clock frequency (meaning a larger counter, from equation 9) would allow more counts to be recorded, and lessen the effect of 0.5 counts as a percentage error. Also apparent is the fact that as the radiation exposure gets lower, the number of counts recorded is higher (also formulated in equation 8), lessening the effect of the 0.5-count error for the lower fluxes, which is important.

The preceding explanations are shown in Figure 9 below, where simulation of the counting-integrating circuit with typical values shows the output of the counter and the percentage error.



[a] [b]

Figure 9: Simulation results for hybrid counting-integrating circuit with dynamic switching, also showing % error; [a] shows the separation of the operation distinctly, while [b] shows the effect of a larger counter (and higher clock frequency).

The simulation of the circuit architecture shows by Figure 9[a] the counter value increasing in counting mode for low radiation exposures. When the counting threshold is reached, operation is switched to integrating mode, where the count value is highest at the lower radiations and decreases for higher radiations. The percentage error is zero in counting mode because only valid photon counts are recorded by the counter, while in integrating mode the error increases as exposure increases on a log scale. However, it is important to note that the percentage error at an exposure as high as 100mR is only about 5%. And this is using typical values with a 12-bit counter; as Figure 9[b] shows, using a larger counter with a higher frequency allows the error to be suppressed significantly even at very high radiation fluxes.

SUMMARY

The presented pixel readout architecture enables operating the detector in both the counting and integrating modes for very low to very high flux radiation, as the circuit can adapt to the radiation incident upon the pixel and operate accordingly, with the readout value able to be easily analyzed and interpreted as such. Thus, the resolvable dynamic range of the imaging system can be extended both below the noise-limited floor of the integrating system and beyond the saturation limit of the photon-counting system to provide a novel architecture where in an imaging array, pixels can dynamically operate in the mode allowing to provide the best resolution. The simplicity of the circuit allows power and die area to be conserved. The spectroscopy results of the operation of the a-Se detector in counting mode have been presented, and the

simulation results show the operation of the dynamic switching of the counting-integrating circuit and the small error percentage which can be shrunk by operating the circuit faster.

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