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Carman

[11] **3,723,956**

[45] **Mar. 27, 1973**

[54] ACOUSTIC CONTROL TRANSMITTER

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[73] Assignee: **Cameron Iron Works, Inc.,** Houston, Tex.

[22] Filed: **Aug. 5, 1970**

[21] Appl. No.: **61,339**

[52] **U.S. Cl.**.....**340/5 R,** 325/122, 325/163, 340/16 C

[51] **Int. Cl.**.....**H04b 11/00**

[58] **Field of Search**...340/5 R, 16 C, 18 NC, 18 CM, 340/18 FM, 15; 325/163, 122

[56] **References Cited**

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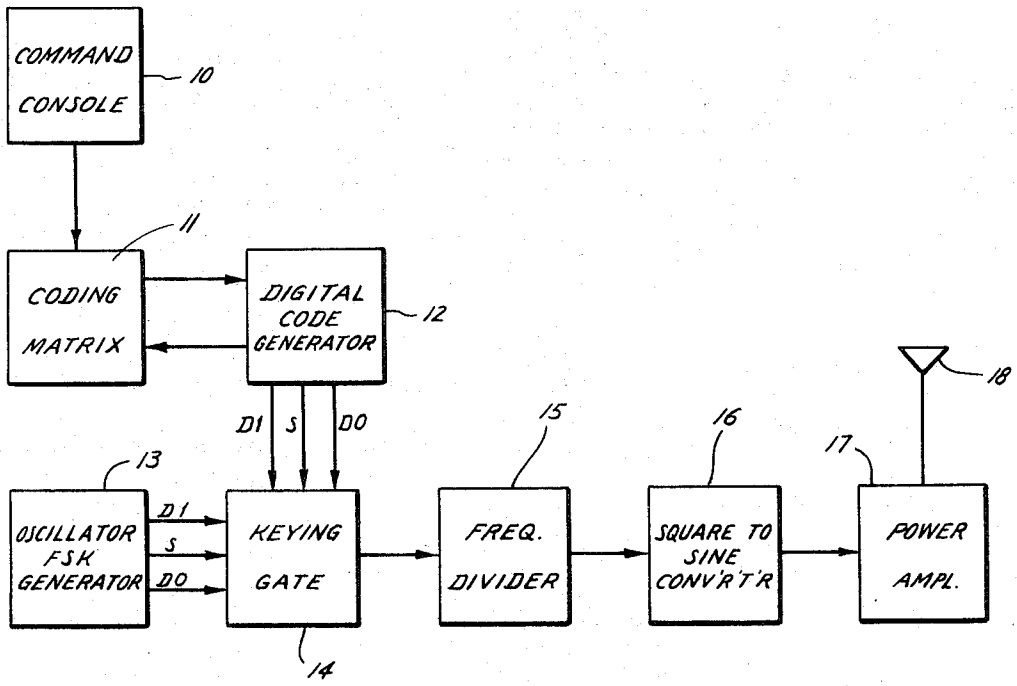
[57] **ABSTRACT**

A transmitter which produces a secure acoustic command signal. The acoustic command signal preferably includes a predetermined number of time slots each including a space tone of one frequency followed by a data tone of another frequency. When a binary code is transmitted by the acoustic command signal, a data tone of a second frequency is transmitted, which represents a binary 1, and a data tone of a third frequency is transmitted, which represents a binary 0. The transmitter preferably includes a signal generator for generating a plurality of different frequency acoustic signals to provide the three different tone signals which make up the acoustic command signal, and a code generator for generating three different control pulses in a coded sequence in response to an operator command to provide a desired sequence of transmission of the space tones and data tones. The outputs of the signal generator and the code generator are combined in a gate circuit to provide the desired acoustic command signal, and means is provided for radiating the acoustic command signal for receipt by a remote receiver.

5 Claims, 6 Drawing Figures



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5 Sheets-Sheet 1

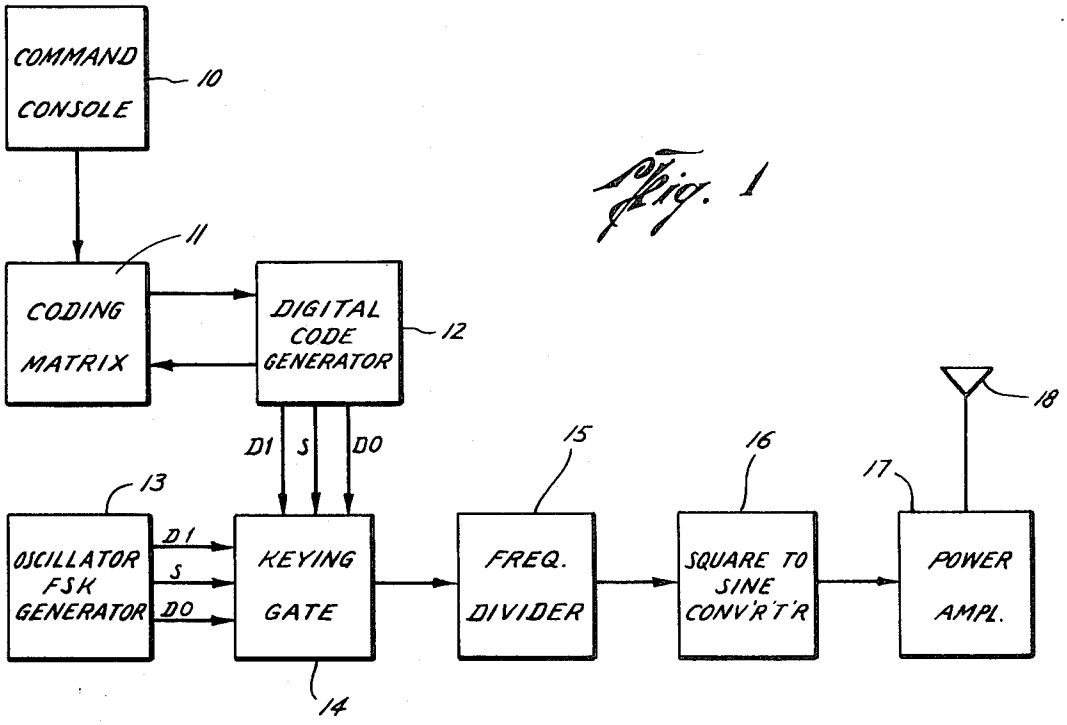
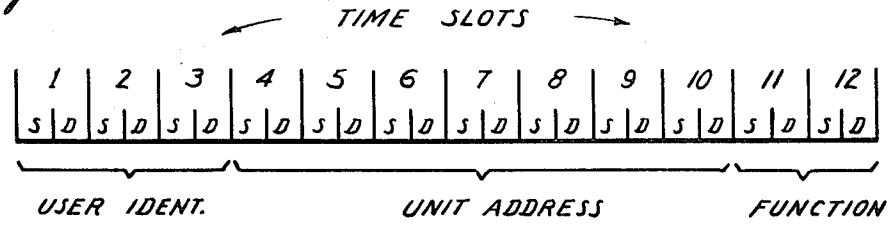


Fig. 1

Fig. 2



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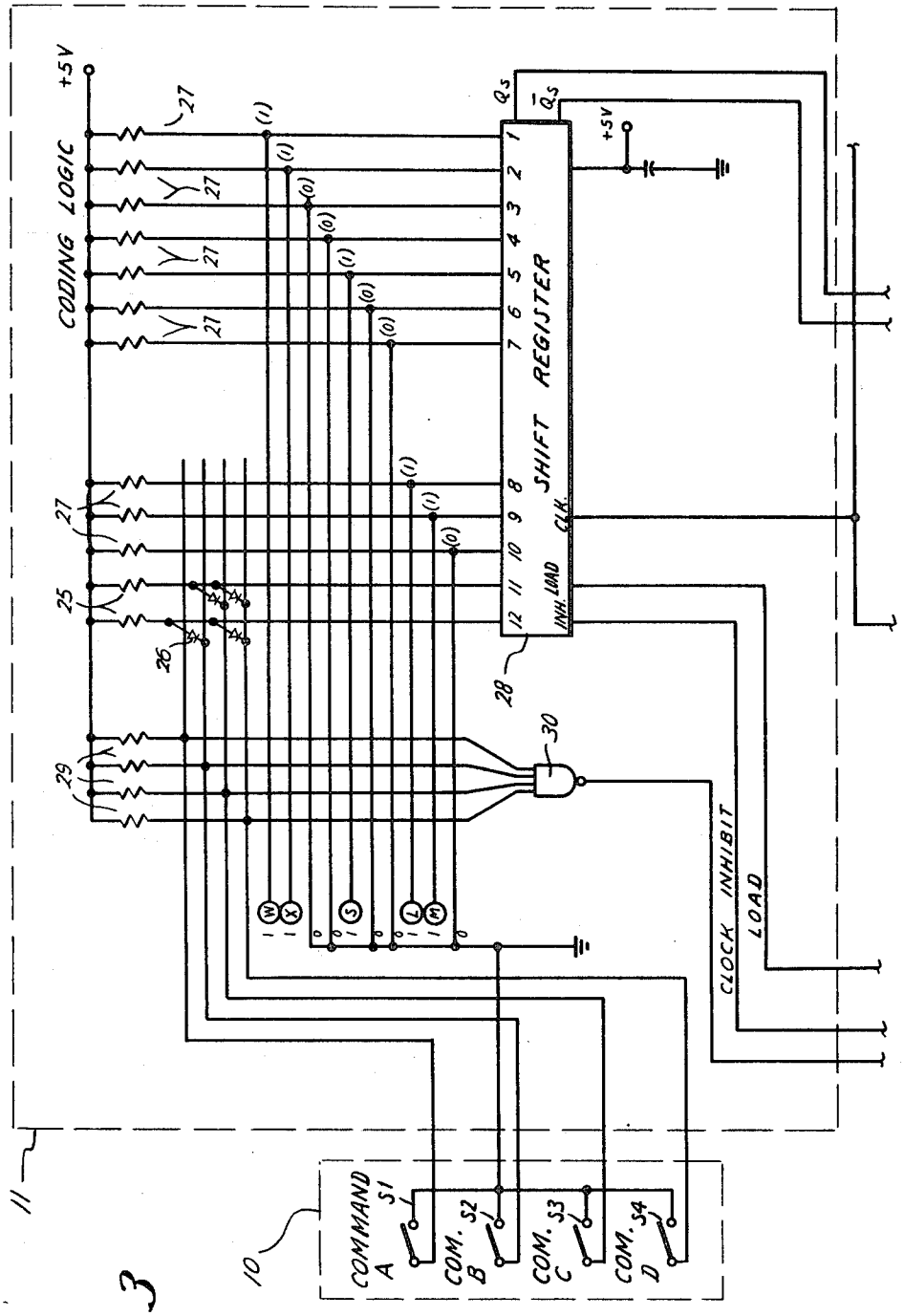

Fig. 3

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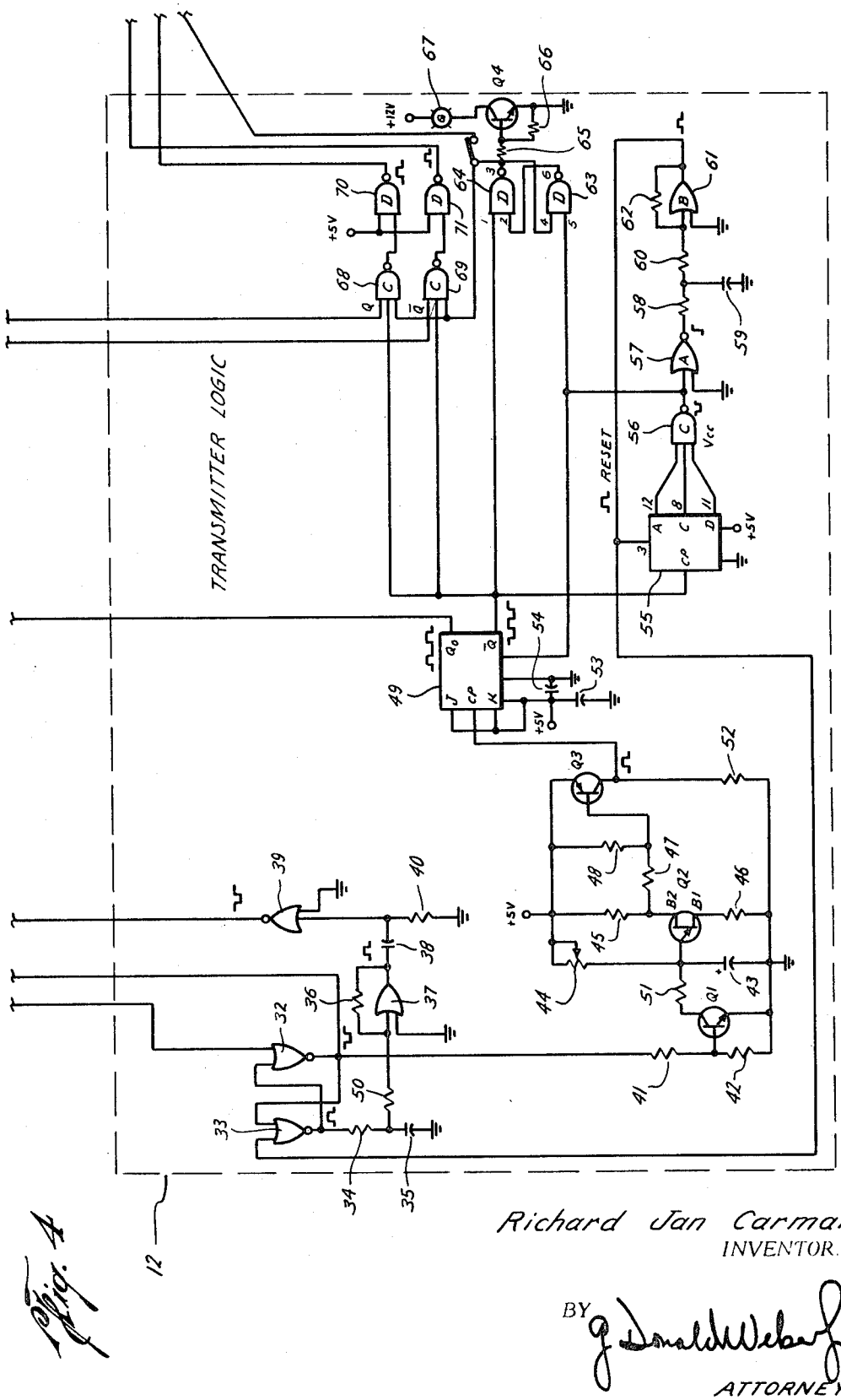

Fig. 4

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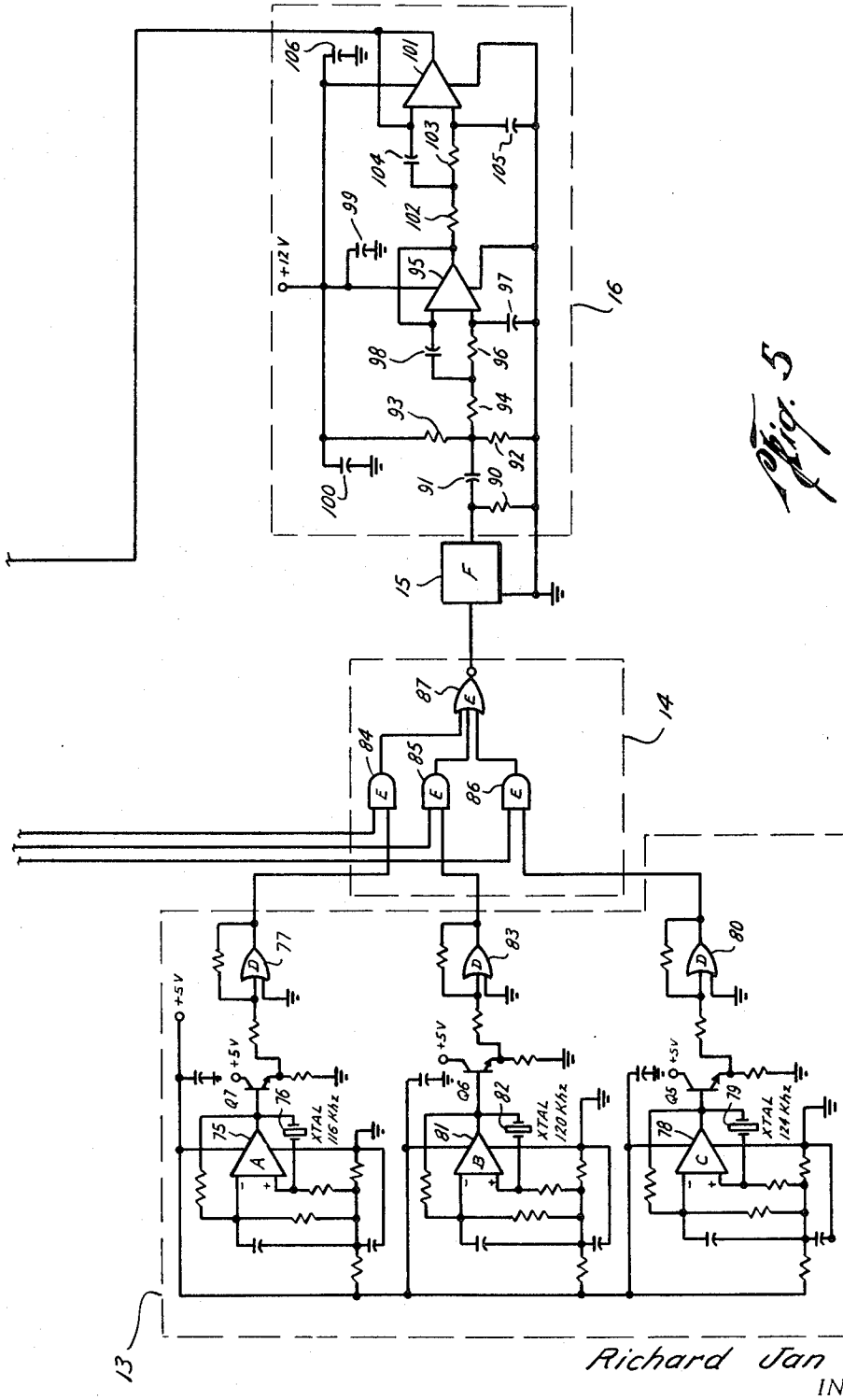

Fig. 5

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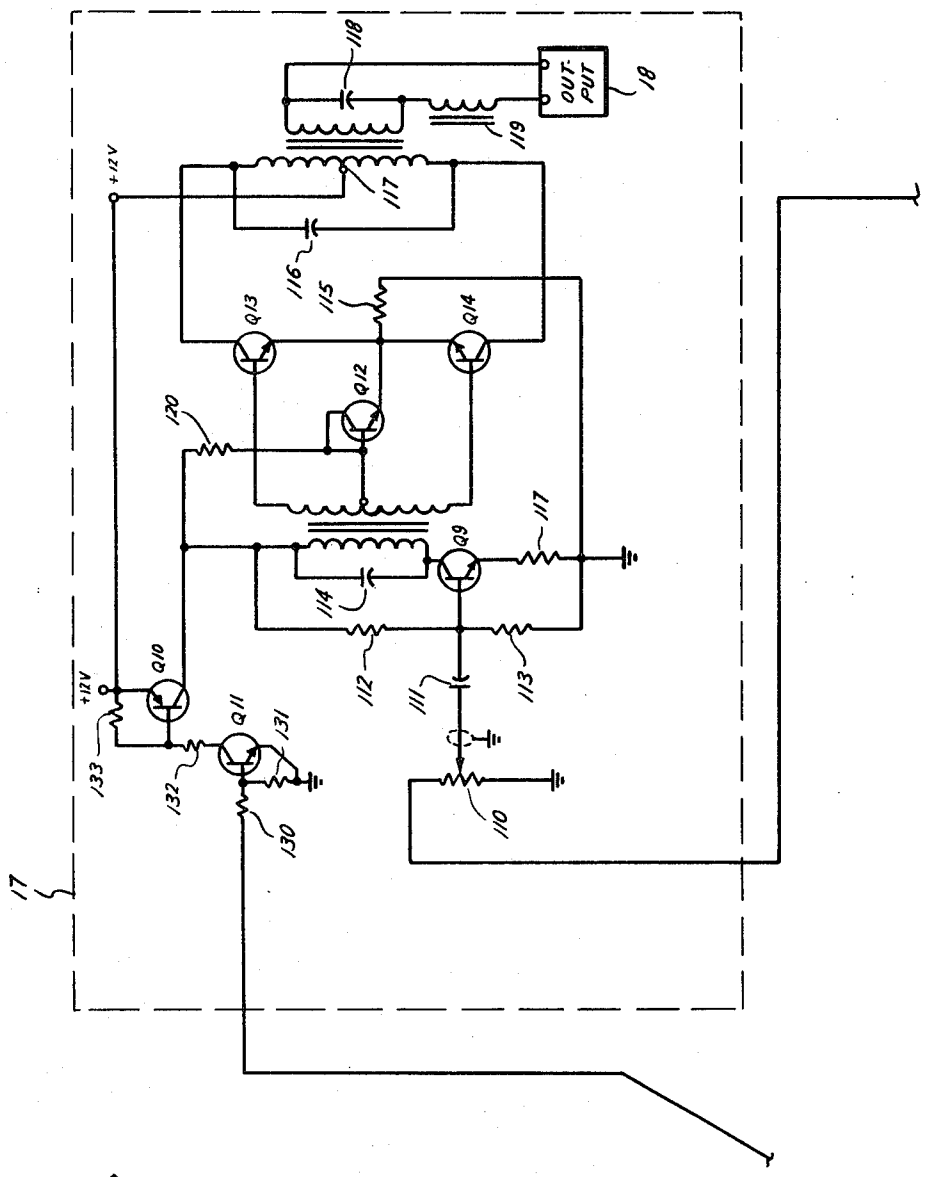

Fig. 9

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ACOUSTIC CONTROL TRANSMITTER

BACKGROUND

In the offshore petroleum industry, the current and future trend is toward operations in deeper water. This fact occurs inasmuch as most of the relatively shallow waters are now being fully exploited. In the deeper water operations, many producers are investigating the desirability of using acoustically controlled subsea systems whereby the subsea equipment can be controlled by an acoustic interface from a surface unit. As has been experienced, subsea acoustic conditions are unusual and difficult. Many random noises and signals are y present. Moreover, many of the signals which are deliberately produced are subject to reflection and other distortions. Furthermore, since one or more producers may be operating in adjacent fields, it is mandatory that coding of the control signals be utilized to identify the particular user and to identify the particular equipment of a specific user as well as to define the function which is to be performed by the subsea equipment.

Several techniques along this line are known in the art. Such background techniques are described in U. S. Pat. No. 3,405,387, entitled Acoustical Underwater Control Apparatus by P. C. Koomey et al. and assigned to the instant assignee. In addition, the co-pending application entitled Acoustic Control System by R. J. Carman bearing Ser. No. 38,761, filed May 19, 1970, now abandoned, and a continuation of that application, Ser. No. 245,582, filed Apr. 19, 1972, and assigned to the instant assignee describes another system for subsea control. The latter named application describes a system which is designed to use a transmitter similar to the one described herein.

SUMMARY OF THE INVENTION

This invention relates to a transmitter circuit which produces a secure coded command signal which is especially adapted for transmission through a water medium. A relatively unique and novel method of coding is utilized to provide a secure message and to minimize multipath and other undesirable propagation factors associated with underwater acoustic transmission. The transmitter uses a reliable and accurate signal generator and a coding device which operates to interact with the signal produced by the generator to provide reliable, accurate signals which are transmitted to the subsurface units. The generator is a precision crystal-controlled oscillator which produces suitable distinct signals representative of different phenomena. The coding matrix is a reliable, accurate circuit for operating upon input signals and converting the signals to a useful digital code. The digital code and the signals from the generator are gated together and then converted relative to frequency and configuration as may be required. Any amplification which is required is supplied.

DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of the transmitter network circuit which forms the subject of this invention.

FIG. 2 is a representation of a preferred coded signal format.

FIGS. 3 through 6 are schematic diagrams of portions of transmitter network.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In each of the figures, similar components bear similar reference numerals.

Referring now to FIG. 1, command console **10** represents a typical console which is used by the operator of the transmitter. For example, console **10** may include a computer or the like which provides signals representative of any number of operations which are to be performed. Conversely, command console **10** may represent a relatively unsophisticated console wherein signals are manually provided by operation of suitable single throw switches as suggested subsequently in FIG. 3.

The output of command console **10** is connected to coding matrix **11**. Coding matrix **11** may be any suitable circuit such as a diode matrix or the like. Suitable shift registers may be incorporated whereby parallel-to-serial conversion is implemented. Thus, the inputs from command console **10** may be parallel in form and the output from matrix **11** may be serial in form. In addition, the coding matrix may include suitable gating arrangements whereby synchronism is provided.

The output signals produced by coding matrix **11** are supplied to digital code generator **12**. Digital code generator **12** incorporates suitable logic circuitry, timing circuitry and the like whereby the signals produced by coding matrix **11** are operated upon in a synchronized fashion. In addition, digital code generator **12** supplies signals to coding matrix **11** whereby the operation of coding matrix **11** and digital code generator **12** are synchronized. The output signals produced by digital code generator **12** are designated as data **1** (D1), Space (S), and data **0** (D0). These signals are supplied to keying gate **14**.

Oscillator FSK generator **13** is an oscillator circuit which utilizes operational amplifiers which are crystal controlled to provide stable, controlled frequency signals. In the particular embodiment shown, three separate and distinct frequency shift keyed FSK tone signals also designated as data **1** (D1), Space (S), and data **0** (D0). These signals are also supplied to keying gate **14**.

Keying gate **14** is a gating circuit utilizing standard components. In this case, the components are integrated circuits but discreet component circuits can be utilized. Keying gate **14** operates to effectively combine the signals produced by digital code generator **12** and oscillator FSK generator **13**. Keying gate **14** operates to selectively pass one of the aforementioned signals D1, S or D0. That is, oscillator **13** is a continuously running circuit; however, the signals supplied by oscillator generator **13** are not passed through keying gate **14** unless a counterpart signal is supplied by digital code generator **12**.

The output signal from keying gate **14** is supplied to frequency divider **15**. Frequency divider **15**, in the preferred embodiment, is a "divide by 8" divider. However, any suitable frequency division may be utilized. The frequency division is necessary only as a function of the input frequency and the output frequency response.

Signals from frequency divider **15** are supplied to square to sine wave converter **16**. Converter **16** is, in essence, a low pass filter utilizing operational amplifiers wherein the harmonics of the input square wave are

suppressed so that a substantially sine wave output signal is provided. The output signal from converter **16** is supplied to power amplifier **17**. Amplifier **17** is a typical amplifier circuit which operates on the sine wave signal to produce any desirable and necessary amplitude. The amplified signal is applied to a suitable transducer or hydrophone **18**. Depending upon the amplitude of the signal supplied by converter **16**, the characteristics of amplifier **17** may be determined. Transducer **18** is, as suggested, a projector which is located in the surrounding environment for transmitting acoustic signals therethrough.

FIG. 2 represents a typical code format. This code format represents the signal which is generated by the transmitter which is the subject of the instant invention. The code format shown herein is illustrative only and is not meant to be limitative. The illustrative signal or code word comprises 12 time slots. The time slots have identical durations which, per se, does not form a portion of this invention. The time slots are arranged to provide certain necessary information. For example, time slots **1–3** are utilized to identify the user or owner of the subsea units or equipment. Time slots **4–10** are utilized to identify the particular unit which is to be operated subsea. Time slots **11** and **12** are set aside to convey the information as to which function is to be performed by the appropriate subsea unit. Thus, the code word, as defined, first chooses the general user, then the specific unit belonging to that user and, finally, generates the information to cause the particular unit to function accordingly. Obviously, the code format may be altered with regard to the number of time slots required for each type of information.

Each of the time slots is divided into two separate portions. The initial portion of each time slot comprises a space tone. That is, during the initial portion of each time slot the space tone, which is a constant frequency, is generated. As will be understood, the space tone which initiates each time slot has several advantages and functions. The space tone can be utilized to synchronize the operation of the transmitter and the subsea receiver. In addition, by requiring a space tone in each time slot, many of the subsea circuit components can be set (or reset) to specified initial conditions.

After the space tone has been generated during each time slot, a data tone is generated. The data tone portion of each time slot is utilized to present signals representative of a binary 1 or a binary 0. The data tone which represents a binary 1 is substantially different from the data tone which represents a binary 0. With this signal format, the receiver can be designed so that a data tone normally is not received and/or decoded unless a space tone precedes the data tone. The code format and the advantages thereof will become more readily apparent when the following detailed description of the circuit is described.

Referring now to FIG. 3, command console **10** is shown in the dashed outline and is schematically represented by single pole, single throw switches **S1**, **S2**, **S3** and **S4**. In the schematic representation, it is seen that closure of any of the respective switches effectively grounds the output line connected therewith. Thus, to represent command A, command B, command D, the respective switch is closed and a ground potential, i.e. binary 0, is provided.

The outputs of console **10** are connected to inputs of coding matrix **11**. The coding matrix includes a typical diode matrix. The output lines from console **10** are connected to the input lines which are represented by the horizontal lines of the matrix. The horizontal lines are connected to the cathodes of the diodes which form the diode matrix. The anodes of the diodes are connected via resistors **25** to a suitable voltage source which supplies, for example, +5 volts. In addition, the junctions of the cathodes of the diodes and the respective resistors **25** are connected to the vertical lines in the matrix which are connected to input terminals of shift register **28**. In addition, other vertical lines are connected to other inputs of shift register **28** via resistors **27**.

In the embodiment shown, the full diode coding matrix is not illustrated. That is, the diode matrix is merely shown representatively to avoid undue complication and repetition. Additional horizontal lines are shown connected to each of the vertical lines associated with resistors **27**. Some of these horizontal lines are connected to ground while some other horizontal lines are not connected to ground. Those horizontal lines connected to ground represent binary 0 signals while the ungrounded horizontal lines represent binary **1** signals. Thus, a simulated code word is supplied to input terminals **1–10** of shift register **28**, as for example for testing or description. The simulated signals represent the user identification and unit address. The signals supplied to input terminals **11** and **12** of shift register **28** represent the command function signals and are supplied by console **10**. While only these two signals are represented by variable signals, it is to be understood that, in normal application, each of the inputs to shift register **28** would receive a coded signal via a diode matrix.

In addition, a plurality of vertical lines are connected to the positive voltage source via resistors **29**. These vertical lines are connected to inputs of NAND gate **30**. In addition, each of the inputs to gate **30** is connected to one of the horizontal input lines. Again, in the illustrative showing herein, only the variable input lines are connected to gate **30**. However, in a typical application, all of the variable input lines would be connected to s similar type gate. The output of gate **30** is connected to an input of digital code generator **12** to supply a signal thereto. When gate **30** receives at least one binary **0** input signal, a binary **1** output is produced thereby. Thus, the output of gate **30** selectively controls the operation of digital code generator **12**. In addition, the Q and $\overline{Q}$ outputs from shift register **28** are connected to digital code generator **12**. Other signals supplied to shift register **28** from digital code generator **12** are the INHIBIT, LOAD and CLK signals as described hereinafter.

The output signal from gate **30** is supplied to one input of NOR gate **32**. Gate **32**, in conjunction with NOR gate **33** forms an R-S flipflop. Thus, the output of gate **32** is connected to one input of gate **33**. The output of gate **33** is connected to another input of gate **32**. Another input of gate **33** is connected to the reset line which will be described hereinafter. The output of gate **33** is further connected to ground via the series combination of resistor **34** and capacitor **35**. The output of gate **32** is further connected to and returned to the inhibit input (INH) of shift register **28**.

The common junction between resistor 34 and capacitor 35 is connected, via resistor 50, to an input of or gate 37. This input of gate 37 is connected to the output thereof via feedback resistor 36. Another input of gate 37 is connected directly to ground. The output of gate 37 is connected via capacitor 38 and resistor 40 to ground. The common junction of capacitor 38 and resistor 40 is connected to one input of NOR gate 39. Another input of NOR gate 39 is connected to ground. The output of NOR gate 39 is connected to the LOAD input of shift resistor 28. Thus, the LOAD and INHIBIT input signals to shift register 28 are supplied by digital code generator circuit 12. However, digital code generator circuit 12 will not be rendered operative until an appropriate input signal is supplied thereto from gate 30.

The output of gate 32 is further connected to supply an input signal to the timing circuit which provides the clock pulse. The signal from gate 32 is supplied to the timing circuit via resistor 41. More particularly, the output of gate 32 is connected to ground via the series combination of resistors 41 and 42. The common junction of resistors 41 and 42 is connected in the base electrode of NPN transistor Q1. The emitter of transistor Q1 is returned to ground while the collector thereof is connected via resistor 51 to the emitter electrode of unijunction transistor Q2. Timing capacitor 43 is connected between the emitter of transistor Q2 and ground. Variable resistor 44 is connected between the positive voltage source and the emitter of transistor Q2. Base B1 of transistor Q2 is connected to ground via resistor 46 while base B2 is connected to the positive terminal via resistor 45. In addition, base B is connected to the positive terminal via the series combination of resistors 47 and 48. The common terminal of resistors 47 and 48 is connected to the base electrode of PNP transistor Q3. The emitter of transistor Q3 is connected to the positive terminal while the collector electrode is connected to ground via resistor 52.

The output of the timing network is detected at the collector of transistor Q3 and connected to the Cp or toggle input of flipflop 49. Flipflop 49 is a JK flipflop with the J and K inputs connected to the positive terminal whereby the output of flipflop 49 is controlled by the Cp or toggle input signal. Filter capacitors 53 and 54 are connected between the JK inputs and ground. The Q and $\overline{Q}$ outputs of flipflop 49 are obviously complementary outputs. The Q output is connected directly to the clock (CLK) input of shift register 28. The $\overline{Q}$ output of flipflop 49 is connected to the reset network.

The reset network includes a counter 55 which has the Cp (i.e. toggle) input thereof connected to the $\overline{Q}$ output of flipflop 49. Power supply terminals are connected to suitable positive and ground potential sources. The A, C and D outputs of counter 55 are connected to the inputs of NAND gate 56. When all of the inputs to gate 56 are of an appropriate level (for example, binary 1), gate 56 produces an output signal representative thereof. The output of gate 56 is connected to the reset input of JK flipflop 49. In addition, the output of gate 56 is connected to one input of NAND gate 63 which will be described hereinafter. Furthermore, the output of gate 56 is connected to an input of NOR gate 57. Another input of gate 57 is connected to ground whereby gate 57 operates as an inverting gate. The output of gate 57 is connected to an input of OR gate 61 via the integrating network comprising resistors 58 and 60 connected (in series) between the gates, and, capacitor 59 which is connected between the common junction of resistors 58 and 60 and ground.

Feedback resistor 62 is connected between the output and the aforementioned input of gate 61. The output of gate 61 is further returned to the second or reset input of gate 33 as described supra. Moreover, the output of gate 61 is connected to the reset input terminal of counter 55.

As noted, one input of gate 63 is connected to the output of gate 56. Gates 63 and 64 are connected to form an RS flipflop network. Thus, the output of gate 63 is connected to one input of gate 64. The output of gate 64 is connected to a second input of gate 63. The second input of gate 64 is connected to the $\overline{Q}$ output of flipflop 49.

The output of gate 64 is connected via series connected resistor 65 and 66 to ground. The common junction between resistors 65 and 66 is connected to the base of NPN transistor Q4. The emitter of transistor Q4 is connected to ground. The collector of transistor Q4 is connected to a +12 volt source via a suitable indicator 67. Thus, when transistor Q4 is rendered conductive, current passes through indicator 67 and causes the operation thereof.

NAND gates 68 and 69 each have one input connected to the Q and $\overline{Q}$ outputs of shift register 28 (see FIG. 1), respectively. In addition, each of gates 68 and 69 has an input connected to the $\overline{Q}$ output of flipflop 49. Further, each of gates 68 and 69 has an input connected to the output of gate 64. Obviously, since the Q and $\overline{Q}$ outputs of shift register 28 will be opposite in sense, gates 68 and 69 (which have other inputs in common) will produce complementary output signals. The output of gate 68 is connected to an input of NAND gate 70 while the output of gate 69 is connected to an input of NAND gate 71. Another input of each of gates 70 and 71 is connected to a +5 volt source. The outputs of gates 70 and 71 represent the D1 and D0 output signals generated by the digital code generator 12. These signals are supplied to keying gate circuit 14.

The operation of digital code generator 12 is initiated by the signal supplied to one input of NOR gate 32. The signal supplied to gate 32 is provided by gate 30 in coding matrix 11. It will be noted that each of the inputs supplied to gate 30 is normally a binary 1. However, the closure of any of switches S1–S4 in command console 10 will provide a momentary binary 0 signal to at least one input of gate 30. With the application of a binary 0 to any input thereof, gate 30 produces a binary 1 output signal. This binary 1 signal is supplied to an input of gate 32 and causes the gate to produce a binary 0 output signal. This binary 0 signal is supplied to the inhibit (INH) input of shift register 28. A binary 0 at the INHIBIT input of shift register 28 permits operation of the shift register.

In addition, the binary 0 output signal of gate 32 is supplied to an input of gate 33. Since the output of gate 61 is normally a binary 0, gate 33 produces a binary 1 output signal which is applied to gate 32 to latch the flip-flop comprising gates 32 and 33. In addition, the binary 1 output of gate 39 is supplied as an input to gate

37. That is, when the output of gate 33 goes high, capacitor 35 is charged through resistor 34. When the voltage on capacitor 35 achieves the threshold level of gate 37, the gate produces a binary 1 at the output thereof. However, the output of gate 37 is delayed relative to the output of gate 35 by the integrating time of capacitor 35. The binary 1 output signal from gate 37 is supplied to an input of gate 39 via the differentiating network comprising capacitor 38 and resistor 40. Gate 39 operates as an emitter and produces a binary 0 output signal which is applied to the LOAD input of shift register 28 to permit shift register 28 to receive signals on input terminals 1–12. The LOAD input signal is a short time duration pulse due to the differentiating network and delayed by the integrating network. Thus, random noise due to switch source or the like is evolved.

In addition, the binary 0 output signal from gate 32 is applied to the base of transistor Q1. This signal causes transistor Q1 to be rendered non-conductive. When transistor Q1 is non-conductive, capacitor 43 is charged via resistor 44 and, periodically, discharged by unijunction transistor Q2 when the threshold potential thereof is achieved. In accordance with the operation of transistor Q2, transistor Q3 is selectively rendered conductive. When transistor Q3 is conductive, a current path from the positive potential source to ground is established whereby the voltage drop across resistor 52 is increased. Thus, a relatively positive going signal is supplied from the collector electrode of transistor Q3 to the Cp input terminal of JK flip-flop 49. Thus, it is seen that the application of a signal to gate 32 and the generation of the signal thereby triggers the timing circuit which produces a clock pulse at the collector electrode of transistor Q3 and supplies the clock pulse to flipflop 49.

In response to the clock pulses supplied from transistor Q3, flip-flop 49 produces the complementary clock signals Q and $\overline{Q}$. The Q or clock signal is supplied to the clock (CLK) input of shift register 28. On the positive going edge of the Q clock signal, shift register 28 shifts one bit and produces its own signals Qs and $\overline{Q}$s. The $\overline{Q}$ signal produced by flipflop 49 is supplied to counter 55. Counter 55 counts a predetermined number of $\overline{Q}$ pulses and produces signals representative thereof. When gate 56 decodes the output of counter 55 and detects an appropriate count, a binary 0 signal is produced thereby. The binary 0 signal is supplied to the reset or clamping input of flipflop 49 to terminate the operation thereof. In addition, the output signals from gate 56 are supplied to inputs of gates 63 and 57. A binary 0 at the input of gate 63 produces a binary 1 output thereby. When flipflop 49 is clamped, the $\overline{Q}$ output is also a binary 1. Consequently, gate 64 receives all binary 1 inputs and produces a binary 0 output which is effective to render transistor Q4 non-conductive whereby indicator lamp 67 is extinguished. Since indicator lamp 67 represents transmitter operation, extinction of this lamp indicates that the transmitter is no longer transmitting signals.

Concurrent with the application of binary 0 signal to flipflop 49 and gate 63, gate 56 supplies a binary 0 signal to the input of inverter gate 57. The output of gate 57 is supplied to the integrating network comprising resistor 58 and capacitor 59. The output of gate 57 is, therefore, delayed relative to the output of gate 56. When capacitor 59 charges sufficiently, gate 61 conducts. Through the operation of gates 57 and 61, the delayed reset signal (a binary 1) is supplied to gate 33 to reset the flipflop comprising gates 32 and 33 so that a binary 1 is produced by gate 32 whereby transistor Q1 is turned on and the timing or clock circuit is, essentially, turned off.

The $\overline{Q}$ signals supplied by flipflop 49 also are supplied to inputs of gates 68 and 69 and operate as enable signals during a portion of a standard time slot. In addition, the output signal from gate 64 operates as an enable signal to gates 68 and 69. Moreover, the outputs of gates 68 and 69 are dependent upon the condition of the Qs and $\overline{Q}$s signals from shift register 28. That is, since gates 68 and 69 are NAND gates, a binary 0 signal is produced only when each of the inputs is a binary 1. Consequently, when the respective Qs or $\overline{Q}$s output of shift register 28 is a binary 1 concurrent with binary 1 signals from gate 64 and the $\overline{Q}$ output of flipflop 49, the appropriate gate 68 or 69 produces a binary 0. This binary 0 signal is supplied to the input of the associated gate 70 or 71 to produce a binary 1 at the output thereof.

Thus, it may be seen that during the portion of the $\overline{Q}$ signal which is a binary 0, each of gates 68 and 69 receives a binary 0 input and produces a binary 1 output whereby gates 70 and 71 produce binary 0 outputs. Thus, no output signal is supplied on the D1 or D0 signal lines which are supplied to keying gate circuit 14. Conversely, when the $\overline{Q}$ signal from flipflop 49 is a binary 0, the Q signal is a binary 1. This signal is supplied to the CLK terminal of shift register 28 to produce a shifting of the information stored in the shift register. In addition, the Q signal is supplied to keying gate 14.

More specifically, the Q signal from flipflop 49 is supplied to the space tone generating network so that a space tone is generated whenever the Q signal of flipflop 49 is a binary 1. Conversely, when the $\overline{Q}$ signal is a binary 0, data tones are not generated. However, when the polarities of the output signals of flipflop 49 reverse, the Q signal becomes a binary 0 and the space tone is no longer generated. However, the $\overline{Q}$ signal becomes a binary 1 and a data tone is generated as a function of the signal level supplied at the inputs of gates 68 and 69 by shift register 28.

Referring now to oscillator FSK generator 13, there have been shown three substantially identical signal or tone generating networks. Each of the tone or frequency generators includes an operational amplifier which has a crystal connected in the feedback path between the output and the non-inverting input thereof. Each of the tone generating networks is substantially identical with the exception of the tuned frequency of the crystal in the feedback path of the amplifier. In the preferred embodiment, crystal 76 has a tuned frequency of 116 KHz, crystal 82 has a tuned frequency of 120 KHz and crystal 79 has a tuned frequency of 124 KHz. It will be observed that the frequency produced by the combination of crystal 82 and amplifier 81 and supplied to transistor Q6 and gate 83 represents the space tone frequency. This frequency is intermediate the other frequencies which represent data tones. For example, the 116 KHz frequency supplied by the circuit comprising crystal 76 in the feedback loop of amplifier 75,

transistor Q7 and gate 77 is the data tone for a binary 1. Obviously, the 124 KHz frequency supplied by crystal 79 in the feedback loop of amplifier 78, and applied to transistor Q5 and gate 80 is the data tone for a binary 0. The outputs of gates 77, 83 and 80 respectively are connected to the inputs of gates 84, 85 and 86, respectively. The tone signals are continuously supplied to these respective gates. Each of the latter gates is a AND gate and is associated with keying gate 14.

Gate 84, in addition to the D1 tone from generator circuit 13 selectively, receives the D1 signal from digital code generator 12. With the application of a D1 signal from gate 70 in circuit 12, a D1 tone or frequency signal is transmitted by gate 84. Similarly, with the application of a D0 signal from gate 71 to an input of gate 86, the D0 tone is transmitted by gate 86. Similarly, the application of a space tone signal from the Q output of flipflop 49 enables gate 85 to transmit the space tone from gate 83. In other words, the signals from code generator 12 are enable signals and the continuously supplied tone signals are transmitted by the appropriate gate only when the appropriate enable signal is supplied. The outputs of gates 84, 85 and 86 are connected to the input of gate 87. Gate 87 operates to gate together, in OR gate fashion, the pulse signals from gates 84, 85 and 86.

The output of gate 87 is connected to divider 15. As noted, divider 15 is any standard type divider such as an integrated circuit or it may be composed of discrete components. In the preferred embodiment, divider 15 divides the signals supplied by gate 87 by a factor of 8. Thus, the output signals produced thereby are 14.5 KHz, 15.0 KHz or 15.5 KHz.

The output of frequency divider 15 is connected to square to sine wave converter 16. In particular, the output of frequency divider 15 is connected across load resistor 90 and to the inputs of amplifier 95 via coupling capacitor 92 which blocks D.C. signals. Resistors 92 and 93 provide suitable bias for amplifier 95. The output of amplifier 95 is connected directly to one of the inputs thereof to provide a stabilizing, gain reducing feedback loop. Positive and negative potentials are connected to amplifier 95. Suitable filter capacitors 99 and 100 are provided to remove spurions, noise and other undesirable frequency variations from the amplifier circuit.

The output of amplifier 95 is connected to amplifier 101 via the filter network comprising resistors 102 and 103 as well as capacitors 104 and 105. Again, a feedback path directly connects the output with one of the inputs of amplifier 101. A suitable filter capacitor 106 is provided relative to amplifier 101. Again, standard positive and negative potentials are supplied to the amplifier.

The purpose of converter circuit 16 is to convert the substantially square wave pulses supplied by frequency divider 15 to sine wave signals. The square wave signals from frequency divider 15 are supplied to the Butteworth low pass filter. The filters comprising the resistors and capacitors at the input of amplifiers 95 and 101, respectively, are especially designed to suppress the harmonic content of the signals supplied thereto. By suppressing the harmonics, the square wave signal is converted to appear as a sine wave signal. The output from the square to sine wave converter is supplied to output power amplifier 17.

In output power amplifier 17, a power switch is provided. The base of Q11 is connected to the common junction of resistors 130 and 131. Resistor 130 is connected to the "transmitter on" terminal at transistor Q4. More specifically, resistor 130 is connected to the outputs of gates 63 and 64. Resistor 131 is connected to ground potential along with the emitter of NPN transistor Q11.

The collector of transmitter Q11 is connected to the +12 volt source via series connected resistors 132 and 133. The common junction of these resistors is connected to the base of PNP transistor Q10. The emitter of transistor Q10 is connected to the +12 volt source. The collector of Q10 is connected to the amplifier as described hereinafter.

Thus, with the application of a binary 1 signal to the base of transistor Q11 current flow therethrough is permitted. Moreover, transistor Q10 is also rendered conductive. With transistor Q10 in the conductive state, the +12 volt source is effectively connected to the remainder of the output amplifier circuit.

The sine wave produced by signal converter 16 is supplied to power amplifier circuit 17 across volume control resistor 110. That is, the output of amplifier 101 is connected to one terminal of resistor 110 while the other terminal thereof is returned to ground. The variable tap of resistor 110 is connected via coupling capacitor 111 to the base of NPN transistor Q9. In addition, resistors 112 and 113 are connected together, and in series, between a positive potential source represented by the collector of Q10. The common junction between resistors 112 and 113 is connected to the base of transistor Q9 to provide bias potential therefor.

The emitter of NPN transistor Q9 is connected to ground via resistor 117 while the collector electrode of transistor Q9 is connected to the positive source via the resonant circuit comprising the parallel combination of the primary winding of transformer T2 and capacitor 114. The opposite ends of the secondary winding of transformer T2 are connected to the bases of NPN transistors Q13 and Q14, respectively. The base of NPN transistor Q12 is connected to a center tap on the secondary winding of transformer T2. The emitters of transistors Q12, Q13 and Q14 are connected together and to ground potential via resistor 115. Resistor 115 provides stability to the circuit. The base and collector of transistor Q12 are connected together so that transistor Q12 operates as a diode. Furthermore, the base of transistor Q12 is connected via bias resistor 120 to the collector of transistor Q10.

The collectors of transistors Q13 and Q14 are connected to opposite ends of the resonant circuit comprising the parallel combination of the primary winding of the transformer T1 and capacitor 116. The center tap 117 of the primary winding of transformer T1 is connected to the +12 volt source. The parallel combination of capacitor 118 and the secondary winding of transformer T1 forms another tuned circuit. Inductor 119 is connected in series between last named tuned circuit and output 18. Inductor 119 provides an impedance match with the output device which is a suitable transducer. Output device 18 produces the output acoustic signals in accordance with the operation of the transmitter system described herein.

In operation, the signal coupled to the amplifier via capacitor 111 is amplified only when the transmitter is turned on due to conduction of transistors Q10 and Q11. Transistor Q9 operates as a class A amplifier and supplies signals to the tuned circuit connected to the collector thereof. These signals are coupled, via transformer T2, to transistors Q13 and Q14 which operate as Class B amplifiers. The signals from transistors Q13 and Q14 are supplied to the tuned circuit of transformer T1 and, thence, to the output device.

Transducer 18 produces the output acoustic signals in accordance with the operation of the transmitter system. Thus, there has been described a transmitter system which is especially adapted to produce an acoustic signal for underwater application. The transmitter produces a plurality of separate and distinct frequency tones which are selectively supplied to a subsea or underwater transducer. The transmitter utilizes a coding technique for transforming manual or other input signals into digital type signals. The transmitter further utilizes logic control circuitry for combining the digital signals and the frequency tone signals whereby the digital signals control the tone signals. The digital control signals provide synchronization and other coding and timing advantages. The coding advantages permit a secure coded signal which is designed to avoid multipath signal generation, noise reflection and other undesirable and unwanted effects.

Several modifications may suggest themselves to those skilled in the art. For example, the specified voltage levels may be altered. Moreover, the logic may be changed so as to invert the levels of signals and the like. Moreover, the suggested tone frequencies, the frequency division, the number of inputs and the like as well as the coded format may be varied as required or desired by the user. However, any modifications of this nature and which fall within the purview of the instant description are intended to be included within the protection of this invention.

Having thus described the preferred embodiment of the invention, the embodiments of the invention in which an exclusive property is claimed are defined as follows:

1. A transmitter for transmitting an acoustic signal which includes a plurality of space tones and a plurality of data tones, the space tones of one such signal being transmitted at successive, spaced-apart time intervals for controlling the operation of a remote receiving device, and the data tones of the same such signal providing a coded command and being transmitted at different successive, spaced-apart time intervals intermingled with the time intervals at which said space tones are transmitted for controlling an utilization device when received by such a receiving device, said transmitter comprising in combination: signal generator means for providing an electrical signal at one acoustic frequency representative of a space tone, a second electrical signal at a different acoustic frequency representative of a first distinctive data tone; and a third electrical signal representative of a second distinctive data tone; command means responsive to an external command to provide coding control signals; electronic code generator means connected to said command means and responding to said coding control signals to provide first enable pulses at time intervals corresponding to the time intervals between said space tones, and second enable pulses at time intervals corresponding to the time intervals between said data tones, said code generator means including encoding means responsive to said coding control signals to provide and store a signal representative of a coded command to be transmitted by said data tones, timing control means connected to said encoding means for providing said first and second enable pulses in a predetermined sequence with the state of said second enable pulses being determined by the coded signals stored in said encoding means; gate means connected to said signal generator means and to said code generator means and responsive to the signals from said signal generator means and the enable pulses from said code generator means to provide said acoustic signal including said plurality of space tones at said first mentioned time intervals and said data tones at said different time intervals; and output means connected to said gate means for radiating said acoustic signal to remotely control such an utilization device.

2. The transmitter of claim 1 wherein said acoustic command signal comprises a predetermined number of sequential time slots, and each time slot includes a space tone followed by a data tone, and wherein said code generating means provides one of said second enable pulses after generation of one of said first enable pulses and before generation of the next first output pulse, and further including counter means for counting the number of time slots generated by said code generating means, and means responsive to said counter means for inhibiting generation of another time slot when said predetermined number of time slots is counted.

3. The transmitter of claim 1 including frequency divider means and wave shaping means connected between said gate means and said output means.

4. The transmitter of claim 1 wherein said encoding means includes diode matrix means connected into said command means to operate on said coding control signals and produce signals representative thereof, and storage register means connected to said diode matrix means to store the signals produced by said diode matrix means for a prescribed duration.

5. The transmitter of claim 1 wherein said coded command is provided by binary signals and wherein said first distinctive data tone represents binary 1 and said second distinctive data tone represents binary 0.

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